Product data sheet

1. General description

Planar passivated high commutation three quadrant triac in a SOT1292 (IITO3P) package intended for use in circuits where high static and dynamic dV/dt and high dI/dt can occur. This "series BT" triac will commutate the full RMS current at the maximum rated junction temperature ($T_{j(max)} = 150~^{\circ}$ C) without the aid of a snubber. It is used in applications where "high junction operating temperature capability" is required.

2. Features and benefits

- High current TRIAC
- 3Q technology for improved noise immunity
- · High commutation capability with maximum false trigger immunity
- High immunity to false turn-on by dV/dt
- High junction operating temperature capability (T_{j(max)} = 150 °C)
- High voltage capability
- · Least sensitive gate for highest noise immunity
- · Low thermal resistance
- · Planar passivated for voltage ruggedness and reliability
- Triggering in three quadrants only
- Insulated tab rated at 2500 V rms

3. Applications

- Applications subject to high temperature (T_{i(max)} = 150 °C)
- · High current / high surge applications
- High power / industrial controls e.g. heating, motors, lighting

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{DRM}	repetitive peak off- state voltage		-	-	800	V
I _{T(RMS)}	RMS on-state current	full sine wave; $T_{mb} \le 110 ^{\circ}\text{C}$; $\overline{\text{Fig. 1}}$; $\overline{\text{Fig. 2}}$; $\overline{\text{Fig. 3}}$	-	-	40	Α
I _{TSM}	non-repetitive peak on- state current	full sine wave; $T_{j(init)} = 25 ^{\circ}\text{C}$; $t_p = 20 \text{ms}$; Fig. 4; Fig. 5	-	-	400	Α
		full sine wave; $T_{j(init)} = 25 \text{ °C}$; $t_p = 16.7 \text{ ms}$	-	-	440	Α
Ti	junction temperature		_	-	150	°C

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
I _{GT}	gate trigger current	$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; T2+ G+;$ $T_j = 25 \text{ °C}; \frac{\text{Fig. 7}}{}$	-	-	50	mA
		$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; T2+ \text{ G-};$ $T_j = 25 \text{ °C}; \frac{\text{Fig. 7}}{}$	-	-	50	mA
		$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; \text{ T2- G-};$ $T_j = 25 \text{ °C}; \frac{\text{Fig. 7}}{}$	-	-	50	mA
I _H	holding current	V _D = 12 V; T _j = 25 °C; <u>Fig. 9</u>	-	-	80	mA
V _T	on-state voltage	I _T = 56.6 A; T _j = 25 °C; <u>Fig. 10</u>	-	-	1.5	V
Dynamic cha	racteristics					
dV _D /dt	rate of rise of off-state voltage	V_{DM} = 536 V; T_j = 150 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit	1000	-	-	V/µs
dl _{com} /dt	rate of change of commutating current	V_D = 400 V; T_j = 150 °C; $I_{T(RMS)}$ = 20 A; dV_{com}/dt = 20 V/ μ s; (snubberless condition); gate open circuit	15	-	-	A/ms

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T1	main terminal 1		T2——T1
2	T2	main terminal 2		G sym051
3	G	gate	0	Symost
mb	n.c.	mounting base; isolated		
			1 2 3 IITO3P (SOT1292)	

6. Ordering information

Table 3. Ordering information

Type number	Package					
	Name	Description	Version			
BTA440Z-800BT	IITO3P	plastic single-ended through-hole package; isolated heatsink mounted; 1 mounting hole; 3-lead TO3P	SOT1292			

7. Marking

Table 4. Marking codes

Type number	Marking code
BTA440Z-800BT	BTA440Z-800BT

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	800	V
I _{T(RMS)}	RMS on-state current	full sine wave; $T_{mb} \le 110 ^{\circ}\text{C}$; $\overline{\text{Fig. 1}}$; $\overline{\text{Fig. 2}}$; $\overline{\text{Fig. 3}}$	-	40	Α
I _{TSM}	non-repetitive peak on- state current	full sine wave; $T_{j(init)}$ = 25 °C; t_p = 20 ms; Fig. 4; Fig. 5	-	400	Α
		full sine wave; T _{j(init)} = 25 °C; t _p = 16.7 ms	-	440	Α
l ² t	I ² t for fusing	t _p = 10 ms; sine-wave pulse	-	800	A²s
dl _T /dt	rate of rise of on-state current	I _G = 0.2 A	-	150	A/µs
I _{GM}	peak gate current	t _p = 20 μs	-	8	Α
P_{GM}	peak gate power	t _p = 20 μs	-	40	W
P _{G(AV)}	average gate power		-	1	W
T _{stg}	storage temperature		-40	150	°C
T _j	junction temperature		-	150	°C

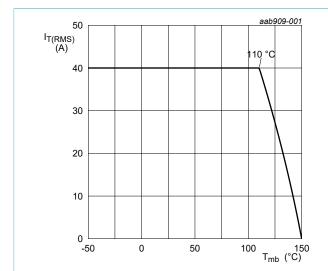


Fig. 1. RMS on-state current as a function of mounting base temperature; maximum values

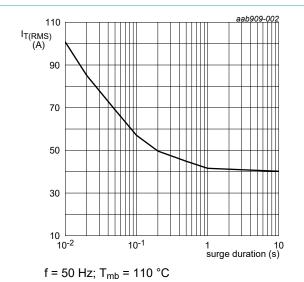


Fig. 2. RMS on-state current as a function of surge duration; maximum values

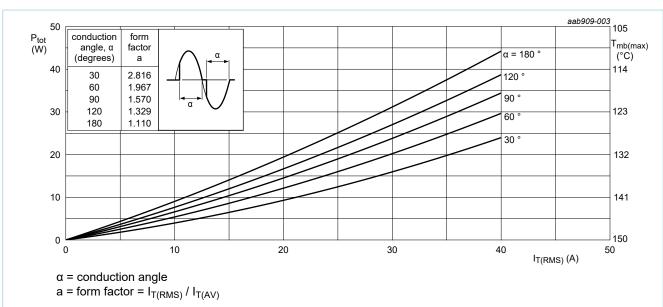


Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

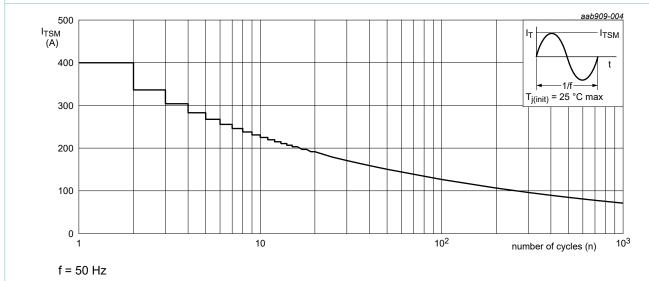
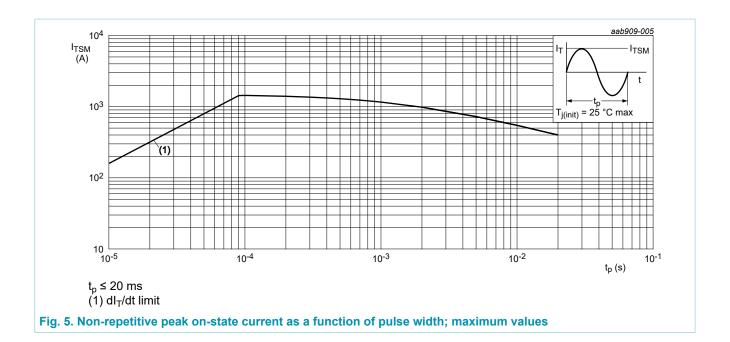


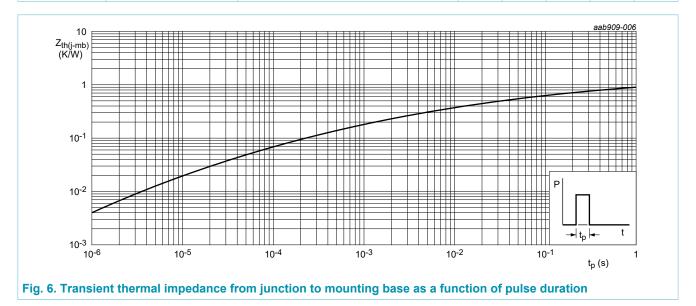
Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R _{th(j-mb)}	thermal resistance from junction to mounting base	Fig. 6	-	-	0.9	K/W
R _{th(j-a)}	thermal resistance from junction to ambient free air	in free air	-	50	-	K/W



10. Isolation characteristics

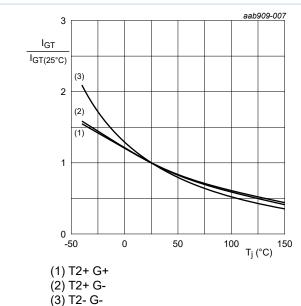
Table 7. Isolation characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{isol(RMS)}	RMS isolation voltage	from all terminals to external heatsink; sinusoidal waveform; clean and dust free; 50 Hz \leq f \leq 60 Hz; RH \leq 65 %; T_{mb} = 25 °C	-	-	2500	V

11. Characteristics

Table 8. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static char	acteristics		'			
I _{GT} gate trigger current	gate trigger current	$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; T2+ G+;$ $T_j = 25 \text{ °C}; Fig. 7$	-	-	50	mA
	$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; T2+ G-;$ $T_j = 25 \text{ °C}; Fig. 7$	-	-	50	mA	
		$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; T2- \text{G-};$ $T_j = 25 \text{ °C}; Fig. 7$	-	-	50	mA
I _L latching current	latching current	$V_D = 12 \text{ V}; I_G = 0.1 \text{ A}; T2+ G+;$ $T_j = 25 \text{ °C}; Fig. 8$	-	-	70	mA
		$V_D = 12 \text{ V}; I_G = 0.1 \text{ A}; T2+ G-;$ $T_j = 25 \text{ °C}; Fig. 8$	-	-	160	mA
		$V_D = 12 \text{ V}; I_G = 0.1 \text{ A}; \text{ T2- G-};$ $T_j = 25 ^{\circ}\text{C}; \text{ Fig. 8}$	-	-	70	mA
I _H	holding current	V _D = 12 V; T _j = 25 °C; <u>Fig. 9</u>	-	-	80	mA
V _T	on-state voltage	I _T = 56.6 A; T _j = 25 °C; <u>Fig. 10</u>	-	-	1.5	V
V _{GT}	gate trigger voltage	V _D = 12 V; T _j = 25 °C; <u>Fig. 11</u>	-	8.0	1.3	V
		V _D = 400 V; T _j = 150 °C; <u>Fig. 11</u>	0.2	0.45	-	V
l _D	off-state current	V _D = 800 V; T _j = 25 °C	-	-	10	μΑ
		V _D = 800 V; T _j = 150 °C	-	-	2	mA
Dynamic cl	haracteristics					
dV _D /dt	rate of rise of off-state voltage	V_{DM} = 536 V; T_j = 150 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit	1000	-	-	V/µs
dl _{com} /dt	rate of change of commutating current	$V_D = 400 \text{ V}; T_j = 150 ^{\circ}\text{C}; I_{T(RMS)} = 20 \text{ A};$ $dV_{com}/dt = 20 \text{ V/}\mu\text{s}; (snubberless condition); gate open circuit$	15	-	-	A/ms



junction temperature

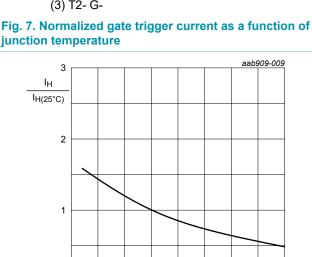


Fig. 9. Normalized holding current as a function of junction temperature

0

50

-50

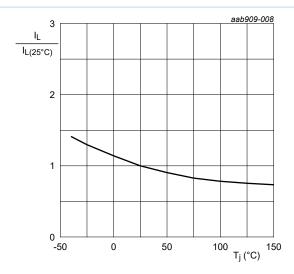
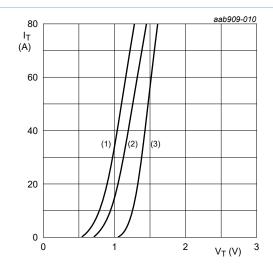


Fig. 8. Normalized latching current as a function of junction temperature



 V_o = 0.928 V; R_s = 0.0068 Ω (1) T_j = 150 °C; typical values (2) T_j = 150 °C; maximum values (3) T_j = 25 °C; maximum values

Fig. 10. On-state current as a function of on-state voltage

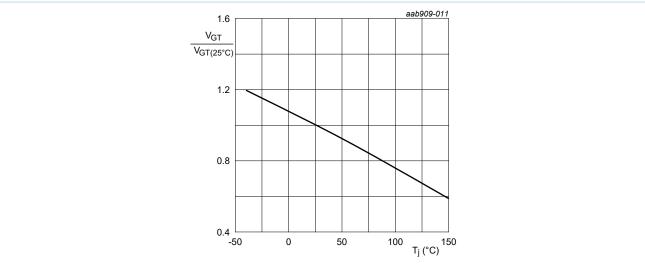
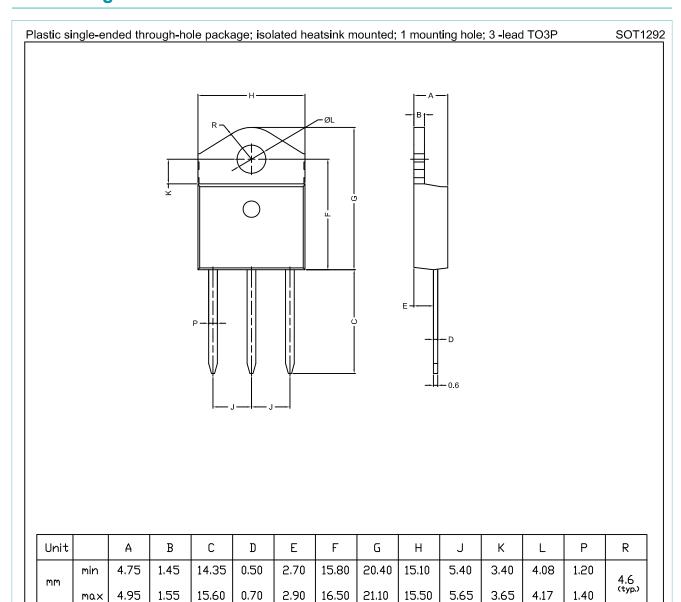


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

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12. Package outline



OUTLINE VERSION	REFERENCES				EUROPEAN	ISSUE DATE
	IEC	JEDEC	EIAJ		PROJECTION	1550E DATE
SOT1292		_				

Fig. 12. Package outline IITO3P (SOT1292)

13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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Наши контакты:

Телефон: +7 812 627 14 35

Электронная почта: sales@st-electron.ru

Адрес: 198099, Санкт-Петербург,

Промышленная ул, дом № 19, литера Н,

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