Atmel ATA6629/ATA6631 Development Board V2.2

Atmel ATA6629/ Atmel ATA6631 Development Board V2.2

Application Note

1. Introduction

The development board for the Atmel® ATA6629/ATA6631 (ATA6629-EK, ATA6631-EK) is designed to give users a quick start using these ICs and prototyping and testing new LIN designs.

The ATA6631 is a fully integrated LIN transceiver in compliance with LIN specification 2.0, 2.1 and SAEJ2602-2 with a 5V/85mA low drop voltage regulator. The ATA6629 is identical, but the output voltage of the regulator is 3.3V instead of 5V.

The Atmel ATA6629/ATA6631 are the successor ICs of the Atmel ATA6623/ATA6625 featuring enhanced EMC performance, reduced current consumption in silent mode, extended TXD time-out time and improved wake-up behavior, resulting in a very low sleep mode and silent mode current consumption even in the case of a floating bus or a short circuit between the bus line and GND.

The ICs are designed to handle the low-speed data communication in vehicles, e.g. in convenience electronics. Improved slope control at the LIN driver ensures secure data communication up to 20Kbaud.

This document has been created as a quick start guide on using the Atmel ATA6629/ATA6631 development board. For more detailed information about the use of these devices, please refer to the corresponding datasheet.

Figure 1-1. Atmel® ATA6629/ATA6631 Development Board V2.2

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1.1 Development Board Features

The development board for the Atmel ATA6629/ATA6631 supports the following features:

- **All Necessary Components are Mounted**
- **All Pins Easily Accessible**
- **Can be Used for Master or Slave Operation**

1.2 Quick Start

The development board for the Atmel ATA6629/ATA6631 is shipped with all necessary components to immediately start the development of a LIN slave node.

Connecting an external 12V DC power supply with the terminals VBAT and GND puts the Atmel ATA6629/ATA6631 in fail-safe mode and a DC voltage of 5V (3.3V) supplied by the internal voltage regulator can be measured between VCC and GND. In addition, the following voltage states can be measured at the pins RXD and LIN.

Table 1-1. Quick Start

	Atmel ATA6629	Atmel ATA6631			
	VCC	VCC	RXD	LIN	Transceiver
Fail-safe mode	3,3V	5V	Low	recessive	Off
Normal mode	3,3V	5V	LIN depending	TXD depending	On

Please note that the communication is still inactive during fail-safe mode.

In order to communicate via the LIN bus interface you have to switch the device to normal mode by applying the VCC voltage (5V or 3.3V respectively) at the EN pin.

2. Hardware Description

The following sections contain a brief description of normal operating conditions. Please refer to the respective datasheet for more information about any of the features mentioned.

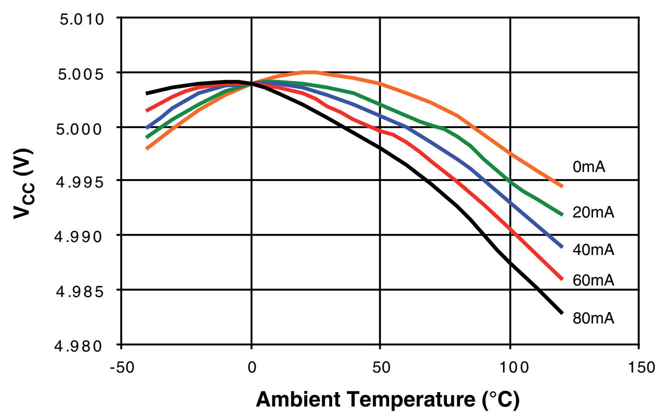
2.1 Power Supply (VBAT and GND)

In order to get the development board running, an external 5.7V - 27V DC power supply is required between the terminals VBAT and GND. The input circuit is protected against inverse polarity with the D1 protection diode, resulting in a difference between the VBAT and VS level of approximately 0.7V.

2.2 Voltage Regulator (VCC)

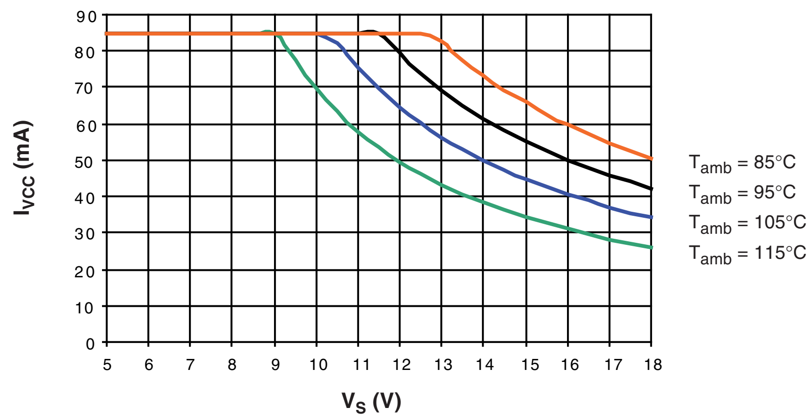
The internal 5V or 3.3V low drop voltage regulator is capable of driving loads up to 50mA over a wide range of supply voltage and ambient temperature with an accuracy of ±2%. This makes it possible to supply a microcontroller, sensors and/or other ICs. The V_{CC} output voltage versus the ambient temperature at different load currents is shown in Figure 2-1.

Figure 2-1. V_{CC} versus Temperature at Different Load Currents



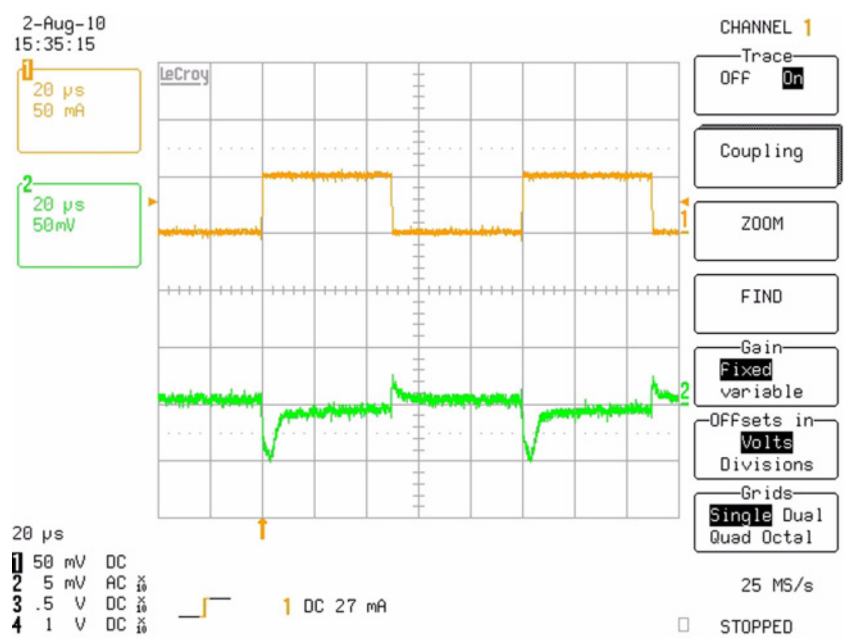
The voltage regulator is able to drive load currents higher than 50mA, but the limiting factor is the resulting power dissipation. The current limitation is specified with at least 85mA, meaning the circuit can deliver at least this current but due to the power dissipation not at a high supply voltage and/or high ambient temperature. With a special lead frame for the SO8 package, it is possible to achieve an excellent RthJA value of 80K/W; the resulting SOA curve is shown in Figure 2-2 on page 4.

Figure 2-2. SOA: IVCC versus V_S at Different Ambient Temperatures



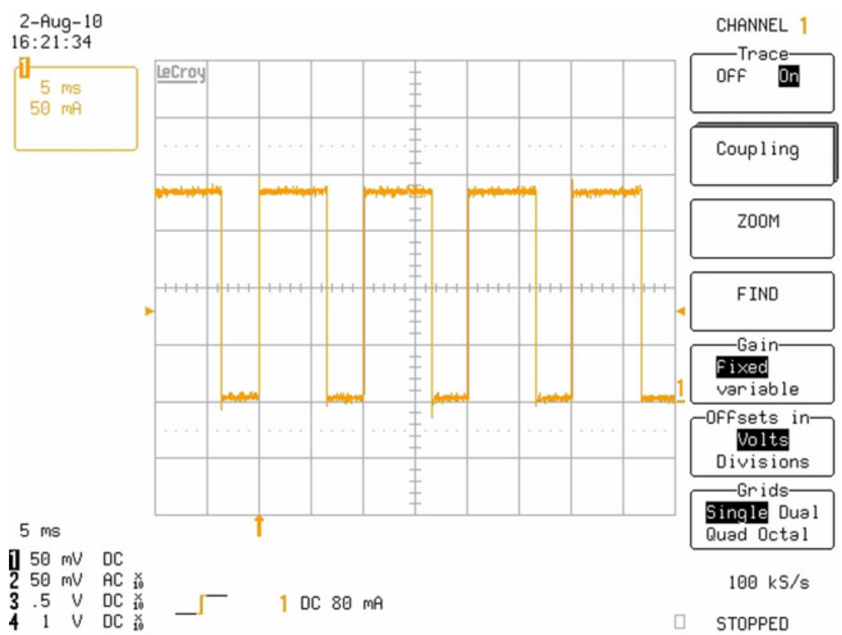
The voltage regulator is protected against overloads by means of current limitation and over-temperature shutdown. In addition, the output voltage is monitored and causes a reset signal at the NRES pin if it drops below the undervoltage threshold. The voltage regulator requires an external capacitor for compensation and for smoothing the disturbances from the microcontroller. Atmel® recommends using an electrolytic capacitor with C $\geq$ 1.8µF and a ceramic capacitor with C = 100nF. The values of these capacitors can be varied by the customer, depending on the application. But the ESR value of the electrolytic capacitor should be $0.2\Omega < ESR < 5\Omega$ in order to guarantee a stable behavior under all conditions (load, supply voltage, temperature). A Tantalum capacitor with 10µF and a ceramic capacitor with 100nF are mounted on the development board at the regulator's output. The diagram in Figure 2-3 shows what the load-transient response looks like with this external circuitry.

Figure 2-3. Load Transient Response, Ch1: I_{OUT}, Ch2: V_{CC}



At a short circuit between VCC and GND, the output limits the output current. Because of undervoltage, NRES switches to low and sends a reset to the microcontroller. The IC switches into fail-safe mode. If the chip temperature exceeds the overtemperature threshold, the VCC output switches off. The chip cools down and after the temperature hysteresis the output switches on again. Because of fail-safe mode, the VCC voltage switches on again even if EN is low. The resulting characteristic of the output current at a short circuit depends on the supply voltage, the ambient temperature, and the thermal connection of the IC to the PCB. The short-circuit current of the voltage regulator at room-temperature and a battery voltage of 13V is depicted in Figure 2-4 (settled state).

Figure 2-4. Voltage Regulator: Current Limitation at a Short-circuit between V_{CC} and GND



2.3 LIN Interface (LIN, TXD and RXD)

2.3.1 Bus Pin (LIN)

A low-side driver with internal current limitation, thermal shutdown, and an internal pull-up resistor in compliance with LIN spec 2.x is implemented. The internal pull-up resistor is active in normal and fail-safe mode. The LIN receiver thresholds comply with the LIN protocol specification. The reverse current from the LIN bus to V_S is < 2µs even in case of Vbat disconnection.

During a short circuit between the pin LIN and the battery voltage, the output limits the output current. Due to the power dissipation, the chip temperature exceeds the overtemperature threshold and the LIN output is switched off. The chip cools down and after the temperature hysteresis the output switches on again. RXD stays high because LIN is high. During LIN overtemperature switch-off the VCC regulator works independently.

On the board the LIN pin is assembled with a 220pF capacitor to GND. Additionally, the two extra components diode D2 (LL4148) in series with resistor R3 (1kΩ) needed for using the development board for a LIN master application have designated placeholders for convenient mounting.

2.3.2 Input Pin (TXD)

In normal mode the TXD pin is the microcontroller interface for controlling the LIN output state. TXD must be pulled to GND in order to have a low LIN Bus (dominant state). The TXD pin has an internal pull-up resistor. If TXD is high, the LIN output transistor is turned off with the bus in recessive state. If TXD is low, the LIN output transistor is turned on and the bus is in the dominant state. An internal timer prevents the bus line from being driven permanently in the dominant state. If TXD is forced to low longer than t_{DOM} > 27ms, the LIN pin is switched off (recessive mode). To reset this mode, TXD needs to be switched to high (> 10µs) before switching LIN to dominant again.

2.3.3 Output Pin (RXD)

This pin reports the state of the LIN bus to the microcontroller. LIN high (recessive state) is indicated by a high level at RXD, LIN low (dominant state) is reported by a low level at RXD. The output has an internal pull-up resistor with typ. 5kΩ to VCC. The output is short-circuit protected. RXD is switched off in unpowered mode.

Please note that the Atmel® ATA6629/ATA6631 has to be in normal mode in order to have the communication via LIN enabled.

After a wake-up the device is in fail-safe mode and the RXD pin switches to low in order to interrupt the microcontroller.

2.4 Undervoltage Reset Output (NRES)

The reset output is an open drain output, which is switched on in case of a V_{CC} undervoltage. The implemented undervoltage delay keeps NRES at a low level for approximately 4ms after V_{CC} reaches its nominal value. In order to pull up the output of the Atmel ATA6629/ATA6631, an external resistor connected to V_{CC} is required. On the development board this resistor (R2) is considered.

If a reset occurs (NRES is low), the circuit switches to fail- safe mode.

2.5 Enable Input (EN)

This pin controls the operating mode of the interface. If EN = 1 the circuit is in normal mode, with transmission paths from TXD to LIN and from LIN to RXD both active and the voltage regulator also switched on.

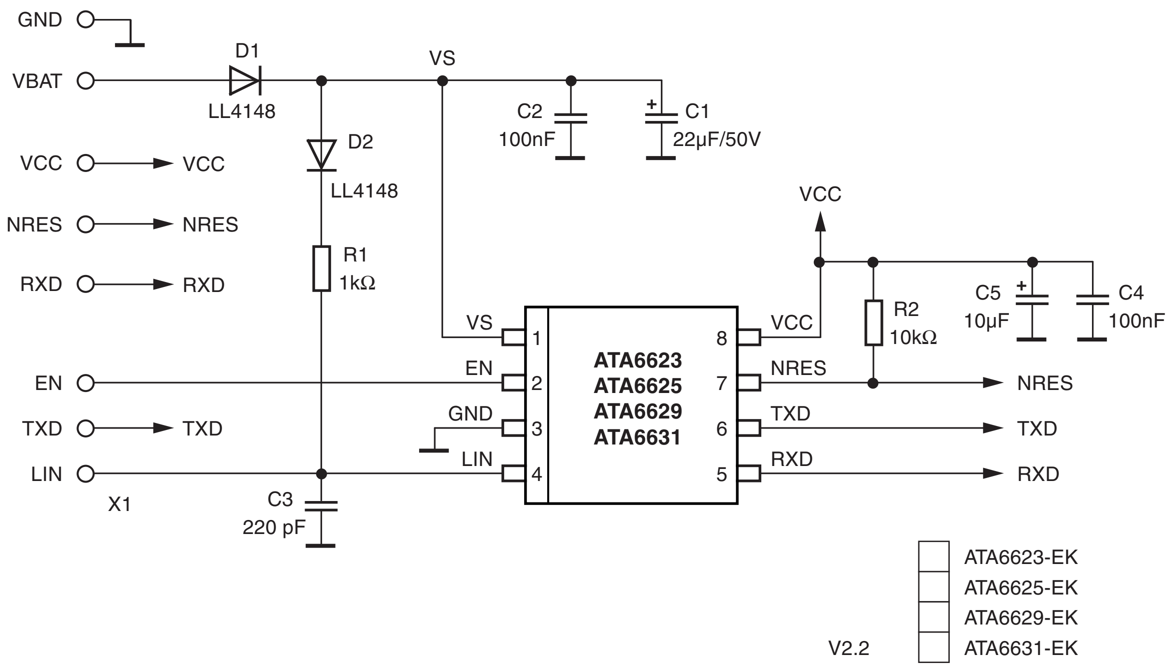
IF EN is switched to low while TXD is still high, the device is forced to silent mode. No data transmission is then possible, the LIN pin is pulled to VS by a weak current source, the current consumption is reduced to IVS typ. 40µA, but the voltage regulator has its full functionality.

If EN is switched to low while TXD is low, the device is forced into sleep mode, the LIN pin is pulled to VS by a weak current source, and the voltage regulator is switched off. During sleep mode the device is still supplied from the battery voltage, the supply current is typically 10µA. The pin EN provides a pull-down resistor in order to force the transceiver into sleep or silent mode if the pin is not connected.

In order to avoid any influence to the LIN pin while switching into sleep mode, it is possible to switch the EN to low up to 3.2µs earlier than the TXD. Therefore, the best and easiest way to switch the Atmel ATA6629/ATA6631 into sleep mode is with two simultaneous falling edges at TXD and EN.

3. Schematic and Layout of the Development Board for the Atmel ATA6629/ATA6631

Figure 3-1. Schematic of the Development Board for the Atmel® ATA6629/ATA6631



Note: 1. D2 and R1 are only necessary for a master node.

Figure 3-2. Board Component Placement; Top Side, Top View

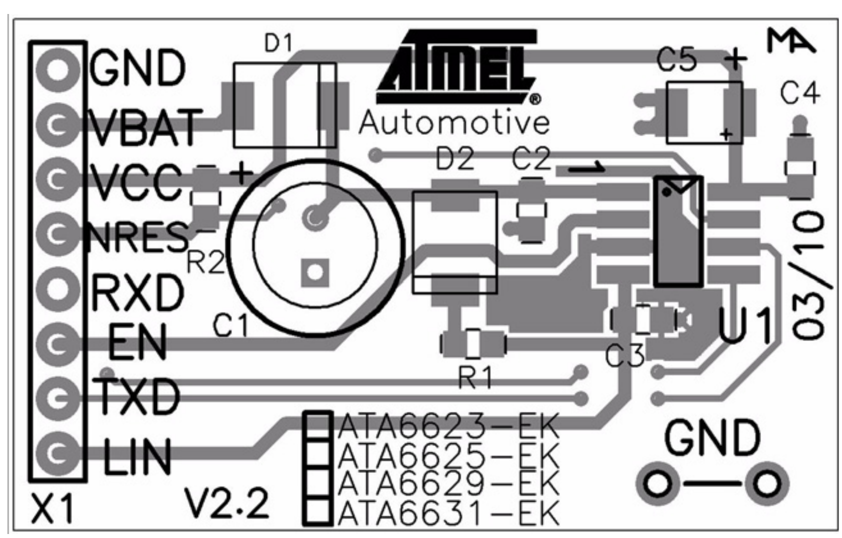


Figure 3-3. Atmel® ATA6629/ATA6631 Development Board; Top Side, Top View

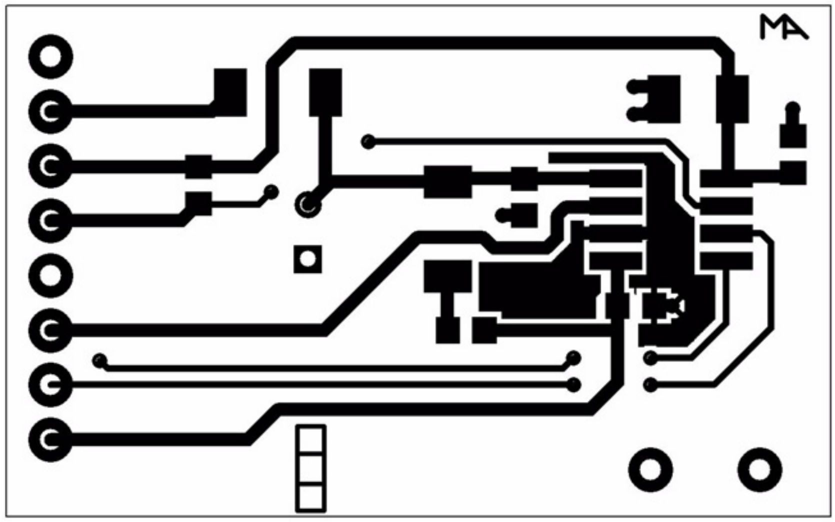
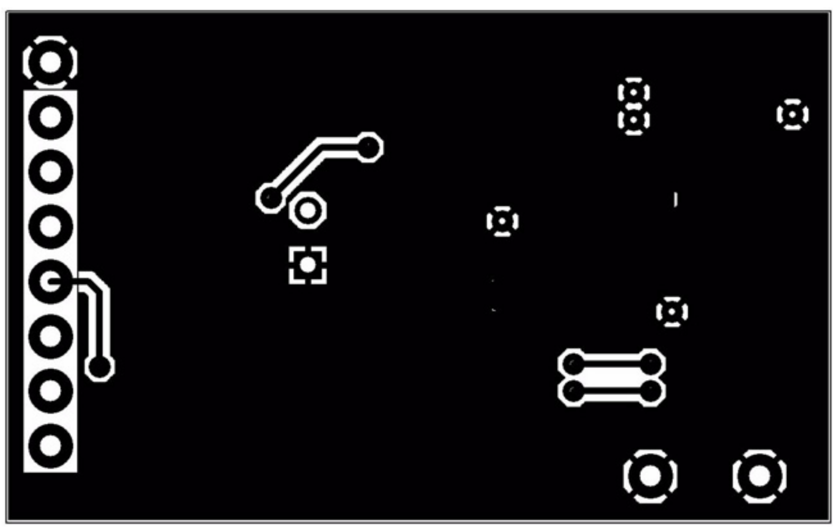


Figure 3-4. Atmel ATA6629/ATA6631 Development Board; Bottom Side, Top View (as if PCB was Transparent)



4. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
9203B-AUTO-03/11	• Section 1 “Introduction” on page 1 changed • Figure 2-2 “SOA: IVCC versus V_S at Different Ambient Temperatures” on page 4 changed

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