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**July 2010** 

## FDME1034CZT

## Complementary PowerTrench® MOSFET

N-channel: 20 V, 3.8 A, 66 m $\Omega$  P-channel: -20 V, -2.6 A, 142 m $\Omega$ 

#### **Features**

#### Q1: N-Channel

- Max  $r_{DS(on)}$  = 66 m $\Omega$  at  $V_{GS}$  = 4.5 V,  $I_D$  = 3.4 A
- Max  $r_{DS(on)} = 86 \text{ m}\Omega$  at  $V_{GS} = 2.5 \text{ V}$ ,  $I_D = 2.9 \text{ A}$
- Max  $r_{DS(on)} = 113 \text{ m}\Omega$  at  $V_{GS} = 1.8 \text{ V}$ ,  $I_D = 2.5 \text{ A}$
- Max  $r_{DS(on)} = 160 \text{ m}\Omega$  at  $V_{GS} = 1.5 \text{ V}$ ,  $I_D = 2.1 \text{ A}$

#### Q2: P-Channel

- Max  $r_{DS(on)}$  = 142 m $\Omega$  at  $V_{GS}$  = -4.5 V,  $I_D$  = -2.3 A
- Max  $r_{DS(on)} = 213 \text{ m}\Omega$  at  $V_{GS} = -2.5 \text{ V}$ ,  $I_D = -1.8 \text{ A}$
- Max  $r_{DS(on)} = 331 \text{ m}\Omega$  at  $V_{GS} = -1.8 \text{ V}$ ,  $I_D = -1.5 \text{ A}$
- Max  $r_{DS(on)}$  = 530 m $\Omega$  at  $V_{GS}$  = -1.5 V,  $I_D$  = -1.2 A
- Low profile: 0.55 mm maximum in the new package MicroFET 1.6x1.6 **Thin**
- Free from halogenated compounds and antimony oxides
- HBM ESD protection level > 1600 V (Note 3)
- RoHS Compliant



This device is designed specifically as a single package solution for a DC/DC 'Switching' MOSFET in cellular handset and other ultra-portable applications. It features an independent N-Channel & P-Channel MOSFET with low on-state resistance for minimum conduction losses. The gate charge of each MOSFET is also minimized to allow high frequency switching directly from the controlling device.

The MicroFET 1.6x1.6 **Thin** package offers exceptional thermal performance for it's physical size and is well suited to switching and linear mode applications.

### **Applications**

- DC-DC Conversion
- Level Shifted Load Switch



MicroFET 1.6x1.6 Thin

## MOSFET Maximum Ratings T<sub>A</sub> = 25 °C unless otherwise noted

Symbol	Symbol Parameter			Q1	Q2	Units
V <sub>DS</sub>	Drain to Source Voltage			20	-20	V
V <sub>GS</sub>	Gate to Source Voltage			±8	±8	V
	Drain Current -Continuous	T <sub>A</sub> = 25 °C	(Note 1a)	3.8	-2.6	^
ID	-Pulsed			6	-6	A
D	Power Dissipation for Single Operation $T_A = 25 ^{\circ}\text{C}$ (Note 1a)		(Note 1a)		1.4	W
$P_{D}$	Power Dissipation for Single Operation	T <sub>A</sub> = 25 °C	(Note 1b)	e 1b) 0.6		VV
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Tempera	ature Range		-55 t	to +150	°C

#### **Thermal Characteristics**

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Single Operation)	(Note 1a)	90	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Single Operation)	(Note 1b)	195	C/VV

#### **Package Marking and Ordering Information**

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
5T	FDME1034CZT	MicroFET 1.6x1.6 <b>Thin</b>	7 "	8 mm	5000 units

## **Electrical Characteristics** $T_J = 25$ °C unless otherwise noted

Symbol	Parameter	Test Conditions	Туре	Min	Тур	Max	Units
Off Chara	cteristics						
BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	Q1	20			V
Dialii to Source Breakdown Voltage	$I_D = -250 \mu A, V_{GS} = 0 V$	Q2	-20			V	
ΔBV <sub>DS</sub> S ΔΤ <sub>J</sub>		$I_D = 250 \mu A$ , referenced to 25 °C	Q1		16		mV/°C
$\Delta T_{J}$	Coefficient	$I_D$ = -250 $\mu$ A, referenced to 25 °C	Q2		-12		IIIV/ C
	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 16 V, V <sub>GS</sub> = 0 V	Q1			1	μА
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	$V_{DS} = -16 \ V, \ V_{GS} = 0 \ V$	Q2			-1	μΑ
I <sub>GSS</sub>	Gate to Source Leakage Current	$V_{GS} = \pm 8 \text{ V}, V_{DS} = 0 \text{ V}$	All			±10	μΑ

#### **On Characteristics**

V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, \ I_D = 250 \ \mu A$ $V_{GS} = V_{DS}, \ I_D = -250 \ \mu A$	Q1 Q2	0.4 -0.4	0.7 -0.6	1.0 -1.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D$ = 250 $\mu$ A, referenced to 25 °C	Q1 Q2		-3 2		mV/°C
		$V_{GS} = 4.5 \text{ V}, I_D = 3.4 \text{ A}$			55	66	
		$V_{GS} = 2.5 \text{ V}, I_D = 2.9 \text{ A}$			68	86	
		$V_{GS} = 1.8 \text{ V}, I_D = 2.5 \text{ A}$	Q1		85	113	- mΩ
		$V_{GS} = 1.5 \text{ V}, I_D = 2.1 \text{ A}$	QI		106	160	
_		$V_{GS} = 4.5 \text{ V}, I_D = 3.4 \text{ A},$ $T_J = 125 ^{\circ}\text{C}$			76	112	
r <sub>DS(on)</sub>	Drain to Source On Resistance	$V_{GS} = -4.5 \text{ V}, I_D = -2.3 \text{ A}$			95	142	
		$V_{GS} = -2.5 \text{ V}, I_D = -1.8 \text{ A}$			120	213	
		$V_{GS} = -1.8 \text{ V}, I_D = -1.5 \text{ A}$	Q2		150	331	
		$V_{GS} = -1.5 \text{ V}, I_D = -1.2 \text{ A}$	QZ		190	530	
		$V_{GS} = -4.5 \text{ V}, I_D = -2.3 \text{ A},$ $T_J = 125 ^{\circ}\text{C}$			128	190	
9 <sub>FS</sub>	Forward Transconductance	$V_{DS} = 4.5 \text{ V}, I_{D} = 3.4 \text{ A}$ $V_{DS} = -4.5 \text{ V}, I_{D} = -2.3 \text{ A}$	Q1 Q2		9 7		S

### **Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	Q1	Q1 Q2	225 305	300 405	pF
C <sub>oss</sub>	Output Capacitance	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0 V, f = 1 MHz Q2	Q1 Q2	40 55	55 75	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	$V_{DS} = -10 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	Q1 Q2	25 50	40 75	pF

### **Switching Characteristics**

t <sub>d(on)</sub>	Turn-On Delay Time	Q1	Q1 Q2	4.5 4.7	10 10	
t <sub>r</sub>	Rise Time	$V_{DD} = 10 \text{ V}, I_{D} = 1 \text{ A},$ $V_{GS} = 4.5 \text{ V}, R_{GEN} = 6 \Omega$	Q1 Q2	2.0 4.8	10 10	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	Q2 V <sub>DD</sub> = -10 V, I <sub>D</sub> = -1 A,	Q1 Q2	15 33	27 53	
t <sub>f</sub>	Fall Time	$V_{GS} = -4.5 \text{ V}, R_{GEN} = 6 \Omega$	Q1 Q2	1.7 16	10 29	
Qg	Total Gate Charge	Q1 V <sub>DD</sub> = 10 V, I <sub>D</sub> = 3.4 A,	Q1 Q2	3 5.5	4.2 7.7	
Q <sub>gs</sub>	Gate to Source Gate Charge	V <sub>GS</sub> = 4.5 V Q2	Q1 Q2	0.4 0.6		nC
Q <sub>gd</sub>	Gate to Drain "Miller" Charge	$V_{DD} = -10 \text{ V}, I_{D} = -2.3 \text{ A}, V_{GS} = -4.5 \text{ V}$	Q1 Q2	0.6 1.4		

## **Electrical Characteristics** $T_J = 25$ °C unless otherwise noted

Symbol	Parameter	Parameter Test Conditions		Min	Тур	Max	Units
Drain-Sou	urce Diode Characteristics						
V <sub>SD</sub>	Source to Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_S = 0.9 \text{ A}$ (Note 2) $V_{GS} = 0 \text{ V}, I_S = -0.9 \text{ A}$ (Note 2)			0.7 -0.8	1.2 -1.2	V
t <sub>rr</sub>	Reverse Recovery Time	Q1 I <sub>F</sub> = 3.4 A, di/dt = 100 A/μS	Q1 Q2		8.5 16	17 29	ns
Q <sub>rr</sub>	Reverse Recovery Time	Q2 I <sub>F</sub> = -2.3 A, di/dt = 100 A/μs	Q1 Q2		1.4 4.4	10 10	nC

#### Notes

Notes. 1. R<sub>0JA</sub> is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R<sub>0JC</sub> is guaranteed by design while R<sub>0CA</sub> is determined by the user's board design.



a. 90 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



 b. 195 °C/W when mounted on a minimum pad of 2 oz copper.

- 2. Pulse Test: Pulse Width < 300  $\mu$ s, Duty cycle < 2.0%.
- 3. The diode connected between the gate and source serves only as protection ESD. No gate overvoltage rating is implied.

### Typical Characteristics (Q1 N-Channel) T<sub>J</sub> = 25°C unless otherwise noted

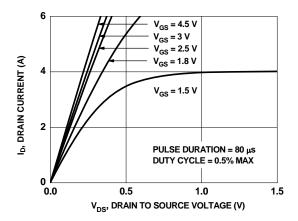


Figure 1. On Region Characteristics

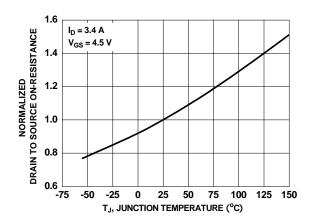


Figure 3. Normalized On Resistance vs Junction Temperature

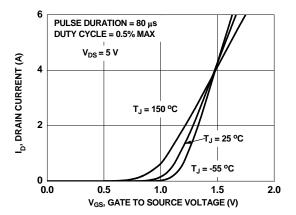


Figure 5. Transfer Characteristics

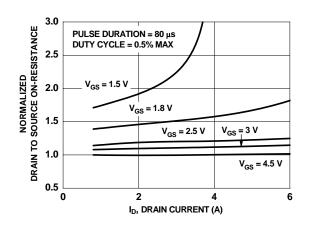


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

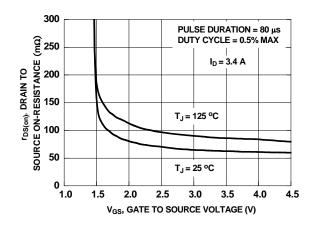


Figure 4. On-Resistance vs Gate to Source Voltage

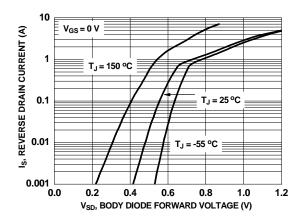


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

### Typical Characteristics (Q1 N-Channel) T<sub>J</sub> = 25°C unless otherwise noted

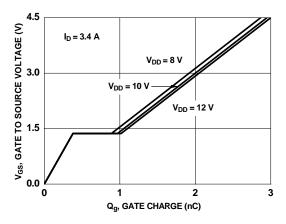


Figure 7. Gate Charge Characteristics

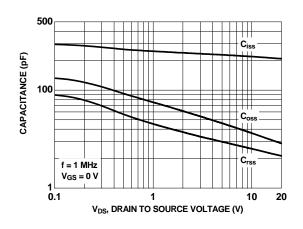


Figure 8. Capacitance vs Drain to Source Voltage

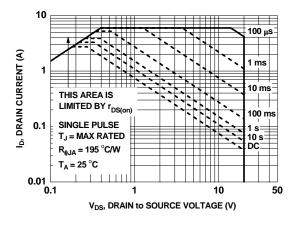


Figure 9. Forward Bias Safe Operating Area

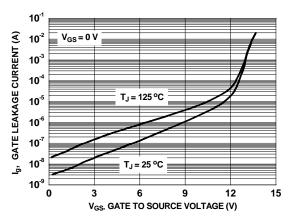


Figure 10. Gate Leakage Current vs Gate to Source Voltage

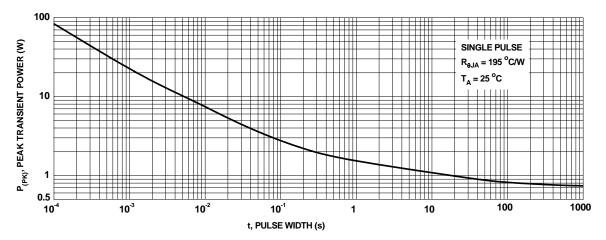


Figure 11. Single Pulse Maximum Power Dissipation

## Typical Characteristics (Q1 N-Channel) $T_J = 25$ °C unless otherwise noted

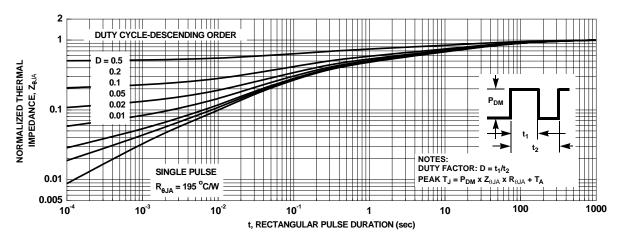


Figure 12. Junction-to-Ambient Transient Thermal Response Curve

### Typical Characteristics (Q2 P-Channel) T<sub>J</sub> = 25 °C unless otherwise noted

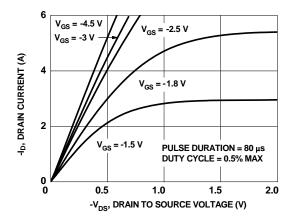


Figure 13. On- Region Characteristics

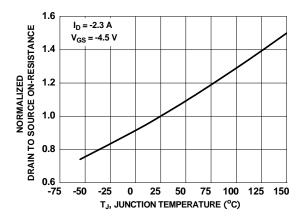


Figure 15. Normalized On-Resistance vs Junction Temperature

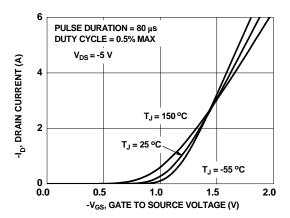


Figure 17. Transfer Characteristics

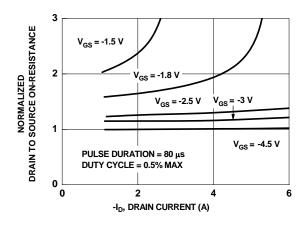


Figure 14. Normalized on-Resistance vs Drain Current and Gate Voltage

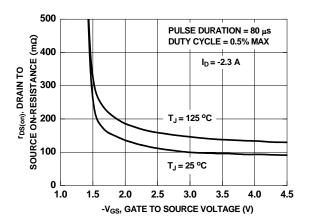


Figure 16. On-Resistance vs Gate to Source Voltage

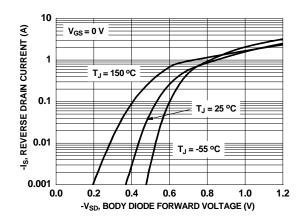


Figure 18. Source to Drain Diode Forward Voltage vs Source Current

#### Typical Characteristics (Q2 P-Channel) T<sub>.i</sub> = 25°C unless otherwise noted

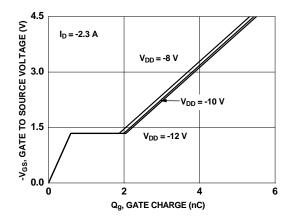


Figure 19. Gate Charge Characteristics

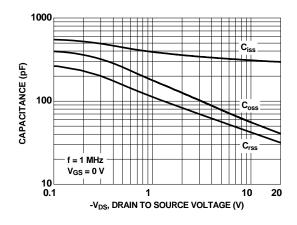


Figure 20. Capacitance vs Drain to Source Voltage

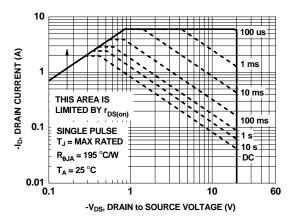


Figure 21. Forward Bias Safe Operating Area

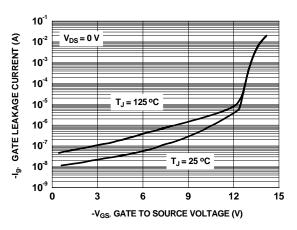


Figure 22. Gate Leakage Current vs Gate to Source Voltage

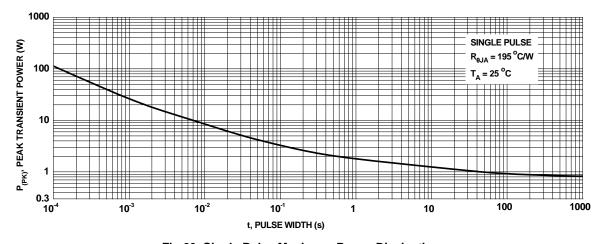


Fig 23. Single Pulse Maximum Power Dissipation

## Typical Characteristics (Q2 P-Channel) T<sub>J</sub> = 25 °C unless otherwise noted

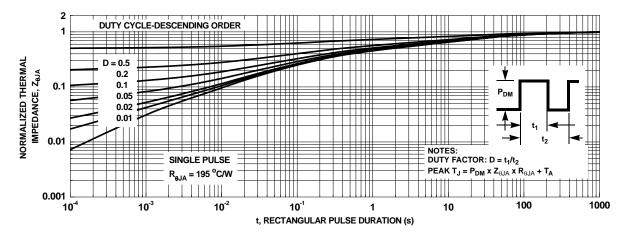
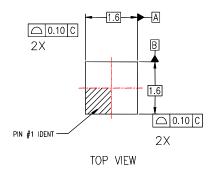
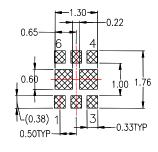


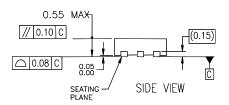
Figure 24. Junction-to-Ambient Transient Thermal Response Curve

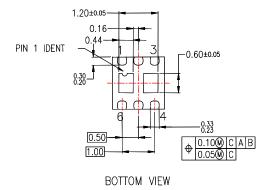
## **Dimensional Outline and Pad Layout**





RECOMMENDED LAND PATTERN









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Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.
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