MP3391

8-Channel, 120mA/ch Step-Up WLED Driver Controller

The Future of Analog IC Technology®

DESCRIPTION

The MP3391 is a step-up controller with 8-channel current sources designed for driving the WLED arrays for large size LCD panel backlighting applications.

The MP3391 uses current mode, fixed frequency architecture. The switching frequency is programmable by an external frequency setting resistor. It drives an external MOSFET to boost up the output voltage from a 9V to 35V input supply. The MP3391 regulates the current in each LED string to the programmed value set by an external current setting resistor.

The MP3391 applies 8 internal current sources for current balance. And the current matching can achieve 2.5% regulation accuracy between strings. Its low regulation voltage on LED current sources reduces power loss and improves efficiency.

PWM dimming is implemented with external PWM input signal or DC input signal. The dimming PWM signal can be generated internally, and the dimming frequency is programmed by an external setting capacitor.

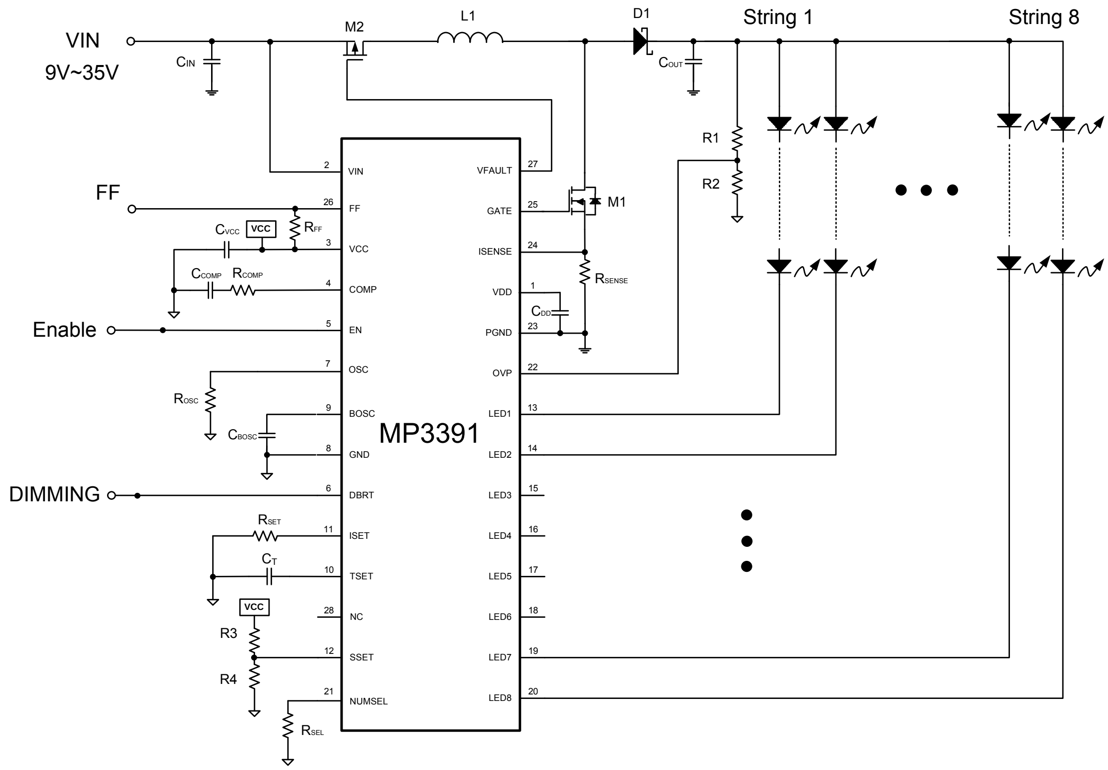
FEATURES

- 9V to 35V Input Voltage Range
- 10V MOSFET Gate Driver
- Drive Selectable 8, 6 and 4 Strings of LEDs
- Maximum 120mA for Each String
- 2.5% Current Matching Accuracy Between Strings
- Programmable Switching Frequency
- PWM or DC Input Burst PWM Dimming
- Open/Short protection and Fault Flag Output
- Programmable Short Protection Voltage and Time Threshold
- Programmable Over-voltage Protection
- Flexible Extendable LED Channels Application
- Thermal Shutdown
- 28-pin TSSOP and 28-pin SOIC Package

APPLICATIONS

- Desktop LCD Flat Panel Displays
- Flat Panel Video Displays
- LCD TVs and Monitors

TYPICAL APPLICATION

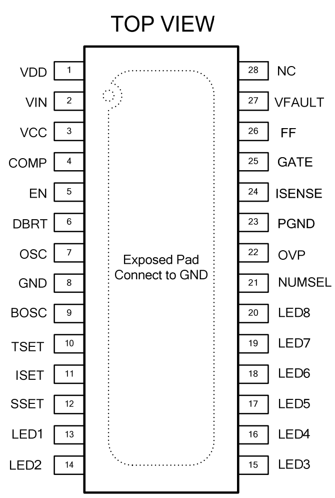


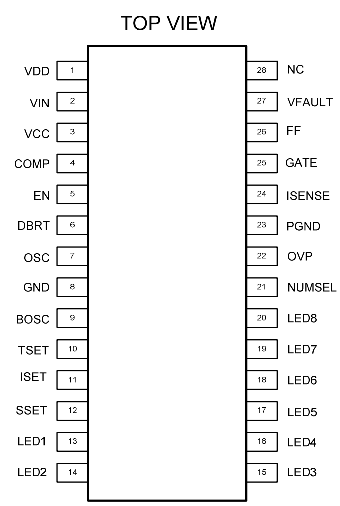
ORDERING INFORMATION

Part Number	Package	Top Marking	Free Air Temperature (T_A)
MP3391EF*	TSSOP28	MP3391EF	-20°C to +85°C
MP3391EY**	SOIC28	MP3391EY	-20°C to +85°C

***For Tape & Reel, add suffix –Z (eg. MP3391EF–Z).**
For RoHS compliant packaging, add suffix –LF (eg. MP3391EF–LF–Z)
****For Tape & Reel, add suffix –Z (eg. MP3391EY–Z).**
For RoHS compliant packaging, add suffix –LF (eg. MP3391EY–LF–Z)

PACKAGE REFERENCE





TSSOP28	SOIC28

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} ....-0.3V to +40V
V_{FAULT} ....V_{IN}-6V to V_{IN}
V_{GATE} ....-0.5V to 12V
V_{LED1} to V_{LED8}....................................-1V to +55V
All Other Pins...............................-0.3V to +6.3V
Continuous Power Dissipation (T_A = +25°C) (2)
TSSOP28……………………………… ...3.9 W
SOIC28………………………………… ...2.1W
Junction Temperature ....150°C
Lead Temperature ....260°C
Storage Temperature............... -65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage V_{IN} ....9V to 35V
LED Current (Backlight) ....10mA to 120mA
Maximum Junction Temp. (T_J)................+125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

TSSOP28................................32 .... 6 .... °C/W
SOIC28 ....60 ...... 30 ... °C/W

Notes:
1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operation conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} =18V, V_{EN} = 5V, T_A = +25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Operating Input Voltage	V_{IN}		9		35	V
Supply Current (Quiescent)	I_Q	V_{IN}=18V, V_{EN}=5V, no load no switching, R_{ISET}=20kΩ		3.5		mA
Supply Current (Shutdown)	I_{ST}	V_{EN}=0V, V_{IN}=18V			2	µA
VCC Output Voltage	V_{CC}	V_{EN}=5V, 6V<V_{IN}<35V, 0<I_{VCC}<10mA	4.5	5	5.5	V
VCC UVLO Threshold	V_{CC_UVLO}	Rising Edge	3.4	3.9	4.3	V
VCC UVLO Hysteresis				200		mV
VDD Output Voltage	V_{DD}	V_{EN}=5V, 12V<V_{IN}<35V, 0<I_{VDD}<15mA	9	10	11	V
VDD UVLO Threshold	V_{CC_UVLO}	Rising Edge	6.8	7.3	7.8	V
VDD UVLO Hysteresis				500		mV
EN High Voltage	V_{EN_HIGH}	V_{EN} Rising	1.6			V
EN Low Voltage	V_{EN_LOW}	V_{EN} Falling			0.8	V
NUMSEL High Threshold	V_{NUMSEL_HI}	Rising, 6 strings	3			V
NUMSEL Low Threshold	V_{NUMSEL_LO}	Falling, 4 strings			0.8	V
STEP-UP CONVERTER						
Gate Driver Impedance (Sourcing)	R_{GH}	V_{DD}=10V,I_{GATE}=10mA		4.5		Ω
Gate Driver Impedance (Sinking)	R_{GL}	V_{DD}=10V,I_{GATE}=-10mA		1.5		Ω
Gate Maximum Source Current	I_{SOURCE}			0.4		A
Gate Maximum Sink Current	I_{SINK}			1		A
Switching Frequency	f_{SW}	R_{OSC}= 50kΩ	235	280	325	kHz
OSC Voltage	V_{OSC}		1.20	1.23	1.26	V
Minimum On Time	T_{ON_MIN}	PWM Mode, when no pulse skipping happens		200		ns
Maximum Duty Cycle	D_{MAX}		90			%
ISENSE Limit		90% Duty Cycle	175	230	285	mV
COMP Source Current Limit	$I_{COMP\ SOLI}$			200		µA
COMP Sink Current Limit	$I_{COMP\ SILI}$			50		µA
PWM DIMMING						
DBRT Leakage Current	I_{DBRT_LK}		-5		+5	µA
BOSC Frequency	F_{BOSC}	C_{BOSC}=2.2nF	1.2	1.6	2	kHz
BOSC Output Current	I_{BOSC}		5.7	7.0	7.9	µA

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} =18V, V_{EN} = 5V, T_A = +25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
LED CURRENT REGULATION						
ISET Voltage	V_{ISET}		1.21	1.23	1.25	V
LEDX Average Current	I_{LED}	R_{ISET}=20kΩ	58.9	60.4	61.9	mA
Current Matching (5)		ILED=60.4mA			2.5	%
LEDX Regulation Voltage	VLEDX	ILED=60.4mA		450		mV
PROTECTION						
OVP Over Voltage Threshold	V_{OVP_OV}	Rising Edge	1.20	1.24	1.28	V
OVP UVLO threshold	V_{OVP_UV}	Step-up Converter Fails	50	80	110	mV
LEDX UVLO Threshold	V_{LEDX_UV}		140	190	240	mV
SSET Voltage Gain		Short LED Voltage Threshold	4.2	4.5	4.8	
TSET Source Current	I_{TSET}		40	50	60	μA
TSET Fault Threshold			1.20	1.24	1.28	V
Thermal Shutdown Threshold	T_{ST}			150		℃
FF Pull Down Resistance	R_{FF}			100		Ω
VFAULT Pull Down Current	IFAULT		40	55	70	μA
VFAULT Blocking-Off Voltage (with Respect to VIN)	VFAULT	VIN =18V, VIN-VFAULT		6		V

Notes:

5) Matching is defined as the difference of the maximum to minimum current divided by 2 times average currents.

PIN FUNCTIONS

Pin #	Name	Description
1	VDD	The Internal 10V Linear Regulator Output. VDD provides power supply for the internal MOSFET switch gate driver circuitry. Bypass VDD to GND with a ceramic capacitor.
2	VIN	Supply Input. VIN supplies the power to the chip, Drive VIN with 9V to 35V power source. Must be locally bypassed with a ceramic capacitor..
3	VCC	Option NC. The Internal 5V Linear Regulator Output. VCC provides power supply for the internal control circuitry. Bypass VCC to GND with a ceramic capacitor.
4	COMP	Step-up Converter Compensation Pin. This pin is used to compensate the regulation control loop. Connect a capacitor or a series RC network from COMP to GND.
5	EN	Enable Control Input. Do not let this pin floating.
6	DBRT	Brightness Control Input. To use external PWM dimming mode, apply a PWM signal on this pin for brightness control. To use DC input PWM dimming mode, apply a DC voltage range from 0.2V to 1.2V on this pin linearly to set the internal dimming duty cycle from 0% to 100%. The MP3391 has positive dimming polarity on DBRT.
7	OSC	Switching Frequency Set. Connect a resistor between OSC and GND to set the step-up converter switching frequency. The voltage at this pin is regulated to 1.23V. The clock frequency is proportional to the current sourced from this pin.
8	GND	Analog Ground.
9	BOSC	Dimming Repetition Set. This is the timing pin for the oscillator to set the dimming frequency. To use DC input PWM dimming mode, connect a capacitor from this pin to GND to set the internal dimming frequency. A saw-tooth waveform is generated on this pin. To use external PWM dimming mode, connect a resistor from this pin to GND, and apply the PWM signal on DBRT pin.
10	TSET	Short LED Protection Timer Set. Connect a ceramic capacitor on this pin to set the protection timer. The protection is triggered when internal 50uA current source charges the capacitor voltage to 1.24V. Tset(ms)=0.0248×C(nF), Tset is about 11.7ms for 470nF capacitor.
11	ISET	LED Current Set. Tie a current setting resistor from this pin to ground to program the current in each LED string. This pin voltage is regulated to 1.23V. the LED current is proportional to the current through the ISET resistor.
12	SSET	Short LED Protection Voltage Threshold Set. Connect this pin to VCC through external divide resistors to set the short LED protection threshold. When LEDX pin voltage reaches 4.5 times of SSET pin voltage, the TSET pin capacitor is charged up for a protection timer. Vshort= 4.5×Vsset.
13	LED1	LED String 1 Current Input. This pin is the open-drain output of an internal dimming control switch. Connect the LED String 1 cathode to this pin.
14	LED2	LED String 2 Current Input. This pin is the open-drain output of an internal dimming control switch. Connect the LED String 2 cathode to this pin.
15	LED3	LED String 3 Current Input. This pin is the open-drain output of an internal dimming control switch. Connect the LED String 3 cathode to this pin.

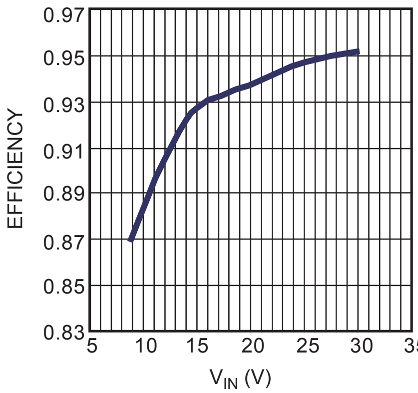
PIN FUNCTIONS *(continued)*

Pin #	Name	Description
16	LED4	LED String 4 Current Input. This pin is the open-drain output of an internal dimming control switch. Connect the LED String 4 cathode to this pin.
17	LED5	LED String 5 Current Input. This pin is the open-drain output of an internal dimming control switch. Connect the LED String 5 cathode to this pin.
18	LED6	LED String 6 Current Input. This pin is the open-drain output of an internal dimming control switch. Connect the LED String 6 cathode to this pin.
19	LED7	LED String 7 Current Input. This pin is the open-drain output of an internal dimming control switch. Connect the LED String 7 cathode to this pin.
20	LED8	LED String 8 Current Input. This pin is the open-drain output of an internal dimming control switch. Connect the LED String 8 cathode to this pin.
21	NUMSEL	Number of LED String Selection. Set this pin high enables the 6 strings (LED1~LED6) operation. Pull this pin low enables the 4 strings (LED1~LED4) operation. Float this pin enables the 8 strings operation.
22	OVP	Over-voltage Protection Input. Connect a resistor divider from output to this pin to program the OVP threshold. When this pin voltage reaches 1.24V, the MP3391 triggers Over Voltage Protection mode.
23	PGND	Step-up Converter Power Ground.
24	ISENSE	Current Sense Input. During normal operation, this pin senses the voltage across the external inductor current sensing resistor for peak current mode control and also to limit the inductor current during every switching cycle.
25	GATE	Step-up Converter Power Switch Gate Output. This pin drives the external power N-MOS device.
26	FF	Fault Flag. It is the drain of internal N-channel MOSFET. When open/short protection is triggered, the FF pin is pulled to GND.
27	VFAULT	Fault Disconnection Switch Driver Output. When the system starts up normally, this pin turns on the external PMOS. When the Vout is shorted to GND or MP3391 is disabled, the external PMOS is turned off to disconnect the input and output.
28	NC	No Connection

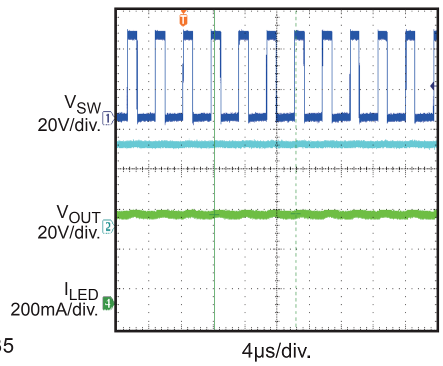
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} =15V, 14 LEDs in series, 8 strings parallel, 60mA/string, unless otherwise noted.

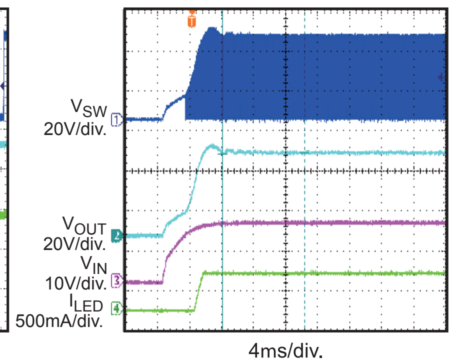
Efficiency vs. Input Voltage



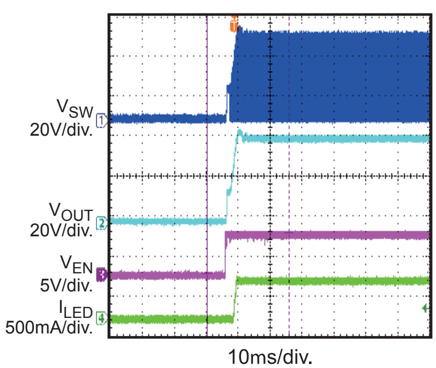
Steady State



Vin Startup

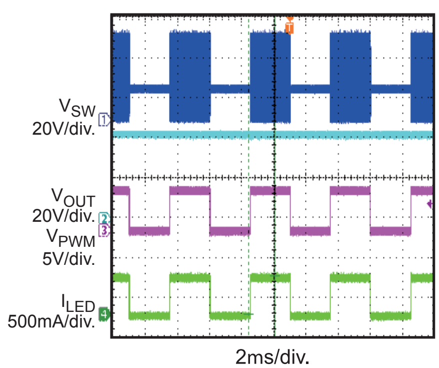


Ven Startup



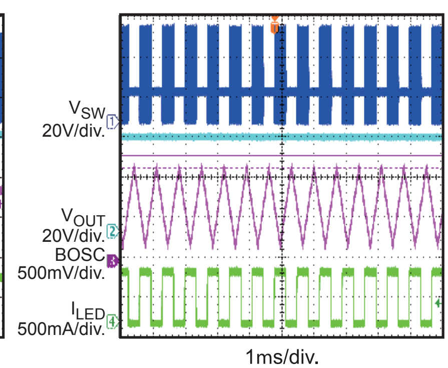
External PWM Dimming

f_{PWM} = 200Hz, D_{PWM} = 50%



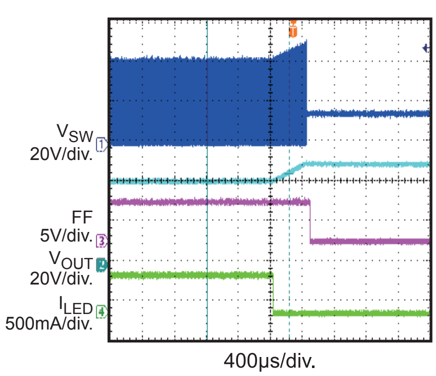
DC Burst Dimming

C_{BOSC} = 2.2nF, V_{PWMI} = 0.7V



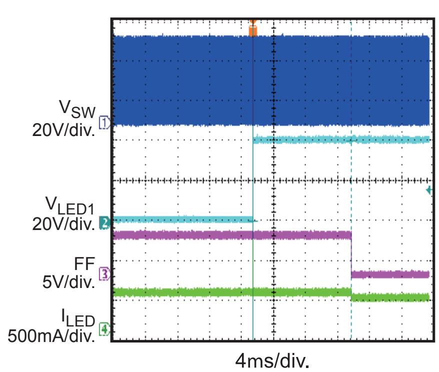
Open LED Protection

open all LED strings at working



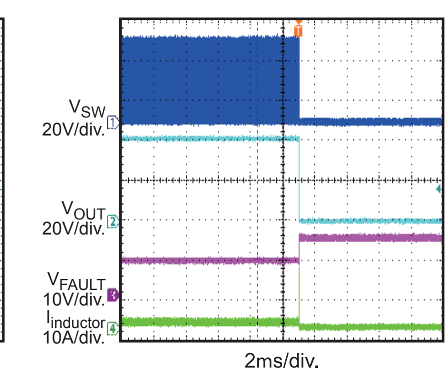
Short LED Protection

short V_{OUT} to LEDx at working



Short LED Protection

short V_{OUT} to GND at working



FUNCTION DIAGRAM

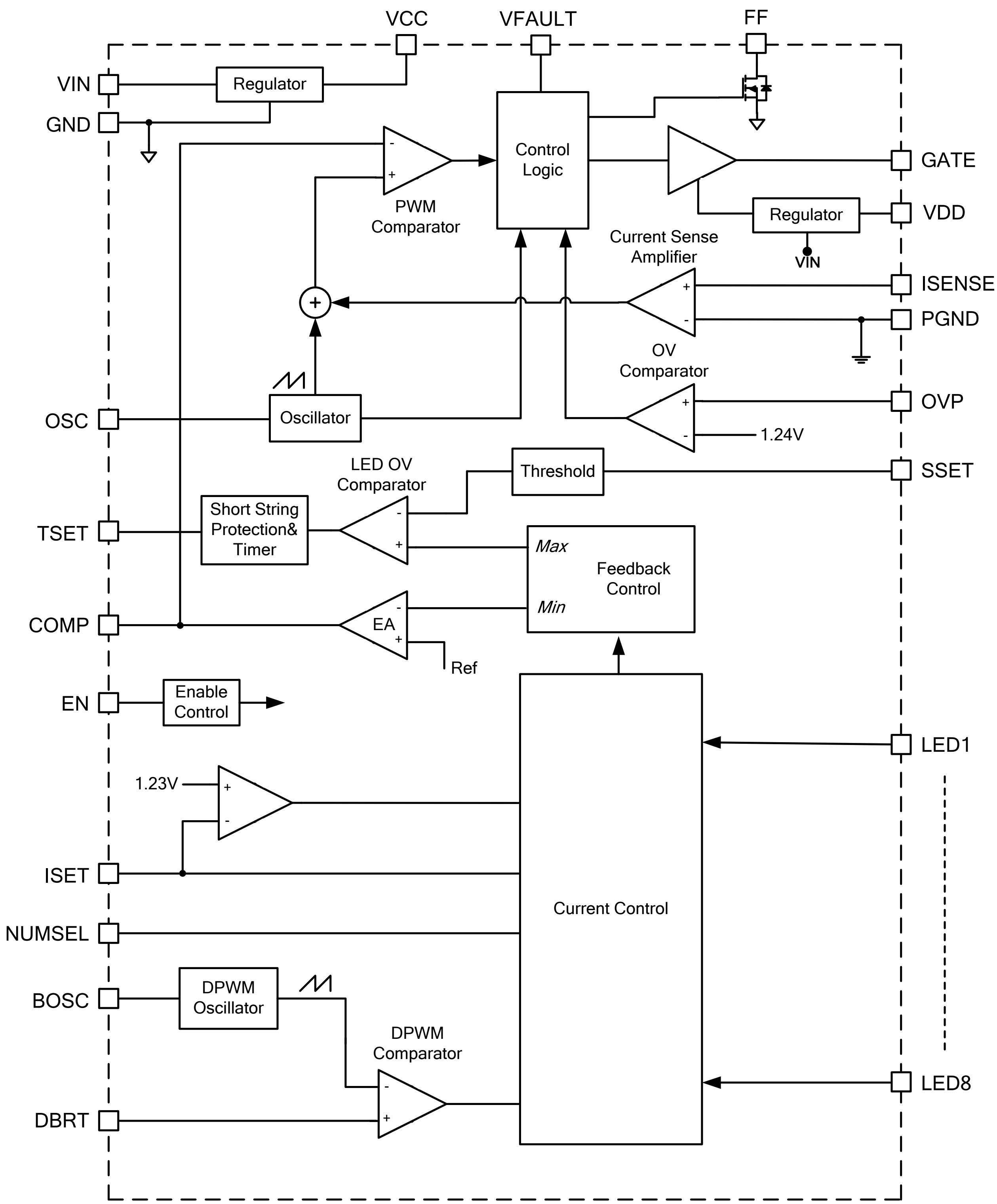


Figure 1—MP3391 Function Block Diagram

OPERATION

The MP3391 employs a programmable constant frequency, peak current mode step-up converter and 8-channels regulated current sources to regulate the array of 8 strings white LEDs. The number of LED string is selected by NUMSEL pin for 8/6/4 LED strings. The operation of the MP3391 can be understood by referring to the block diagram of Figure 1.

Internal Regulator

The MP3391 includes two internal linear regulators (VCC and VDD). VCC regulator offers a 5V power supply for the internal control circuitry. VDD regulator offers a 10V power supply for the external MOSFET switch gate driver. The VCC and VDD voltage drops to 0V when the chip shuts down. The MP3391 features Under Voltage Lockout. The chip is disabled until VCC exceeds the UVLO threshold. And the hysteresis of UVLO is approximately 200mV.

System Startup

When the MP3391 is enabled, the chip monitors the OVP pin to see if the Schottky diode is not connected or the boost output is short to GND. If the OVP voltage is lower than 80mV, the chip will be disabled. The MP3391 will also check other safety limits, including UVLO and OTP after the OVP test is passed. If they are all in function, it then starts boosting the step-up converter with an internal soft-start.

It is recommended on the start up sequence that the enable signal comes after input voltage and PWM dimming signal established.

Step-up Converter

The converter operation frequency is programmable (from 60kHz to 900kHz) with a external set resistor on OSC pin, which is helpful for optimizing the external components sizes and improving the efficiency.

At the beginning of each cycle, the external MOSFET is turned with the internal clock. To prevent sub-harmonic oscillations at duty cycles greater than 50 percent, a stabilizing ramp is added to the output of the current sense amplifier and the result is fed into the PWM comparator. When this result voltage reaches the output voltage of the error amplifier (V_{COMP}) the external MOSFET is turned off.

The voltage at the output of the internal error amplifier is an amplified signal of the difference between the reference voltage and the feedback voltage. The converter automatically chooses the lowest active LEDX pin voltage for providing enough bus voltage to power all the LED arrays.

If the feedback voltage drops below the 450mV reference, the output of the error amplifier increases. It results in more current flowing through the power FET, thus increasing the power delivered to the output. In this way it forms a close loop to make the output voltage in regulation.

At light-load or Vout near to Vin operation, the converter runs into the pulse-skipping mode, the FET is turned on for a minimum on-time of approximately 100ns, and then the converter discharges the power to the output in the remain period. The external MOSFET will keep off until the output voltage needs to be boosted again.

Dimming Control

The MP3391 provides two PWM dimming methods: external PWM signal or DC input PWM Dimming mode (see Figure 2). Both methods results in PWM chopping of the current in the LEDs for all 8 channels to provide LED control.

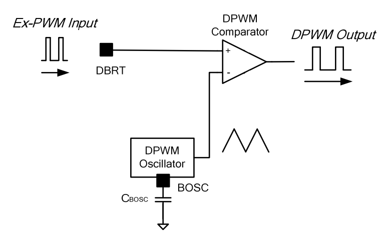


Figure 2—PWM Dimming Method

When bias the BOSC pin to a DC level, applying a PWM signal to the DBRT pin to achieve the PWM dimming. A DC analog signal can be directly applied to the DBRT pin to modulate the LED current with a capacitor on BOSC pin. And the DC signal is then converted to a DPWM dimming signal at the setting oscillation frequency.

The brightness of the LED array is proportional to the duty cycle of the DPWM signal. The DPWM signal frequency is set by the cap at the BOSC pin.

Open String Protection

The open string protection is achieved through detecting the voltage of OVP and LED1~8 pin. If one or more strings are open, the respective LEDX pins are pulled to ground and the IC keeps charging the output voltage until it reach OVP threshold. Then the part marks off the open strings whose LEDX pin voltage is less than 190mV. Once the mark-off operation completes, the remaining LED strings will force the output voltage back into tight regulation. The string with the highest voltage drop is the ruling string during output regulation.

The MP3391 always tries to light at least one string and if all strings in use are open, theMP3391 shuts down the step-up converter. The part maintains mark-off information until resetting it.

Short String Protection

The MP3391 monitors the LEDX pin voltage to judge if the short string occurs. If one or more strings are short, the respective LEDX pins tolerate high voltage stress. If the LEDX pin voltage is higher than threshold programmed by SSET pin, the short string condition is detected on the respective string. When the short string fault (LEDX over-voltage fault) continues for greater than protection timer programmed by TSET capacitor, the string is marked off and disabled. Once a string is marked off, its current regulation is forced to disconnect from the output voltage loop regulation. The marked-off LED strings will be shut off totally until the part restarts. If all strings in use are short, the MP3391 shuts down the step-up converter.

When the open or short protection is triggered, the FF pin will be pull to GND. the pull-up resistor R_{FF} and FF pin achieve the fault flag function to indicate the system status.

APPLICATION INFORMATION

Selecting the Switching Frequency

The switching frequency of the step-up converter is programmable from 60kHz to 900kHz. An oscillator resistor on OSC pin sets the internal oscillator frequency for the step-up converter according to the equation:

$$f_{SW}\,(kHz) = 17000 / (10+R_{OSC})\,(k\Omega)$$

For R_{OSC}=50kΩ, the switching frequency is set to 283 kHz.

Setting the LED Current

The LED string currents are identical and set through the current setting resistor on the ISET pin.

$$I_{LED} = 1000 \times 1.23V / R_{SET}$$

For R_{SET}=60.4kΩ, the LED current is set to 20mA. The ISET pin can not be open.

The Number of LED Strings Selection

The MP3391 can drive 8 strings, 6 strings or 4 strings of LEDs. Set the NUMSEL high level for driving 6 strings of LEDs (LED1~LED6). Set the NUMSEL low level for driving 4 strings of LEDs (LED1~LED4). Float the NUMSEL pin for driving 8 strings of LEDs.

Selecting the Input Capacitor

The input capacitor reduces the surge current drawn from the input supply and the switching noise from the device. The input capacitor impedance at the switching frequency should be less than the input source impedance to prevent high frequency switching current from passing through the input. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 4.7µF ceramic capacitor paralleled a 220µF electrolytic capacitor is sufficient.

Selecting the Inductor and Current Sensing Resistor

The inductor is required to force the higher output voltage while being driven by the input voltage. A larger value inductor results in less ripple current, resulting in lower peak inductor current and reducing stress on the internal N-Channel MOSFET. However, the larger value inductor has a larger physical size, higher series resistance, and lower saturation current.

Choose an inductor that does not saturate under the worst-case load conditions. A good rule for determining the inductance is to allow the peak-to-peak ripple current to be approximately 30% to 40% of the maximum input current. Calculate the required inductance value by the equation:

$$L = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{V_{OUT} \times f_{SW} \times \Delta I}$$

$$I_{IN(MAX)} = \frac{V_{OUT} \times I_{LOAD(MAX)}}{V_{IN} \times \eta}$$

$$\Delta I = (30\% \sim 40\%) \times I_{IN(MAX)}$$

Where V_{IN} is the minimum input voltage, f_{SW} is the switching frequency, $I_{LOAD(MAX)}$ is the maximum load current, ΔI is the peak-to-peak inductor ripple current and η is the efficiency.

The switch current is usually used for the peak current mode control. In order to avoid hitting the current limit, the voltage across the sensing resistor R_{SENSE} should be less than 80% of the worst case current limit voltage, V_{SENSE}.

$$R_{SENSE} = \frac{0.8 \times V_{SENSE}}{I_{L(PEAK)}}$$

Where $I_{L(PEAK)}$ is the peak value of the inductor current. V_{SENSE} is shown in Figure 3.

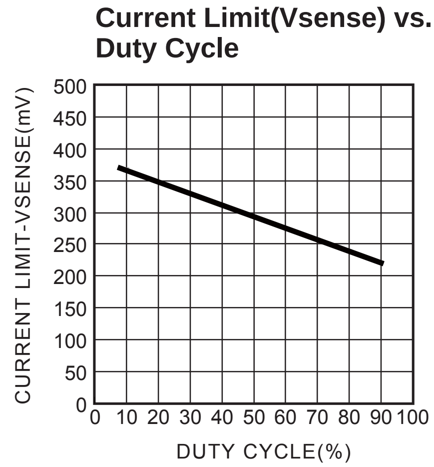


Figure 3—V_{SENSE} vs Duty Cycle

Selecting the Power MOSFET

The MP3391 is capable of driving a wide variety of N-Channel power MOSFETS. The critical parameters of selection of a MOSFET are:

1. Maximum drain to source voltage, $V_{DS(MAX)}$
2. Maximum current, $I_{D(MAX)}$

3. On-resistance, $R_{DS(ON)}$
4. Gate source charge Q_{GS} and gate drain charge Q_{GD}
5. Total gate charge, Q_G

Ideally, the off-state voltage across the MOSFET is equal to the output voltage. Considering the voltage spike when it turns off, $V_{DS(MAX)}$ should be greater than 1.5 times of the output voltage.

The maximum current through the power MOSFET happens when the input voltage is minimum and the output power is maximum. The maximum RMS current through the MOSFET is given by

$$I_{RMS(MAX)} = I_{IN(MAX)} \times \sqrt{D_{MAX}}$$

Where:

$$D_{MAX} \approx \frac{V_{OUT} - V_{IN(MIN)}}{V_{OUT}}$$

The current rating of the MOSFET should be greater than 1.5 times I_{RMS},

The on resistance of the MOSFET determines the conduction loss, which is given by:

$$P_{cond} = I_{RMS}{}^2 \times R_{DS(on)} \times k$$

Where k is the temperature coefficient of the MOSFET.

The switching loss is related to Q_{GD} and Q_{GS1} which determine the commutation time. Q_{GS1} is the charge between the threshold voltage and the plateau voltage when a driver charges the gate, which can be read in the chart of V_{GS} vs. Q_G of the MOSFET datasheet. Q_{GD} is the charge during the plateau voltage. These two parameters are needed to estimate the turn on and turn off loss.

$$P_{SW} = \frac{Q_{GS1} \times R_G}{V_{DR} - V_{TH}} \times V_{DS} \times I_{IN} \times f_{SW} + \frac{Q_{GD} \times R_G}{V_{DR} - V_{PLT}} \times V_{DS} \times I_{IN} \times f_{SW}$$

Where V_{TH} is the threshold voltage, V_{PLT} is the plateau voltage, R_G is the gate resistance, V_{DS} is the drain-source voltage. Please note that the switching loss is the most difficult part in the loss estimation. The formula above provides a simple physical expression. If more accurate estimation is required, the expressions will be much more complex.

For extended knowledge of the power loss estimation, readers should refer to the book “Power MOSFET Theory and Applications” written by Duncan A. Grant and John Gowar.

The total gate charge, Q_G, is used to calculate the gate drive loss. The expression is

$$P_{DR} = Q_G \times V_{DR} \times f_{SW}$$

where V_{DR} is the drive voltage.

Selecting the Output Capacitor

The output capacitor keeps the output voltage ripple small and ensures feedback loop stability.

The output capacitor impedance should be low at the switching frequency. Ceramic capacitors with X7R dielectrics are recommended for their low ESR characteristics. For most applications, a 4.7μF ceramic capacitor paralleled 10μF electrolytic capacitor will be sufficient.

Setting the Over Voltage Protection

The open string protection is achieved through the over voltage protection (OVP). In some cases, an LED string failure results in the feedback voltage always zero. The part then keeps boosting the output voltage higher and higher. If the output voltage reaches the programmed OVP threshold, the protection will be triggered.

To make sure the chip functions properly, the OVP setting resistor divider must be set with a proper value. The recommended OVP point is about 1.2 times higher than the output voltage for normal operation.

$$V_{OVP} = 1.24 \times (1 + \frac{R_{HIGH}}{R_{LOW}})$$

Selecting Dimming Control Mode

The MP3391 provides 2 different dimming methods

1. Direct PWM Dimming

An external PWM dimming signal is employed to achieve PWM dimming control. Connect a 100kΩ resistor from BOSC pin to GND and apply the 100Hz to 20kHz PWM dimming signal to DBRT pin. The minimum recommended amplitude of the PWM signal is 1.2V, The low level should less than 0.4V (See Figure 4).

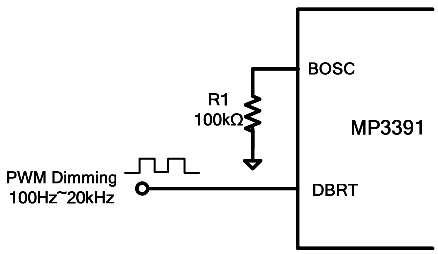


Figure 4—Direct PWM Dimming

Table 1 shows the PWM dimming duty Range with different PWM dimming frequency.

Tab 1 The Range of PWM Dimming Duty

fpwm(Hz)	Dmin	Dmax
100<f≤200	0.30%	100%
200<f≤500	0.75%	100%
500<f≤1k	1.50%	100%
1k<f≤2k	3.00%	100%
2k<f≤5k	7.50%	100%
5k<f≤10k	15.00%	100%
10k<f≤13k	19.00%	100%
13k<f≤20k	30.00%	100%

2. DC Input PWM Dimming

To apply DC input PWM dimming, apply an analog signal (range from 0.2 V to 1.2V) to the DBRT pin to modulate the LED current directly. If the PWM is applied with a zero DC voltage, the PWM duty cycle will be 0%. If the DBRT pin is applied with a DC voltage>1.2V, the output will be 100% (See Figure 5). The capacitor on BOSC pin set the frequency of internal triangle waveform according to the equation:

$$F_{DPWM}(Hz) = 3.5 / C_{BOSC}(\mu F)$$

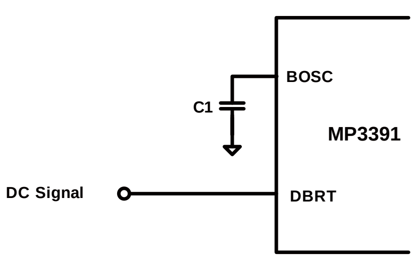


Figure 5—DC input PWM Dimming

Layout Considerations

Careful attention must be paid to the PCB board layout and components placement. Proper layout of the high frequency switching path is critical to prevent noise and electromagnetic interference problems. The loop of external MOSFET (M2), output diode (D1), and output capacitor (C2,C3) is flowing with high frequency pulse current. it must be as short as possible (See Figure 6).

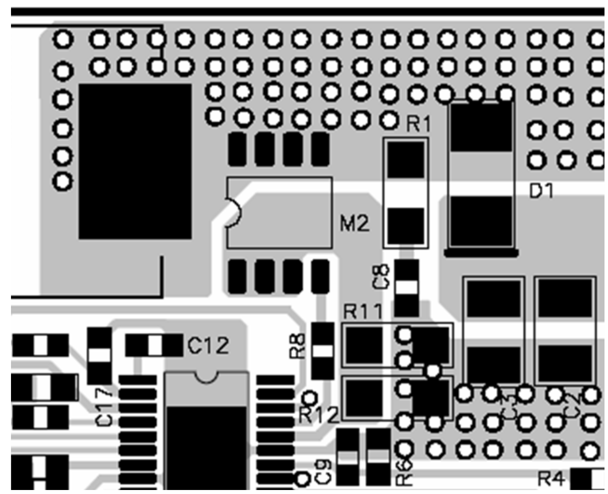


Figure 6—Layout Consideration

The IC exposed pad is internally connected to GND pin, and all logic signals are refer to the GND. The PGND should be externally connected to GND and is recommended to keep away from the logic signals.

TYPICAL APPLICATION CIRCUIT

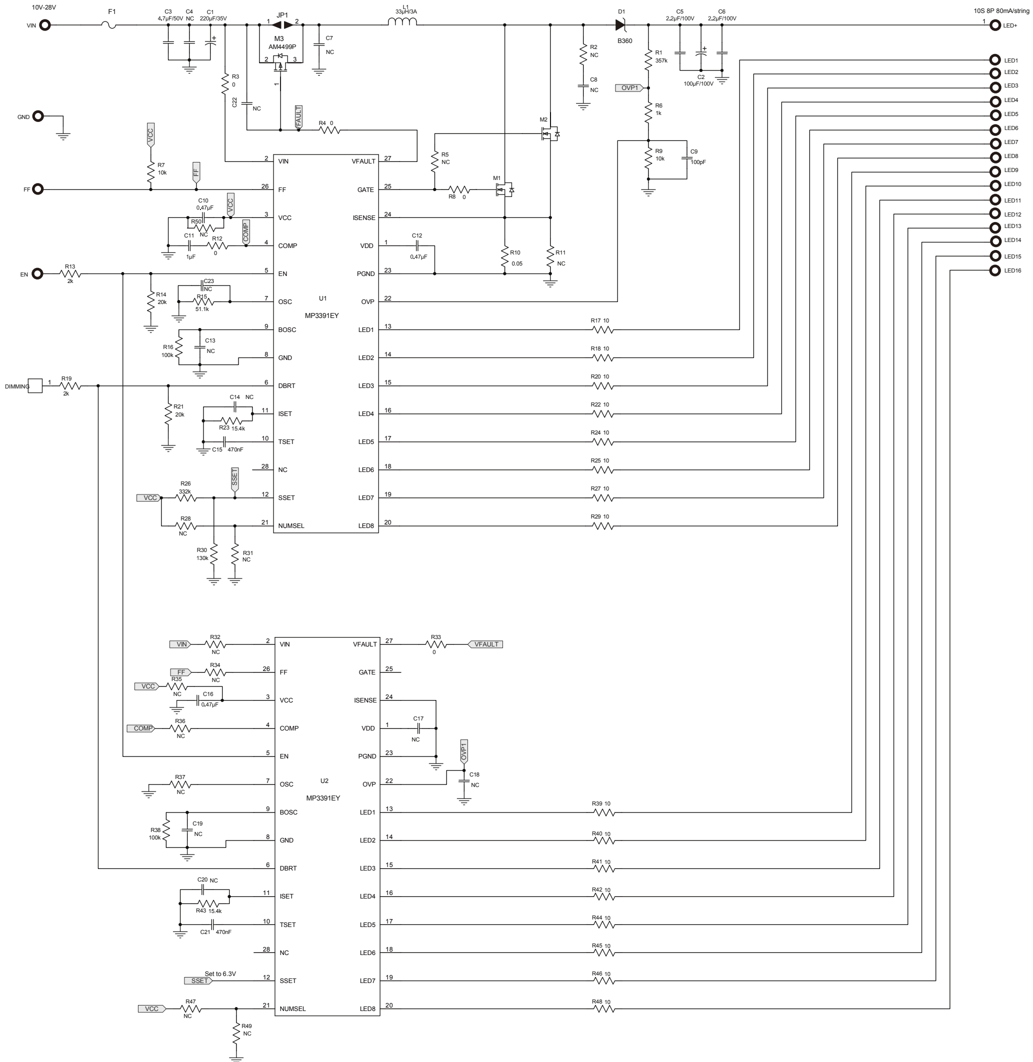


Figure 7— 2 MP3391 Extended Solution for 16 Strings Application

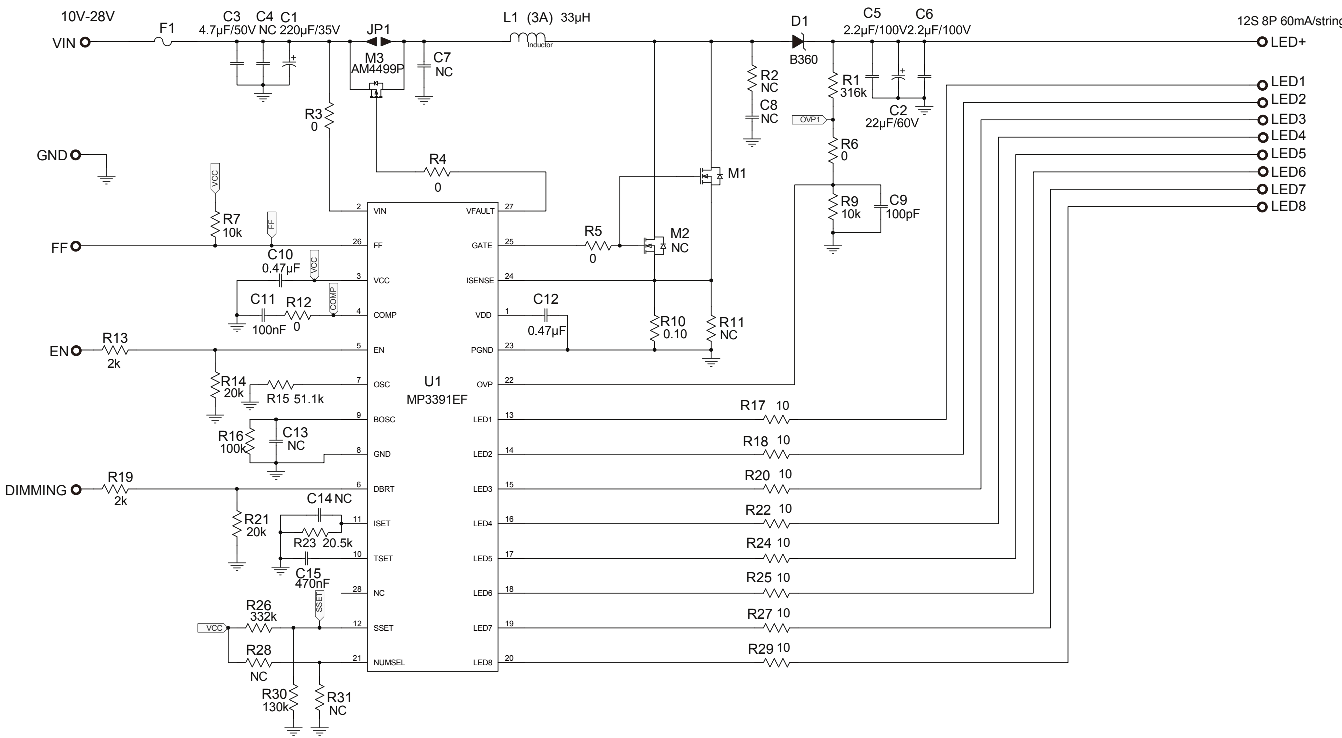
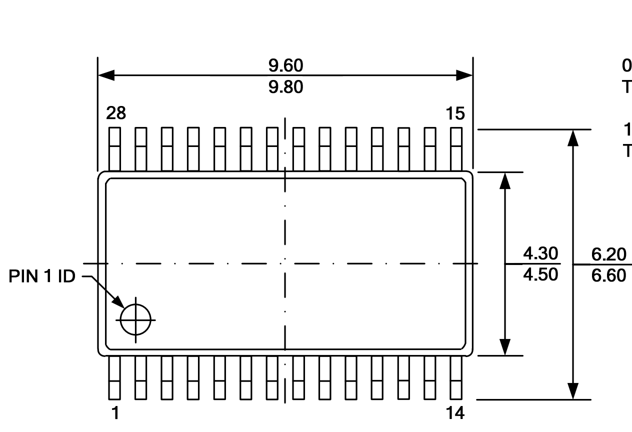


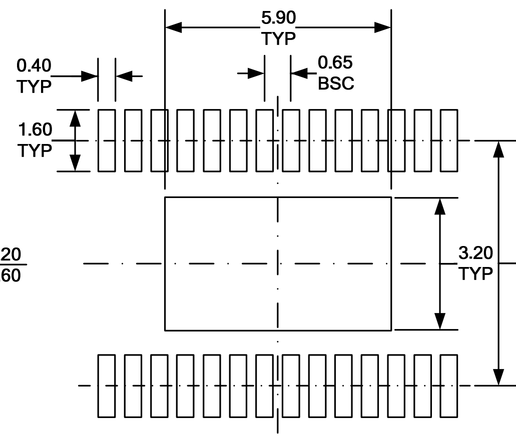
Figure 8— MP3391 Application with Disconnection Function

PACKAGE INFORMATION

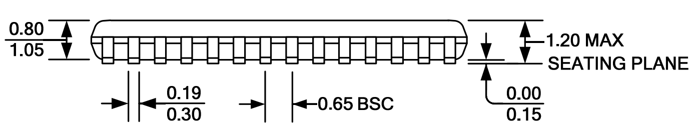
TSSOP28



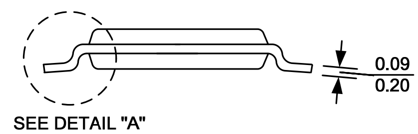
TOP VIEW



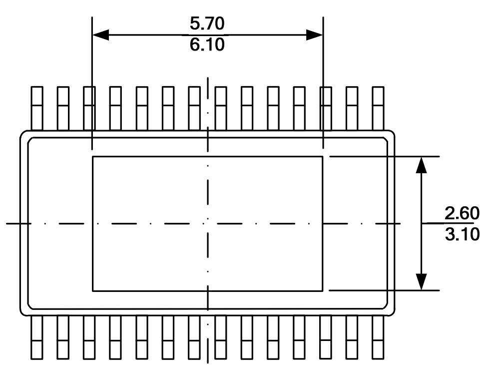
RECOMMENDED LAND PATTERN



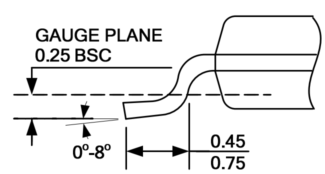
FRONT VIEW



SIDE VIEW



BOTTOM VIEW



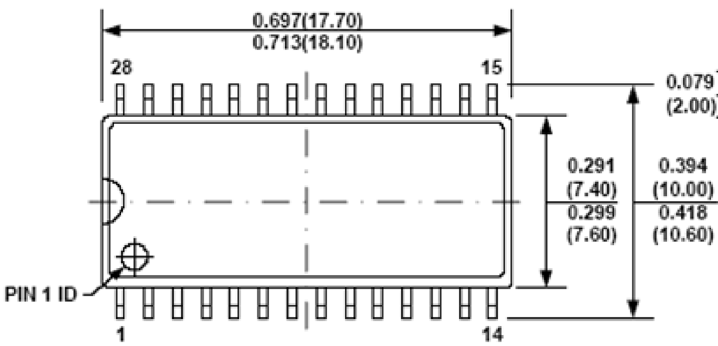
DETAIL "A"

NOTE:

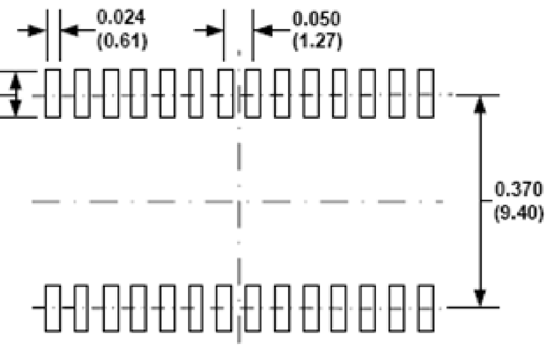
1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-153, VARIATION AET.
6) DRAWING IS NOT TO SCALE.

PACKAGE INFORMATION

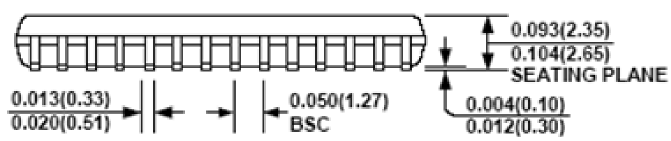
SOIC28



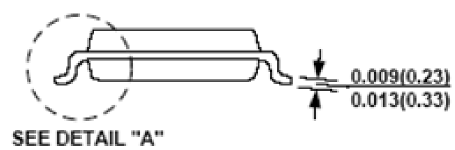
TOP VIEW



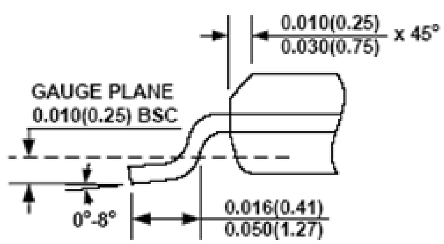
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MS-013, VARIATION AE.
6) DRAWING IS NOT TO SCALE.

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