19-3594; Rev 0; 2/05

EVALUATION KIT AVAILABLE

EEPROM-Programmable, Hex Power-Supply Supervisory Circuits

General Description

The MAX6884/MAX6885 EEPROM-configurable, multivoltage power-supply supervisors monitor six voltage-detector inputs, one auxiliary input, and one watchdog input, and feature three programmable outputs for highly configurable power-supply monitoring applications. Manual reset and margin disable inputs offer additional flexibility.

Each voltage-detector input offers a programmable primary undervoltage and secondary undervoltage/overvoltage threshold. Voltage-detector inputs IN1–IN6 monitor voltages from 1V to 5.8V in 20mV increments or 0.5V to 3.05V in 10mV increments.

Programmable outputs $\overline{RESET}$, $\overline{UV}/\overline{OV}$, and $\overline{WDO}$ provide system resets/interrupts. Programmable output options include open-drain or weak pullup. Programmable timing delay blocks configure each output to wait between 25µs and 1600ms after their respective assertion-causing conditions have been cleared. A fault register logs condition-causing events (undervoltage, overvoltage, manual reset, etc.).

An internal 10-bit, 1% accurate ADC (MAX6884 only) converts the voltages at IN1–IN6, AUXIN, and V_{CC} through a multiplexer that automatically sequences through all inputs every 200ms. An SMBus™/I²C-compatible serial data interface programs and communicates with the configuration EEPROM, configuration registers, internal 512-bit user EEPROM, and reads the ADC registers (MAX6884 only) and fault registers.

The MAX6884/MAX6885 are available in a 5mm x 5mm x 0.8mm 20-pin thin QFN package and operate over the extended temperature range (-40°C to +85°C).

Applications

Telecommunications/Central-Office Systems
Networking Systems
Servers/Workstations
Base Stations
Storage Equipment
Multimicroprocessor/Voltage Systems

Features

- **6 Configurable Input Voltage Detectors**
  Programmable Thresholds 0.5V to 3.05V (in 10mV Increments) or 1V to 5.8V (in 20mV Increments)
  Primary UV and Secondary UV/OV Thresholds
- **One Configurable Watchdog Timer from 6.25ms to 102.4s**
- **Configurable $\overline{RESET}$, $\overline{UV}/\overline{OV}$, and $\overline{WDO}$ Outputs**
- **Three Programmable Outputs**
  Open-Drain or Weak Pullup $\overline{RESET}$, $\overline{UV}/\overline{OV}$, and $\overline{WDO}$
  Active-Low Output Logic
  Timing Delays from 25µs to 1600ms
- **Margining Disable and Manual Reset Controls**
- **Internal 1.25V Reference or External Reference Input**
- **10-Bit Internal ADC Samples the Input Voltage Detectors, V_{CC} and Auxiliary Input**
- **512-Bit User EEPROM**
  Endurance: 100,000 Erase/Write Cycles
  Data Retention: 10 Years
- **SMBus/I²C-Compatible Serial Configuration/Communication Interface**
- **±1% Threshold Accuracy**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX6884ETP	-40°C to +85°C	20 Thin QFN	T2055-5
MAX6885ETP	-40°C to +85°C	20 Thin QFN	T2055-5

Pin Configurations and Typical Operating Circuit appear at end of data sheet.

Selector Guide

PART	VOLTAGE-DETECTOR INPUTS	INTERNAL ADC	PROGRAMMABLE OUTPUTS	REFERENCE INPUT	AUXILIARY INPUT
MAX6884ETP	6	Yes	3	Yes	Yes
MAX6885ETP	6	No	3	No	No

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

EEPROM-Programmable, Hex Power-Supply Supervisory Circuits

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)
IN1–IN6, V_{CC}, $\overline{RESET}$, $\overline{UV}/\overline{OV}$, $\overline{WDO}$.....-0.3V to +6V
WDI, $\overline{MR}$, $\overline{MARGIN}$, SDA, SCL, A0.....-0.3V to +6V
AUXIN, DBP, REFIN .....-0.3V to +3V
Input/Output Current (all pins).....±20mA
Continuous Power Dissipation (T_A = +70°C)
20-Pin (5mm x 5mm) Thin QFN
(derate 21.3mW/°C above +70°C).....1702mW
Maximum Junction Temperature .....+150°C
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN1}–V_{IN4} or V_{CC} = 2.7V to 5.8V, AUXIN = WDI = GND, $\overline{MARGIN}$ = $\overline{MR}$ = DBP, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 1, 2, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range		Voltage on either one of IN1–IN4 or V_{CC} to guarantee the device is fully operational		2.7		5.8	V
Undervoltage Lockout	V_{UVLO}	Minimum voltage on one of IN1–IN4 or V_{CC} to guarantee device is EEPROM configured				2.5	V
Digital Bypass Voltage	V_{DBP}	No load		2.48	2.55	2.67	V
Supply Current	I_{CC}	V_{IN1} = 5.8V, IN2–IN6 = GND, no load			0.9	1.2	mA
		Writing to configuration registers or EEPROM, no load			1.1	1.5	mA
Threshold Range	V_{TH}	V_{IN1}–V_{IN6} (in 20mV increments)		1.0		5.8	V
		V_{IN1}–V_{IN6} (in 10mV increments)		0.50		3.05	
		V_{IN1}–V_{IN6} (Inputs high impedance; in 3.3mV increments)		0.167		1.017	
IN1–IN6 Threshold Accuracy		T_A = +25°C to +85°C, ($V_{IN_}$ falling)	$V_{IN_}$ = 2.5V to 5.8V (20mV increments)	-1		+1	%
			$V_{IN_}$ = 1V to 2.5V (20mV increments)	-25		+25	mV
			$V_{IN_}$ = 1.25V to 3.05V (10mV increments)	-1		+1	%
			$V_{IN_}$ = 0.5V to 1.25V (10mV increments)	-12.5		+12.5	mV
		T_A = -40°C to +85°C, ($V_{IN_}$ falling)	$V_{IN_}$ = 2.5V to 5.8V (20mV increments)	-1.5		+1.5	%
			$V_{IN_}$ = 1V to 2.5V (20mV increments)	-25		+25	mV
			$V_{IN_}$ = 1.25V to 3.05V (10mV increments)	-1.5		+1.5	%
			$V_{IN_}$ = 0.5V to 1.25V (10mV increments)	-12.5		+12.5	mV

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN1}–V_{IN4} or V_{CC} = 2.7V to 5.8V, AUXIN = WDI = GND, $\overline{MARGIN}$ = $\overline{MR}$ = DBP, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 1, 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Threshold Hysteresis	$V_{TH-HYST}$			0.3		% V_{TH}
Threshold Tempco	ΔV_{TH}/°C			10		ppm/°C
Threshold Differential Nonlinearity	V_{TH} DNL		-1		+1	LSB
IN_ Input Impedance	R_{IN}	For $V_{IN_}$ < highest of $V_{IN1–IN4}$ and $V_{IN_}$ < V_{CC}	130	200	300	kΩ
IN_ Input Leakage Current	I_{IN_LKG}	IN_ high impedance	-150		+150	nA
Power-Up Delay	t_{D-PO}	$V_{CC} \geq V_{UVLO}$			2.5	ms
IN_ to $\overline{RESET}$ or $\overline{UV/OV}$ Delay	t_{D-R}	IN_ falling/rising, 100mV overdrive		20		µs
$\overline{RESET}$ and $\overline{UV/OV}$ Timeout Period (Tables 6 and 7)	t_{RP}, t_{UP}	000		0.025		ms
		001	1.406	1.5625	1.719	
		010	5.625	6.25	6.875	
		011	22.5	25	27.5	
		100	45	50	55	
		101	180	200	220	
		110	360	400	440	
		111	1440	1600	1760	
$\overline{RESET}$, $\overline{UV/OV}$, $\overline{WDO}$ Output Low		I_{SINK} = 4mA, output asserted			0.4	V
$\overline{RESET}$, $\overline{UV/OV}$, $\overline{WDO}$ Output Open-Drain Leakage Current		Output high impedance	-1		+1	µA
$\overline{RESET}$, $\overline{UV/OV}$, $\overline{WDO}$ Output Pullup Resistance	R_{PU}	$V_{\overline{RESET}}$, $V_{\overline{UV/OV}}$, $V_{\overline{WDO}}$ = 2V	6.6	10	15.0	kΩ
$\overline{MR}$, $\overline{MARGIN}$, WDI Input Voltage	V_{IL}				0.6	V
	V_{IH}		1.4			
$\overline{MR}$ Input Pulse Width	$t_{\overline{MR}}$		1			µs
$\overline{MR}$ Glitch Rejection				100		ns

EEPROM-Programmable, Hex Power-Supply Supervisory Circuits

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN1}–V_{IN4} or V_{CC} = 2.7V to 5.8V, AUXIN = WDI = GND, $\overline{MARGIN}$ = $\overline{MR}$ = DBP, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 1, 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{MR}$ to $\overline{RESET}$ or $\overline{UV}/\overline{OV}$ Delay	$t_{D-\overline{MR}}$			200		ns
$\overline{MR}$ to Internal V_{DBP} Pullup Current	$I_{\overline{MR}}$	$V_{\overline{MR}}$ = 1.4V	5	10	15	µA
$\overline{MARGIN}$ to DBP Pullup Current	$I_{\overline{MARGIN}}$	$V_{\overline{MARGIN}}$ = 1.4V	5	10	15	µA
WDI Pulldown Current	I_{WDI}	V_{WDI} = 0.6V	5	10	15	µA
WDI Input Pulse Width	t_{WDI}		50			ns
Watchdog Timeout Period (Table 8)	t_{WD}	000	5.625	6.25	6.875	ms
		001	22.5	25	27.5	
		010	90	100	110	
		011	360	400	440	
		100	1.44	1.60	1.76	s
		101	5.76	6.40	7.04	
		110	23.04	25.60	28.16	
		111	92.16	102.40	112.64	
Reference Input Voltage Range	V_{REF}	MAX6884 only	1.225	1.25	1.275	V
Reference Input Resistance	R_{REF}	V_{REF} = 1.25V, MAX6884 only		500		kΩ
ADC Range	ADC_{RANGE}	IN1–IN6, V_{CC}; LSB = 7.32mV, MAX6884 only	0		5.8	V
		IN1–IN6; LSB = 3.66mV, MAX6884 only	0		3.746	
		AUXIN, IN1–IN6 high-impedance mode; LSB = 1.2mV, MAX6884 only	0		1.25	
ADC Total Unadjusted Error (Note 4)	TUE	Internal reference, MAX6884 only			±1.0	%FSR
		External reference, MAX6884 only (Note 5)			±1.0	
ADC Differential Nonlinearity	DNL	MAX6884 only (Note 6)		±1		LSB
ADC Total Monitoring Cycle Time	t_C	Converts all six IN_ inputs, AUXIN, and V_{CC}, MAX6884 only		200	266	ms
AUXIN Input Leakage Current	I_{AUXIN}	V_{AUXIN} = 1.25V, MAX6884 only	-1		+1	µA
SERIAL INTERFACE LOGIC (SDA, SCL, A0)						
Logic-Input Low Voltage	V_{IL}				0.8	V
Logic-Input High Voltage	V_{IH}		2.0			V
Input Leakage Current	I_{LKG}				1	µA
Output-Voltage Low	V_{OL}	I_{SINK} = 3mA			0.4	V
Input/Output Capacitance	$C_{I/O}$				10	pF

TIMING CHARACTERISTICS

(V_{IN1}–V_{IN4} or V_{CC} = 2.7V to 5.8V, AUXIN = WDI = GND, $\overline{MARGIN}$ = $\overline{MR}$ = DBP, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_{IN1} = +25°C.) (Notes 1, 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIMING CHARACTERISTICS (Figure 6)						
Serial Clock Frequency	f_{SCL}				400	kHz
Clock Low Period	t_{LOW}		1.3			µs
Clock High Period	t_{HIGH}		0.6			µs
Bus Free Time	t_{BUF}		1.3			µs
START Setup Time	$t_{SU:STA}$		0.6			µs
START Hold Time	$t_{HD:STA}$		0.6			µs
STOP Setup Time	$t_{SU:STO}$		0.6			µs
Data In Setup Time	$t_{SU:DAT}$		100			ns
Data In Hold Time	$t_{HD:DAT}$		30		900	ns
Receive SCL/SDA Minimum Rise Time	t_R	(Note 7)		20 + 0.1 x C_{BUS}		ns
Receive SCL/SDA Maximum Rise Time	t_R	(Note 7)		300		ns
Receive SCL/SDA Minimum Fall Time	t_F	(Note 7)		20 + 0.1 x C_{BUS}		ns
Receive SCL/SDA Maximum Fall Time	t_F	(Note 7)		300		ns
Transmit SDA Fall Time	t_F	C_{BUS} = 400pF (Note 5)	20 + 0.1 x C_{BUS}		300	ns
Pulse Width of Spike Suppressed	t_{SP}	(Note 8)		50		ns
EEPROM Byte Write Cycle Time	t_{WR}	(Note 9)			11	ms

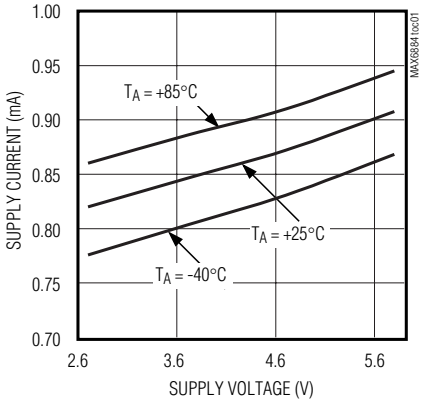
Note 1: 100% production tested at T_A = +25°C and T_A = +85°C. Specifications at T_A = -40°C are guaranteed by design.
Note 2: Device may be supplied from IN1–IN4 or V_{CC}.
Note 3: The internal supply voltage, measured at V_{CC}, equals the maximum of IN1–IN4.
Note 4: $V_{IN_}$ > 0.3 x ADC range.
Note 5: Does not include the inaccuracy of the 1.25V input reference voltage (MAX6884 only).
Note 6: DNL is implicitly guaranteed by design in a ΣΔ converter.
Note 7: C_{BUS} = total capacitance of one bus line in picofarads. Rise and fall times are measured between 0.1 x V_{BUS} and 0.9 x V_{BUS}.
Note 8: Input filters on SDA, SCL, and A0 suppress noise spikes <50ns.
Note 9: An additional cycle is required when writing to configuration memory for the first time.

EEPROM-Programmable, Hex Power-Supply Supervisory Circuits

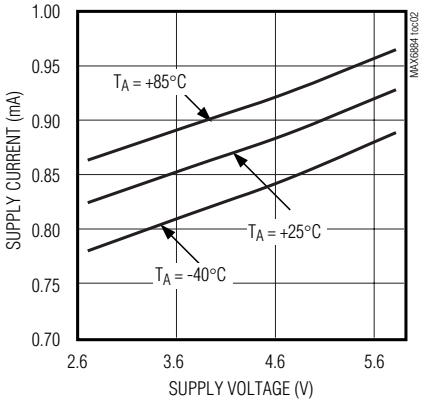
Typical Operating Characteristics

(V_{IN1}–V_{IN4} or V_{CC} = 5V, AUXIN = WDI = GND, $\overline{MARGIN}$ = $\overline{MR}$ = DBP. Typical values are at T_A = +25°C, unless otherwise noted.)

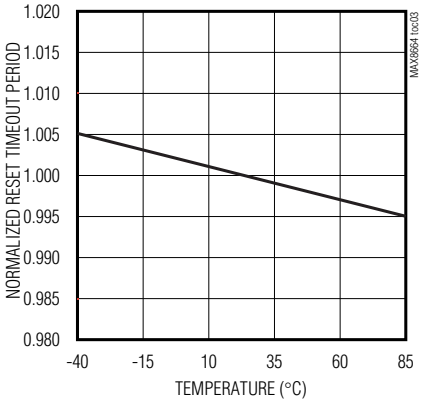
V_{CC} SUPPLY CURRENT vs. V_{CC} SUPPLY VOLTAGE



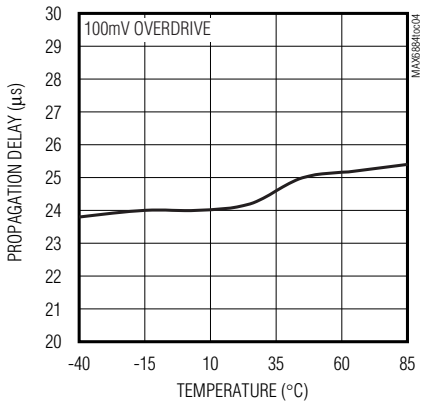
IN1–IN4 SUPPLY CURRENT vs. IN1–IN4 SUPPLY VOLTAGE



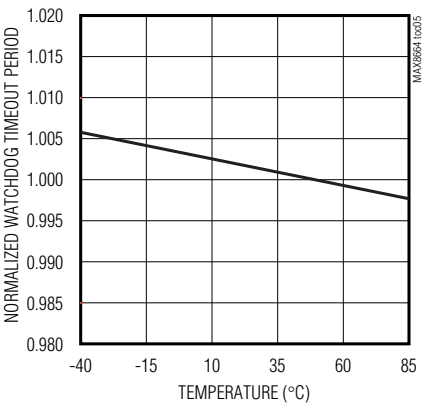
NORMALIZED RESET OR $\overline{UV/OV}$ TIMEOUT PERIOD vs. TEMPERATURE



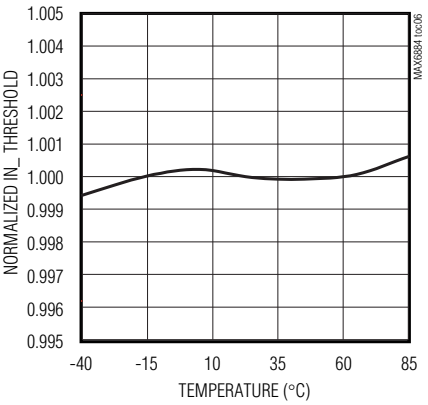
IN_ TO $\overline{RESET}$ OR $\overline{UV/OV}$ PROPAGATION DELAY vs. TEMPERATURE



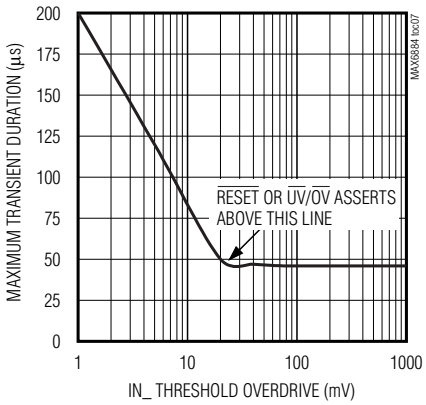
NORMALIZED WATCHDOG TIMEOUT PERIOD vs. TEMPERATURE



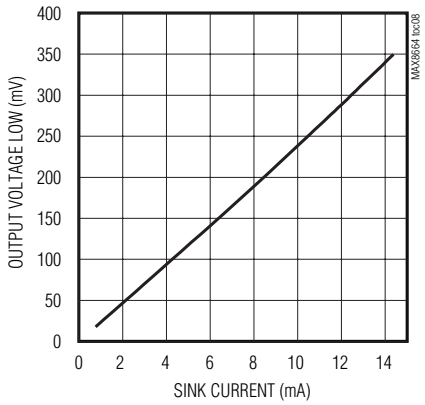
NORMALIZED IN_ THRESHOLD vs. TEMPERATURE



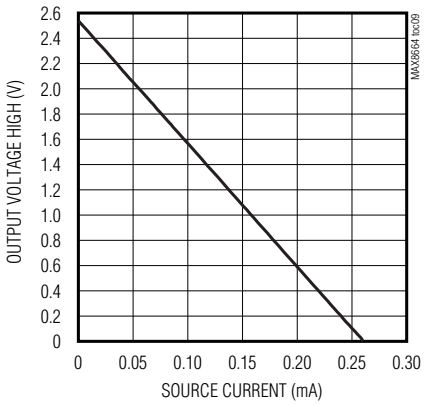
MAXIMUM IN_ TRANSIENT vs. IN_ THRESHOLD OVERDRIVE



OUTPUT VOLTAGE LOW vs. SINK CURRENT



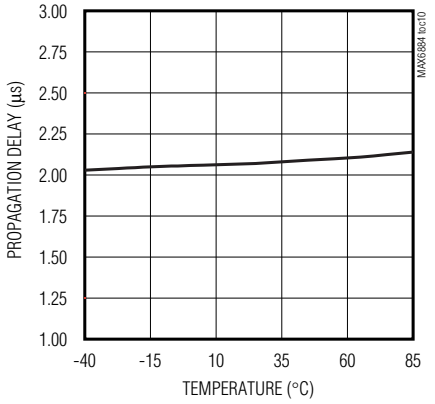
OUTPUT VOLTAGE HIGH vs. SOURCE CURRENT (WEAK PULLUP)



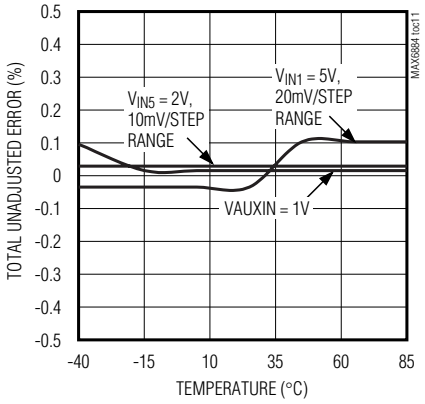
Typical Operating Characteristics (continued)

(V_{IN1}–V_{IN4} or V_{CC} = 5V, AUXIN = WDI = GND, $\overline{MARGIN}$ = $\overline{MR}$ = DBP. Typical values are at T_A = +25°C, unless otherwise noted.)

$\overline{MR}$ TO $\overline{RESET}$ OR $\overline{UV/OV}$ OUTPUT PROPAGATION DELAY vs. TEMPERATURE



ADC ACCURACY vs. TEMPERATURE



Pin Description

PIN		NAME	FUNCTION
MAX6884	MAX6885		
1	1	$\overline{RESET}$	Reset Output. Configurable, active-low, open drain, or weak pullup. $\overline{RESET}$ assumes its programmed conditional output state when V_{CC} exceeds UVLO (2.5V).
2	2	$\overline{WDO}$	Watchdog Timer Output. Configurable, active-low, open drain, or weak pullup. $\overline{WDO}$ asserts when WDI is not toggled with a valid high-to-low or low-to-high transition within the watchdog timeout period.
3	3	$\overline{UV/OV}$	Undervoltage/Overvoltage Output. Configurable, active-low, open drain, or weak pullup. $\overline{UV/OV}$ assumes its programmed conditional output state when V_{CC} exceeds UVLO (2.5V).
4	4	GND	Ground
5	5	WDI	Watchdog Timer Input. Logic input for the watchdog timer function. If $\overline{WDI}$ is not toggled with a valid low-to-high or high-to-low transition within the watchdog timeout period, $\overline{WDO}$ asserts. Progam initial and normal watchdog timeout periods from 6.25ms to 102.4s. WDI is internally pulled down to GND through a 10µA current sink.
6	6	$\overline{MR}$	Manual Reset Input. Program $\overline{MR}$ to assert $\overline{RESET}$ and/or $\overline{UV/OV}$ when $\overline{MR}$ is asserted. Leave $\overline{MR}$ unconnected or connect to DBP if unused. $\overline{MR}$ is internally pulled up to DBP through a 10µA current source.

EEPROM-Programmable, Hex Power-Supply Supervisory Circuits

Pin Description (continued)

PIN		NAME	FUNCTION
MAX6884	MAX6885		
7	7	$\overline{\text{MARGIN}}$	Margin Input. $\overline{\text{MARGIN}}$ holds $\overline{\text{RESET}}$, $\overline{\text{UV}}$/$\overline{\text{OV}}$, and $\overline{\text{WDO}}$ in their existing states when $\overline{\text{MARGIN}}$ is driven low. Leave $\overline{\text{MARGIN}}$ unconnected or connect to DBP if unused. $\overline{\text{MARGIN}}$ is internally pulled up to DBP through a 10µA current source. $\overline{\text{MARGIN}}$ overrides $\overline{\text{MR}}$ if both are asserted at the same time.
8	8	SDA	Serial Data Input/Output (Open Drain). SDA requires an external pullup resistor.
9	9	SCL	Serial-Interface Clock Input. SCL requires an external pullup resistor.
10	10	A0	Serial Address Input 0. Allows up to 2 devices to share a common bus. Connect A0 to ground or the serial-interface power supply.
11	—	REFIN	Reference Voltage Input. Program the device for external or internal reference. Connect an external +1.225V to +1.275V reference to REFIN when using an external reference. Leave REFIN unconnected when using the internal reference.
12	—	AUXIN	Auxiliary Input. A 10-bit ADC converts the input voltage at AUXIN. The high-impedance AUXIN input accepts input voltages up to 1.25V. AUXIN does not affect programmable outputs.
—	11, 12	N.C.	No Connection. Not internally connected.
13	13	V_{CC}	Internal Power-Supply Voltage. Bypass V_{CC} to GND with a 1µF ceramic capacitor as close to the device as possible. V_{CC} supplies power to the internal circuitry. V_{CC} is internally powered from the highest of the monitored IN1–IN4 voltages. Do not use V_{CC} to supply power to external circuitry. To externally supply V_{CC}, see the *Powering the MAX6884/MAX6885* section.
14	14	DBP	Internal Digital Power-Supply Voltage. Bypass DBP to GND with a 1µF ceramic capacitor. DBP supplies power to the EEPROM memory, the internal logic circuitry, and the programmable outputs. Do not use DBP to supply power to external circuitry.
15	15	IN6	Voltage-Detector Input 6. Program two thresholds per voltage-detector input (undervoltage UV and undervoltage/overvoltage UV/OV). Program IN6 detector thresholds from 1V to 5.8V in 20mV increments, 0.5V to 3.05V in 10mV increments. For improved noise immunity, bypass IN6 to GND with a 0.1µF capacitor installed as close to the device as possible.
16	16	IN5	Voltage-Detector Input 5. Program two thresholds per voltage-detector input (undervoltage UV and undervoltage/overvoltage UV/OV). Program IN5 detector thresholds from 1V to 5.8V in 20mV increments, 0.5V to 3.05V in 10mV increments. For improved noise immunity, bypass IN5 to GND with a 0.1µF capacitor installed as close to the device as possible.
17	17	IN4	Voltage-Detector Input 4. Program two thresholds per voltage-detector input (undervoltage UV and undervoltage/overvoltage UV/OV). Program IN4 detector thresholds from 1V to 5.8V in 20mV increments, 0.5V to 3.05V in 10mV increments. For improved noise immunity, bypass IN4 to GND with a 0.1µF capacitor installed as close to the device as possible. Program the device to receive power through IN1–IN4 inputs or V_{CC} (see the *Powering the MAX6884/MAX6885* section).

Pin Description (continued)

PIN		NAME	FUNCTION
MAX6884	MAX6885		
18	18	IN3	Voltage-Detector Input 3. Program two thresholds per voltage-detector input (undervoltage UV and undervoltage/overvoltage UV/OV). Program IN3 detector thresholds from 1V to 5.8V in 20mV increments, or 0.5V to 3.05V in 10mV increments. For improved noise immunity, bypass IN3 to GND with a 0.1µF capacitor installed as close to the device as possible. Program the device to receive power through IN1–IN4 inputs or V_{CC} (see the *Powering the MAX6884/MAX6885* section).
19	19	IN2	Voltage-Detector Input 2. Program two thresholds per voltage-detector input (undervoltage UV and undervoltage/overvoltage UV/OV). Program IN2 detector thresholds from 1V to 5.8V in 20mV increments, or 0.5V to 3.05V in 10mV increments. For improved noise immunity, bypass IN2 to GND with a 0.1µF capacitor installed as close to the device as possible. Program the device to receive power through IN1–IN4 inputs or V_{CC} (see the *Powering the MAX6884/MAX6885* section).
20	20	IN1	Voltage-Detector Input 1. Program two thresholds per voltage-detector input (undervoltage UV and undervoltage/overvoltage UV/OV). Program IN1 detector thresholds from 1V to 5.8V in 20mV increments, or 0.5V to 3.05V in 10mV increments. For improved noise immunity, bypass IN1 to GND with a 0.1µF capacitor installed as close to the device as possible. Program the device to receive power through IN1–IN4 inputs or V_{CC} (see the *Powering the MAX6884/MAX6885* section).
—	—	EP	Exposed Paddle. Internally connected to GND. Connect EP to GND or leave floating.

Detailed Description

The MAX6884/MAX6885 EEPROM-configurable, multivoltage supply supervisors monitor six voltage-detector inputs, one auxiliary input, and one watchdog input, and feature three programmable outputs for highly configurable, power-supply monitoring applications (see Table 1 for programmable features). Manual reset and margin disable inputs offer additional flexibility.

Each voltage detector provides a programmable primary undervoltage and secondary undervoltage/overvoltage threshold. Program thresholds from 0.5V to 3.05V in 10mV increments, 1.0V to 5.8V in 20mV increments, or from 0.1667V to 1.0167V in 3.3mV increments. To achieve thresholds from 0.1667V to 1.0167V in 3.3mV increments, the respective input voltage detector must be programmed for high impedance and an external voltage-divider must be connected. A fault register logs undervoltage and overvoltage conditions for each voltage-detector input.

An internal 10-bit ADC (MAX6884 only) converts voltages at IN1–IN6, AUXIN, and V_{CC} through a multiplexer that automatically sequences through all inputs every 200ms. Access the device's internal 512-bit user EEPROM, configuration EEPROM, configuration registers, ADC registers, and fault registers through an SMBus/I²C-compatible serial interface (see the *SMBus/I²C-Compatible Serial Interface* section). The MAX6884/MAX6885 also feature an accurate internal 1.25V reference. For greater accuracy, connect an external 1.25V reference to REFIN (MAX6884 only).

Program outputs $\overline{\text{RESET}}$, $\overline{\text{UV/OV}}$, and $\overline{\text{WDO}}$ for open-drain or weak pullup. Program $\overline{\text{RESET}}$ and $\overline{\text{UV/OV}}$ to assert on any voltage-detector input, $\overline{\text{MR}}$, or each other. $\overline{\text{RESET}}$ can also depend on $\overline{\text{WDO}}$. Programmable timing delay blocks configure each output to wait between 25µs and 1600ms before deasserting. Fault registers log the assertion of $\overline{\text{RESET}}$, $\overline{\text{UV/OV}}$, and $\overline{\text{WDO}}$.

EEPROM-Programmable, Hex Power-Supply Supervisory Circuits

The MAX6884/MAX6885 feature a watchdog timer with programmable initial and normal timeout periods from 6.25ms to 102.4s. $\overline{WDO}$ asserts when WDI is not toggled from high-to-low or low-to-high within the appropriate watchdog timeout period. Program $\overline{WDO}$ to assert $\overline{RESET}$.

Program the MAX6884/MAX6885 to receive power through IN1–IN4 or V_{CC} (see the *Powering the MAX6884/MAX6885* section). Outputs remain asserted while the voltage that is supplying the device is below UVLO (2.5V) and above 1V (see Figure 1).

Table 1. Programmable Features

FEATURE	DESCRIPTION
Input Voltages IN1–IN6	• Primary undervoltage threshold • Secondary undervoltage or overvoltage threshold • 1V to 5.8V thresholds in 20mV increments • 0.5V to 3.05V thresholds in 10mV increments • 0.1667V to 1.017V thresholds in 3.3mV increments in high-impedance mode
Programmable Output $\overline{RESET}$	• Dependency on IN1–IN6, $\overline{MR}$, $\overline{UV/OV}$, and/or $\overline{WDO}$ • Active-low, weak pullup, or open-drain output • Programmable timeout periods of 25µs, 1.5625ms, 6.25ms, 25ms, 50ms, 200ms, 400ms, or 1.6s
Programmable Output $\overline{UV/OV}$	• Dependency on IN1–IN6, $\overline{MR}$, and/or $\overline{RESET}$ • Active-low, weak pullup, or open-drain output • Programmable timeout periods of 25µs, 1.5625ms, 6.25ms, 25ms, 50ms, 200ms, 400ms, or 1.6s
Programmable Output $\overline{WDO}$	• Active-low, weak pullup, or open-drain output
Watchdog Timer	• Initial watchdog timeout period of 6.25ms, 25ms, 100ms, 400ms, 1.6s, 6.4s, 25.6s, or 102.4s • Normal watchdog timeout period of 6.25ms, 25ms, 100ms, 400ms, 1.6s, 6.4s, 25.6s, or 102.4s • Watchdog enable/disable
V_{CC} Power Mode	• Programs whether the device is powered from the highest IN_ input or from an external supply connected to V_{CC}
Manual Reset Input $\overline{MR}$	• Program $\overline{RESET}$ or $\overline{UV/OV}$ to assert while $\overline{MR}$ is asserted
Reference Input REFIN	• Internal +1.25V reference voltage • Goes high impedance when internal reference is selected • External reference voltage input from 1.225V to 1.275V • Sets ADC voltage range
10-Bit ADC*	• Samples voltages at IN1–IN6, AUXIN, and V_{CC} • Completes conversion of all eight inputs in 200ms • Reference voltage sets ADC range • Read ADC data from SMBus/I^2C interface
Write Disable	• Locks user EEPROM based on $\overline{RESET}$ or $\overline{UV/OV}$ assertion
Configuration Lock	• Locks configuration registers and EEPROM

**ADC does not affect programmable outputs.*

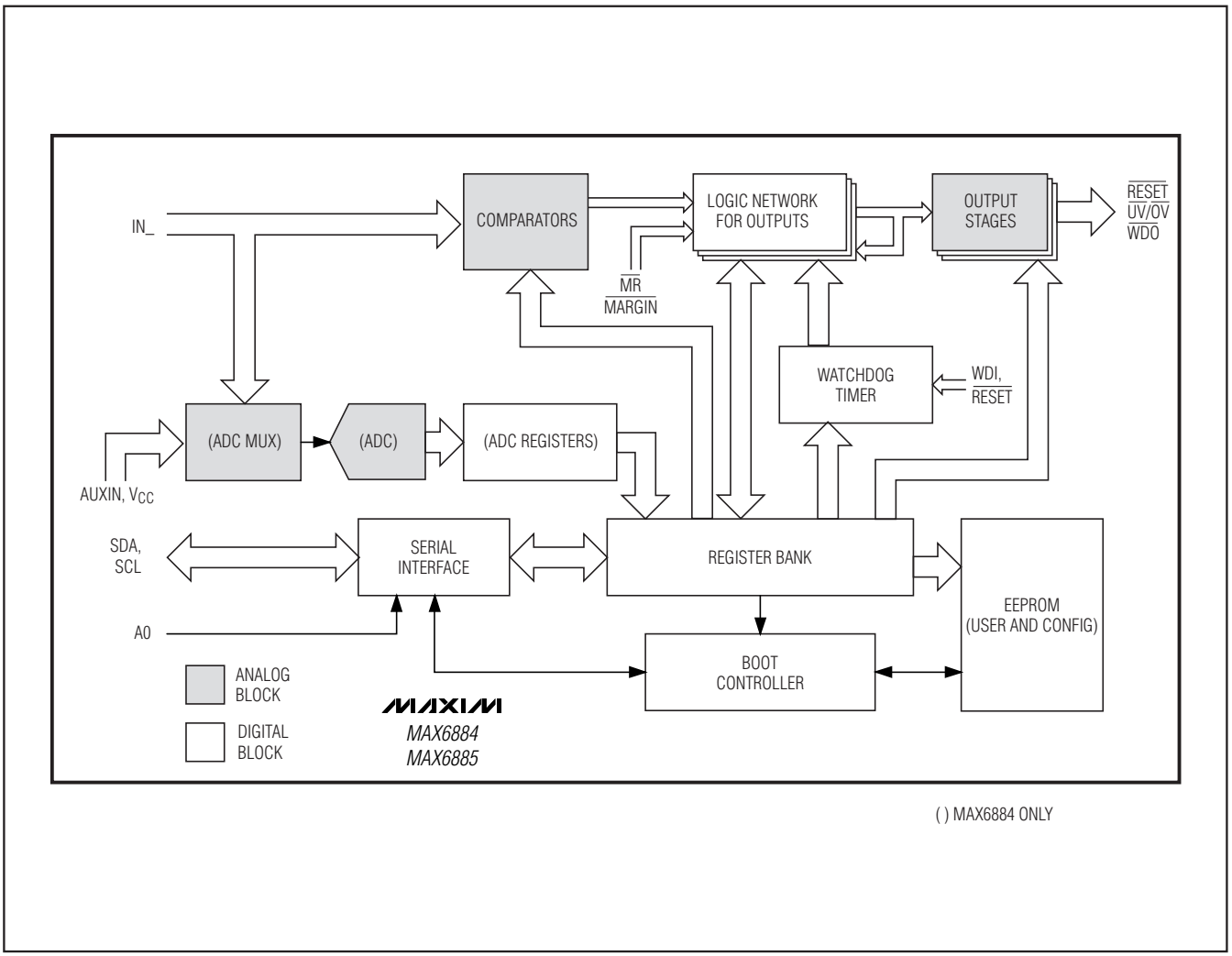
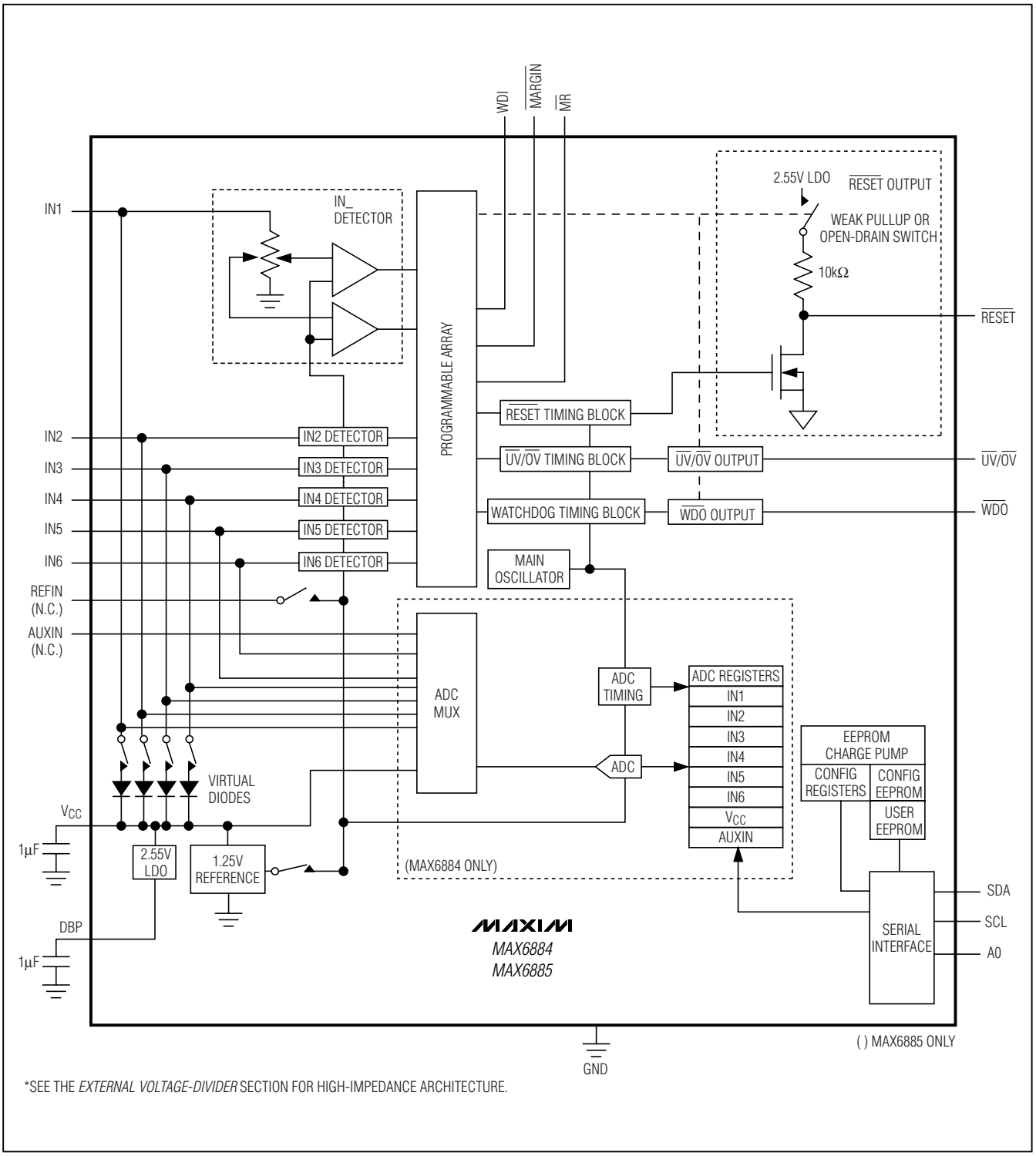


Figure 1. Top-Level Block Diagram

EEPROM-Programmable, Hex Power-Supply Supervisory Circuits

Functional Diagram



*SEE THE *EXTERNAL VOLTAGE-DIVIDER* SECTION FOR HIGH-IMPEDANCE ARCHITECTURE.

Powering the MAX6884/MAX6885

The MAX6884/MAX6885 derive power from the voltage-detector inputs: IN1–IN4 or through an externally supplied V_{CC}. A virtual diode-ORing scheme selects the positive input that supplies power to the device (see the *Functional Diagram*). The highest input voltage on IN1–IN4 supplies power to the device. One of V_{IN1}–V_{IN4} must be at least 2.7V to ensure proper operation.

Internal hysteresis ensures that the supply input that initially powered the device continues to power the device when multiple input voltages are within 50mV of each other.

V_{CC} powers the analog circuitry and is the bypass connection for the MAX6884/MAX6885 internal supply. Bypass V_{CC} to GND with a 1µF ceramic capacitor installed as close to the device as possible. The internal supply voltage, measured at V_{CC}, equals the maximum of IN1–IN4. If V_{CC} is externally supplied, V_{CC} must be at least 200mV higher than any voltage applied to IN–IN4 and V_{CC} must be brought up first. V_{CC} always powers the device when all IN_ are factory set as "ADJ." Do not use the internally generated V_{CC} to provide power to external circuitry. Externally supply power through V_{CC}. To externally supply power through V_{CC}:

1) Apply a voltage to only one of V_{CC} (2.7V to 5.5V) or IN1–IN4 (2.7V to 5.8V).
2) Program the internal/external V_{CC} Power EEPROM at 96h, Bit[5] = 1 (see Table 2).
3) Power down the device.

Subsequent power-ups and software reboots require an externally supplied V_{CC} to ensure the device is fully operational.

Table 2. Internal/External V_{CC}

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT RANGE	DESCRIPTION
16h	96h	[5]	1 = V_{CC} Powered 0 = IN1–IN4 or V_{CC} Powered
		[2]	Not Used
		[4]	Not Used
		[6]	Not Used

The MAX6884/MAX6885 also generate a digital supply voltage (DBP) for the internal logic circuitry and the EEPROM. Bypass DBP to GND with a 1µF ceramic capacitor installed as close to the device as possible. The nominal DBP output voltage is 2.55V. Do not use DBP to provide power to external circuitry.

ADC (MAX6884 Only)

An internal 10-bit ADC (MAX6884 only) converts voltages at IN1–IN4, AUXIN, and V_{CC} through a multiplexer that automatically sequences through all inputs every 200ms. Registers 18h to 27h store the ADC data (see Table 3). Read the ADC data from the MAX6884 with the serial interface. The ADC has no effect on programmable outputs $\overline{RESET}$, $\overline{UV/OV}$, or $\overline{WDO}$.

Inputs

The MAX6884/MAX6885 offer the following inputs: voltage-detector inputs IN1–IN4, auxiliary input AUXIN (MAX6884 only), manual reset input $\overline{MR}$, margin input $\overline{MARGIN}$, and reference input REFIN (MAX6884 only).

IN1–IN6

The MAX6884/MAX6885 offer six voltage-detector inputs: IN1–IN6. Each voltage-detector input offers a programmable primary undervoltage threshold and a secondary undervoltage/overvoltage threshold. Program thresholds from 0.5V to 3.05V in 10mV increments, 1.0V to 5.8V in 20mV increments, or from 0.1667V to 1.0167V in 3.3mV increments. Use the following equations to program thresholds in the appropriate registers:

$$X = \frac{V_{TH} - 1V}{0.02V}$$

for 1V to 5.8V range in 20mV increments (program bits R0Fh[5:0]).

$$X = \frac{V_{TH} - 0.5V}{0.01V}$$

for 0.5V to 3.05V range in 10mV increments (program bits R0Fh[5:0]).

$$X = \frac{V_{TH} - 0.1667V}{0.0033V}$$

for 0.1667V to 1.0167V in 3.3mV increments (see the *External Voltage-Divider* section).

where V_{TH} is the desired threshold voltage and X is the decimal code for the desired threshold (see Table 4). To set a threshold for the 1V to 5.8V range, X must equal 240 or less. Set the secondary threshold for an undervoltage or overvoltage threshold by programming bits R0Eh[5:0]. To achieve thresholds in between the 10mV and 20mV steps or to monitor voltages higher than 5.8V, program a voltage-detector input for high impedance through bits R10h[5:0] and add a resister voltage-divider (see the *External Voltage-Divider* section).

Table 3. ADC Registers (MAX6884 Only)

REGISTER ADDRESS	BIT RANGE	DESCRIPTION
18h	[7:0]	ADC IN1 Conversion Result (8 MSBs)
19h	[1:0]	ADC IN1 Conversion Result (2 LSBs)
	[7:2]	Not Used
1Ah	[7:0]	ADC IN2 Conversion Result (8 MSBs)
1Bh	[1:0]	ADC IN2 Conversion Result (2 LSBs)
	[7:2]	Not Used
1Ch	[7:0]	ADC IN3 Conversion Result (8 MSBs)
1Dh	[1:0]	ADC IN3 Conversion Result (2 LSBs)
	[7:2]	Not Used
1Eh	[7:0]	ADC IN4 Conversion Result (8 MSBs)
1Fh	[1:0]	ADC IN4 Conversion Result (2 LSBs)
	[7:2]	Not Used
20h	[7:0]	ADC IN5 Conversion Result (8 MSBs)
21h	[1:0]	ADC IN5 Conversion Result (2 LSBs)
	[7:2]	Not Used
22h	[7:0]	ADC IN6 Conversion Result (8 MSBs)
23h	[1:0]	ADC IN6 Conversion Result (2 LSBs)
	[7:2]	Not Used
24h	[7:0]	ADC AUXIN Conversion Result (8 MSBs)
25h	[1:0]	ADC AUXIN Conversion Result (2 LSBs)
	[7:2]	Not Used
26h	[7:0]	ADC V_{CC} Conversion Result (8 MSBs)
27h	[1:0]	ADC V_{CC} Conversion Result (2 LSBs)
	[7:2]	Not Used

Table 4. IN1–IN6 Threshold Register Settings

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT RANGE	DESCRIPTION
00h	80h	[7:0]	IN1 Primary Undervoltage Detector Threshold (see equations in the *IN1–IN6* section)
01h	81h	[7:0]	IN2 Primary Undervoltage Detector Threshold
02h	82h	[7:0]	IN3 Primary Undervoltage Detector Threshold
03h	83h	[7:0]	IN4 Primary Undervoltage Detector Threshold
04h	84h	[7:0]	IN5 Primary Undervoltage Detector Threshold
05h	85h	[7:0]	IN6 Primary Undervoltage Detector Threshold
06h	86h	[7:0]	IN1 Secondary Undervoltage/Overvoltage Detector Threshold (see equations in the *IN1–IN6* section)
07h	87h	[7:0]	IN2 Secondary Undervoltage/Overvoltage Detector Threshold
08h	88h	[7:0]	IN3 Secondary Undervoltage/Overvoltage Detector Threshold
09h	89h	[7:0]	IN4 Secondary Undervoltage/Overvoltage Detector Threshold
0Ah	8Ah	[7:0]	IN5 Secondary Undervoltage/Overvoltage Detector Threshold
0Bh	8Bh	[7:0]	IN6 Secondary Undervoltage/Overvoltage Detector Threshold
0Eh	8Eh	[0]	IN1 Secondary Undervoltage or Overvoltage Selection 0 = Undervoltage 1 = Overvoltage
		[1]	IN2 Secondary Undervoltage or Overvoltage Selection
		[2]	IN3 Secondary Undervoltage or Overvoltage Selection
		[3]	IN4 Secondary Undervoltage or Overvoltage Selection
		[4]	IN5 Secondary Undervoltage or Overvoltage Selection
		[5]	IN6 Secondary Undervoltage or Overvoltage Selection
		[7:6]	Not Used
0Fh	8Fh	[0]	IN1 Voltage Threshold Range 0 = 1V to 5.8V (20mV steps) 1 = 0.5V to 3.05V (10mV steps)
		[1]	IN2 Voltage Threshold Range
		[2]	IN3 Voltage Threshold Range
		[3]	IN4 Voltage Threshold Range
		[4]	IN5 Voltage Threshold Range
		[5]	IN6 Voltage Threshold Range
		[7:6]	Not Used
10h	90h	[0]	IN1 Input Impedance 0 = Normal Mode 1 = High-Z Mode (connect external resistor voltage-divider)
		[1]	IN2 Input Impedance
		[2]	IN3 Input Impedance
		[3]	IN4 Input Impedance
		[4]	IN5 Input Impedance
		[5]	IN6 Input Impedance
		[7:6]	Not Used

EEPROM-Programmable, Hex Power-Supply Supervisory Circuits

External Voltage-Divider

To achieve thresholds from 0.1667V to 1.0167V in 3.3mV increments, program the respective input voltage detector for high impedance and use an external voltage-divider (see Figure 2). Set voltage-detector inputs for high impedance by programming bits R10h[5:0]. Design the resistor voltage-divider to scale the input voltage to between 0.1667V and 1.0167V at the input of the device. In this way, voltages higher than 5.8V and in between the 10mV and 20mV steps can be monitored. Program R00h through R0Eh to adjust the thresholds between 0.1667V and 1.0167V in 3.3mV steps.

AUXIN (MAX6884 Only)

The AUXIN high-impedance analog input is intended to monitor additional system voltages not required for reset purposes. The internal 10-bit ADC converts the voltage at AUXIN and stores the data in the ADC registers (see Table 3). AUXIN does not affect any of the programmable outputs. The AUXIN input accepts power-supply voltages or other system voltages scaled to the 1.25V ADC input voltage range.

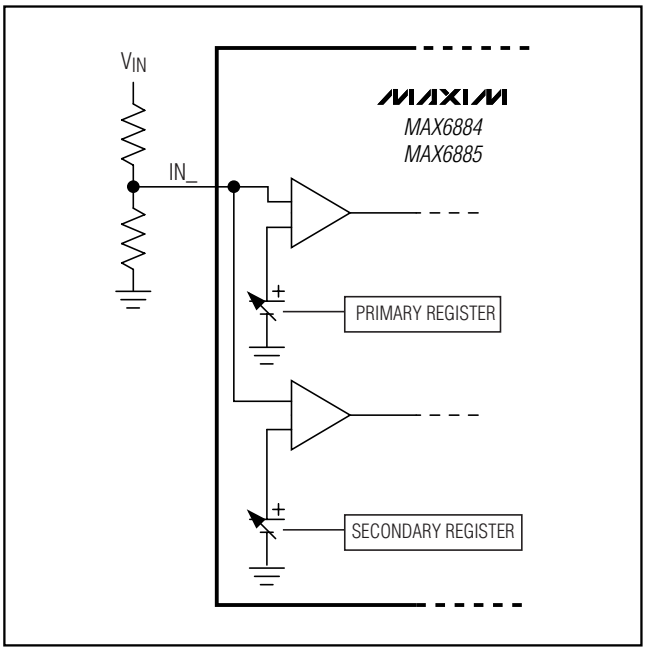


Figure 2. External Voltage-Divider Architecture

$\overline{MR}$

Program $\overline{RESET}$ and/or $\overline{UV}/\overline{OV}$ to assert when manual reset input $\overline{MR}$ is brought low (see Tables 5 and 6). Outputs programmed to assert when $\overline{MR}$ is brought low remain asserted after $\overline{MR}$ is brought high for their respective programmed timeout periods. An internal 10µA current source pulls $\overline{MR}$ to V_{DBP}. Leave $\overline{MR}$ unconnected or connect to DBP if unused.

$\overline{MARGIN}$

$\overline{MARGIN}$ allows system-level testing while power supplies exceed the normal ranges. Drive $\overline{MARGIN}$ low to hold the programmable outputs in their existing state while system-level testing occurs. Leave $\overline{MARGIN}$ unconnected or connect to DBP if unused. An internal 10µA current source pulls $\overline{MARGIN}$ to V_{DBP}. The internal ADC continues to convert voltages while $\overline{MARGIN}$ is low. The state of each programmable output does not change while $\overline{MARGIN}$ = GND. $\overline{MARGIN}$ overrides $\overline{MR}$ if both are asserted at the same time.

REFIN (MAX6884 Only)

The MAX6884/MAX6885 feature an internal 1.25V voltage reference. The voltage reference sets the threshold of the voltage detectors and provides a reference voltage for the internal ADC. Program the MAX6884 to use an internal or external reference by programming bit R16h[7] (see Table 5). Leave REFIN unconnected when using the internal reference. REFIN accepts an external reference in the 1.225V to 1.275V range.

Table 5. Internal/External Reference

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT RANGE	DESCRIPTION
16h	96h	[7]	1 = Enable External Reference 0 = Enable Internal Reference

Programmable Outputs

The MAX6884/MAX6885 feature three programmable active-low outputs: $\overline{RESET}$, $\overline{UV/OV}$, and $\overline{WDO}$. Program each output for open-drain or weak pullup. An internal 10kΩ resistor connected from each output to a 2.55V internal LDO provides a weak pullup. During power-up, the outputs are held low for $1V < V_{CC} < V_{UVLO}$. Any output programmed to depend on no condition always remains in its active state. For example, if the state of $\overline{UV/OV}$ is not programmed to depend on any condition, $\overline{UV/OV}$ will always be low. Figure 3 shows a timing diagram of a typical relationship between a monitored input voltage and outputs $\overline{RESET}$ and $\overline{UV/OV}$. $\overline{RESET}$ and $\overline{UV/OV}$ are a function of only IN1.

$\overline{RESET}$

Program $\overline{RESET}$ to depend on $\overline{MR}$, $\overline{UV/OV}$, $\overline{WDO}$, or any programmable primary voltage-detector input (see Table 6). As an example, $\overline{RESET}$ may depend on the IN3 primary undervoltage threshold, $\overline{MR}$, $\overline{UV/OV}$, and $\overline{WDO}$. Write 1's to R11h[1:0], R11h[4], and R12h[7] to configure as indicated. IN3 must be above the undervoltage threshold, $\overline{MR}$ must be high, $\overline{UV/OV}$ must be deasserted, and $\overline{WDO}$ must be deasserted to be a logic "1," then $\overline{RESET}$ deasserts. The logic state of $\overline{RESET}$, in this example, is equivalent to the logical statement:

$$IN3 \cdot \overline{MR} \cdot \overline{UV/OV} \cdot \overline{WDO}$$

$\overline{RESET}$ remains low for its programmed timeout period (t_{RP}) after all assertion-causing conditions are removed. Program timeout periods for $\overline{RESET}$ from 25µs to 1600ms (see Table 6). Configure $\overline{RESET}$ for open-drain or weak pullup through bit R12h[0].

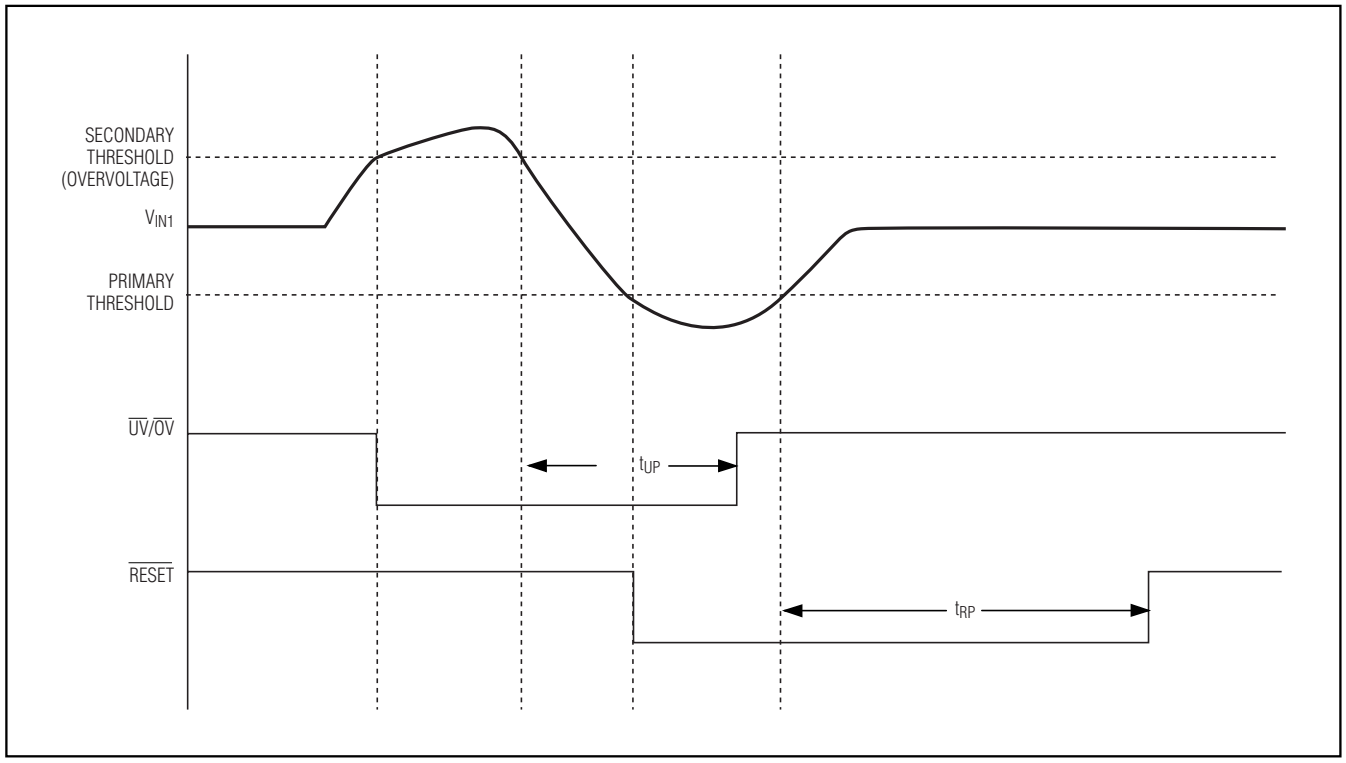


Figure 3. Output Timing Diagram

Table 6. Programmable $\overline{\text{RESET}}$ Options

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT RANGE	DESCRIPTION
11h	91h	[0]	1 = $\overline{\text{RESET}}$ Assertion Depends on $\overline{\text{MR}}$ 0 = $\overline{\text{RESET}}$ Assertion Does Not Depend on $\overline{\text{MR}}$
		[1]	1 = $\overline{\text{RESET}}$ Assertion Depends on $\overline{\text{UV}}$/$\overline{\text{OV}}$ 0 = $\overline{\text{RESET}}$ Assertion Does Not Depend on $\overline{\text{UV}}$/$\overline{\text{OV}}$
		[2]	1 = $\overline{\text{RESET}}$ Assertion Depends on IN1 Primary Undervoltage 0 = $\overline{\text{RESET}}$ Assertion Does Not Depend on IN1 Primary Undervoltage
		[3]	1 = $\overline{\text{RESET}}$ Assertion Depends on IN2 Primary Undervoltage 0 = $\overline{\text{RESET}}$ Assertion Does Not Depend on IN2 Primary Undervoltage
		[4]	1 = $\overline{\text{RESET}}$ Assertion Depends on IN3 Primary Undervoltage 0 = $\overline{\text{RESET}}$ Assertion Does Not Depend on IN3 Primary Undervoltage
		[5]	1 = $\overline{\text{RESET}}$ Assertion Depends on IN4 Primary Undervoltage 0 = $\overline{\text{RESET}}$ Assertion Does Not Depend on IN4 Primary Undervoltage
		[6]	1 = $\overline{\text{RESET}}$ Assertion Depends on IN5 Primary Undervoltage 0 = $\overline{\text{RESET}}$ Assertion Does Not Depend on IN5 Primary Undervoltage
		[7]	1 = $\overline{\text{RESET}}$ Assertion Depends on IN6 Primary Undervoltage 0 = $\overline{\text{RESET}}$ Assertion Does Not Depend on IN6 Primary Undervoltage
12h	92h	[0]	$\overline{\text{RESET}}$ Output Type 1 = Open Drain 0 = Weak Pullup
		[3:1]	$\overline{\text{RESET}}$ Deassertion Time Delay 000 = 25µs 001 = 1.56ms 010 = 6.25ms 011 = 25ms 100 = 50ms 101 = 200ms 110 = 400ms 111 = 1600ms
		[6:4]	Not Used
		[7]	1 = $\overline{\text{RESET}}$ Assertion Depends on $\overline{\text{WDO}}$ Assertion 0 = $\overline{\text{RESET}}$ Assertion Does Not Depend on $\overline{\text{WDO}}$ Assertion

$\overline{UV}/\overline{OV}$

Program $\overline{UV}/\overline{OV}$ to depend on $\overline{MR}$, $\overline{RESET}$, or any programmable secondary voltage detector input (see Table 7). As an example, $\overline{UV}/\overline{OV}$ may depend on the IN1 secondary overvoltage threshold, $\overline{MR}$, and $\overline{RESET}$. Write 1's to R13h[2:0] and R0Eh[1] to configure as indicated. IN1 must be below the overvoltage threshold, $\overline{MR}$ must be high, and $\overline{RESET}$ must be deasserted to be a logic "1," then UV/OV deasserts. The logic state of $\overline{UV}/\overline{OV}$, in this example, is equivalent to the logical statement:

$$IN1 \cdot \overline{MR} \cdot \overline{RESET}$$

$\overline{UV}/\overline{OV}$ remains low for its programmed time delay (t_{UP}) after all assertion-causing conditions are removed. Program time delays for $\overline{UV}/\overline{OV}$ from 25µs to 1600ms (see Table 7). Configure $\overline{UV}/\overline{OV}$ for open drain or weak pullup through bit R14h[0].

Table 7. Programmable $\overline{UV}/\overline{OV}$ Options

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT RANGE	DESCRIPTION
13h	93h	[0]	1 = $\overline{UV}/\overline{OV}$ Assertion Depends on $\overline{MR}$ 0 = $\overline{UV}/\overline{OV}$ Assertion Does Not Depend on $\overline{MR}$
		[1]	1 = $\overline{UV}/\overline{OV}$ Assertion Depends on $\overline{RESET}$ 0 = $\overline{UV}/\overline{OV}$ Assertion Does Not Depend on $\overline{RESET}$
		[2]	1 = $\overline{UV}/\overline{OV}$ Assertion Depends on IN1 Secondary Undervoltage/Overvoltage Threshold 0 = $\overline{UV}/\overline{OV}$ Assertion Does Not Depend on IN1 Secondary Undervoltage/Overvoltage Threshold
		[3]	1 = $\overline{UV}/\overline{OV}$ Assertion Depends on IN2 Secondary Undervoltage/Overvoltage Threshold 0 = $\overline{UV}/\overline{OV}$ Assertion Does Not Depend on IN2 Secondary Undervoltage/Overvoltage Threshold
		[4]	1 = $\overline{UV}/\overline{OV}$ Assertion Depends on IN3 Secondary Undervoltage/Overvoltage Threshold 0 = $\overline{UV}/\overline{OV}$ Assertion Does Not Depend on IN3 Secondary Undervoltage/Overvoltage Threshold
		[5]	1 = $\overline{UV}/\overline{OV}$ Assertion Depends on IN4 Secondary Undervoltage/Overvoltage Threshold 0 = $\overline{UV}/\overline{OV}$ Assertion Does Not Depend on IN4 Secondary Undervoltage/Overvoltage Threshold
		[6]	1 = $\overline{UV}/\overline{OV}$ Assertion Depends on IN5 Secondary Undervoltage/Overvoltage Threshold 0 = $\overline{UV}/\overline{OV}$ Assertion Does Not Depend on IN5 Secondary Undervoltage/Overvoltage Threshold
		[7]	1 = $\overline{UV}/\overline{OV}$ Assertion Depends on IN6 Secondary Undervoltage/Overvoltage Threshold 0 = $\overline{UV}/\overline{OV}$ Assertion Does Not Depend on IN6 Secondary Undervoltage/Overvoltage Threshold
14h	94h	[0]	$\overline{UV}/\overline{OV}$ Output Type 1 = Open Drain 0 = Weak Pullup
		[3:1]	$\overline{UV}/\overline{OV}$ Deassertion Time Delay 000 = 25µs 001 = 1.56ms 010 = 6.25ms 011 = 25ms 100 = 50ms 101 = 200ms 110 = 400ms 111 = 1600ms
		[7:4]	Unused

EEPROM-Programmable, Hex Power-Supply Supervisory Circuits

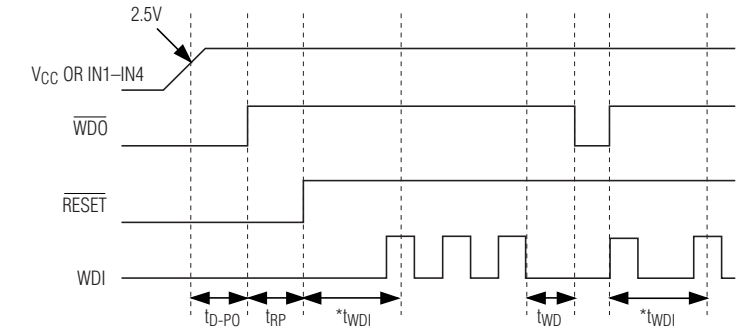
WDO

The MAX6884/MAX6885 offer a separate output for the watchdog timer system. WDO is active low and programmable for open-drain or weak pullup. Program WDO to assert RESET when the watchdog timer expires. See the *Configuring the Watchdog Timer* section for a complete description of the watchdog timer system.

Configuring the Watchdog Timer

A watchdog timer monitors microprocessor (µP) software execution for a stalled condition and resets the µP if it stalls. The output of the watchdog timer (WDO) connects to the reset input or a nonmaskable interrupt of the µP. Program R15h to configure the watchdog timer functions (see Table 8). The watchdog timer features independent initial and normal watchdog timeout periods between 6.25ms and 102.4s (see Figure 4).

The initial watchdog timeout period (t_{WDI}) is active immediately after power-up, after a reset event takes place, after enabling the watchdog timer, or after the watchdog timer expires. The initial watchdog timeout period allows the µP to perform its initialization process.



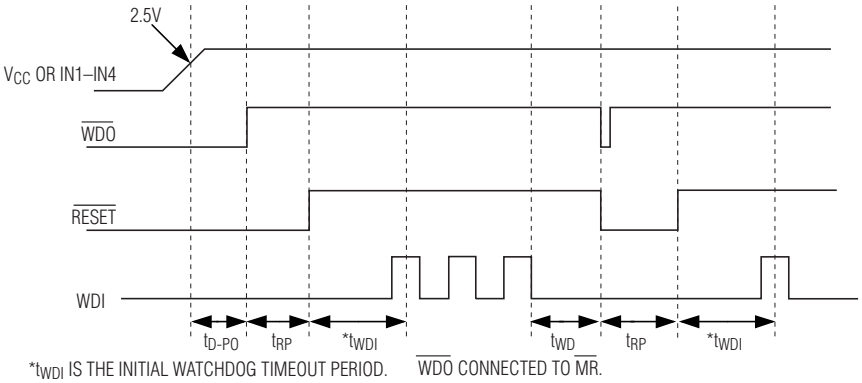


Figure 4. Watchdog Timing Diagrams

The normal watchdog timeout period (t_{WD}) is active after the initial watchdog timer and continues to be active until the watchdog timer expires. The normal watchdog timeout period monitors a pulsed output of the µP that indicates when normal processor behavior occurs. If no pulse occurs during the normal watchdog timeout period, this indicates that the processor has stopped operating or is stuck in an infinite execution loop and $\overline{WDO}$ asserts. Disable or enable the watchdog timer through R15h[7].

If $\overline{RESET}$ is programmed to depend on $\overline{WDO}$ and the watchdog timer expires, $\overline{WDO}$ will assert for a short pulse, just long enough to assert $\overline{RESET}$ (typically less than 5µs; see Figure 4). If $\overline{WDO}$ is not programmed to depend on $\overline{RESET}$ and the watchdog timer expires, $\overline{WDO}$ will remain asserted until a low-to-high or high-to-low edge occurs on WDI. Program $\overline{WDO}$ for open-drain or weak pullup (see Table 8).

Fault Register

Registers 28h to 2Ah store all fault conditions including undervoltage, overvoltage, and watchdog timer faults (see Table 9). Fault registers are read-only and lose contents upon power removal. The first read command from the fault registers after power-up gives invalid data. Reading the fault register clears all fault flags in the register.

Table 8. Watchdog Register Settings

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT RANGE	DESCRIPTION
15h	95h	[0]	$\overline{WDO}$ Output Type 1 = Open Drain 0 = Weak Pullup
		[3:1]	Initial Watchdog Timeout 000 = 6.25ms 001 = 25ms 010 = 100ms 011 = 400ms 100 = 1.6s 101 = 6.4ms 110 = 25.6s 111 = 102.4s
		[6:4]	Normal Watchdog Timeout 000 = 6.25ms 001 = 25ms 010 = 100ms 011 = 400ms 1100 = 1.6s 101 = 6.4ms 110 = 25.6s 111 = 102.4s
		[7]	Watchdog Enable 1 = Enabled 0 = Disabled

Table 9. Fault Registers (28h–2Ah)

REGISTER ADDRESS	BIT RANGE	DESCRIPTION
28h	[0]	1 = IN1 Voltage Falls Below Primary Undervoltage Threshold
	[1]	1 = IN2 Voltage Falls Below Primary Undervoltage Threshold
	[2]	1 = IN3 Voltage Falls Below Primary Undervoltage Threshold
	[3]	1 = IN4 Voltage Falls Below Primary Undervoltage Threshold
	[4]	1 = IN5 Voltage Falls Below Primary Undervoltage Threshold
	[5]	1 = IN6 Voltage Falls Below Primary Undervoltage Threshold
	[7:6]	Unused
29h	[0]	1 = IN1* Voltage Falls Below Secondary Threshold
	[1]	1 = IN2* Voltage Falls Below Secondary Threshold
	[2]	1 = IN3* Voltage Falls Below Secondary Threshold
	[3]	1 = IN4* Voltage Falls Below Secondary Threshold
	[4]	1 = IN5* Voltage Falls Below Secondary Threshold
	[5]	1 = IN6* Voltage Falls Below Secondary Threshold
	[7:6]	Unused
2Ah	[0]	1 = $\overline{UV}/\overline{OV}$ Has Been Asserted
	[1]	1 = $\overline{RESET}$ Has Been Asserted
	[6:2]	Unused
	[7]	1 = $\overline{WDO}$ Has Been Asserted

**Does not matter if set as undervoltage or overvoltage.*

Configuration Lock

Lock the configuration register bank and configuration EEPROM contents after initial programming by setting the lock bit high (see Table 10). Locking the configuration prevents write operations to configuration EEPROM and configuration registers except the configuration lock bit. Set the lock bit to 0 to reconfigure the device.

Write Disable

A unique write disable feature protects the MAX6884/MAX6885 from inadvertent user EEPROM writes. As input voltages that power the serial interface, a µP, or any other writing devices fall, unintentional data may be written onto the data bus. The user EEPROM write-disable function (see Table 11) ensures that unintentional data does not corrupt the MAX6884/MAX6885 user EEPROM data.

Table 10. Configuration Lock Bit

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT RANGE	DESCRIPTION
16h	96h	[3]	1 = Configuration Locked 0 = Configuration Unlocked

Table 11. User EEPROM Write Disable Bits

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT RANGE	DESCRIPTION
16h	96h	[1]	1 = User EEPROM Writes Disabled on $\overline{\text{RESET}}$ Assertion 0 = User EEPROM Writes Enabled on $\overline{\text{RESET}}$ Assertion
		[0]	1 = User EEPROM Writes Disabled on $\overline{\text{UV}}/\overline{\text{OV}}$ Assertion 0 = User EEPROM Writes Enabled on $\overline{\text{UV}}/\overline{\text{OV}}$ Assertion

Configuration Register Bank and EEPROM

The configuration registers can be directly modified by the serial interface without modifying the EEPROM after the power-up procedure terminates and the configuration EEPROM data has been loaded into the configuration register bank. Use the write byte or block write protocols to write directly to the configuration registers. Changes to the configuration registers take effect immediately and are lost upon power removal. At device power-up, the register bank loads configuration data from the EEPROM. Configuration data may be directly altered in the register bank during application development, allowing maximum flexibility. Transfer the new configuration data, byte by byte, to the configuration EEPROM with the write byte protocol. The next device power-up or software reboot automatically loads the new configuration. See Table 12 for a complete register map.

Configuration EEPROM

The configuration EEPROM addresses range from 80h to 97h. Write data to the configuration EEPROM to set up the MAX6884/MAX6885 automatically upon power-up. Data transfers from the configuration EEPROM to the configuration registers when V_{CC} exceeds UVLO during power-up or after a software reboot. After V_{CC} exceeds UVLO, an internal 1MHz clock starts after a 5µs delay, and data transfer begins. Data transfer disables access to the configuration registers and EEPROM. The data transfer from EEPROM to configuration registers takes 2.5ms maximum. Read configuration EEPROM and configuration register data any time after power-up or software reboot. Write commands to the configuration EEPROM and configuration registers are allowed at any time after power-up or software reboot unless the configuration lock bit is set (see Table 10). When the configuration lock bit is set, all write access to EEPROM and registers is disabled with the exception of the configuration lock bit itself. The maximum cycle time to write a single byte in EEPROM is 11ms (max).

User EEPROM

The 512-bit user EEPROM addresses range from 40h to 7Fh (see Figure 11). Store revision data, board revision data, or other data in these registers. The maximum cycle time to write a single byte is 11ms (max). Disable writes to the user EEPROM during $\overline{\text{RESET}}$ or $\overline{\text{UV}}/\overline{\text{OV}}$ assertion by programming bit R16h[1] or R16h[0], respectively (see Table 11).

Table 12. Register Map

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	READ/ WRITE	DESCRIPTION
00h	80h	R/W	IN1 Primary Undervoltage Detector Threshold (Table 4)
01h	81h	R/W	IN2 Primary Undervoltage Detector Threshold (Table 4)
02h	82h	R/W	IN3 Primary Undervoltage Detector Threshold (Table 4)
03h	83h	R/W	IN4 Primary Undervoltage Detector Threshold (Table 4)
04h	84h	R/W	IN5 Primary Undervoltage Detector Threshold (Table 4)
05h	85h	R/W	IN6 Primary Undervoltage Detector Threshold (Table 4)
06h	86h	R/W	IN1 Secondary Undervoltage/Overvoltage Detector Threshold (Table 4)
07h	87h	R/W	IN2 Secondary Undervoltage/Overvoltage Detector Threshold (Table 4)
08h	88h	R/W	IN3 Secondary Undervoltage/Overvoltage Detector Threshold (Table 4)
09h	89h	R/W	IN4 Secondary Undervoltage/Overvoltage Detector Threshold (Table 4)
0Ah	8Ah	R/W	IN5 Secondary Undervoltage/Overvoltage Detector Threshold (Table 4)
0Bh	8Bh	R/W	IN6 Secondary Undervoltage/Overvoltage Detector Threshold (Table 4)
0Ch	8Ch	R	Unused. Returns 0h when read.
0Dh	8Dh	R	Unused. Returns 0h when read.
0Eh	8Eh	R/W	Secondary Threshold Undervoltage/Overvoltage Selection (Table 4)
0Fh	8Fh	R/W	Threshold Range Selection (Table 4)
10h	90h	R/W	High-Z Mode Selection (Table 4)
11h	91h	R/W	$\overline{\text{RESET}}$ Dependency Selection (Table 6)
12h	92h	R/W	$\overline{\text{RESET}}$ Output Type, Timeout Period, and $\overline{\text{WDO}}$ Dependency Selection (Table 6)
13h	93h	R/W	$\overline{\text{UV}}/\overline{\text{OV}}$ Dependency Selection (Table 7)
14h	94h	R/W	$\overline{\text{UV}}/\overline{\text{OV}}$ Output Type and Timeout Period (Table 7)
15h	95h	R/W	Watchdog Initial and Normal Timeout Selection (Table 8)
16h	96h	R/W	Internal/External V_{CC} (Table 2), Internal/External Reference (Table 5), Configuration Lock Bit (Table 10), User EEPROM Write Disable (Table 11)
17h	97h	R	Unused (Table 5)
18h	—	R	ADC Conversion Data for IN1 (8 MSBs) (Table 3)
19h	—	R	ADC Conversion Data for IN1 (2 LSBs) (Table 3)
1Ah	—	R	ADC Conversion Data for IN2 (8 MSBs) (Table 3)
1Bh	—	R	ADC Conversion Data for IN2 (2 LSBs) (Table 3)
1Ch	—	R	ADC Conversion Data for IN3 (8 MSBs) (Table 3)
1Dh	—	R	ADC Conversion Data for IN3 (2 LSBs) (Table 3)
1Eh	—	R	ADC Conversion Data for IN4 (8 MSBs) (Table 3)
1Fh	—	R	ADC Conversion Data for IN4 (2 LSBs) (Table 3)
20h	—	R	ADC Conversion Data for IN5 (8 MSBs) (Table 3)
21h	—	R	ADC Conversion Data for IN5 (2 LSBs) (Table 3)
22h	—	R	ADC Conversion Data for IN6 (8 MSBs) (Table 3)
23h	—	R	ADC Conversion Data for IN6 (2 LSBs) (Table 3)
24h	—	R	ADC Conversion Data for AUXIN (8 MSBs) (Table 3)

Table 12. Register Map (continued)

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	READ/ WRITE	DESCRIPTION
25h	—	R	ADC Conversion Data for AUXIN (2 LSBs) (Table 3)
26h	—	R	ADC Conversion Data for V_{CC} (8 MSBs) (Table 3)
27h	—	R	ADC Conversion Data for V_{CC} (2 LSBs) (Table 3)
28h	—	R	Fault Flags for Primary Voltage Detectors (Table 9)
29h	—	R	Fault Flags for Secondary Voltage Detectors (Table 9)
2Ah	—	R	Fault Flags for $\overline{RESET}$, $\overline{UV}/\overline{OV}$, and $\overline{WDO}$ (Table 9)

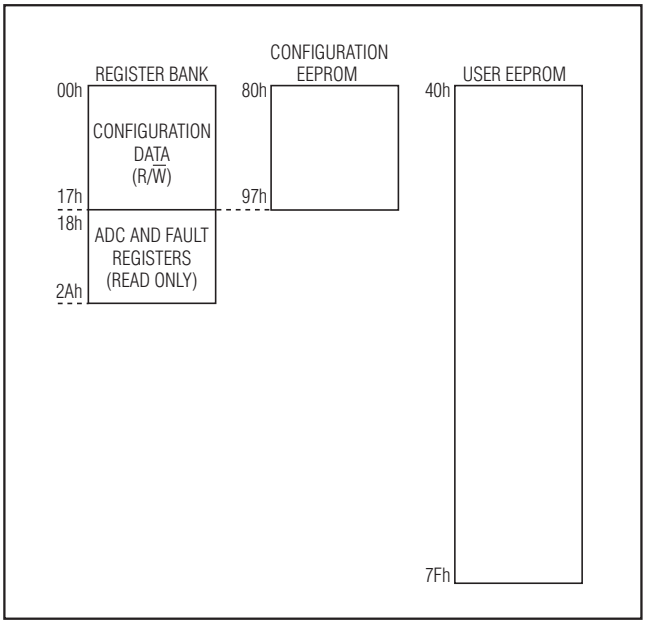


Figure 5. Memory Map

Configuring the MAX6884/MAX6885

The MAX6884/MAX6885 factory-default configuration sets all registers to 00h except for bits R91h[0], R92h[0], R93h[0], R94h[0], R95h[0], which are set to 1. This configuration sets all three programmable outputs ($\overline{RESET}$, $\overline{UV}/\overline{OV}$, $\overline{WDO}$) as open drain, and $\overline{RESET}$ and $\overline{UV}/\overline{OV}$ dependent on $\overline{MR}$ (putting all outputs into high-impedance states until the device is reconfigured by the user). Each device requires configuration before full power is applied to the system. Below is a general step-by-step procedure for programming the MAX6884/MAX6885:

1) Apply a supply voltage to IN1–IN4 or V_{CC}, depending on the programmed configuration (see the *Powering the MAX6884/MAX6885* section). The applied voltage must be 2.7V or higher.
2) Transmit data through the serial interface. Write to the configuration registers first to ensure the device is configured properly (see the *Write Byte* and *Block Write* sections).
3) Use the read word protocol to read back the data from the configuration registers to verify the data was written (see the *Receive Byte* and *Block Read* sections).
4) Write the same data written to the configuration registers to the appropriate configuration EEPROM registers. After completing EEPROM configuration, apply full power to the system to begin normal operation. The nonvolatile EEPROM stores the configuration information while power is off.

Software Reboot

A software reboot restores the EEPROM configuration to the volatile registers without cycling the power supplies. Use the send byte command with data byte C4h to initiate a software reboot. The 2.5ms (max) power-up delay also applies after a software reboot.

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SMBus/I²C-Compatible Serial Interface

The MAX6884/MAX6885 feature an I²C/SMBus-compatible 2-wire serial interface consisting of a serial data line (SDA) and a serial clock line (SCL). SDA and SCL facilitate bidirectional communication between the MAX6884/MAX6885 and the master device at clock rates up to 400kHz. Figure 6 shows the 2-wire interface timing diagram. The MAX6884/MAX6885 are transmit/receive slave-only devices, relying upon a master device to generate a clock signal. The master device (typically a microcontroller) initiates data transfer on the bus and generates SCL to permit that transfer.

A master device communicates to the MAX6884/MAX6885 by transmitting the proper address followed by command and/or data words. Each transmit sequence is framed by a START (S) or REPEATED START (SR) condition and a STOP (P) condition. Each word transmitted over the bus is 8 bits long and is always followed by an acknowledge pulse.

SCL is a logic input, while SDA is an open-drain input/output. SCL and SDA both require external pullup resistors to generate the logic-high voltage. Use 4.7kΩ resistors for most applications.

Bit Transfer

Each clock pulse transfers one data bit. The data on SDA must remain stable while SCL is high (see Figure 7), otherwise the MAX6884/MAX6885 register a START or STOP condition (see Figure 8) from the master. SDA and SCL idle high when the bus is not busy.

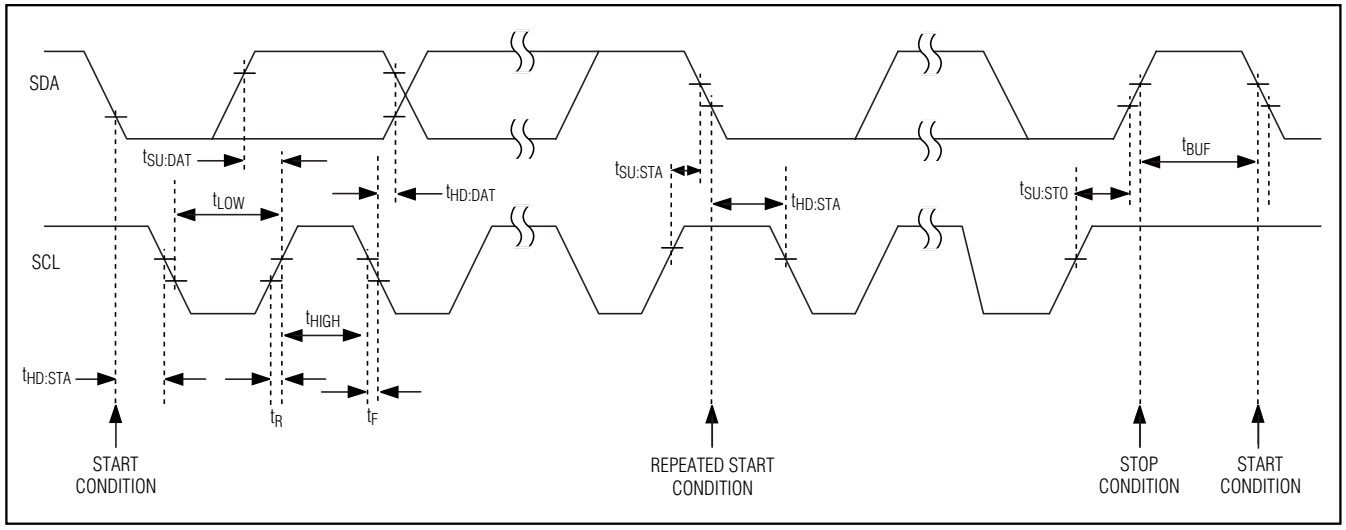

Figure 6. Serial Interface Timing

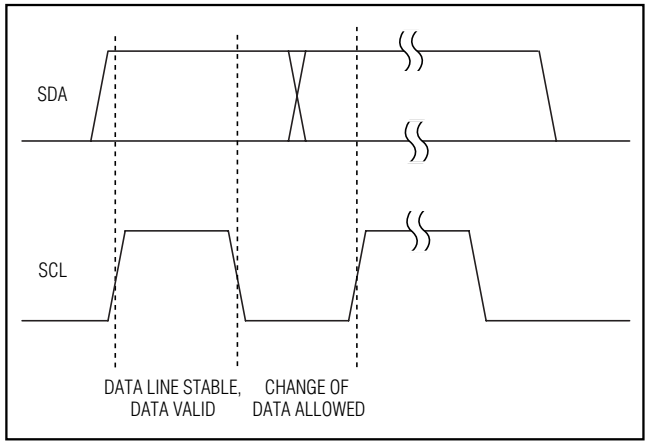

Figure 7. Bit Transfer

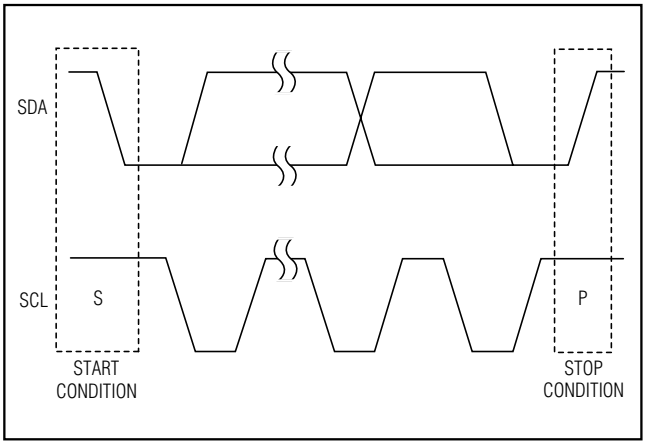

Figure 8. Start and Stop Conditions

Start and Stop Conditions

Both SCL and SDA idle high when the bus is not busy. A master device signals the beginning of a transmission with a START (S) condition (see Figure 8) by transitioning SDA from high to low while SCL is high. The master device issues a STOP (P) condition (see Figure 8) by transitioning SDA from low to high while SCL is high. A STOP condition frees the bus for another transmission. The bus remains active if a REPEATED START condition is generated, such as in the block read protocol (see Figure 11).

Early STOP Conditions

The MAX6884/MAX6885 recognize a STOP condition at any point during transmission except if a STOP condition occurs in the same high pulse as a START condition. This condition is not a legal I²C format; at least one clock pulse must separate any START and STOP condition.

Repeated START Conditions

A REPEATED START (SR) condition may indicate a change of data direction on the bus. Such a change occurs when a command word is required to initiate a read operation (see Figure 11). SR may also be used when the bus master is writing to several I²C devices and does not want to relinquish control of the bus. The MAX6884/MAX6885 serial interface supports continuous write operations with or without an SR condition separating them. Continuous read operations require SR conditions because of the change in direction of data flow.

Acknowledge

The acknowledge bit (ACK) is the 9th bit attached to any 8-bit data word. The receiving device always generates an ACK. The MAX6884/MAX6885 generate an ACK when receiving an address or data by pulling SDA low during the 9th clock period (see Figure 9). When transmitting data, such as when the master device reads data back from the MAX6884/MAX6885, the MAX6884/MAX6885 wait for the master device to generate an ACK. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if the receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master should reattempt communication at a later time. The MAX6884/MAX6885 generate a NACK after the command byte during a software reboot, while writing to the EEPROM, or when receiving an illegal memory address.

Slave Address

The MAX6884/MAX6885 slave address conforms to the following table:

SA7 (MSB)	SA6	SA5	SA4	SA3	SA2	SA1	SA0 (LSB)
1	0	1	0	0	A0	X	R/$\overline{W}$

X = Don't care.

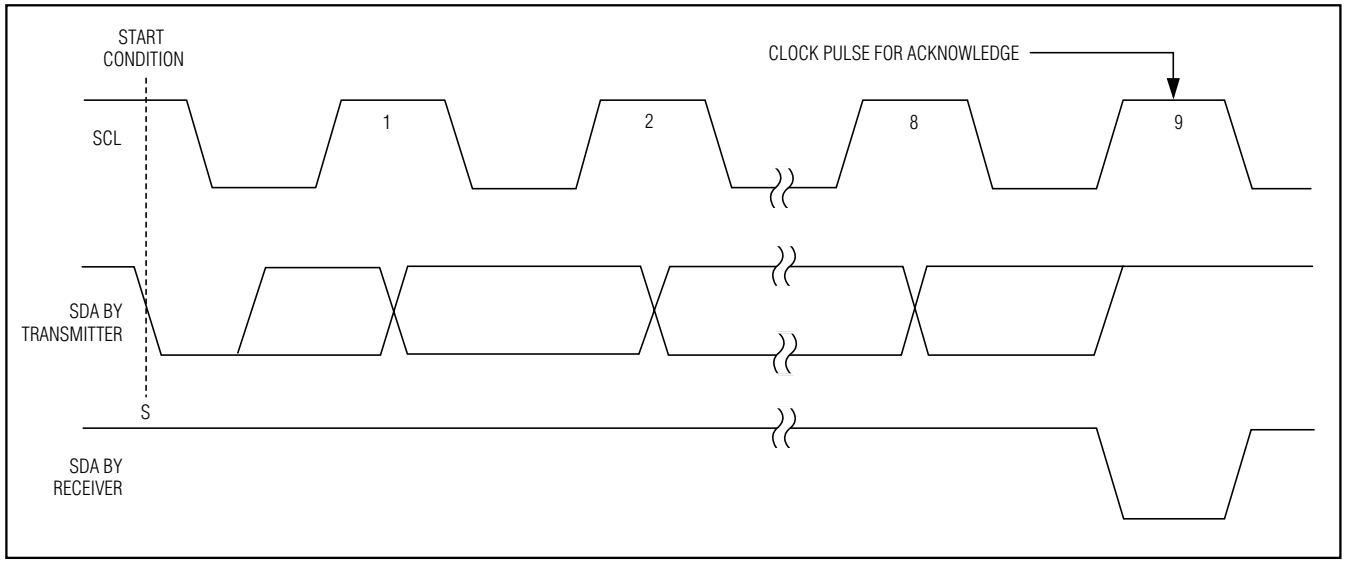

Figure 9. Acknowledge

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SA7 through SA4 represent the standard 2-wire interface address (1010); for devices with EEPROM, SA2 corresponds to the A0 address inputs of the MAX6884/MAX6885 (hardwired as logic-low or logic-high). SA0 is a read/write flag bit (0 = write, 1 = read).

The A0 address input allows up to two MAX6884/MAX6885s to connect to one bus. Connect A0 to GND or to the 2-wire serial-interface power supply (see Figure 10).

Send Byte

The send byte protocol allows the master device to send one byte of data to the slave device (see Figure 11). The send byte presets a register pointer address for a subsequent read or write. The slave sends a NACK instead of an ACK if the master tries to send an address that is not allowed or if the device is writing data to EEPROM or is booting. If the master sends C0h, the data is ACK, because this could be the start of the block write protocol, and the slave expects following data byte. If the master sends a STOP condition, the internal address pointer does not change. If the master sends C1h, this signifies that the block read protocol is expected, and a repeated START condition should follow. The device reboots if the master sends C4h. The send byte procedure follows:

1) The master sends a START condition.
2) The master sends the 7-bit slave address and a write bit (low).
3) The addressed slave asserts an ACK on SDA.
4) The master sends an 8-bit data byte.
5) The addressed slave asserts an ACK on SDA.
6) The master sends a STOP condition.

Write Byte

The write byte protocol allows the master device to write a single byte in the register bank or in the EEPROM (see Figure 11). The write byte/word procedure follows:

1) The master sends a START condition.
2) The master sends the 7-bit slave address and a write bit (low).
3) The addressed slave asserts an ACK on SDA.
4) The master sends an 8-bit command code.

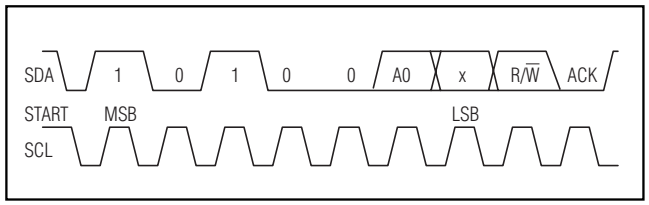

Figure 10. Slave Address

5) The addressed slave asserts an ACK on SDA.
6) The master sends an 8-bit data byte.
7) The addressed slave asserts an ACK on SDA.
8) The master sends a STOP condition.

To write a single byte to the register bank, only the 8-bit command code and a single 8-bit data byte are sent. The command code must be in the 00h to 2Fh range. The data byte is written to the register bank if the command code is valid. The slave generates a NACK at step 5 if the command code is invalid or any internal operations are ongoing. To write a single byte of data to the user or configuration EEPROM, the 8-bit command code and a single 8-bit data byte are sent.

Block Write

The block write protocol allows the master device to write a block of data (1 to 16 bytes) to the EEPROM or to the register bank (see Figure 11). The destination address must already be set by the send byte protocol and the command code must be C0h. If the number of bytes to be written causes the address pointer to exceed 2Fh for the configuration register or 9Fh for the configuration EEPROM, the address pointer stops incrementing, overwriting the last memory address with the remaining bytes of data. Only the last data byte sent is stored in 17h (as 2Fh is read only and a write cause no change in the content). If the number of bytes to be written exceeds the address pointer 9Fh for the user EEPROM, the address pointer stops incrementing and continues writing exceeding data to the last address. Only the last data is actually written to 9Fh. The block write procedure follows:

1) The master sends a START condition.
2) The master sends the 7-bit slave address and a write bit (low).
3) The addressed slave asserts an ACK on SDA.
4) The master sends the 8-bit command code for block write (C0h).
5) The addressed slave asserts an ACK on SDA.
6) The master sends the 8-bit byte count (1 to 16 bytes) N.
7) The addressed slave asserts an ACK on SDA.
8) The master sends 8 bits of data.
9) The addressed slave asserts an ACK on SDA.
10) Repeat steps 8 and 9 N - 1 times.
11) The master generates a STOP condition.

Read Byte

The read byte protocol allows the master device to read the register or an EEPROM location (user or configuration) content of the MAX6884/MAX6885 (see Figure 11). The read byte procedure follows:

1) The master sends a START condition.
2) The master sends the 7-bit slave address and a write bit (low).
3) The addressed slave asserts an ACK on the data line.
4) The master sends 8 data bits.
5) The active slave asserts an ACK on the data line.
6) The master sends a repeated start condition.
7) The master sends the 7-bit slave ID plus a read bit (high).
8) The addressed slave asserts an ACK on the data line.
9) The slave sends 8 data bits.
10) The master asserts a NACK on the data line.
11) The master generates a STOP condition.

SEND BYTE FORMAT

S	ADDRESS	$\overline{WR}$	ACK	DATA	ACK	P
	7 BITS	0		8 BITS		

SLAVE ADDRESS: EQUIVALENT TO CHIP-SELECT LINE OF A 3-WIRE INTERFACE

DATA BYTE: PRESETS THE INTERNAL ADDRESS POINTER

RECEIVE BYTE FORMAT

S	ADDRESS	$\overline{WR}$	ACK	DATA	$\overline{ACK}$	P
	7 BITS	1		8 BITS		

SLAVE ADDRESS: EQUIVALENT TO CHIP-SELECT LINE OF A 3-WIRE INTERFACE

DATA BYTE: READS DATA FROM THE REGISTER COMMANDED BY THE LAST READ BYTE OR WRITE BYTE TRANSMISSION. ALSO DEPENDENT ON A SEND BYTE.

WRITE BYTE FORMAT

S	ADDRESS	$\overline{WR}$	ACK	COMMAND	ACK	DATA	ACK	P
	7 BITS	0		8 BITS		8 BITS		

SLAVE ADDRESS: EQUIVALENT TO CHIP-SELECT LINE OF A 3-WIRE INTERFACE

COMMAND BYTE: SELECTS REGISTER YOU ARE WRITING TO

DATA BYTE: DATA GOES INTO THE REGISTER SET BY THE COMMAND BYTE IF THE COMMAND IS BELOW 50h. IF THE COMMAND is 80h, 81h, or 82h, THE DATA BYTE PRESETS THE LSB OF AN EEPROM ADDRESS.

BLOCK WRITE FORMAT

S	ADDRESS	$\overline{WR}$	ACK	COMMAND	ACK	BYTE COUNT = N	ACK	DATA BYTE 1	ACK	DATA BYTE •••	ACK	DATA BYTE N	ACK	P
	7 BITS	0		8 BITS		8 BITS		8 BITS		8 BITS		8 BITS		

SLAVE ADDRESS: EQUIVALENT TO CHIP-SELECT LINE OF A 3-WIRE INTERFACE

COMMAND BYTE: PREPARES DEVICE FOR BLOCK OPERATION

DATA BYTE: DATA GOES INTO THE REGISTER SET BY THE COMMAND BYTE

BLOCK READ FORMAT

S	ADDRESS	$\overline{WR}$	ACK	COMMAND	ACK	SR	ADDRESS	WR	ACK	BYTE COUNT = 16	ACK	DATA BYTE 1	ACK	DATA BYTE •••	ACK	DATA BYTE N	ACK	P
	7 BITS	0		8 BITS			7 BITS	1		10h		8 BITS		8 BITS		8 BITS		

SLAVE ADDRESS: EQUIVALENT TO CHIP-SELECT LINE OF A 3-WIRE INTERFACE

COMMAND BYTE: PREPARES DEVICE FOR BLOCK OPERATION

SLAVE ADDRESS: EQUIVALENT TO CHIP-SELECT LINE OF A 3-WIRE INTERFACE

DATA BYTE: DATA GOES INTO THE REGISTER SET BY THE COMMAND BYTE

S = START CONDITON
P = STOP CONDITION
SHADED = SLAVE TRANSMISSION
SR = REPEATED START CONDTION

Figure 11. SMBus/I²C Protocols

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Note that once the read has been done, the internal pointer is increased by one, unless a memory boundary is hit. If the device is busy or if the address is not an allowed one, the command code is NACKed and the internal address pointer is not altered. The master must then interrupt the communication issuing a STOP condition.

Block Read

The block read protocol allows the master device to read a block of 16 bytes from the EEPROM or register bank (see Figure 11). Read fewer than 16 bytes of data by issuing an early STOP condition from the master, or by generating a NACK with the master. Previous actions through the serial interface predetermine the first source address. It is suggested to use a send byte protocol, before the block read, to set the initial read address. The block read protocol is initiated with a command code of C1h. The block read procedure follows:

1) The master sends a START condition.
2) The master sends the 7-bit slave address and a write bit (low).
3) The addressed slave asserts an ACK on SDA.
4) The master sends 8 bits of the block read command (C1h).
5) The slave asserts an ACK on SDA, unless busy.
6) The master generates a repeated START condition.
7) The master sends the 7-bit slave address and a read bit (high).
8) The slave asserts an ACK on SDA.
9) The slave sends the 8-bit byte count (16).
10) The master asserts an ACK on SDA.
11) The slave sends 8 bits of data.
12) The master asserts an ACK on SDA.
13) Repeat steps 8 and 9 15 times.
14) The master generates a STOP condition.

Address Pointers

Use the send byte protocol to set the register address pointers before read and write operations. For the configuration registers, valid address pointers range from 00h to 2Fh. Register addresses outside of this range result in a NACK being issued from the MAX6884/MAX6885. When using the block write protocol, the address pointer automatically increments after each data byte, except when the address pointer is already at 2Fh. If the address pointer is already 2Fh, and more data bytes are being sent, these subsequent bytes overwrite address 2Fh repeatedly, but no data will be left in 2Fh as this is a read-only address.

For the configuration EEPROM, valid address pointers range from 80h to 9Fh. When using the block write protocol, the address pointer automatically increments after each data byte, except when the address pointer is already at 9Fh. If the address pointer is already 9Fh, and more data bytes are being sent, these subsequent bytes overwrite address 9Fh repeatedly, leaving only the last data byte sent stored at this register address.

For the user EEPROM, valid address pointers range from 40h to 7Fh. As for the configuration EEPROM, block write and block read protocols can also be used. The internal address pointer will automatically increment up to the user EEPROM boundary 7Fh where the pointer moves to the first address of the configuration memory section 80h, as there is no forbidden address in the middle.

Applications Information

Configuration Download at Power-Up

The configuration of the MAX6884/MAX6885 (undervoltage/overvoltage thresholds, reset time delays, watchdog behavior, programmable output conditions and configurations, etc.) at power-up depends on the contents of the EEPROM. The EEPROM is comprised of buffered latches that store the configuration. The local volatile memory latches lose their contents at power-down. Therefore, at power-up, the device configuration must be restored by downloading the contents of the EEPROM (nonvolatile memory) to the local latches. This download occurs in a number of steps:

1) Programmable outputs are high impedance with no power applied to the device.
2) When V_{CC} or IN1–IN4 (see the *Powering the MAX6884/MAX6885* section) exceeds +1V, all programmable outputs are asserted low.
3) When V_{CC} or IN1–IN4 exceeds UVLO (2.5V), the configuration EEPROM starts to download its contents to the volatile configuration registers. The download takes 2.5ms (max). The programmable outputs assume their programmed conditional output state when V_{CC} or IN1–IN4 exceeds the UVLO (see the *Powering the MAX6884/MAX6885* section).
4) Any attempt to communicate with the device prior to this download completion results in a NACK being issued from the MAX6884/MAX6885.

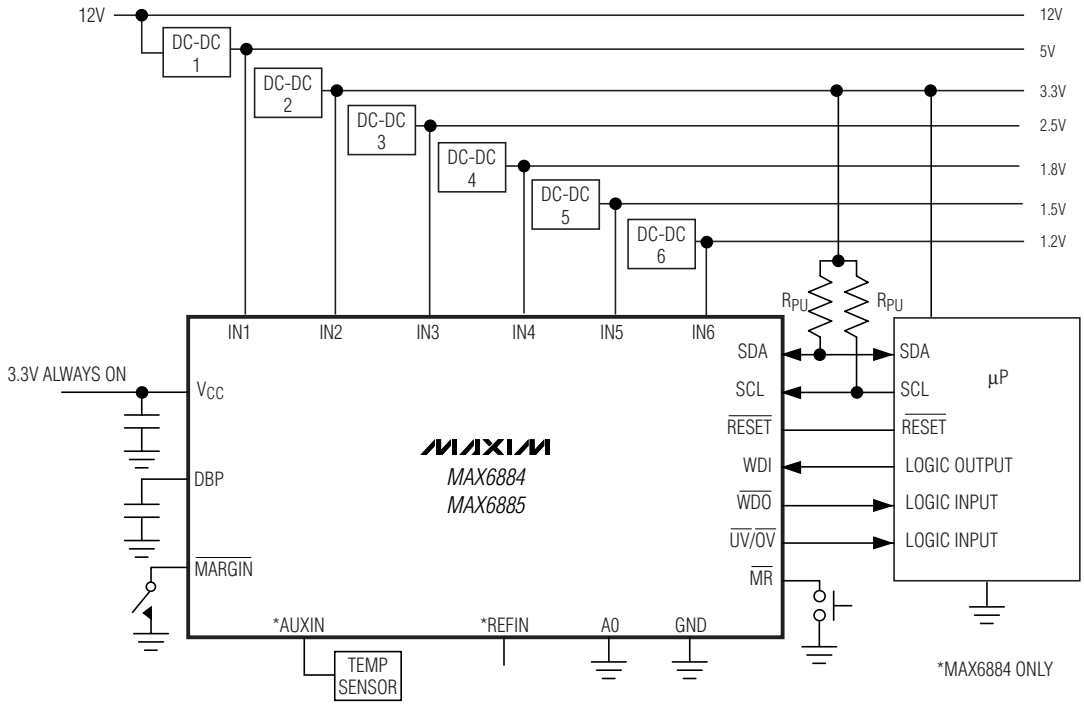
Layout and Bypassing

For better noise immunity, bypass each of the voltage-detector inputs to GND with a 0.1µF capacitor installed as close to the device as possible. Bypass V_{CC} and DBP to GND with 1µF capacitors installed as close to the device as possible. V_{CC} (when not externally supplied) and DBP are internally generated voltages and should not be used to supply power to external circuitry.

Configuration Latency Period

A delay of less than 5µs occurs between writing to the configuration registers and the time when these changes actually take place, except when changing one of the voltage-detector thresholds. Changing a voltage-detector threshold typically takes 150µs. When changing EEPROM contents, a software reboot or cycling of power is required for these changes to transfer to volatile memory.

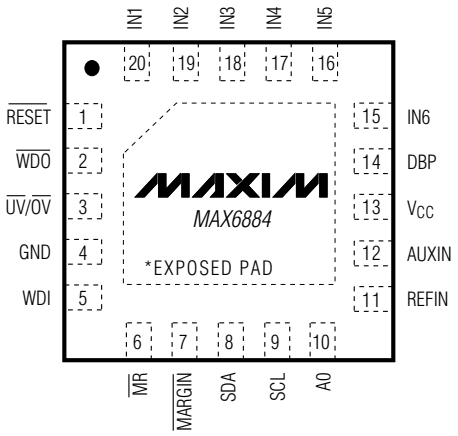
Typical Operating Circuit



EEPROM-Programmable, Hex Power-Supply Supervisory Circuits

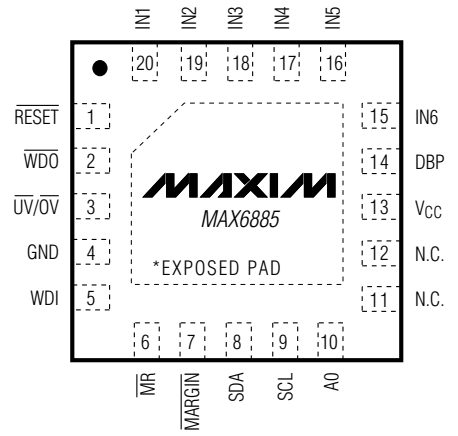
Pin Configurations

TOP VIEW



THIN QFN

*EXPOSED PAD CONNECTED TO GND.



THIN QFN

*EXPOSED PAD CONNECTED TO GND.

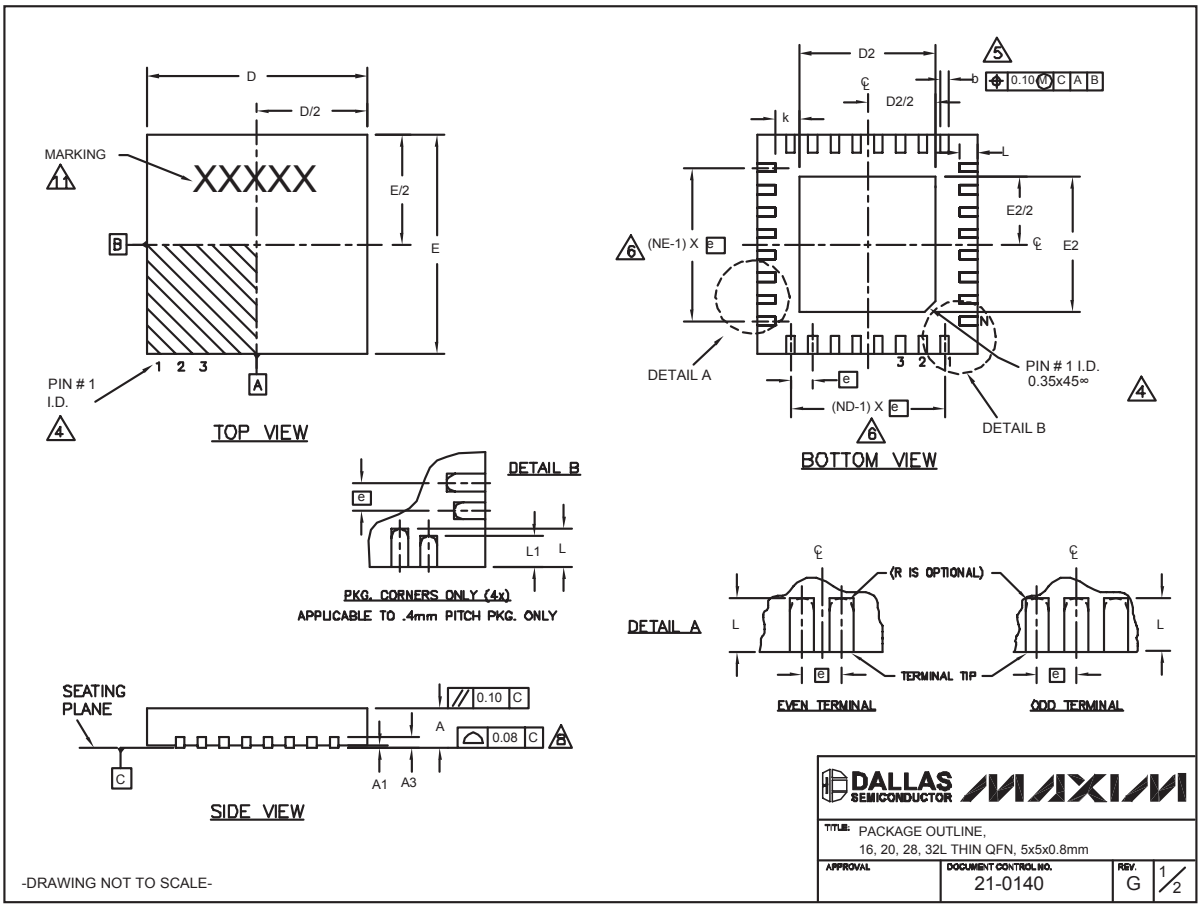
Chip Information

PROCESS: BiCMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

QFN THIN.EPS



EEPROM-Programmable, Hex Power-Supply Supervisory Circuits

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS												
PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A3	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50
L1	-	-	-	-	-	-	-	-	-	-	-	-
N	16			20			28			32		
ND	4			5			7			8		
NE	4			5			7			8		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2		

EXPOSED PAD VARIATIONS								
PKG. CODES	D2			E2			L	DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	±0.15	
T1655-1	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T1655N-1	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T2055-2	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35	0.40	Y
T2855-1	3.15	3.25	3.35	3.15	3.25	3.35	**	NO
T2855-2	2.60	2.70	2.80	2.60	2.70	2.80	**	NO
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35	**	YES
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80	**	YES
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80	**	NO
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35	**	NO
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80	**	YES
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35	0.40	Y
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35	**	N
T3255-2	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20	**	NO

**SEE COMMON DIMENSIONS TABLE

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-1, T2855-3 AND T2855-6.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 16, 20, 28, 32L THIN QFN, 5x5x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0140	G	2/2

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