GDDR6 SGRAM for Networking

MT61M256M32

2 Channels x 256 Meg x 16 I/O, 2 Channels x 512 Meg x 8 I/O

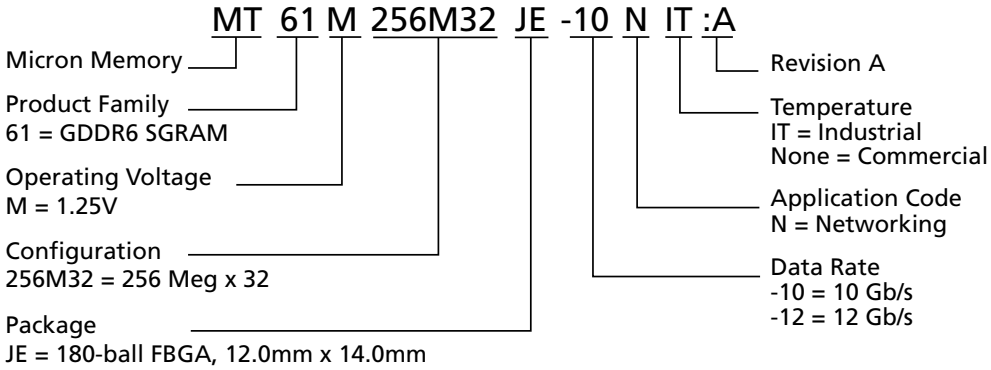
Features

- $V_{DD} = V_{DDQ} = 1.25V$ –3%/+6%
- $V_{PP} = 1.8V$ –3%/+6%
- Data rate: 10 Gb/s, 12 Gb/s
- 2 separate independent channels (x16)
- x16/x8 and 2-channel/pseudo channel (PC) mode configurations set at reset
- Single ended interfaces per channel for command/address (CA) and data
- Differential clock input CK_t/CK_c for CA per 2 channels
- One differential clock input WCK_t/WCK_c per channel for data (DQ, DBI_n, EDC)
- Double data rate (DDR) command/address (CK)
- Quad data rate (QDR) and double data rate (DDR) data (WCK), depending on operating frequency
- 16*n* prefetch architecture with 256 bits per array read or write access
- 16 internal banks
- 4 bank groups for $^{t}CCDL = 3^{t}CK$ and $4^{t}CK$
- Programmable READ latency
- Programmable WRITE latency
- Write data mask function via CA bus with single and double byte mask granularity
- Data bus inversion (DBI) and CA bus inversion (CABI)
- Input/output PLL
- CA bus training: CA input monitoring via DQ/DBI_n/EDC signals
- WCK2CK clock training with phase information via EDC signals
- Data read and write training via read FIFO (depth = 6)
- Read/write data transmission integrity secured by cyclic redundancy check
- Programmable CRC READ latency
- Programmable CRC WRITE latency
- Programmable EDC hold pattern for CDR
- RDQS mode on EDC pins
- Low power modes
- On-chip temperature sensor with read-out
- Auto precharge option for each burst access
- Auto refresh mode (32ms, 16k cycles) with per-bank and per-2-bank refresh options
- Temperature sensor controlled self refresh rate
- Digital ^{t}RAS lockout
- On-die termination (ODT) for all high-speed inputs
- Pseudo open drain (POD125) compatible outputs
- ODT and output driver strength auto calibration with external resistor ZQ pin (120Ω)
- Internal V_{REF} with DFE for data inputs, with input receiver characteristics programmable per pin
- Selectable external or internal V_{REF} for CA inputs; programmable V_{REF} offsets for internal V_{REF}
- Vendor ID for device identification
- IEEE 1149.1 compliant boundary scan
- 180-ball BGA package
- Lead-free (RoHS-compliant) and halogen-free packaging
- T_C = 0°C to +95°C (Commercial) and –40°C to +95°C (Industrial)

Options[1]	Marking
• Organization	
– 256 Meg × 32 (words × bits)	256M32
• FBGA package	
– 180-ball (12.0mm × 14.0mm)	JE
• Timing – maximum data rate	
– 10 Gb/s	-10
– 12 Gb/s	-12
• Application code	N
• Operating temperature	
– Commercial (0°C ≤ T_C ≤ +95°C)	None
– Industrial (–40°C ≤ T_C ≤ +95°C)	IT
• Revision	:A

Note: 1. Not all options listed can be combined to define an offered product. Use the part catalog search on http://www.micron.com for available offerings.

Figure 1: Part Numbering



FBGA Part Marking Decoder

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. For a quick conversion of an FBGA code, see the FBGA Part Marking Decoder on Micron's web site: http://www.micron.com.

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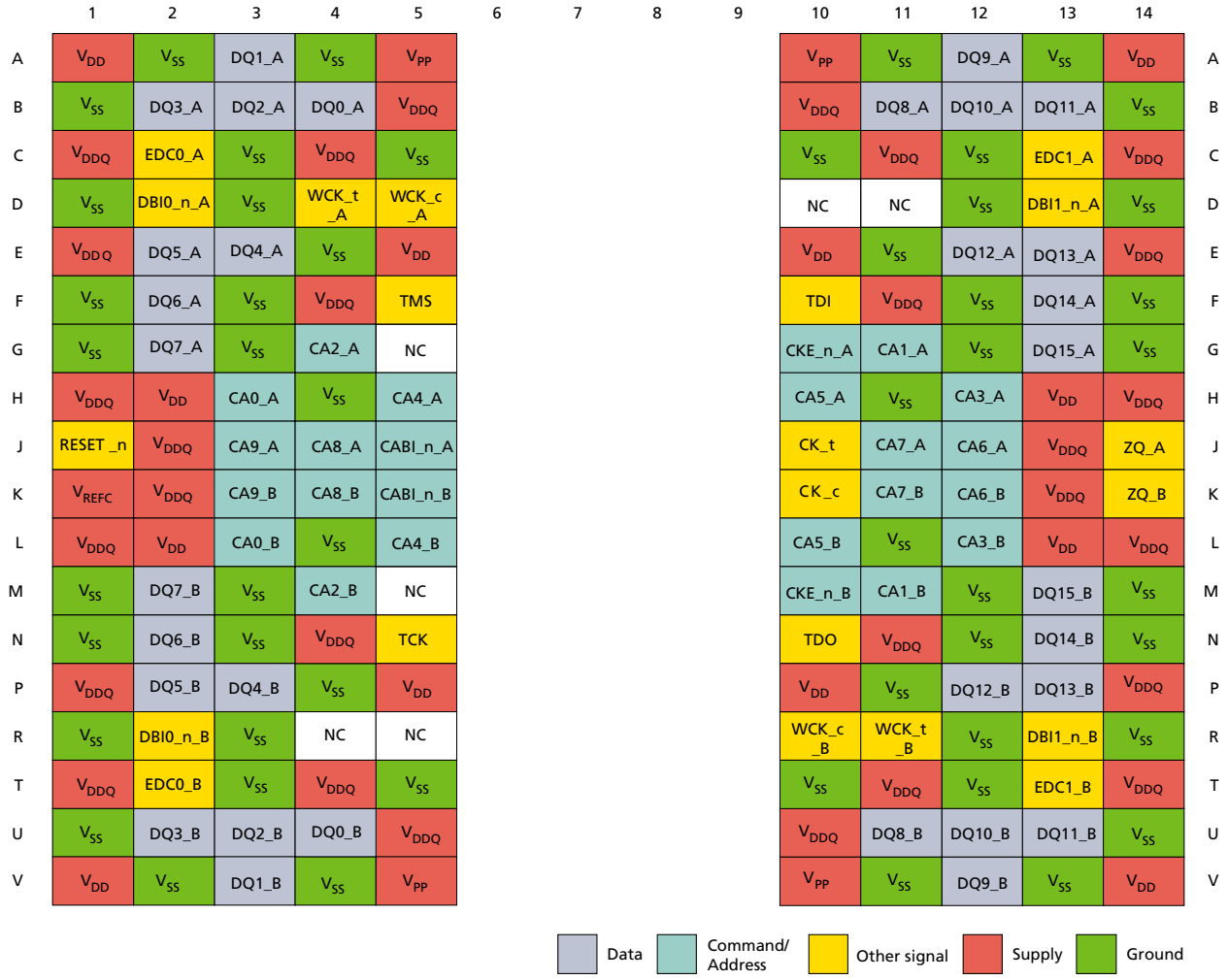
Ball Assignments and Descriptions

Figure 2: 180-Ball FBGA (Top View)



Note: 1. Channel A byte 1 and channel B byte 0 are disabled when the device is configured to x8 mode.

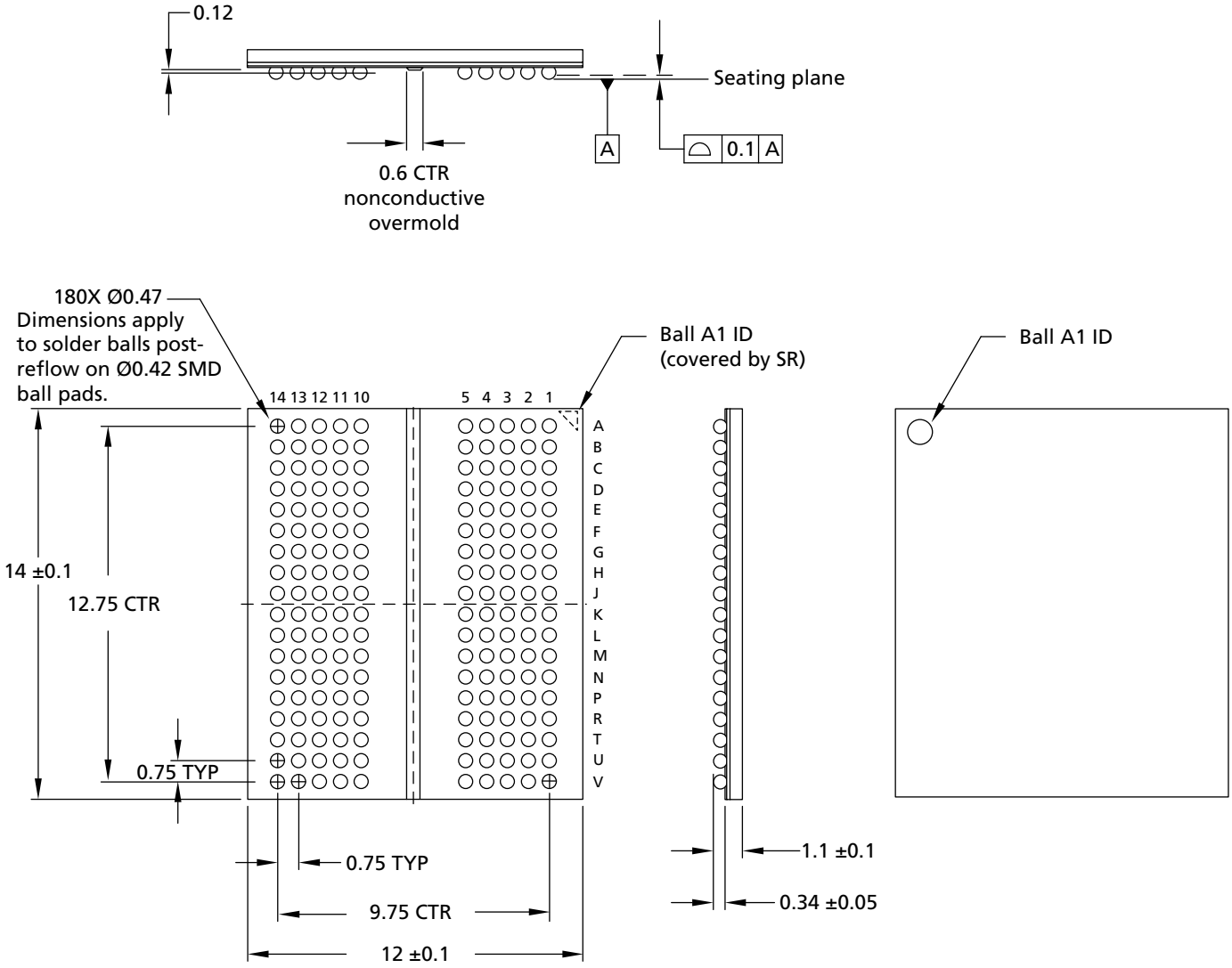
Table 1: 180-Ball FBGA Ball Descriptions

Symbol	Type	Description
CK_t, CK_c	Input	**Clock:** CK_t and CK_c are differential clock inputs. CK_t and CK_c do not have channel indicators as one clock is shared between both channel A and channel B on a device. Command address (CA) inputs are latched on the rising and falling edge of CK. All latencies are referenced to CK.
WCK_t, WCK_c	Input	**Write clock:** WCK_t and WCK_c are differential clocks used for write data capture and read data output. WCK_t/WCK_c are associated with DQ[15:0], DBI[1:0]_n, and EDC[1:0].
CKE_n	Input	**Clock enable:** CKE_n LOW activates and CKE_n HIGH deactivates the internal clock, device input buffers, and output drivers excluding RESET_n, TDI, TDO, TMS, and TCK. Taking CKE_n HIGH provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any bank). CKE_n must be maintained LOW throughout read and write accesses.
CA[9:0]	Input	**Command address (CA):** The CA inputs receive packetized DDR command, address or other information, for example, the op-code for the MRS command. See Command Truth Table for details.
CABI_n	Input	**Command address bus inversion**
DQ[15:0]	I/O	**Data input/output:** Bidirectional 16-bit data bus.
DBI[1:0]_n	I/O	**Data bus inversion:** DBI0_n is associated with DQ[7:0], DBI1_n is associated with DQ[15:8].
EDC[1:0]	Output	**Error detection code:** The calculated CRC data is transmitted on these signals. In addition these signals drive a "hold" pattern when idle. EDC0 is associated with DQ[7:0], EDC1 is associated with DQ[15:8].
V_{DDQ}	Supply	**I/O power supply:** Isolated on the die for improved noise immunity.
V_{DD}	Supply	**Power supply**
V_{SS}	Supply	**Ground**
V_{PP}	Supply	**Pump voltage**
V_{REFC}	Supply	**Reference voltage for CA, CABI_n, and CKE_n signals**
ZQ	Reference	**External reference for auto calibration**
TDI	Input	**JTAG test data input**
TDO	Output	**JTAG test data output**
TMS	Input	**JTAG test mode select**
TCK	Input	**JTAG test clock**
RESET_n	Input	**Reset:** RESET_n low asynchronously initiates a full chip reset. With RESET_n LOW all ODTs are disabled. A full chip reset may be performed at any time by pulling RESET_n LOW.
NC	–	**No connect**

Note: 1. Index "_A" or "_B" represents the channel indicator "A" and "B" of the device. Signal names including the channel indicator are used whenever more than one channel is referenced, for example, with the ball assignment. The channel indicator is omitted whenever features and functions common to both channels are described.

Package Dimensions

Figure 3: 180-Ball FBGA (JE)



Notes:
1. Package dimension specification is compliant to JC11 MO328 variation PBGA-B180[252]_I0p75-R12p0x14p0Z#-C0p525Z0p22.
2. All dimensions are in millimeters.
3. Solder ball material: SAC-Q (92.5% Sn, 4% Ag, 3% Bi, 0.5% Cu).

Functional Description

The GDDR6 SGRAM is a high-speed dynamic random-access memory designed for applications requiring high bandwidth. It is internally configured as 16-bank memory and contains 8,589,934,592 bits.

The GDDR6 SGRAM's high-speed interface is optimized for point-to-point connections to a host controller. On-die termination (ODT) is provided for all high-speed interface signals to eliminate the need for termination resistors in the system.

GDDR6 uses a 16*n*-prefetch architecture and a DDR or QDR interface to achieve high-speed operation. The device's architecture consists of two 16-bit-wide fully independent channels.

Read and write accesses to GDDR6 are burst oriented; accesses start at a selected location and consist of a total of 16 data words. Accesses begin with the registration of an ACTIVATE command, which is then followed by a READ, WRITE (WOM), or masked WRITE (WDM, WSM) command. The row and bank address to be accessed is registered coincident with the ACTIVATE command. The address bits registered coincident with the READ, WRITE, or masked WRITE command are used to select the bank and the starting column location for the burst access.

Clocking

GDDR6 operates from a differential clock CK_t and CK_c. CK is common to both channels. Command and address (CA) are registered at every rising and falling CK edge. There are both single-cycle and multi-cycle commands. See Command Truth Table for details.

GDDR6 uses a free running differential forwarded clock (WCK_t/WCK_c) with both input and output data registered and driven respectively at both edges of the forwarded WCK.

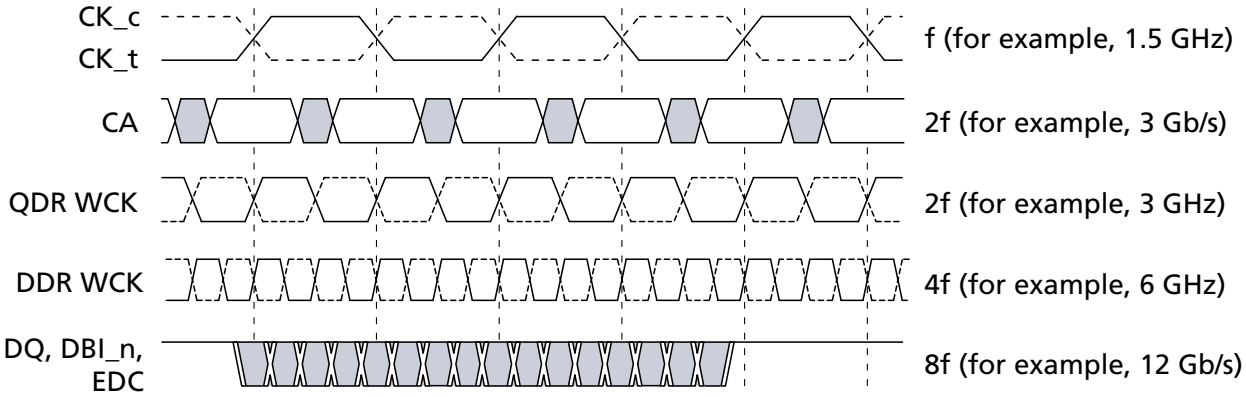
GDDR6 supports DDR and QDR operating modes for WCK frequency which differ in the DQ/DBI_n pin to WCK clock frequency ratio. The figure below illustrates the difference between both modes.

This GDDR6 SGRAM device is designed with a WCK/word granularity which is equivalent to one WCK per channel. The DRAM info bits for WCK granularity, WCK frequency, and internal WCK can be read by the host during the initialization process to determine the WCK architecture for the device.

Table 2: Example Clock and Interface Signal Frequency Relationship

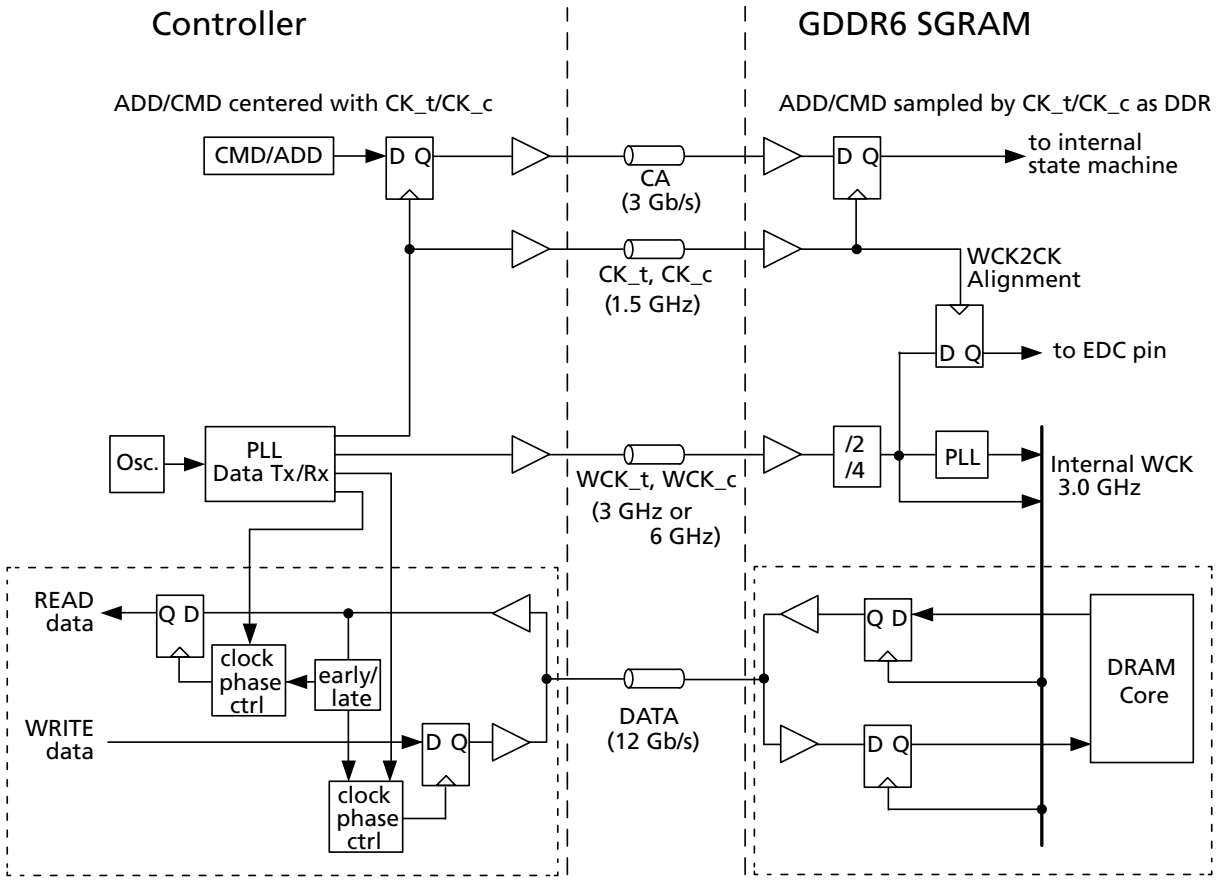
Pin	DDR WCK	QDR WCK	Unit
CK_t, CK_c	1.5	1.5	GHz
CA	3.0	3.0	Gb/s/pin
WCK_t, WCK_c	6.0	3.0	GHz
DQ, DBI_n	12.0	12.0	Gb/s/pin
EDC	6.0	6.0	Gb/s/pin

Figure 4: Clocking and Interface Relationship



Note: 1. The figure shows the relationship between the data rate of the buses and the clocks; it is not a timing diagram.

Figure 5: Block Diagram of an Example Clock System



Addressing

GDDR6 addressing is defined for a single channel with devices having two channels per device.

Table 3: Addressing

Parameter	8Gb Density	
	x16 Mode	x8 Mode
Number of channels	2	
Memory density (per channel)	4Gb	
Memory prefetch (per channel)	256b	128b
Bank address (per channel)	BA[3:0]	
Row address (per channel)	R[13:0]	
Column address (per channel)	C[5:0]	C[6:0]
Page size (per channel)	2KB	
Refresh	16k/32ms	

Notes:
1. The column address notation for GDDR6 does not include the lower four address bits as the burst order is always fixed for READ and WRITE.
2. Page size = 2^COLBITS × (Prefetch_Size/8) where COLBITS is the number of column address bits.

Operations

Command Truth Table

GDDR6 uses a packetized DDR command/address bus that encodes all commands and addresses on a 10-bit CA bus as outlined in the table below.

Figure 6: Command Truth Table

Operation	Symbol	CK Edge	CKE_n		CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0	Notes
			n - 1	n											
NO OPERATION	NOP (1)	R	L	L	H	H	V	V	V	V	V	V	V	V	1, 10
		F			H	H	V	V	V	V	V	V	V	V	
	NOP (2)	R	L	L	H	H	V	V	V	V	V	V	V	V	
		F			H	L	V	V	V	V	V	V	V	V	
	NOP (3)	R	L	L	H	L	V	V	V	V	V	V	V	V	
		F			H	H	V	V	V	V	V	V	V	V	
MODE REGISTER SET	MRS	R	L	L	H	L	M3	M2	M1	M0	OP3	OP2	OP1	OP0	1, 2, 3, 11
		F			H	L	OP11	OP10	OP9	OP8	OP7	OP6	OP5	OP4	
ACTIVATE	ACT	R	L	L	L	V	BA3	BA2	BA1	BA0	R3	R2	R1	R0	1, 2, 4
		F			R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	
READ	RD	R	L	L	H	H	BA3	BA2	BA1	BA0	C3	C2	C1	C0	1, 2, 5, 6
		F			L	H	L	L	V	L	CE	C6	C5	C4	
READ with AUTO PRECHARGE	RDA	R	L	L	H	H	BA3	BA2	BA1	BA0	C3	C2	C1	C0	1, 2, 5, 6
		F			L	H	L	L	V	H	CE	C6	C5	C4	
LOAD FIFO	LDFF	R	L	L	H	H	B3	B2	B1	B0	D3	D2	D1	D0	1, 2, 8
		F			L	H	H	L	D9	D8	D7	D6	D5	D4	
READ TRAINING	RDTR	R	L	L	H	H	V	V	V	V	V	V	V	V	1, 2, 6
		F			L	H	H	H	V	L	CE	V	V	V	
WRITE	WOM	R	L	L	H	H	BA3	BA2	BA1	BA0	C3	C2	C1	C0	1, 2, 5, 6
		F			L	L	L	L	V	L	CE	C6	C5	C4	
WRITE with AUTO PRECHARGE	WOMA	R	L	L	H	H	BA3	BA2	BA1	BA0	C3	C2	C1	C0	1, 2, 5, 6
		F			L	L	L	L	V	H	CE	C6	C5	C4	
WRITE SINGLE BYTE MASK	WSM	R	L	L	H	H	BA3	BA2	BA1	BA0	C3	C2	C1	C0	1, 2, 5, 6
		F			L	L	L	H	V	L	CE	C6	C5	C4	
		R			H	H	Byte 0 BST7	Byte 0 BST6	Byte 0 BST5	Byte 0 BST4	Byte 0 BST3	Byte 0 BST2	Byte 0 BST1	Byte 0 BST0	
		F			H	H	Byte 0 BST15	Byte 0 BST14	Byte 0 BST13	Byte 0 BST12	Byte 0 BST11	Byte 0 BST10	Byte 0 BST9	Byte 0 BST8	
		R			H	H	Byte 1 BST7	Byte 1 BST6	Byte 1 BST5	Byte 1 BST4	Byte 1 BST3	Byte 1 BST2	Byte 1 BST1	Byte 1 BST0	
		F			H	H	Byte 1 BST15	Byte 1 BST14	Byte 1 BST13	Byte 1 BST12	Byte 1 BST11	Byte 1 BST10	Byte 1 BST9	Byte 1 BST8	

Figure 7: Command Truth Table (Continued)

Operation	Symbol	CK Edge	CKE_n		CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0	Notes
			n - 1	n											
WRITE SINGLE BYTE MASK with AUTO PRECHARGE	WSMA	R	L	L	H	H	BA3	BA2	BA1	BA0	C3	C2	C1	C0	1, 2, 5, 6
		F			L	L	L	H	V	H	CE	C6	C5	C4	
		R			H	H	Byte 0 BST7	Byte 0 BST6	Byte 0 BST5	Byte 0 BST4	Byte 0 BST3	Byte 0 BST2	Byte 0 BST1	Byte 0 BST0	
		F			H	H	Byte 0 BST15	Byte 0 BST14	Byte 0 BST13	Byte 0 BST12	Byte 0 BST11	Byte 0 BST10	Byte 0 BST9	Byte 0 BST8	
		R			H	H	Byte 1 BST7	Byte 1 BST6	Byte 1 BST5	Byte 1 BST4	Byte 1 BST3	Byte 1 BST2	Byte 1 BST1	Byte 1 BST0	
		F			H	H	Byte 1 BST15	Byte 1 BST14	Byte 1 BST13	Byte 1 BST12	Byte 1 BST11	Byte 1 BST10	Byte 1 BST9	Byte 1 BST8	
WRITE DOUBLE BYTE MASK	WDM	R	L	L	H	H	BA3	BA2	BA1	BA0	C3	C2	C1	C0	1, 2, 5, 6
		F			L	L	H	L	V	L	CE	C6	C5	C4	
		R			H	H	BST7	BST6	BST5	BST4	BST3	BST2	BST1	BST0	
		F			H	H	BST15	BST14	BST13	BST12	BST11	BST10	BST9	BST8	
WRITE DOUBLE BYTE MASK with AUTO PRECHARGE	WDMA	R	L	L	H	H	BA3	BA2	BA1	BA0	C3	C2	C1	C0	1, 2, 5, 6
		F			L	L	H	L	V	H	CE	C6	C5	C4	
		R			H	H	BST7	BST6	BST5	BST4	BST3	BST2	BST1	BST0	
		F			H	H	BST15	BST14	BST13	BST12	BST11	BST10	BST9	BST8	
WRITE TRAINING	WRTR	R	L	L	H	H	V	V	V	V	V	V	V	V	1, 2, 6
		F			L	L	H	H	V	L	CE	V	V	V	
PRECHARGE	PREpb	R	L	L	H	L	BA3	BA2	BA1	BA0	V	V	V	V	1, 2, 9
		F			L	L	V	V	V	L	V	V	V	V	
PRECHARGE ALL	PREab	R	L	L	H	L	V	V	V	V	V	V	V	V	1, 2
		F			L	L	V	V	V	H	V	V	V	V	
PER-BANK REFRESH	REFpb/ REFp2b	R	L	L	H	L	BA3	BA2	BA1	BA0	V	V	V	V	1, 2, 7, 9
		F			L	H	V	V	V	L	V	V	V	V	
REFRESH	REFab	R	L	L	H	L	V	V	V	V	V	V	V	V	1, 2, 7
		F			L	H	V	V	V	H	V	V	V	V	
POWER-DOWN ENTRY	PDE	R	L	H	H	H	V	V	V	V	V	V	V	V	1, 2
		F			H	H	V	V	V	V	V	V	V	V	
POWER-DOWN EXIT	PDX	R	H	L	H	H	V	V	V	V	V	V	V	V	1, 2
		F			H	H	V	V	V	V	V	V	V	V	
SELF REFRESH ENTRY	SRE	R	L	H	H	L	V	V	V	V	V	V	V	V	1, 2, 7
		F			L	H	V	V	V	V	V	V	V	V	
SELF REFRESH EXIT	SRX	R	H	L	H	H	V	V	V	V	V	V	V	V	1, 2
		F			H	H	V	V	V	V	V	V	V	V	
COMMAND/ADDRESS TRAINING CAPTURE	CAT	R	L	H	V	V	V	V	V	V	V	V	V	V	1, 2
		F			V	V	V	V	V	V	V	V	V	V	

Notes: 1. H = Logic HIGH level; L = Logic LOW level; V = Valid signal (H or L, but not floating). R, F = Rising, Falling CK clock edge.

2. Values shown for CA[9:0] are logical values; the physical values are inverted when command/address bus inversion (CABI) is enabled and CABI_n = L.
3. M[3:0] provide the mode register address (MRA), OP[11:0] the opcode to be loaded.
4. BA[3:0] provide the bank address, R[13:0] provide the row address.
5. BA[3:0] provide the bank address, C[6:0] provide the column address; no sub-word addressing within a burst of 16. BST[15:0] provide the write data mask for each burst position with WDM(A) and WSM(A) commands.
6. CE (channel enable) is intended for PC mode. The command is active when CE = H. When CE = L the data access is suppressed.
7. The command is REFRESH or PER-BANK REFRESH/PER-2-BANK REFRESH when CKE_n(n) = L and SELF REFRESH ENTRY when CKE_n(n) = H.
8. B[3:0] select the burst position, and D[9:0] provide the data.
9. BA[3:0] provide the bank address.
10. All three encodings perform the same NOP. NOP (2) and NOP (3) encodings are only allowed during CA Training.
11. MRS command to MR15 with M[3:0] = 1111, CKE_n(n-1) = H, and CKE_n(n) = H is allowed during the change to the mapping while in CA training mode or the exit of CA training mode. See CA training for more details.

Clamshell (x8) Mode Enable

A GDDR6 SGRAM-based memory system is typically divided into several channels. GDDR6 has been optimized for a 16-bit-wide channel. A channel can be comprised of a single device operated in x16 mode, or two devices each operated in x8 mode. For x8 mode the devices are typically assembled on opposite sides of the PCB in what is referred as a clamshell layout.

Whether in x16 mode or x8 mode the device will operate with a point-to-point connection on the high-speed data signals. The disabled signals in x8 mode should all be in a High-Z state, non-terminating.

The x8 mode is detected at power-up on EDC1_A and EDC0_B. For x8 mode these signals are tied to V_{SS}; they are part of the bytes that are disabled in this mode and therefore not needed for EDC functionality. For x16 mode these signals are active and always terminated to V_{DDQ} in the system or by the controller.

The configuration is set with RESET_n going HIGH. Once the configuration has been set, it cannot be changed during normal operation. Typically, the configuration is fixed in the system. Details of the x8 mode detection are depicted in Figure 8. A comparison of x16 mode and x8 mode systems is shown in Figure 9.

Table 4: Clamshell (x8) Mode Enable

Mode	EDC0_A	EDC1_A	EDC0_B	EDC1_B
x8	V_{DDQ}	V_{SS} (on board)	V_{SS} (on board)	V_{DDQ}
x16	V_{DDQ} (terminated by the system or controller)			

Figure 8: Enabling Clamshell (x8) Mode

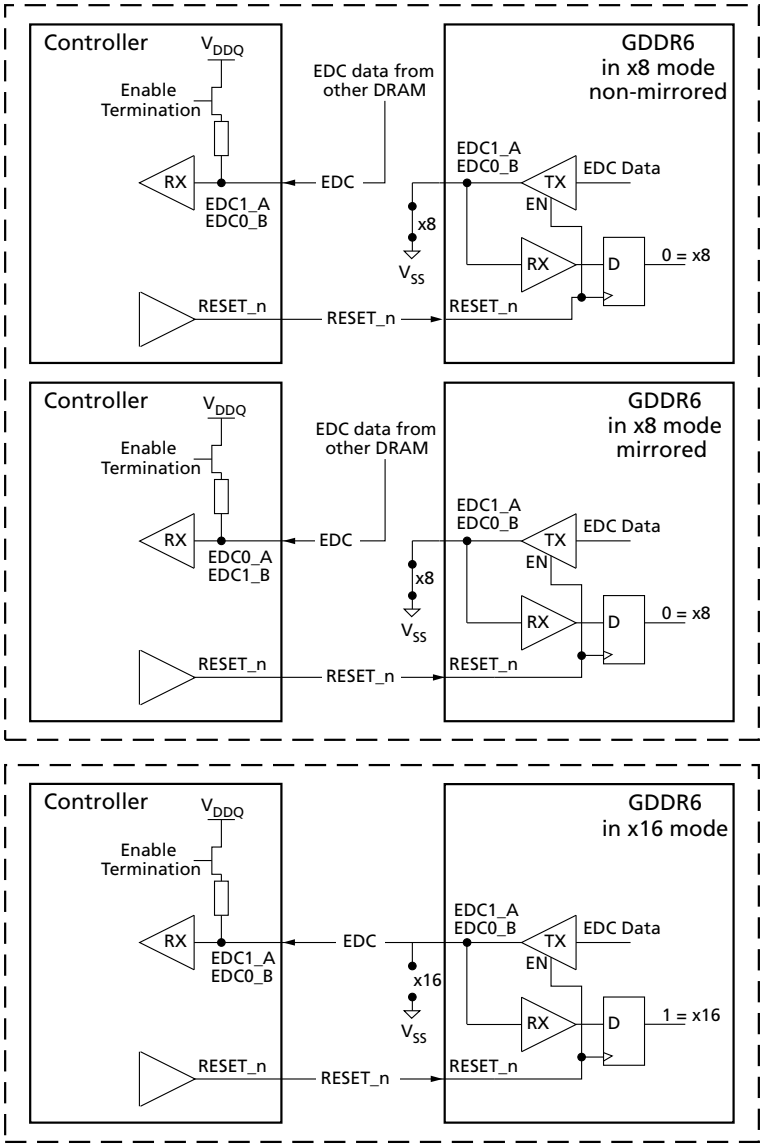


Figure 9: System View for x16 and x8 Modes

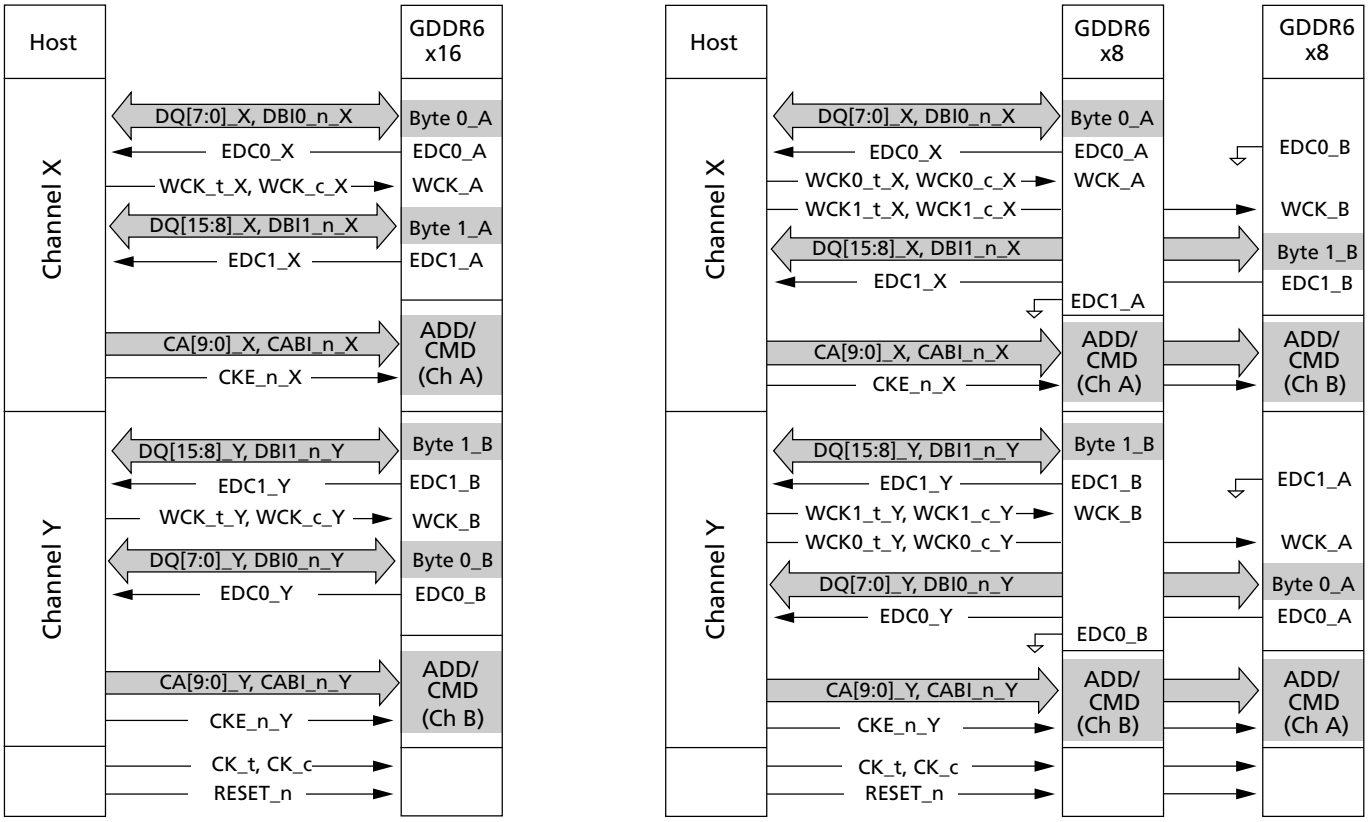
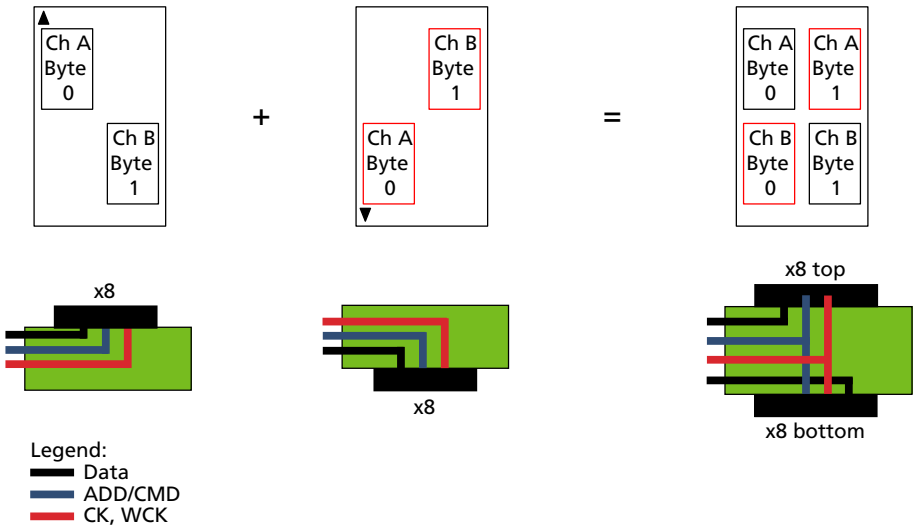


Figure 10 clarifies the use of x8 mode and how the bytes are enabled/disabled to give the controller the view of the same bytes that a controller sees with a single x16 device. For a 16-bit channel using two devices in a clamshell design, byte 0 comes from channel A from the top device and byte 1 comes from channel B from the bottom device and will look equivalent at the controller to a x16 mode.

Figure 10: Byte Orientation in Clamshell Topology

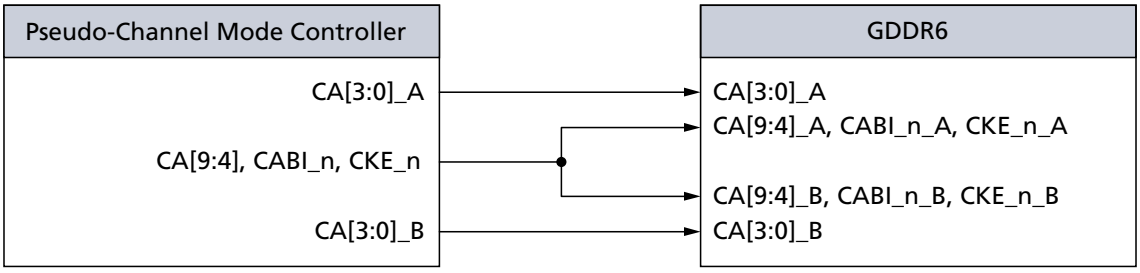


Pseudo-Channel Mode

GDDR6 has been optimized for a 32B access across a 16-bit channel by providing a unique CA bus to each 16-bit-wide channel. For applications requiring fewer CA pins, GDDR6 includes support for a pseudo-channel (PC) mode where CA[9:4], CKE_n, and CABI_n on each channel are connected to a common bus, while CA[3:0] of each channel are connected to a separate bus. The command truth table is organized such that in PC mode the same command is decoded in both pseudo-channels, but READ and WRITE commands support a unique column address to each pseudo-channel. In PC mode, CKE_n and CABI_n are also shared across pseudo-channels.

In PC mode, the only difference in the DRAM is that termination on CA[9:4], CKE_n, and CABI_n can be configured differently from CA[3:0]. PC mode can be selected during initialization by driving CA6 = LOW on both channels when RESET_n is driven HIGH.

Figure 11: CA Pins in Pseudo-Channel Mode



Operating Conditions

Absolute Maximum Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 5: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
V_{DD}	Voltage on V_{DD} pin relative to V_{SS}	–0.3	2.0	V	1
V_{DDQ}	Voltage on V_{DDQ} pin relative to V_{SS}	–0.3	2.0	V	1
V_{PP}	Voltage on V_{PP} pin relative to V_{SS}	–0.3	2.3	V	2
V_{IN}/V_{OUT}	Voltage on any pins relative to V_{SS}	–0.3	2.0	V	
T_{STG}	Storage temperature	–55	+125	°C	3

Notes:
1. V_{DD} and V_{DDQ} must be within 300mV of each other at all times the device is powered-up.
2. V_{PP} must be equal or greater than V_{DD} and V_{DDQ} at all times the device is powered-up.
3. Storage temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, refer to the JESD51-2 standard.

DC and AC Operating Conditions

The interface of GDDR6 with 1.25V V_{DDQ} will follow POD125 Standard (JESD8-30), Class A. All AC and DC values are referenced to the ball.

Table 6: DC Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V_{DD}	Device supply voltage	1.2125	1.25	1.3250	V	1, 2
V_{DDQ}	Output supply voltage	1.2125	1.25	1.3250	V	1, 2
V_{PP}	Pump voltage	1.746	1.8	1.908	V	2
V_{REFD}	Reference voltage for DQ and DBI_n	–	0.7 × V_{DDQ} or 0.725 × V_{DDQ}	–	V	3, 4
V_{REFD2}		–	0.5 × V_{DDQ}	–	V	3, 4, 5
V_{REFC}	Reference voltage for CA	0.69 × V_{DDQ}	–	0.71 × V_{DDQ}	V	3, 6
V_{REFC2}		0.49 × V_{DDQ}	–	0.51 × V_{DDQ}	V	3, 6, 7
$V_{IHA(DC)}$	DC input logic HIGH voltage with V_{REFC} for CA	V_{REFC} + 0.125	–	–	V	
$V_{ILA(DC)}$	DC input logic LOW voltage with V_{REFC} for CA	–	–	V_{REFC} - 0.125	V	
$V_{IHA2(DC)}$	DC input logic HIGH voltage with V_{REFC2} for CA	V_{REFC2} + 0.25	–	–	V	
$V_{ILA2(DC)}$	DC input logic LOW voltage with V_{REFC2} for CA	–	–	V_{REFC2} - 0.25	V	
$V_{IHD(DC)}$	DC input logic HIGH voltage with V_{REFD} for DQ and DBI_n	V_{REFD} + 0.085	–	–	V	
$V_{ILD(DC)}$	DC input logic LOW voltage with V_{REFD} for DQ and DBI_n	–	–	V_{REFD} - 0.085	V	
$V_{IHD2(DC)}$	DC input logic HIGH voltage with V_{REFD2} for DQ and DBI_n	V_{REFD2} + 0.25	–	–	V	
$V_{ILD2(DC)}$	DC input logic LOW voltage with V_{REFD2} for DQ and DBI_n	–	–	V_{REFD2} - 0.25	V	
V_{IHR}	RESET_n and boundary scan input logic HIGH voltage; EDC and CA input logic HIGH voltage for x16/x8 mode, PC vs. 2-channel mode, CK and CA ODT select at reset	0.8 × V_{DDQ}	–	–	V	8
V_{ILR}	RESET_n and boundary scan input logic LOW voltage; EDC and CA input logic LOW voltage for x16/x8 mode, PC vs. 2-channel mode, CK and CA ODT select at reset	–	–	0.2 × V_{DDQ}	V	8
V_{IN}	Single ended clock input voltage level: CK_t, CK_c, WCK_t, WCK_c	–0.30	–	V_{DDQ} + 0.30	V	9
$V_{MP(DC)}$	CK_t, CK_c clock input midpoint voltage	V_{REFC} - 0.1	–	V_{REFC} + 0.1	V	10, 13
$V_{IDCK(DC)}$	CK_t, CK_c clock input differential voltage	0.18	–	–	V	11, 13
$V_{IDWCK(DC)}$	WCK_t, WCK_c clock input differential voltage	0.165	–	–	V	12, 14
I_L	Input leakage current (any input 0V ≤ V_{IN} ≤ V_{DDQ}; all other signals not under test = 0V)	–5	–	5	µA	
I_{OZ}	Output leakage current (outputs are disabled; 0V ≤ V_{OUT} ≤ V_{DDQ})	–5	–	5	µA	

Table 6: DC Operating Conditions (Continued)

Symbol	Parameter	Min	Typ	Max	Unit	Notes
$V_{OL(DC)}$	Output logic low voltage	–	–	0.52	V	
ZQ	External resistor value	115	120	125	Ω	

Notes:
1. GDDR6 SGRAM devices are designed to tolerate PCB designs with separate V_{DD} and V_{DDQ} power regulators.
2. DC bandwidth is limited to 20 MHz.
3. AC noise in the system is estimated at 50mV peak-to-peak for the purpose of DRAM design.
4. The reference voltage for DQ and DBI_n pins is generated internally, and its values are determined by the half V_{REFD} and V_{REFD} level mode register bits. The typical V_{REFD} level depends on the selected data termination value (48 ohm or 60 ohm); See Mode Register 6 (MR6) for details.
5. Programmable V_{REFD} levels are not supported with V_{REFD2}.
6. The reference voltage source (external or internal) is determined at power-up; the reference voltage level is determined by half V_{REFC} and the V_{REFC} offset mode register bit.
7. Programmable V_{REFC} offsets are not supported with V_{REFC2}.
8. V_{IHR} and V_{ILR} apply to boundary scan input pins TDI, TMS, and TCK. V_{IHR} and V_{ILR} apply to EDC and CA inputs at reset when latching default device configurations. V_{IHR} and V_{ILR} also apply to CA, CABI_n, CKE_n, CK, DQ, DBI_n, EDC, and WCK inputs when boundary scan mode is active and input data are latched in the capture-DR TAP controller state.
9. Use V_{IHR} and V_{ILR} when boundary scan mode is active and input data are latched in the capture-DR TAP controller state.
10. This provides a minimum of 0.775V to a maximum of 0.975V with POD125, and is normally 70% of V_{DDQ}. DRAM timings relative to CK cannot be guaranteed if these limits are exceeded.
11. V_{IDCK} is the magnitude of the difference between the input level in CK_t and the input level on CK_c. The input reference level for signals other than CK_t and CK_c is V_{REFC}.
12. V_{IDWCK} is the magnitude of the difference between the input level on WCK_t and the input level on WCK_c. The input reference level for signals other than WCK_t and WCK_c is either V_{REFC}, V_{REFC2}, V_{REFD}, or V_{REFD2}.
13. The CK_t and CK_c input reference level (for timing referenced to CK_t and CK_c) is the point at which CK_t and CK_c cross. Refer to the applicable timings in the AC Timings table.
14. The WCK_t and WCK_c input reference level (for timing referenced to WCK_t and WCK_c) is the point at which WCK_t and WCK_c cross. Refer to the applicable timings in the AC Timings table.

Table 7: AC Operating Conditions (For Design Only[9])

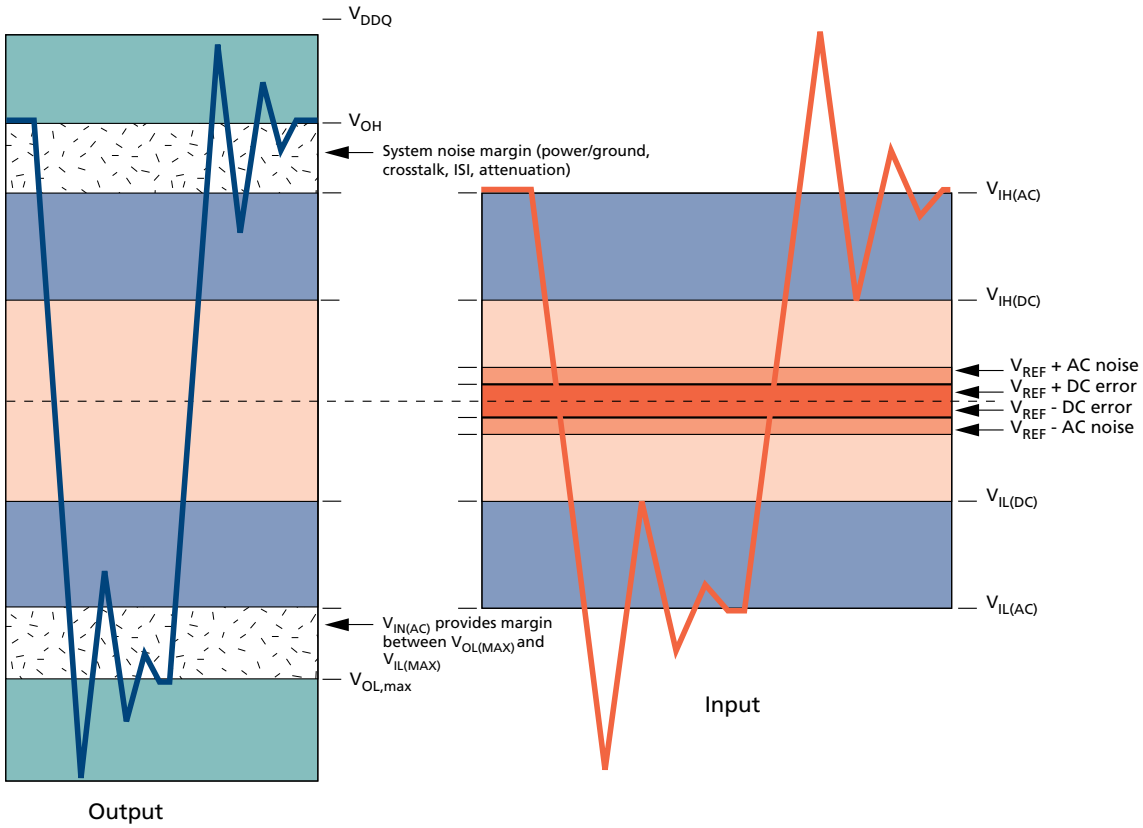
Symbol	Parameter	Min	Typ	Max	Unit	Notes
$V_{IHA(AC)}$	AC input logic HIGH voltage with V_{REFC} for CA	V_{REFC} + 0.165	–	–	V	
$V_{ILA(AC)}$	AC input logic LOW voltage with V_{REFC} for CA	–	–	V_{REFC} - 0.165	V	
$V_{IHA2(AC)}$	AC input logic HIGH voltage with V_{REFC2} for CA	V_{REFC} + 0.333	–	–	V	
$V_{ILA2(AC)}$	AC input logic LOW voltage with V_{REFC2} for CA	–	–	V_{REFC} - 0.333	V	
$V_{IHD(AC)}$	AC input logic HIGH voltage with V_{REFD} for DQ, DBI_n	V_{REFD} + 0.125	–	–	V	

Table 7: AC Operating Conditions (For Design Only[9]) (Continued)

Symbol	Parameter	Min	Typ	Max	Unit	Notes
$V_{ILD(AC)}$	AC input logic LOW voltage with V_{REFD} for DQ, DBI_n	–	–	V_{REFD} - 0.125	V	
$V_{IHD2(AC)}$	AC input logic HIGH voltage with V_{REFD2} for DQ, DBI_n	V_{REFD2} + 0.333	–	–	V	
$V_{ILD2(AC)}$	AC input logic LOW voltage with V_{REFD2} for DQ, DBI_n	–	–	V_{REFD2} - 0.333	V	
$V_{IDCK(AC)}$	CK_t, CK_c clock differential voltage	0.333	–	–	V	1, 3, 5
$V_{IDWCK(AC)}$	WCK_t, WCK_c clock input differential voltage	0.25	–	–	V	1, 4, 6
$V_{IXCK(AC)}$	CK_t, CK_c clock input crossing point voltage	V_{REFC} - 0.10	–	V_{REFC} + 0.10	V	1, 2, 5
$V_{IXWCK(AC)}$	WCK_t, WCK_c clock input crossing point voltage	V_{REFC} - 0.09	–	V_{REFC} + 0.09	V	1, 2, 6, 7

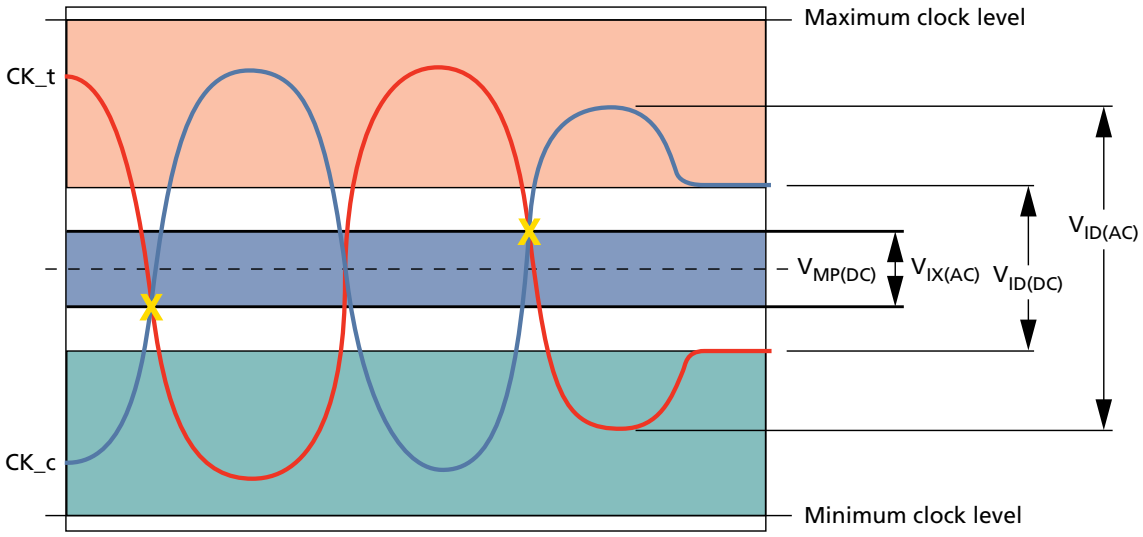
Notes:
1. For AC operations, all DC clock requirements must be satisfied as well.
2. The value of V_{IXCK} and V_{IXWCK} is expected to equal 70% V_{DDQ} for the transmitting device and must track variations in the DC level of the same.
3. V_{IDCK} is the magnitude of the difference between the input level on CK_t and the input level on CK_c. The input reference level for signals other than CK_t and CK_c is V_{REFC}.
4. V_{IDWCK} is the magnitude of the difference between the input level on WCK_t and the input level on WCK_c. The input reference level for signals other than WCK_t and WCK_c is either V_{REFC}, V_{REFC2}, V_{REFD}, or V_{REFD2}.
5. The CK_t and CK_c input reference level (for timing referenced to CK_t and CK_c) is the point at which CK_t and CK_c cross. Refer to the applicable timings in the AC Timings table.
6. The WCK_t and WCK_c input reference level (for timing referenced to WCK_t and WCK_c) is the point at which WCK_t and WCK_c cross. Refer to the applicable timings in the AC Timings table.
7. V_{REFD} is either V_{REFD}, V_{REFD2}, or V_{REFC}.
8. Figure 13 (page 20) illustrates the exact relationship between (CK_t - CK_c) or (WCK_t - WCK_c) and $V_{ID(AC)}$, $V_{ID(DC)}$.
9. The AC operating conditions are for DRAM design only and are valid on the silicon at the input of the receiver. They are not intended to be measured.

Figure 12: Voltage Waveform



Note: 1. V_{REF}, V_{IH}, and V_{IL} refer to whichever V_{REFxx} (V_{REFD}, V_{REFD2}, V_{REFC}, or V_{REFC2}) is being used.

Figure 13: Clock Waveform



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