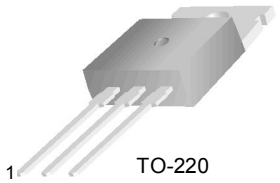
FAIRCHILD SEMICONDUCTOR®

November 2008

TIP47/TIP48/TIP49/TIP50

NPN Silicon Transistor

- High Voltage and Switching Applications
- High Sustaining Voltage : V_{CEO}(sus) = 250 - 400V
- 1A Rated Collector Current



1 TO-220

1.Base 2.Collector 3.Emitter

Absolute Maximum Ratings* T_a = 25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{CBO}	Collector-Base Voltage : TIP47	350	V
	: TIP48	400	V
	: TIP49	450	V
	: TIP50	500	V
V_{CEO}	Collector-Emitter Voltage : TIP47	250	V
	: TIP48	300	V
	: TIP49	350	V
	: TIP50	400	V
V_{EBO}	Emitter-Base Voltage	5	V
I_C	Collector Current (DC)	1	A
I_{CP}	Collector Current (Pulse)	2	A
I_B	Base Current	0.6	A
P_C	Collector Dissipation (T_C=25°C)	40	W
	Collector Dissipation (T_a=25°C)	2	W
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	- 65 ~ 150	°C

* These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

Electrical Characteristics* T_a=25°C unless otherwise noted

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_{CEX}(sus)	Collector-Emitter Sustaining Voltage					
	: TIP47	I_C = 30mA, I_B = 0	250			V
	: TIP48		300			V
	: TIP49		350			V
	: TIP50		400			V
I_{CEO}	Collector Cut-off Current : TIP47	V_{CE} = 150V, I_B = 0			1	mA
	: TIP48	V_{CE} = 200V, I_B = 0			1	mA
	: TIP49	V_{CE} = 250V, I_B = 0			1	mA
	: TIP50	V_{CE} = 300V, I_B = 0			1	mA
I_{CEX}	Collector Cut-off Current : TIP47	V_{CE} = 350V, V_{BE} = 0			1	mA
	: TIP48	V_{CE} = 400V, V_{BE} = 0			1	mA
	: TIP49	V_{CE} = 450V, V_{BE} = 0			1	mA
	: TIP50	V_{CE} = 500V, V_{BE} = 0			1	mA
I_{EBO}	Emitter Cut-off Current	V_{EB} = 5V, I_C = 0			1	mA
h_{FE}	* DC Current Gain	V_{CE} = 10V, I_C = 0.3A	30		150	
		V_{CE} = 10V, I_C = 1A	10			
V_{CE}(sat)	* Collector-Emitter Saturation Voltage	I_C = 1A, I_B = 0.2A			1	V
V_{BE}(sat)	* Base-Emitter Saturation Voltage	V_{CE} = 10V, I_C = 1A			1.5	V
f_T	Current Gain Bandwidth Product	V_{CE} =10V, I_C = 0.2A, f = 1MHz	10			MHz

* Pulse Test: Pulse Width≤300μs, Duty Cycle≤2%

Typical Characteristics

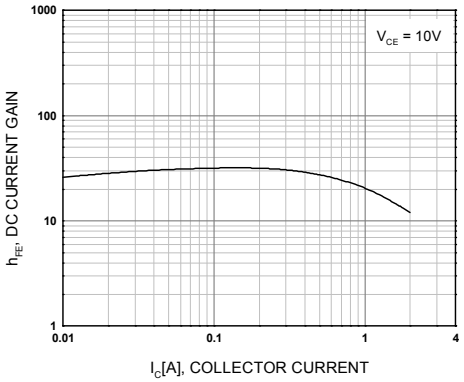


Figure 1. DC current Gain

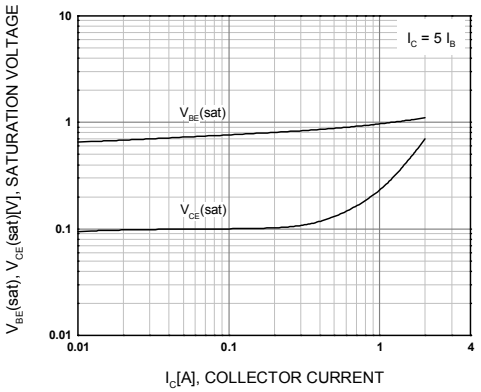


Figure 2. Collector-Emitter Saturation Voltage Base-Emitter Saturation Voltage

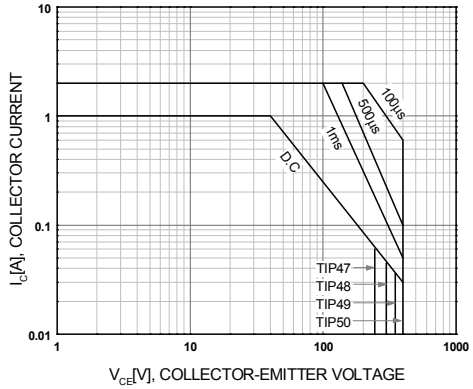


Figure 3. Safe Operating Area

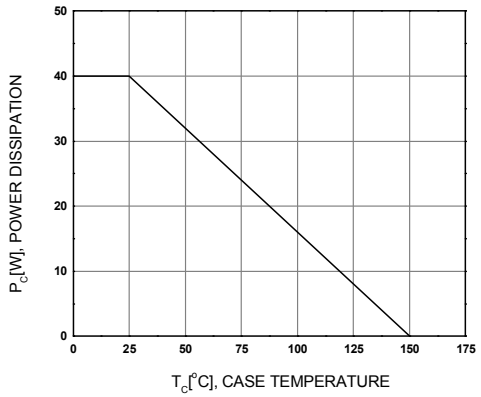
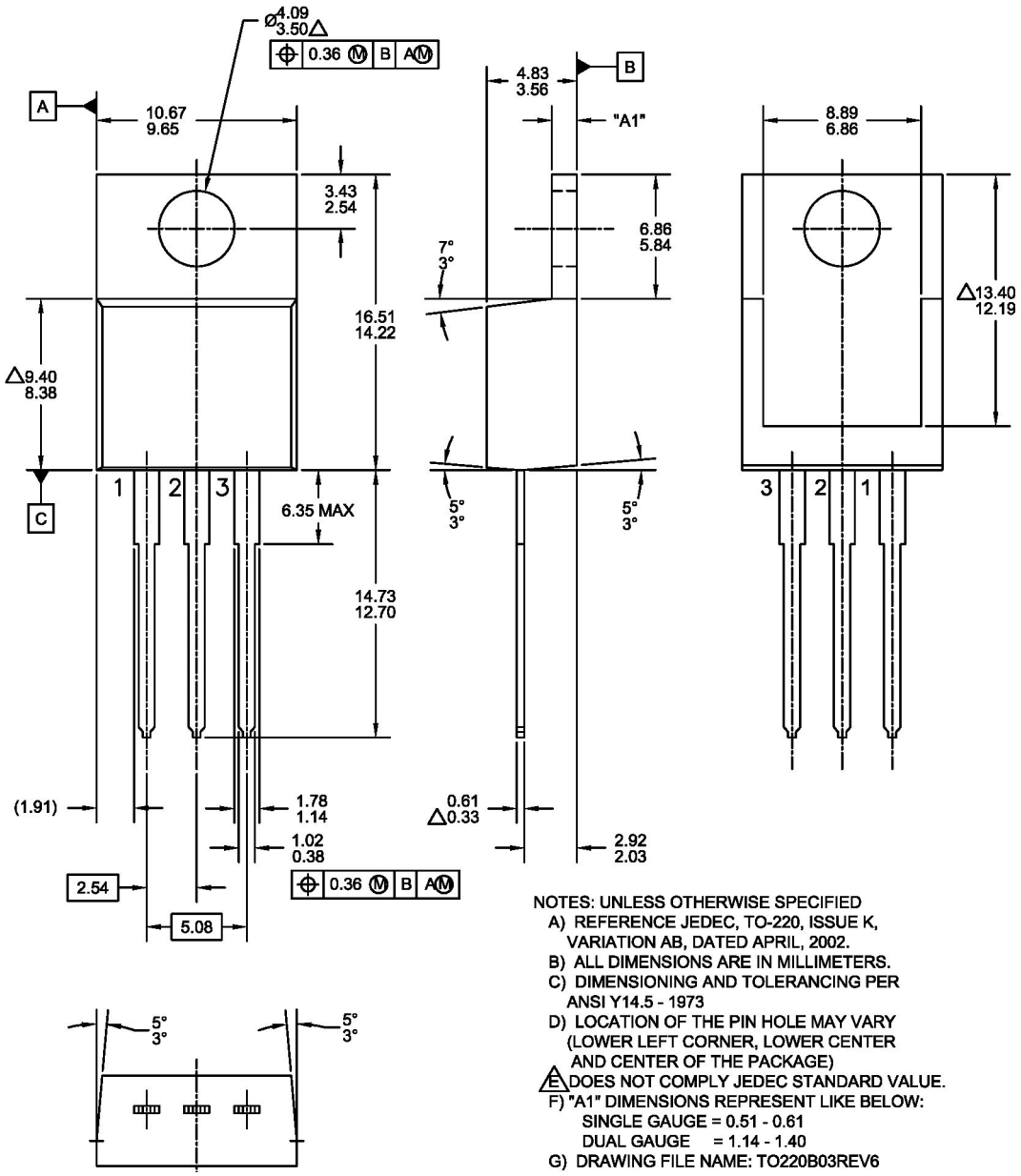


Figure 4. Power Derating

Mechanical Dimensions

TO220



NOTES: UNLESS OTHERWISE SPECIFIED

A) REFERENCE JEDEC, TO-220, ISSUE K, VARIATION AB, DATED APRIL, 2002.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONING AND TOLERANCING PER ANSI Y14.5 - 1973
D) LOCATION OF THE PIN HOLE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE)
△E DOES NOT COMPLY JEDEC STANDARD VALUE.
F) "A1" DIMENSIONS REPRESENT LIKE BELOW:
SINGLE GAUGE = 0.51 - 0.61
DUAL GAUGE = 1.14 - 1.40
G) DRAWING FILE NAME: TO220B03REV6

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No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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Rev. I31

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