

2.4-2.5 GHz Power Amplifier

SST12LP00



EOL Data Sheet

FEATURES:

- **High Gain:**
 - Typically 28 dB gain across 2.4– 2.5 GHz over temperatures 0– 85°C
- **High linear output power:**
 - >24 dBm P1dB
- **High power-added efficiency/low operating current for Bluetooth applications**
 - ~50% PAE or 115 mA total current consumption @ P_{out} = 23 dBm for V_{CC} = 3.3V and GCTL = 3.0V
- **Low idle current**
 - ~10 mA I_{CQ}
- **Simple input/output matching**
- **Packages available**
 - 6-contact VQFN and UQFN (3 x 1.6mm²)

APPLICATIONS:

- **Bluetooth**
- **USB Dongles**
- **2.4 GHz Cordless phones**

PRODUCT DESCRIPTION

The SST12LP00 is a high-power and high-gain power amplifier based on the highly reliable InGaP/GaAs HBT technology. SST12LP00 is easily configured for high-power and high-efficiency applications while operating over the 2.4- 2.5 GHz frequency band. This device typically provides 30 dB gain with better than 50% power added efficiency @ P_{out} = 23 dBm.

The SST12LP00's excellent linearity is well suited for Class 1 Bluetooth operation. The power amplifier IC also features easy board-level usage along with high speed power up/down control. A low reference current makes SST12LP00 ideal for the final stage power amplification in battery-powered Bluetooth, USB Dongle, or cordless phone transmitter applications.

The SST12LP00 is offered in both 6-contact VQFN and UQFN packages. See Figure 2 for pin assignments and Table 1 for pin descriptions.



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FUNCTIONAL BLOCKS

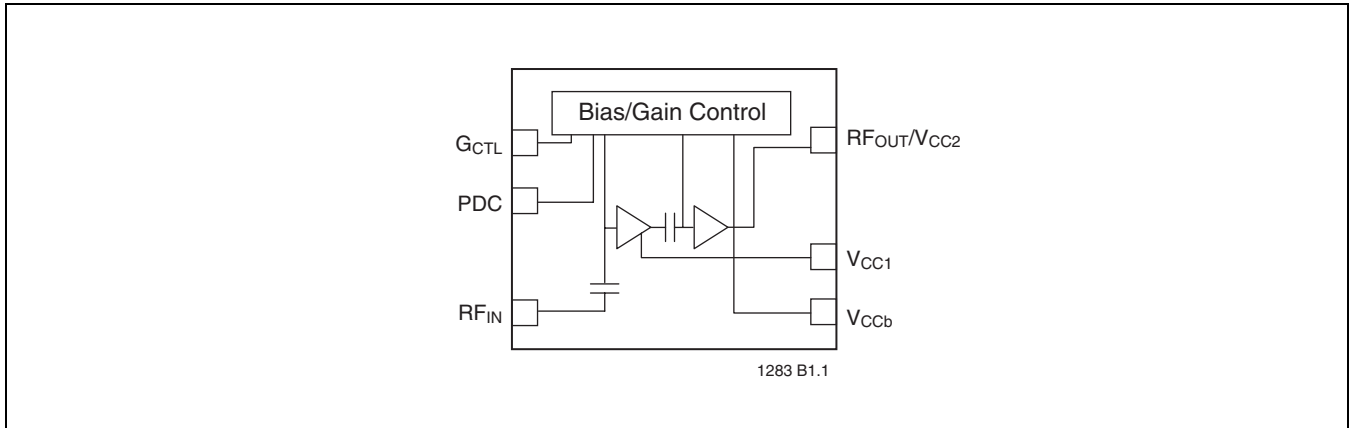


FIGURE 1: Functional Block Diagram

PIN ASSIGNMENTS

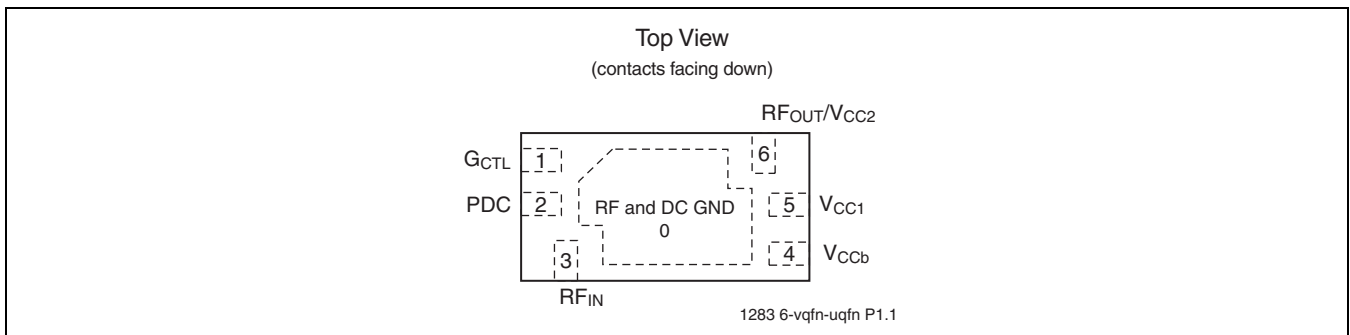


FIGURE 2: Pin Assignments for 6-contact VQFN and UQFN

PIN DESCRIPTIONS

TABLE 1: Pin Description

Symbol	Pin No.	Pin Name	Type ¹	Function
GND	0	Ground		The center pad should be connected to RF ground with several low inductance, low resistance vias.
G _{CTL}	1			Power Amplifier Gain Control
PDC	2			Power-down Control
RF _{IN}	3		I	RF input, DC decoupled
V _{CCb}	4	Power Supply	PWR	Vcc power supply, bias circuit
V _{CC1}	5	Power Supply	PWR	Vcc power supply, 1st stage
RF _{OUT} /V _{CC2}	6		O/PWR	Vcc power supply, 2nd stage

1. I=Input, O=Output

T1.1 1283



2.4-2.5 GHz Power Amplifier SST12LP00

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ELECTRICAL SPECIFICATIONS

The AC and DC specifications for the power amplifier interface signals. Refer to Table 2 for the DC voltage and current specifications. Refer to Figure 3 for the RF performance.

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under “Absolute Maximum Stress Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Supply Voltage at pins 4, 5, and 6 (V_{CC})	-0.3V to +3.6V
Power-down Control Voltage (PDC)	-0.3V to V_{CC}
Gain Control Voltage (G_{CTL})	-0.3V to V_{CC}
Radio Frequency Input Power (RF_{IN})	+10 dBm
Operating Temperature (T_A)	-40°C to +85°C
Storage Temperature (T_{STG})	-40°C to +120°C
Maximum Junction Temperature (T_J)	+150°C
Surface Mount Solder Reflow Temperature	260°C for 10 seconds

Operating Range

Range	Ambient Temp	V_{CC}
Industrial	-40°C to +85°C	3.3V

TABLE 2: DC Electrical Characteristics

Symbol	Parameter	Min.	Typ	Max.	Unit	Test Conditions
V_{CC}	Supply Voltage at pins 4, 5, and 6	2.7	3.3	3.6	V	
I_{CC}	Supply Current @ $P_{OUT} = 23$ dBm		115		mA	
G_{CTL}	Power Amplifier Gain Control Voltage	0.1	3.0	3.3	V	
I_{GCTL}	Current through G_{CTL} pin		55	100	μ A	
PDC	Logic High Voltage	2.6			V	
	Logic Low Voltage			0.8	V	
I_{CQ}	Idle Current ($G_{CTL} = 3.0V$)		10		mA	

T2.3 1283

TABLE 3: AC Electrical Characteristics

Symbol	Parameter	Min.	Typ	Max.	Unit
F_{L-U}	Frequency range	2402		2480	MHz
P_{OUT}	Output power @ $PIN = -7$ dBm, $V_{CC} = 3.3V$, $G_{CTL} = 3.0V$		23		dBm
G	Small signal gain		27		dB
G_{VAR}	Gain variation over band (2400~2485 MHz)		0.2	0.5	dB

T3.2 1283



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TYPICAL PERFORMANCE CHARACTERISTICS

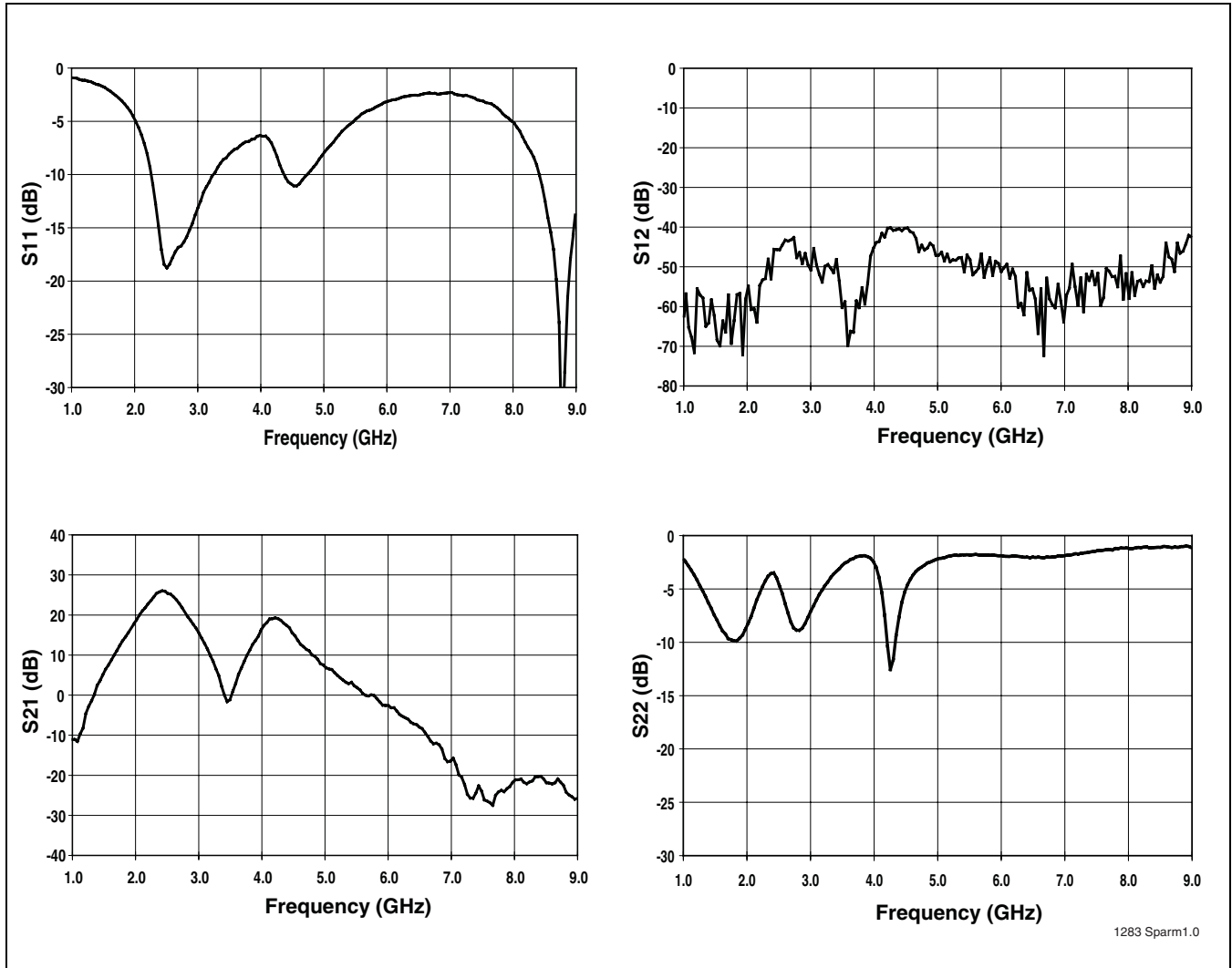


FIGURE 3: S-parameters for SST12LP00

2.4-2.5 GHz Power Amplifier SST12LP00



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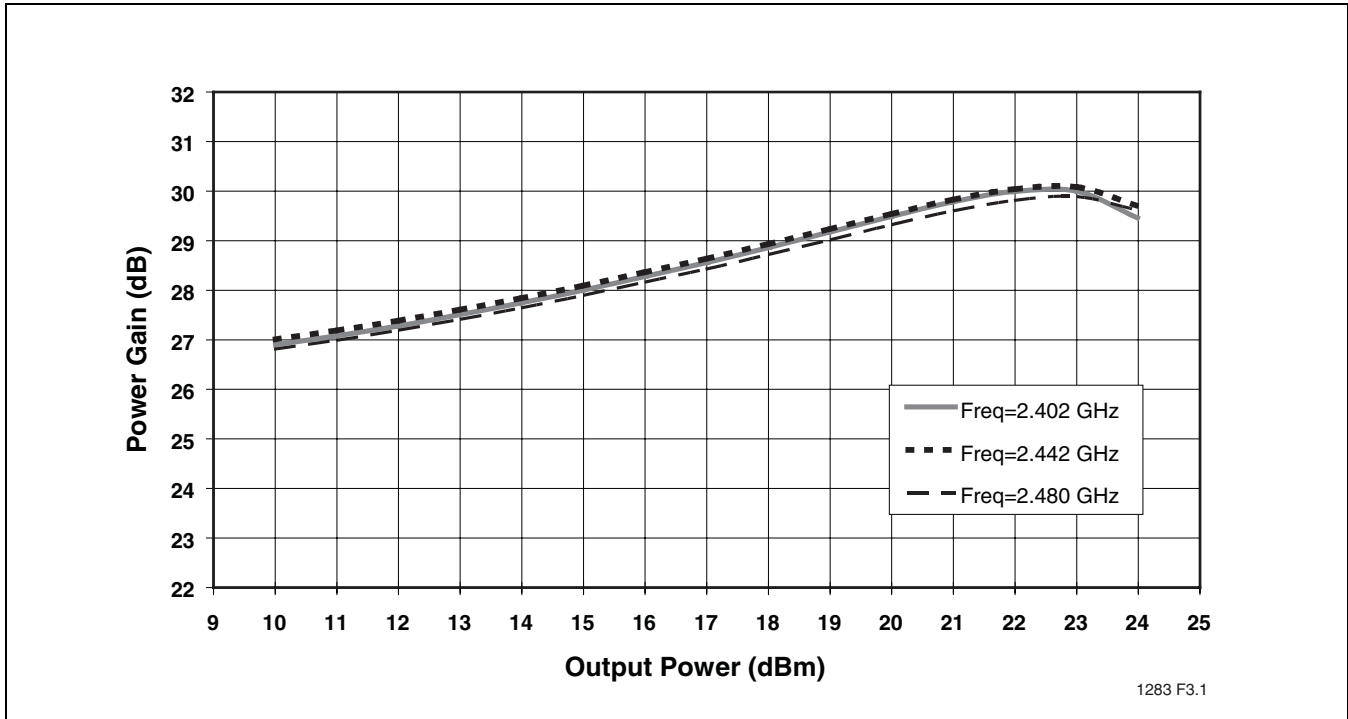


FIGURE 4: Power Gain versus Output Power

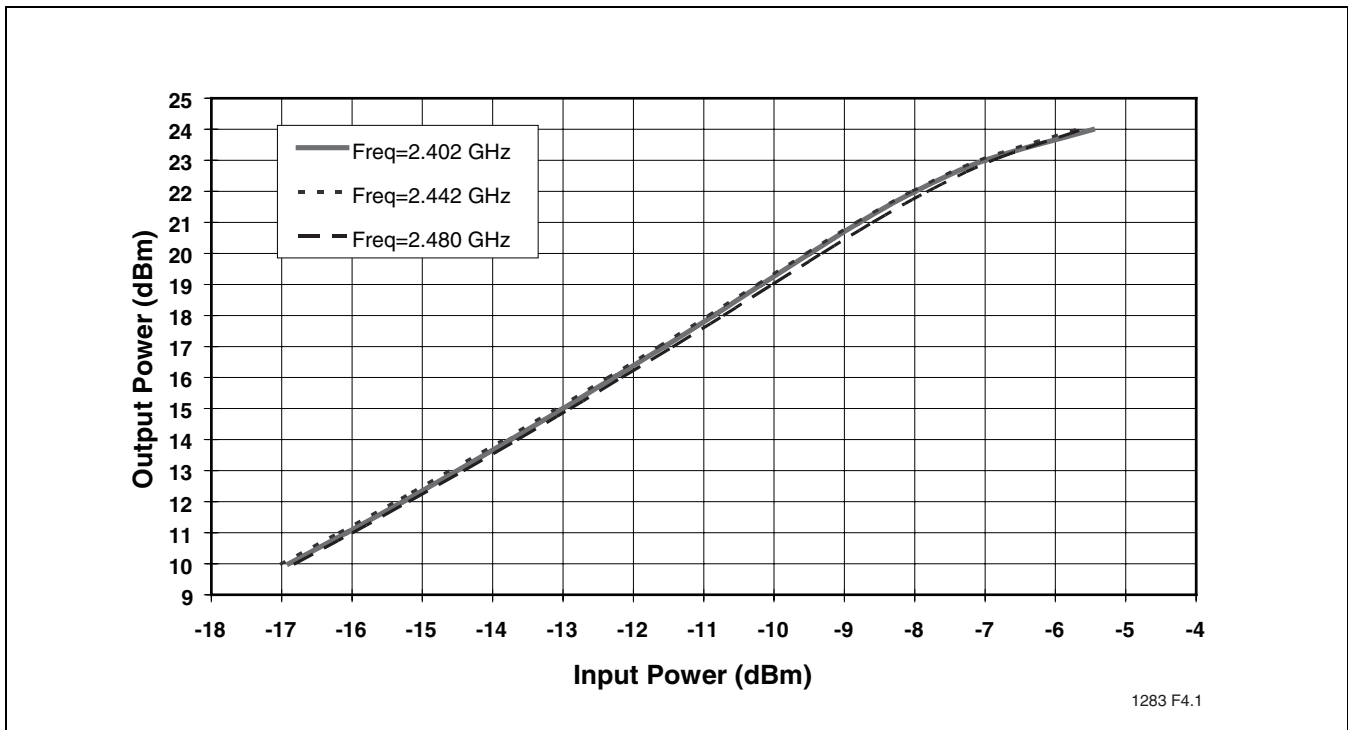


FIGURE 5: Output Power versus Input Power

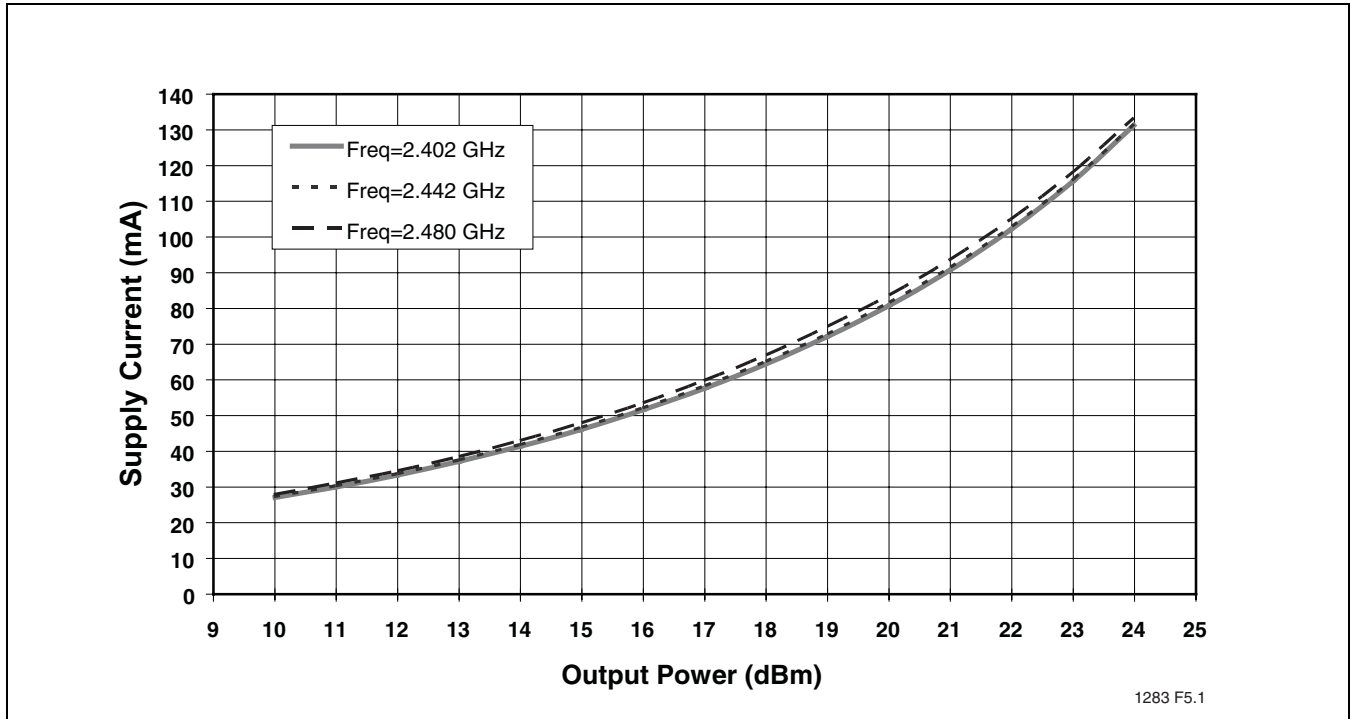


FIGURE 6: Supply Current versus Output Power

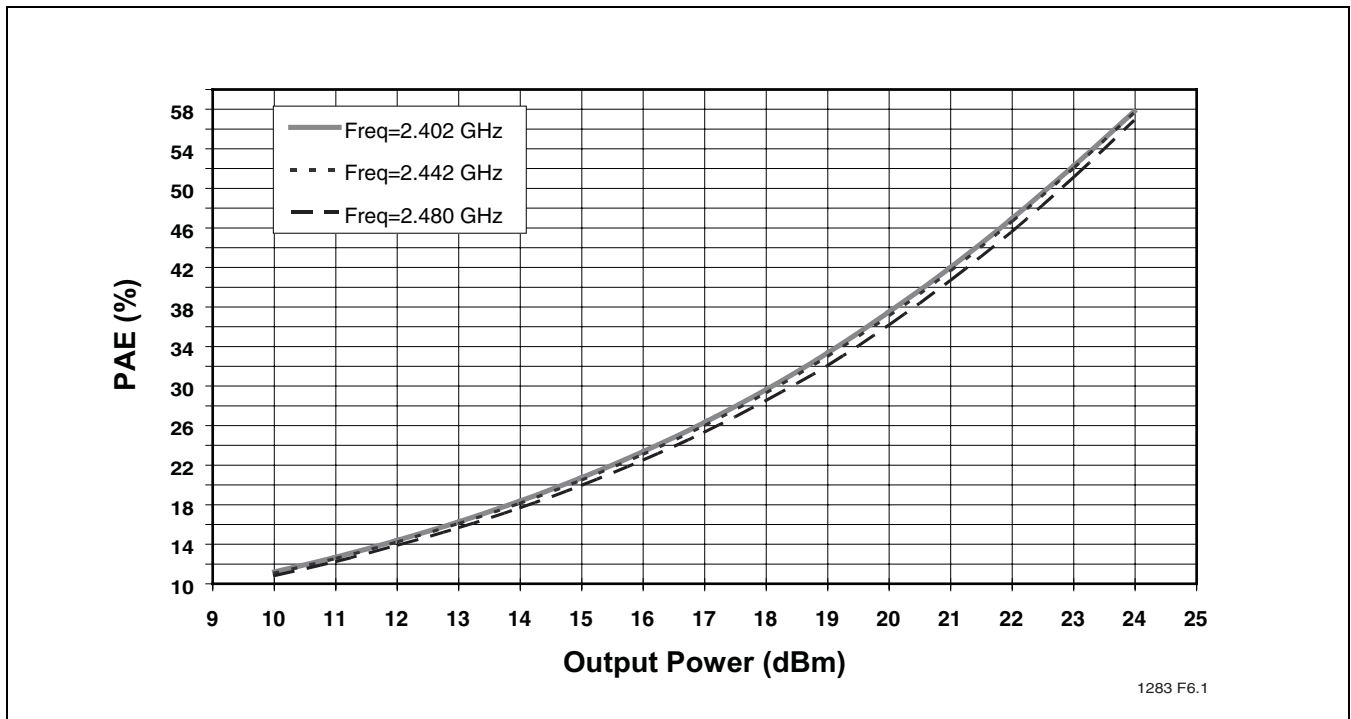


FIGURE 7: PAE versus Output Power

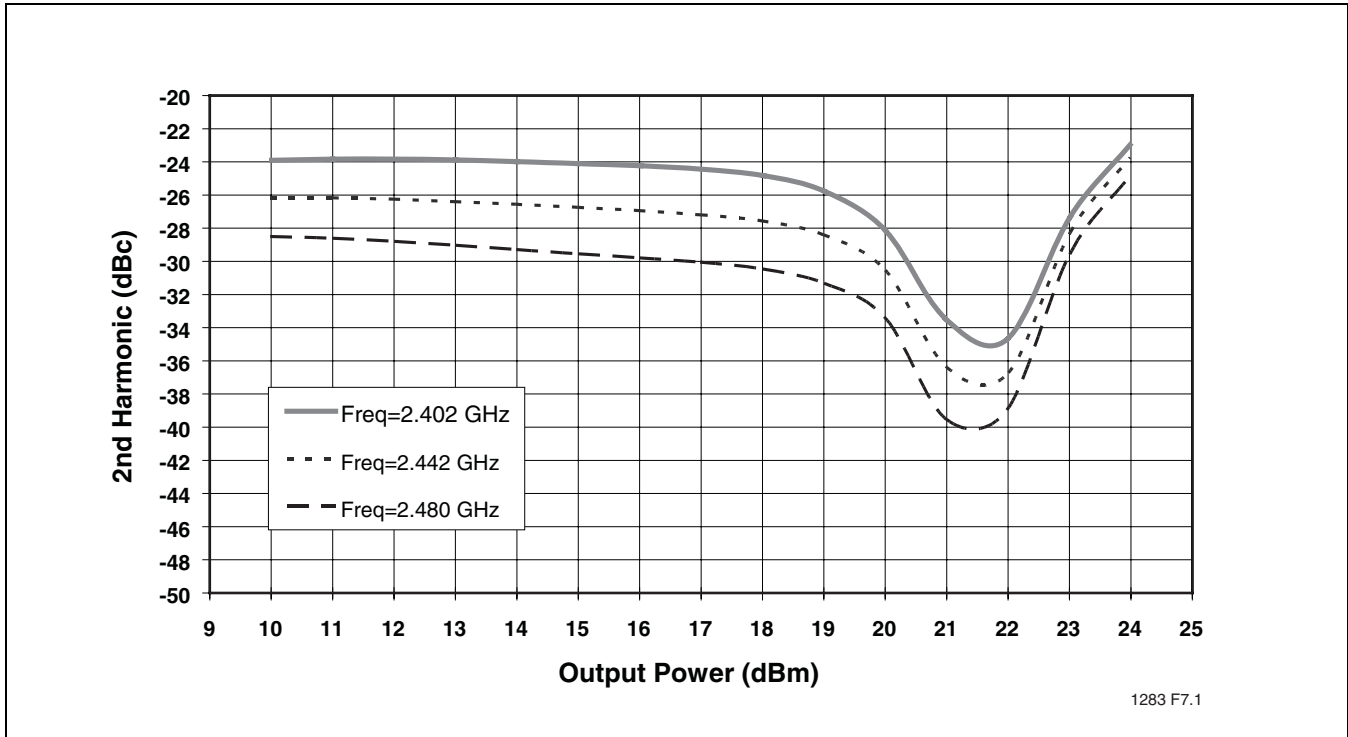


FIGURE 8: 2nd Harmonic versus Output Power

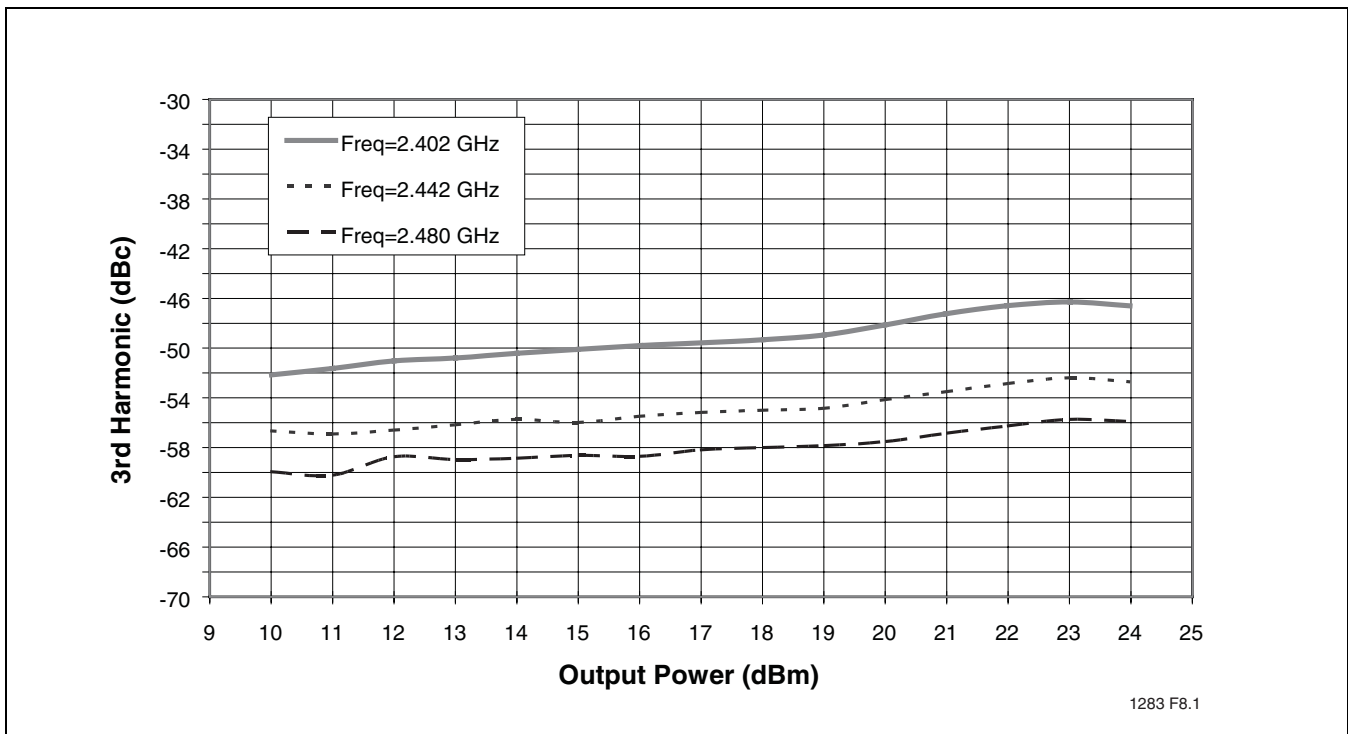


FIGURE 9: 3rd Harmonic versus Output Power

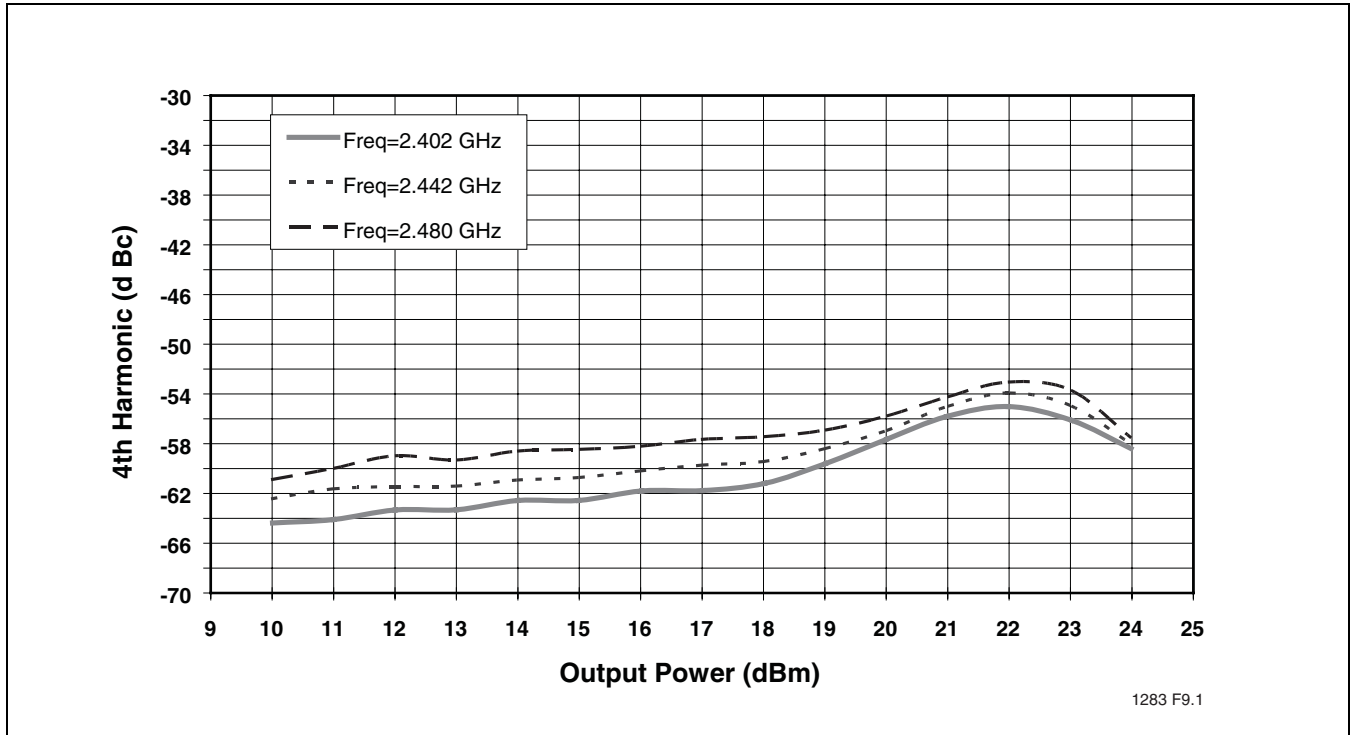


FIGURE 10: 4th Harmonic versus Output Power

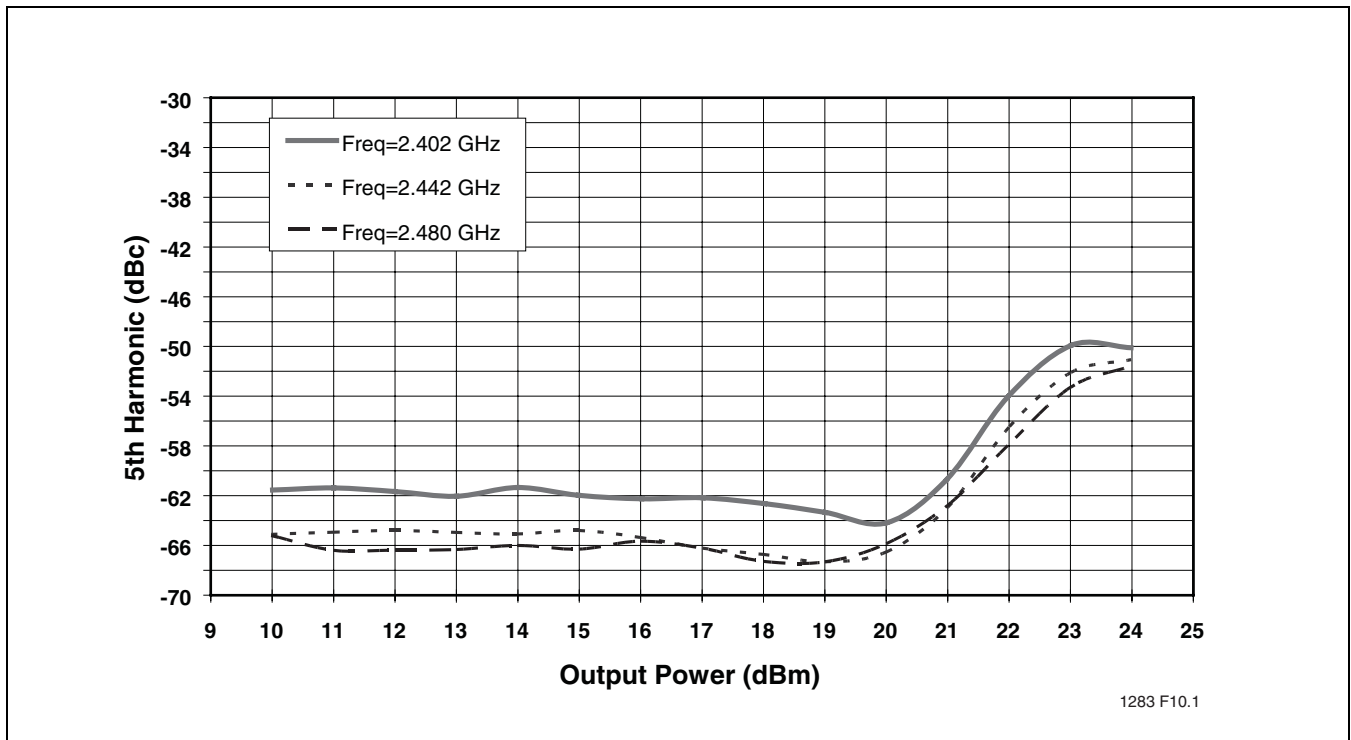


FIGURE 11: 5th Harmonic versus Output Power

2.4-2.5 GHz Power Amplifier SST12LP00



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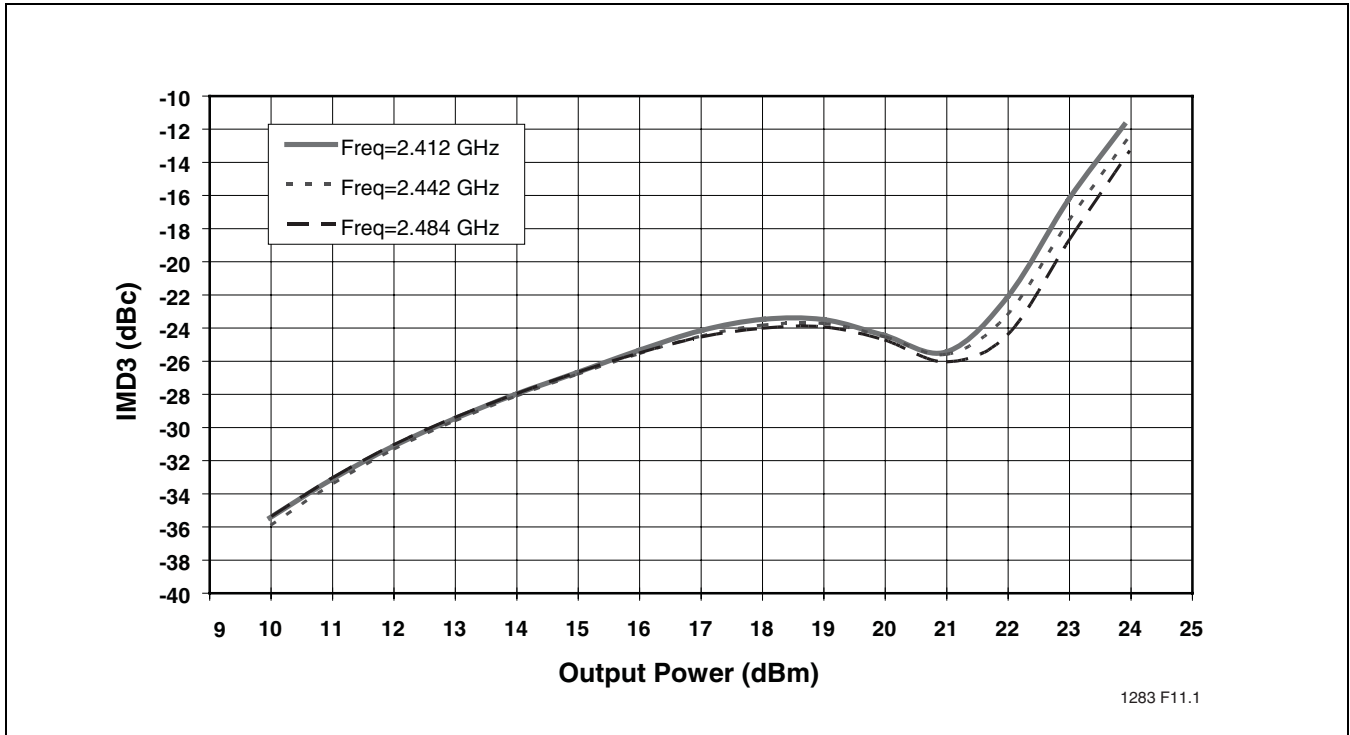
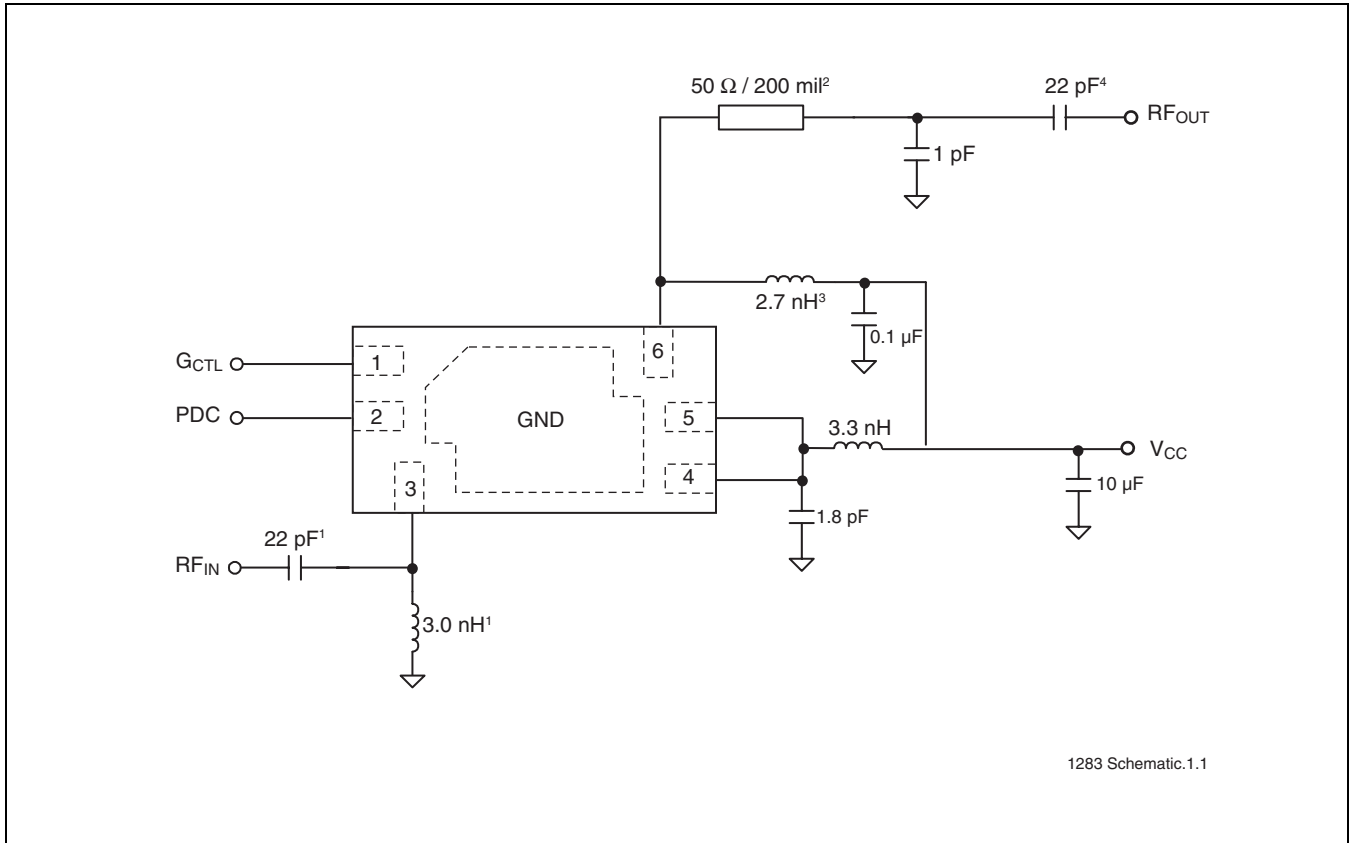


FIGURE 12: IMD3 versus Output Power



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TYPICAL APPLICATION



1. Optional and only necessary for achieving high input return loss.
2. Replaceable by 1 nH (0402) inductor for compactness.
3. Shunt capacitor can be added to the inductor to lower the 2nd harmonic.
4. LC low-pass filter can be added to lower the 2nd harmonic.

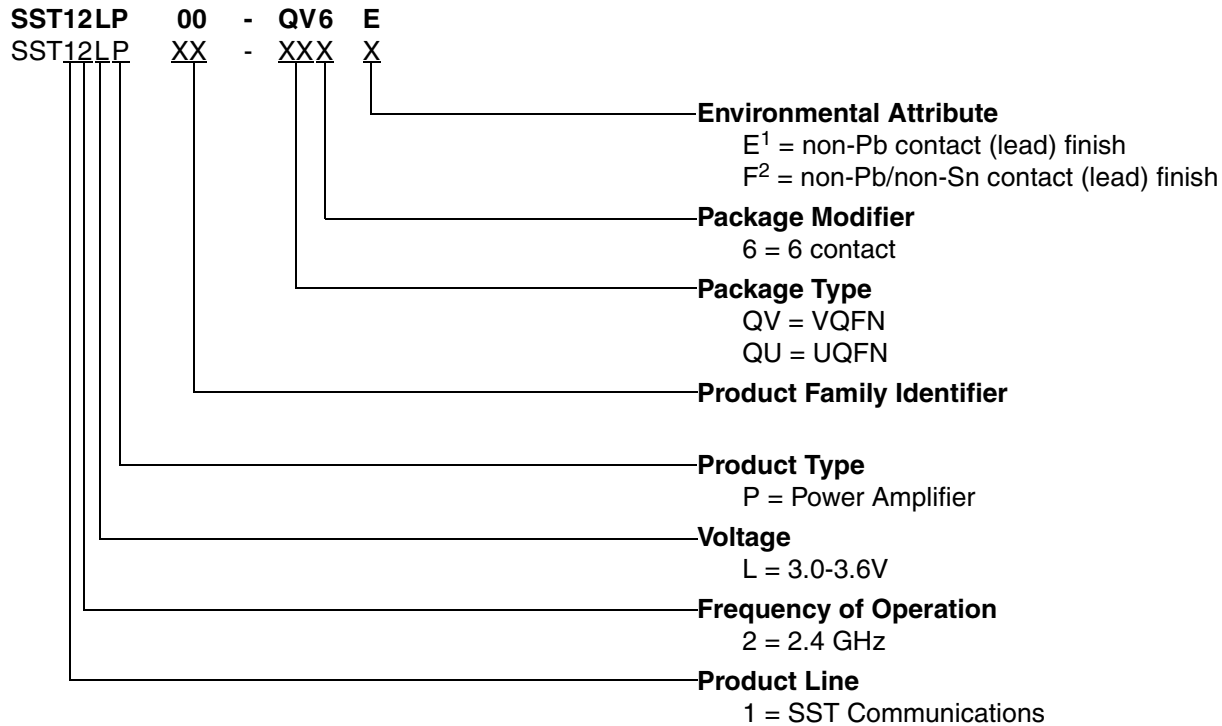
FIGURE 13: Typical Application Schematic (Top View)

2.4-2.5 GHz Power Amplifier SST12LP00



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PRODUCT ORDERING INFORMATION



1. Environmental suffix "E" denotes non-Pb solder. SST non-Pb solder devices are "RoHS Compliant".
2. Environmental suffix "F" denotes non-Pb/non-Sn solder. SST non-Pb/non-Sn solder devices are "RoHS Compliant".

Valid combinations for SST12LP00

SST12LP00-QV6E SST12LP00-QU6F

SST12LP00 Evaluation Kits

SST12LP00-QV6E-K SST12LP00-QU6F-K

Note: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.



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PACKAGING DIAGRAMS

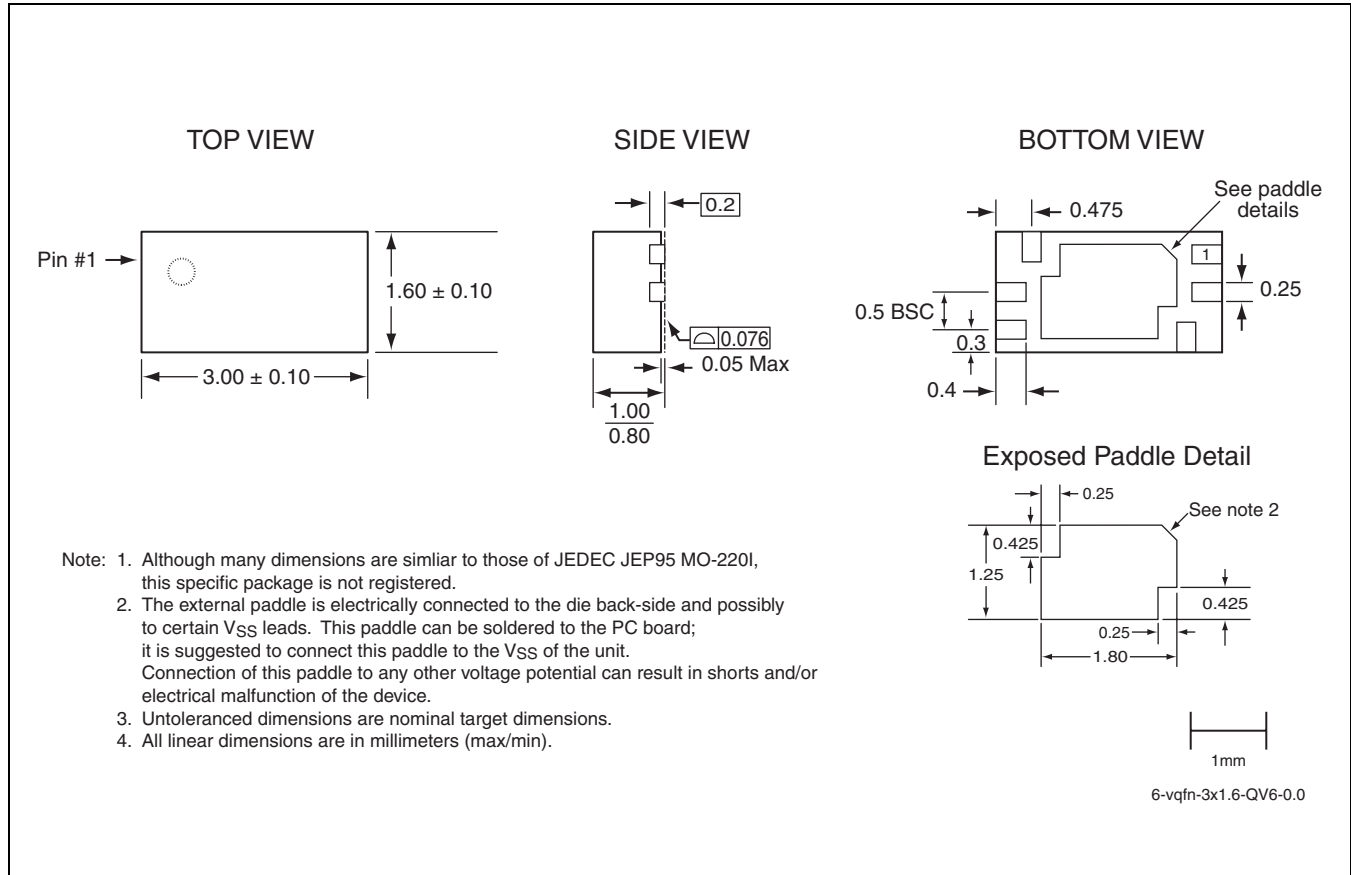
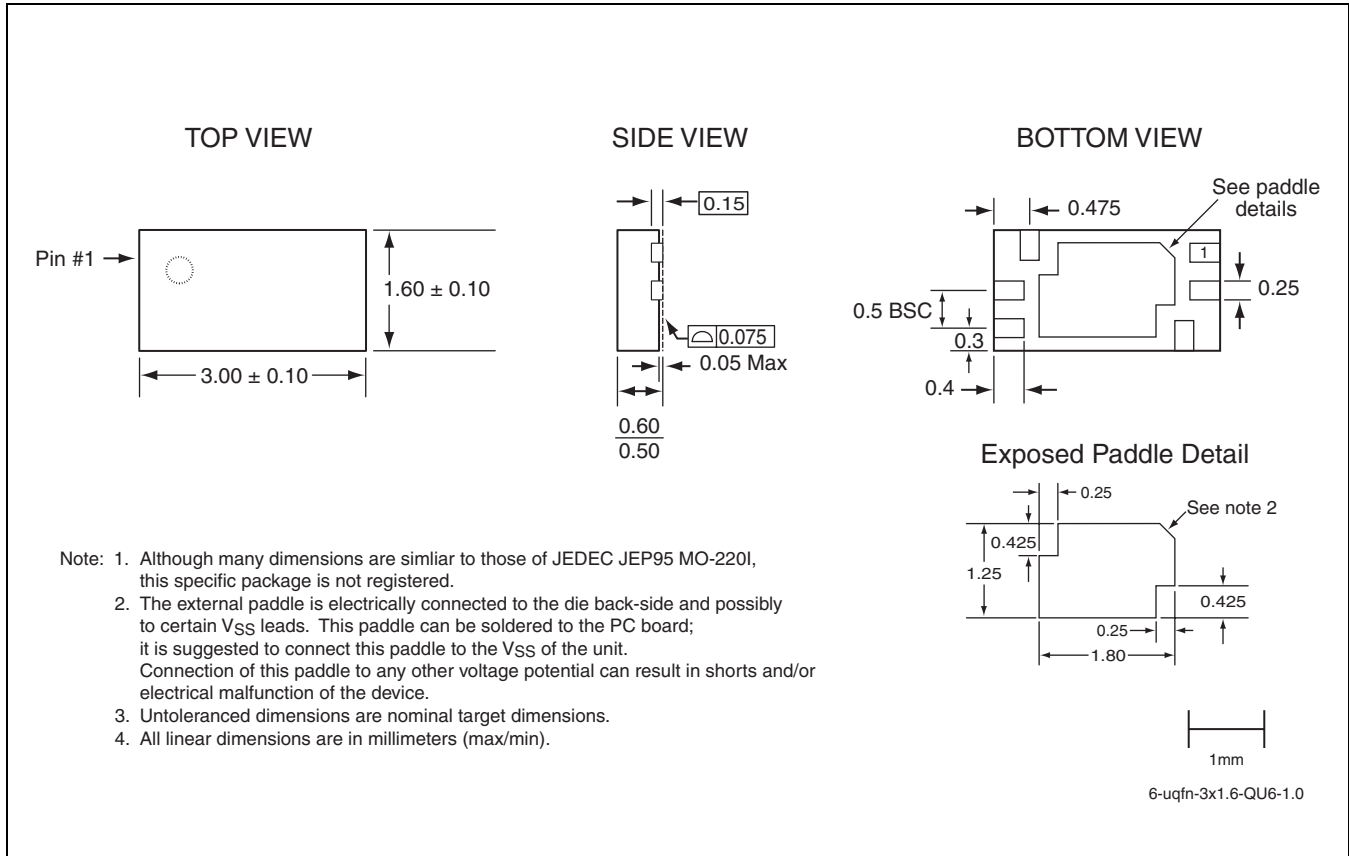


FIGURE 14: 6-contact Very-thin Quad Flat No-lead (VQFN)
SST Package Code: QV6

2.4-2.5 GHz Power Amplifier SST12LP00



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**FIGURE 15: 6-Contact Ultra-thin Quad Flat No-lead (UQFN)
SST Package Code: QU6**

TABLE 4: Revision History

Revision	Description	Date
00	• S71283: SST conversion of data sheet GP1200	Jan 2005
01	• Made various changes to include UQFN package • Updated Information in "Features:" on page 1 • Updated "Product Description" on page 1 • Updated Table 1 on page 2 • Updated "Electrical Specifications" on page 3 • Updated Table 2 on page 3 • Updated Table 3 on page 3 • Updated Figure 13 on page 10 • Applied new formatting styles.	Mar 2006
02	• Updated document status from Preliminary Specification to Data Sheet	Apr 2008
03	• Updated "Contact Information" on page 14.	Feb 2009
04	• End of Life all valid combinations in this data sheet	Apr 2009



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CONTACT INFORMATION

Marketing

SST Communications Corp.
5340 Alla Road, Ste. 210
Los Angeles, CA 90066
Tel: 310-577-3600
Fax: 310-577-3605

Sales and Marketing Offices

NORTH AMERICA

Silicon Storage Technology, Inc.
1171 Sonora Court
Sunnyvale, CA 94086-5308
Tel: 408-735-9110
Fax: 408-735-9036

EUROPE

Silicon Storage Technology Ltd.
Mark House
9-11 Queens Road
Hersham, Surrey
KT12 5LU UK
Tel: 44 (0) 1932-238133
Fax: 44 (0) 1932-230567

JAPAN

SST Japan
NOF Tameike Bldg, 9F
1-1-14 Akasaka, Minato-ku
Tokyo, Japan 107-0052
Tel: 81-3-5575-5515
Fax: 81-3-5575-5516

ASIA PACIFIC NORTH

SST Macao
Room N, 6th Floor,
Macao Finance Center, No. 202A-246,
Rua de Pequim, Macau
Tel: 853-2870-6022
Fax: 853-2870-6023

ASIA PACIFIC SOUTH

SST Communications Co.
16F-6, No. 75, Sec.1, Sintai 5th Rd
Sijhih City, Taipei County 22101
Taiwan, R.O.C.
Tel: 886-2-8698-1198
Fax: 886-2-8698-1190

KOREA

SST Korea
6F, Heungkuk Life Insurance Bldg 6-7
Sunae-Dong, Bundang-Gu, Sungnam-Si
Kyungki-Do, Korea, 463-020
Tel: 82-31-715-9138
Fax: 82-31-715-9137



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Наши контакты:

Телефон: +7 812 627 14 35

Электронная почта: sales@st-electron.ru

Адрес: 198099, Санкт-Петербург,
Промышленная ул, дом № 19, литера Н,
помещение 100-Н Офис 331