ANALOG DEVICES

Quad 3000 V/μs, 35 mW Current Feedback Amplifier

AD8004

FEATURES

High Speed
- **250 MHz –3 dB Bandwidth (G = +1)**
- **3000 V/μs Slew Rate**
- **21 ns Settling Time to 0.1%**
- **1.8 ns Rise Time for 2 V Step**

Low Power
- **3.5 mA/Amp Power Supply Current (35 mW/Amp)**

Single Supply Operation
- **Fully Specified for +5 V Supply**

Good Video Specifications (R_L = 150 Ω, G = +2)
- **Gain Flatness 0.1 dB to 30 MHz**
- **0.04% Differential Gain Error**
- **0.10° Differential Phase Error**

Low Distortion
- **–78 dBc THD at 5 MHz**
- **–61 dBc THD at 20 MHz**

High Output Current of 50 mA

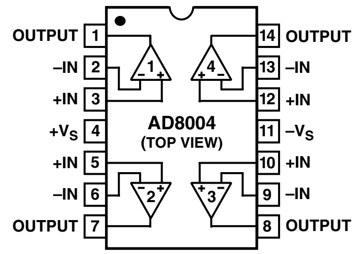
Available in a 14-Lead PDIP, SOIC, and CERDIP

APPLICATIONS

Image Scanners
Active Filters
Video Switchers
Special Effects

CONNECTION DIAGRAM

PDIP (N), CERDIP (Q), and SOIC (R) Packages



GENERAL DESCRIPTION

The AD8004 is a quad, low power, high speed amplifier designed to operate on single or dual supplies. It utilizes a current feedback architecture and features high slew rate of 3000 V/μs making the AD8004 ideal for handling large amplitude pulses. Additionally, the AD8004 provides gain flatness of 0.1 dB to 30 MHz while offering differential gain and phase error of 0.04% and 0.10°. This makes the AD8004 suitable for video electronics such as cameras and video switchers.

The AD8004 offers low power of 3.5 mA/amplifier and can run on a single +4 V to +12 V power supply, while being capable of delivering up to 50 mA of load current. All this is offered in a small 14-lead DIP or 14-lead SOIC package. These features make this amplifier ideal for portable and battery powered applications where size and power are critical.

The outstanding bandwidth of 250 MHz along with 3000 V/μs of slew rate make the AD8004 useful in many general-purpose, high speed applications where dual power supplies of up to ±6 V and single supplies from 4 V to 12 V are needed. The AD8004 is available in the industrial temperature range of –40°C to +85°C in the N and R packages, and in the military temperature range of –55°C to +125°C in the Q package.

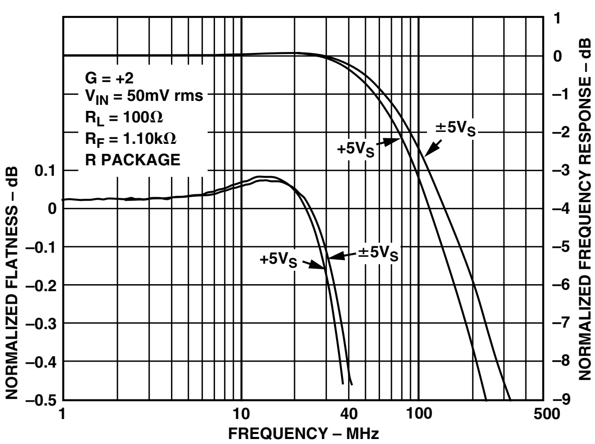


Figure 1. Frequency Response and Flatness, G = +2

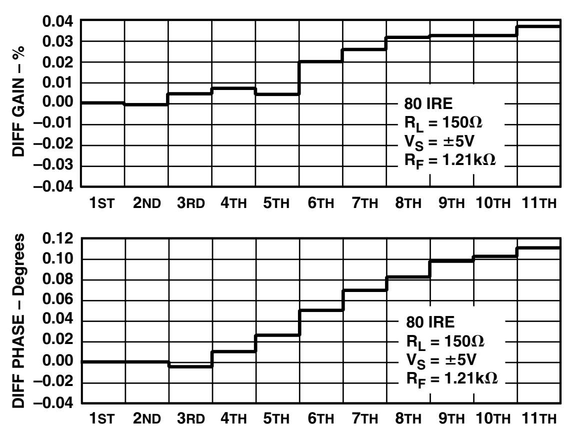


Figure 2. Differential Gain/Differential Phase

REV. C

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 www.analog.com
Fax: 781/326-8703

AD8004–SPECIFICATIONS (@ T_A = +25°C, V_S = ±5 V, R_L = 100 Ω, unless otherwise noted.)

Parameter	Conditions	AD8004A Min	AD8004A Typ	AD8004A Max	AD8004S Min	AD8004S Typ	AD8004S Max	Unit
DYNAMIC PERFORMANCE								
–3 dB Bandwidth, N Package	G = +2, R_F = 698 Ω		185					MHz
	G = +1, R_F = 806 Ω		250					MHz
Bandwidth for 0.1 dB Flatness	G = +2		30			30		MHz
Slew Rate	G = +2, V_O = 4 V Step		3000			3000		V/µs
	G = –2, V_O = 4 V Step		2000			2000		V/µs
Settling Time to 0.1%	G = +2, V_O = 2 V Step		21			21		ns
Rise and Fall Time (10% to 90%)	G = +2, V_O = 2 V Step		1.8			1.8		ns
NOISE/HARMONIC PERFORMANCE								
Total Harmonic Distortion	f_C = 5 MHz, V_O = 2 V p-p, R_L = 1 kΩ		–78			–78		dBc
Crosstalk, R Package, Worst Case	f = 5 MHz, G = +2, R_L = 1 kΩ		–69					dB
Crosstalk, N Package, Worst Case	f = 5 MHz, G = +2, R_L = 1 kΩ		–64					dB
Input Voltage Noise	f = 10 kHz		1.5			1.5		nV/√Hz
Input Current Noise	f = 10 kHz, +In		38			38		pA/√Hz
	–In		38			38		pA/√Hz
Differential Gain Error	NTSC, G = +2, R_L = 150 Ω, R_F = 1.21 kΩ		0.04			0.04		%
Differential Phase Error	NTSC, G = +2, R_L = 150 Ω, R_F = 1.21 kΩ		0.10			0.10		Degree
Differential Gain Error	NTSC, G = +2, R_L = 1 kΩ, R_F = 1.21 kΩ		0.01			0.01		%
Differential Phase Error	NTSC, G = +2, R_L = 1 kΩ, R_F = 1.21 kΩ		0.04			0.04		Degree
DC PERFORMANCE								
Input Offset Voltage			1.0	3.5		1.0	3.5	mV
	T_{MIN} to T_{MAX}		1.5	5		1.5	6	mV
Offset Drift			15			15		µV/°C
–Input Bias Current			±35	±90		±35	±90	µA
	T_{MIN} to T_{MAX}			±110			±120	µA
+Input Bias Current			±40	±110		±40	±110	µA
	T_{MIN} to T_{MAX}			±120			±130	µA
Open-Loop Transresistance	V_O = ±2.5 V	170	290		170	290		kΩ
	T_{MIN} to T_{MAX}		220			220		kΩ
INPUT CHARACTERISTICS								
Input Resistance	+Input		2			2		MΩ
	–Input		50			50		Ω
Input Capacitance	+Input		1.5			1.5		pF
Input Common-Mode Voltage Range			3.2			3.2		±V
Common-Mode Rejection Ratio								
Offset Voltage	V_{CM} = ±2.5 V	52	58		52	58		dB
–Input Current	V_{CM} = ±2.5 V, T_{MIN} to T_{MAX}		1			1		µA/V
+Input Current	V_{CM} = ±2.5 V, T_{MIN} to T_{MAX}		12			12		µA/V
OUTPUT CHARACTERISTICS								
Output Voltage Swing	R_L = 150 Ω		3.9			3.9		±V
Output Current			50			50		mA
Short Circuit Current		100	180		100	180		mA
POWER SUPPLY								
Operating Range		±2.0		±6.0	±2.0		±6.0	V
Total Quiescent Current			14	17		14	17	mA
	T_{MIN} to T_{MAX}		16	20		16	23	mA
Power Supply Rejection Ratio	ΔV_S = ±2 V	56	62		56	62		dB
–Input Current	T_{MIN} to T_{MAX}		0.5			0.5		µA/V
+Input Current	T_{MIN} to T_{MAX}		4			4		µA/V

Specifications subject to change without notice.

SPECIFICATIONS (@ T_A = +25°C, V_S = +5 V, R_L = 100 Ω, unless otherwise noted.)

Parameter	Conditions	AD8004A Min	AD8004A Typ	AD8004A Max	AD8004S Min	AD8004S Typ	AD8004S Max	Unit
DYNAMIC PERFORMANCE								
–3 dB Bandwidth, N Package	G = +2, R_F = 698 Ω		150					MHz
	G = +1, R_F = 806 Ω		200					MHz
Bandwidth for 0.1 dB Flatness	G = +2		30			30		MHz
Slew Rate	G = +2, V_O = 2 V Step		1100			1100		V/µs
Settling Time to 0.1%	G = +2, V_O = 2 V Step		24			24		ns
Rise and Fall Time (10% to 90%)	G = +2, V_O = 2 V Step		2.3			2.3		ns
NOISE/HARMONIC PERFORMANCE								
Total Harmonic Distortion	f_C = 5 MHz, V_O = 2 V p-p, R_L = 1 kΩ		–65			–65		dBc
Crosstalk, R Package, Worst Case	f = 5 MHz, G = +2, R_L = 1 kΩ		–69					dB
Crosstalk, N Package, Worst Case	f = 5 MHz, G = +2, R_L = 1 kΩ		–64					dB
Input Voltage Noise	f = 10 kHz		1.5			1.5		nV/√Hz
Input Current Noise	f = 10 kHz, +In		38			38		pA/√Hz
	–In		38			38		pA/√Hz
Differential Gain Error	NTSC, G = +2, R_L = 150 Ω, R_F = 1.21 kΩ		0.06			0.06		%
Differential Phase Error	NTSC, G = +2, R_L = 150 Ω, R_F = 1.21 kΩ		0.25			0.25		Degree
Differential Gain Error	NTSC, G = +2, R_L = 1 kΩ, R_F = 1.21 kΩ		0.01			0.01		%
Differential Phase Error	NTSC, G = +2, R_L = 1 kΩ, R_F = 1.21 kΩ		0.08			0.08		Degree
DC PERFORMANCE								
Input Offset Voltage			1.0	2.5		1.0	2.5	mV
	T_{MIN} to T_{MAX}		1	3		1	4	mV
Offset Drift			15			15		µV/°C
–Input Bias Current			±20	±80		±20	±80	µA
	T_{MIN} to T_{MAX}			±100			±110	µA
+Input Bias Current			±35	±100		±35	±100	µA
	T_{MIN} to T_{MAX}			±115			±125	µA
Open Loop Transresistance	V_O = +1.5 V to +3.5 V	140	230		140	230		kΩ
	T_{MIN} to T_{MAX}		170			170		kΩ
INPUT CHARACTERISTICS								
Input Resistance	+Input		2			2		MΩ
	–Input		50			50		Ω
Input Capacitance	+Input		1.5			1.5		pF
Input Common-Mode Voltage Range			3.2			3.2		V
Common-Mode Rejection Ratio								
Offset Voltage	V_{CM} = +1 V to +3 V	52	57		52	57		dB
–Input Current	V_{CM} = +1 V to +3 V, T_{MIN} to T_{MAX}		2			2		µA/V
+Input Current	V_{CM} = +1 V to +3 V, T_{MIN} to T_{MAX}		15			15		µA/V
OUTPUT CHARACTERISTICS								
Output Voltage Swing	R_L = 150 Ω		0.9 to 4.1			0.9 to 4.1		V
Output Current			50			50		mA
Short Circuit Current			95			95		mA
POWER SUPPLY								
Operating Range		0, +4		+12	0, +4		+12	V
Total Quiescent Current			13	14		13	14	mA
	T_{MIN} to T_{MAX}		14.5	15.5		14.5	17.5	mA
Power Supply Rejection Ratio	ΔV_S = +1 V, V_{CM} = +2.5 V	56	62		56	62		dB
–Input Current	T_{MIN} to T_{MAX}		1			1		µA/V
+Input Current	T_{MIN} to T_{MAX}		6			6		µA/V

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . 12.6 V
Internal Power Dissipation . . . . Note 2
Input Voltage (Common Mode) . . . . $\pm V_S$
Differential Input Voltage . . . . ±2.5 V
Output Short Circuit Duration
. . . . Observe Power Derating Curves
Storage Temperature Range (N, Q, R) . . . . –65°C to +125°C
Operating Temperature Range
  A Grade . . . . –40°C to +85°C
  S Grade . . . . –55°C to +125°C
Lead Temperature Range (Soldering 10 sec) . . . . +300°C

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Specification is for device in free air:
14-Lead PDIP Package: θ_{JA} = 90°C/W, θ_{JC} = 30°C/W
14-Lead SOIC Package: θ_{JA} = 140°C/W, θ_{JC} = 30°C/W
14-Lead CERDIP Package: θ_{JA} = 110°C/W, θ_{JC} = 30°C/W

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD8004 is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately +150°C. Exceeding this limit temporarily may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of +175°C for an extended period can result in device failure.

While the AD8004 is internally short circuit protected, this may not be sufficient to guarantee that the maximum junction temperature is not exceeded under all conditions. To ensure proper operation, it is necessary to observe the maximum power ratings.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8004AN	–40°C to +85°C	14-Lead PDIP	N-14
AD8004AR-14	–40°C to +85°C	14-Lead SOIC	R-14
AD8004AR-14-REEL	–40°C to +85°C	13" Tape and Reel	R-14
AD8004AR-14-REEL7	–40°C to +85°C	7" Tape and Reel	R-14
AD8004SQ	–55°C to +125°C	14-Lead CERDIP	Q-14

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8004 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

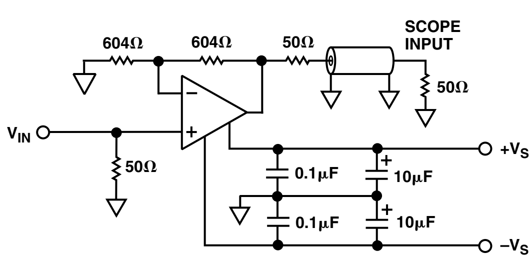


Figure 3. Test Circuit; Gain = –2

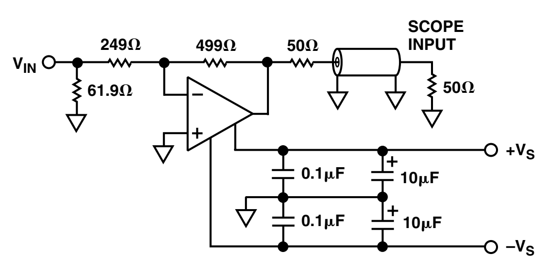
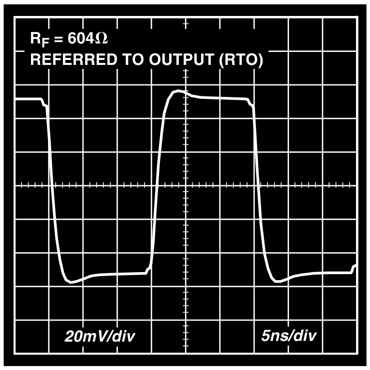
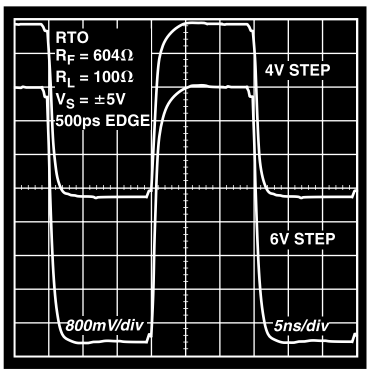


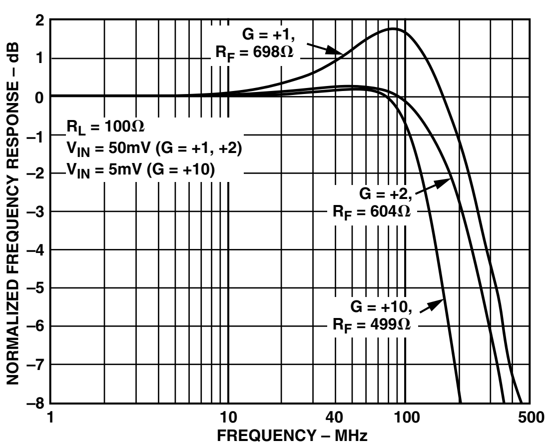
Figure 4. Test Circuit; Gain = –2



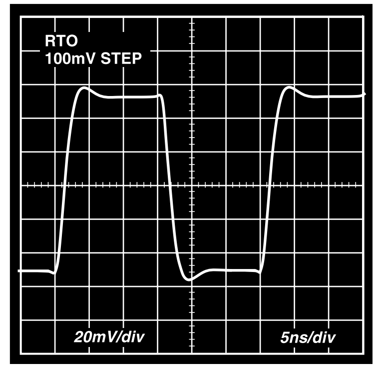
TPC 1.* 100 mV Step Response; G = +2, V_S = ±2.5 V or ±5 V



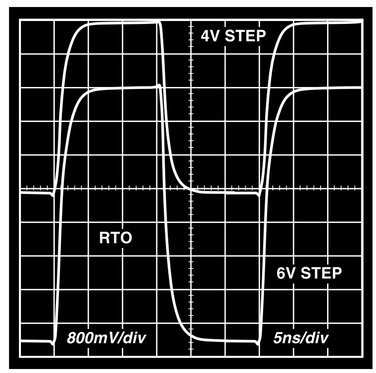
TPC 2.* Step Response; G = +2, V_S = ±5 V



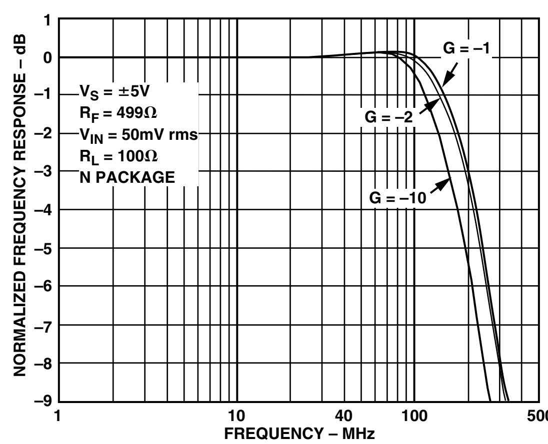
TPC 3. Frequency Response; G = +1, +2, +10; V_S = ±5 V



TPC 4.* 100 mV Step Response; G = –2, V_S = ±2.5 V or ±5 V

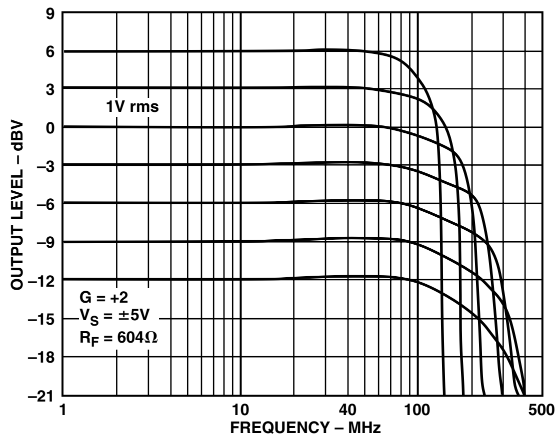


TPC 5.* Step Response; G = –2, V_S = ±5 V

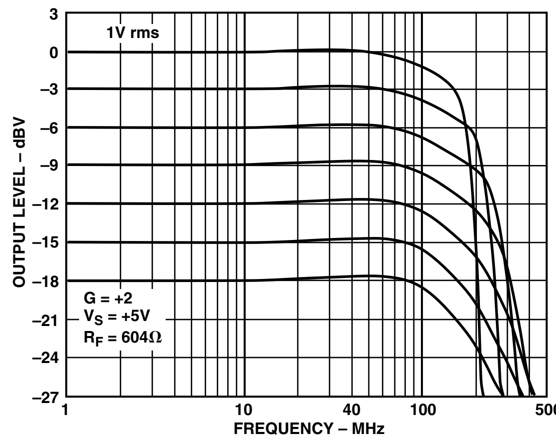


TPC 6. Frequency Response; G = –1, –2, –10

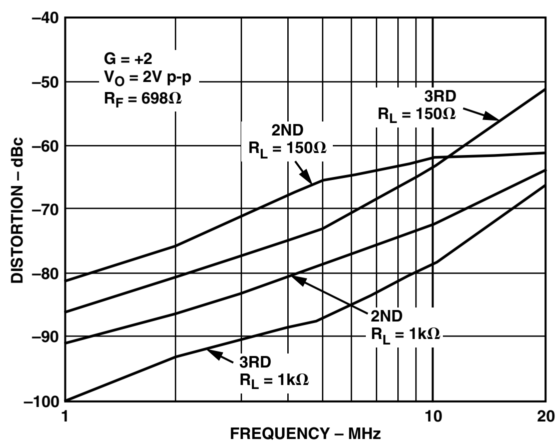
*V_S = ±2.5 V operation is identical to V_S = +5 V single-supply operation.



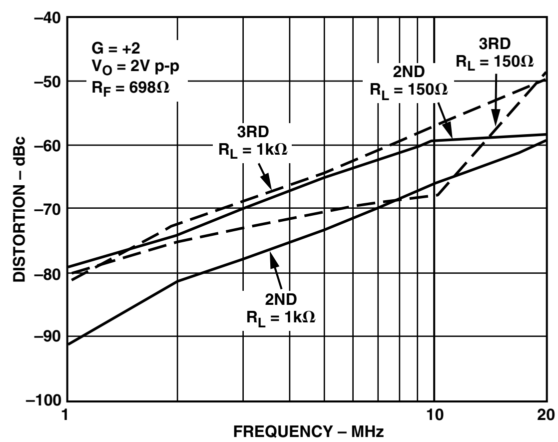
TPC 7. Large Signal Frequency Response; V_S = ±5.0 V, G = +2, R_F = 604 Ω



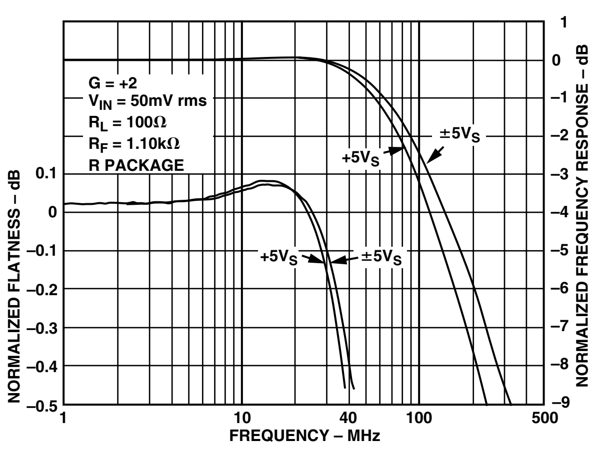
TPC 10. Large Signal Frequency Response; V_S = +5.0 V, G = +2, R_F = 604 Ω



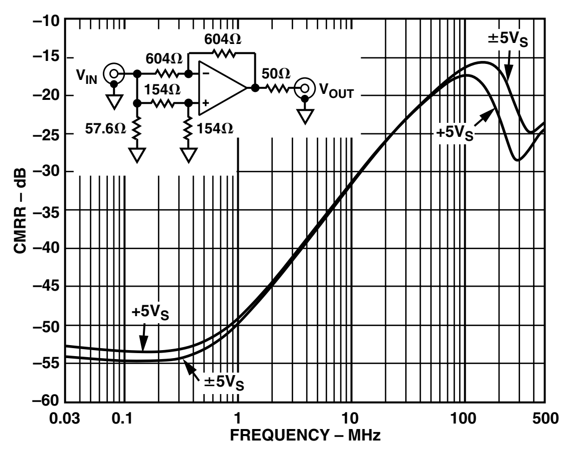
TPC 8. Distortion vs. Frequency; V_S = ±5 V



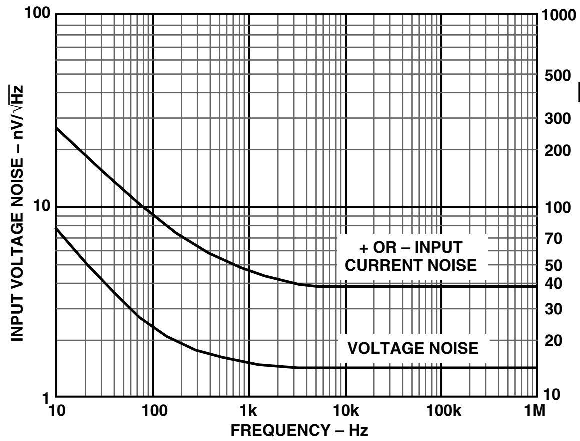
TPC 11. Distortion vs. Frequency; V_S = +5 V



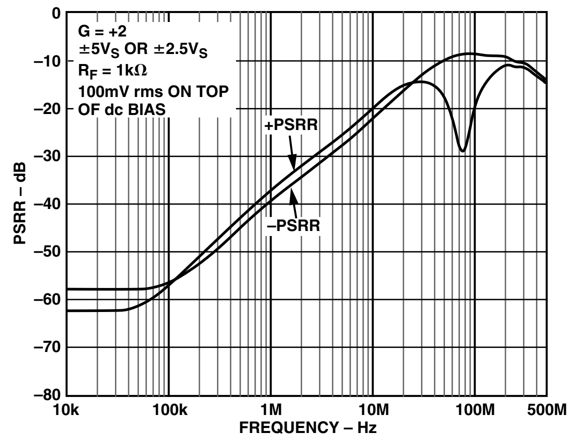
TPC 9. Frequency Response and Flatness, G = +2



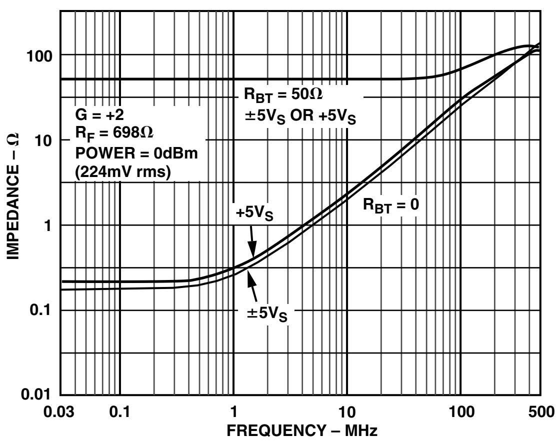
TPC 12. CMRR vs. Frequency; V_S = ±5 V or +5 V, V_{IN} = 200 mV rms, Other Sides Are Equal, RTO



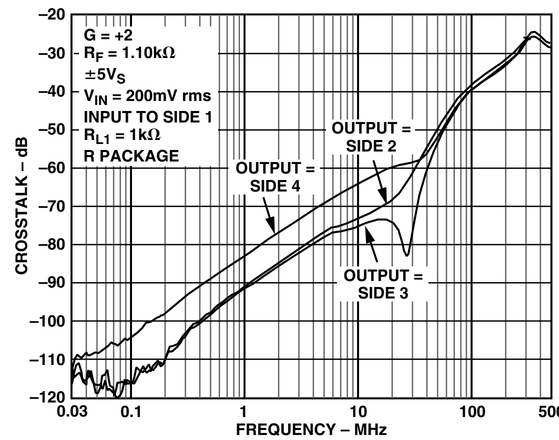
TPC 13. Noise vs. Frequency, V_S = +5 V or ±5 V_S



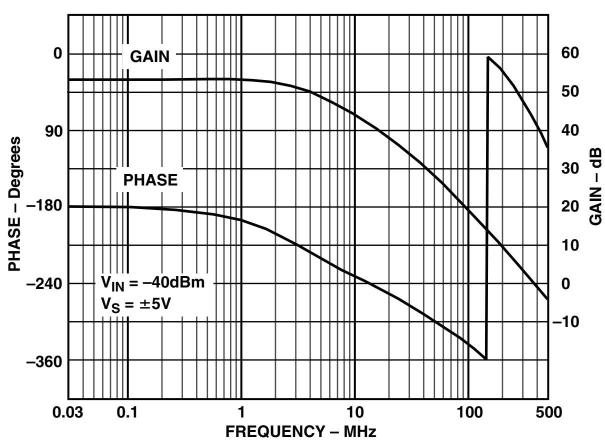
TPC 16. PSRR vs. Frequency



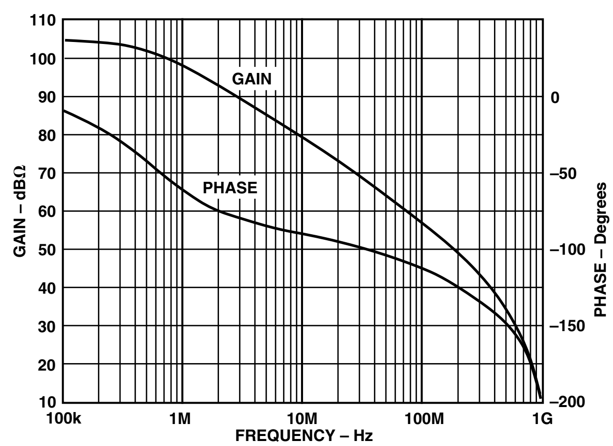
TPC 14. Output Impedance vs. Frequency



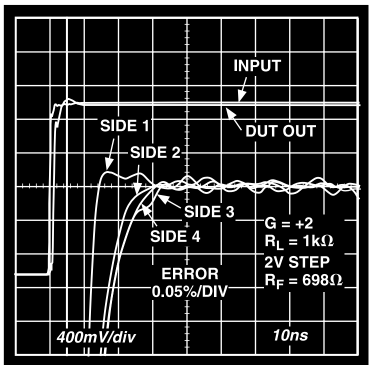
TPC 17. Crosstalk (Output to Output) vs. Frequency



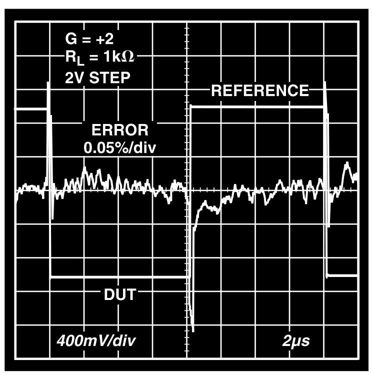
TPC 15. Open-Loop Voltage Gain and Phase



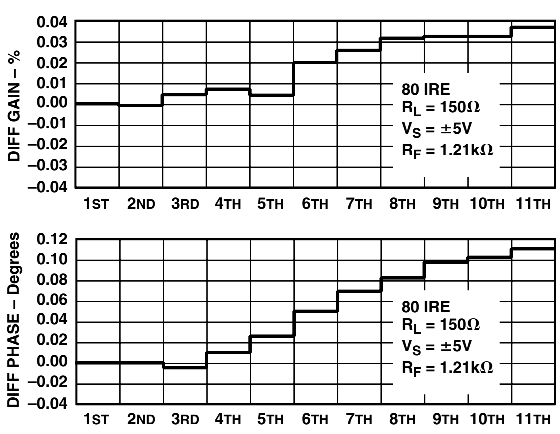
TPC 18. Open-Loop Transimpedance Gain



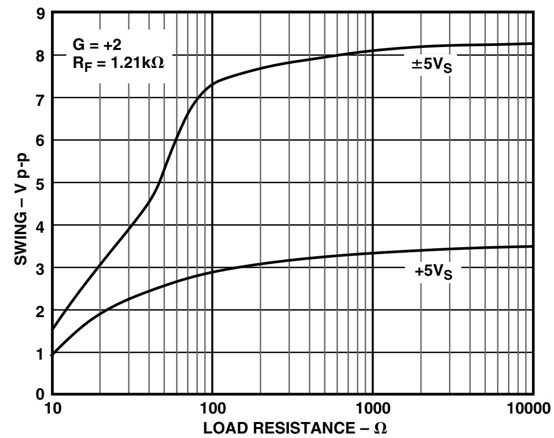
TPC 19. Short-Term Settling Time



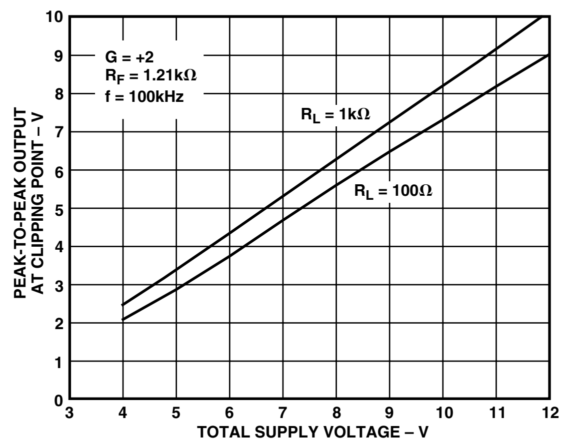
TPC 20. Long-Term Settling Time



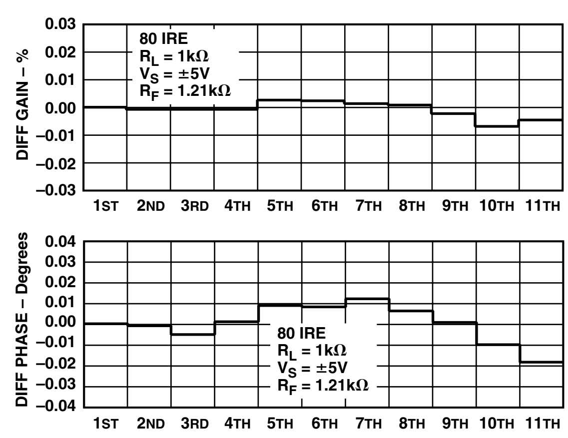
TPC 21. Differential Gain/Differential Phase



TPC 22. Output Voltage Swing vs. Load



TPC 23. Output Swing vs. Supply



TPC 24. Differential Gain/Phase, R_L = 1 kΩ

THEORY OF OPERATION

The AD8004 is a member of a new family of high speed current-feedback (CF) amplifiers offering new levels of bandwidth, distortion, and signal-swing capability vs. power. Its wide dynamic range capabilities are due to both a complementary high speed bipolar process and a new design architecture. The AD8004 is basically a two stage (Figure 30) rather than the conventional one stage design. Both stages feature the current-on-demand property associated with current feedback amplifiers. This gives an unprecedented ratio of quiescent current to dynamic performance. The important properties of slew rate and full power bandwidth benefit from this performance. In addition the second gain stage buffers the effects of load impedance, significantly reducing distortion.

A full discussion of this new amplifier architecture is available on the data sheet for the AD8011. This discussion only covers the basic principles of operation.

DC AND AC CHARACTERISTICS

As with traditional op amp circuits the dc closed-loop gain is defined as:

$$A_V = G = 1 + \frac{R_F}{R_N} \quad \text{noninverting operation}$$

$$A_V = G = -\frac{R_F}{R_N} \quad \text{inverting operation}$$

The more exact relationships that take into account open-loop gain errors are:

$$A_V = \frac{G}{1 + \frac{1-G}{A_O(s)} + \frac{R_F}{T_O(s)}} \quad \text{for inverting (G is negative)}$$

$$A_V = \frac{G}{1 + \frac{G}{A_O(s)} + \frac{R_F}{T_O(s)}} \quad \text{for noninverting (G is positive)}$$

In these equations the open-loop voltage gain ($A_O(s)$) is common to both voltage and current-feedback amplifiers and is the ratio of output voltage to differential input voltage. The open-loop transimpedance gain ($T_O(s)$) is the ratio of output voltage to inverting input current and is applicable to current-feedback amplifiers. The open-loop voltage gain and open-loop transimpedance gain ($T_O(s)$) of the AD8004 are plotted vs. frequency in TPCs 15 and 18. These plots and the basic relationships can be used to predict the first order performance of the AD8004 over frequency. At low closed-loop gains the term ($R_F/T_O(s)$) dominates the frequency response characteristics. This gives the result that bandwidth is constant with gain, a familiar property of current feedback amplifiers.

An R_F of 1 kΩ has been chosen as the nominal value to give optimum frequency response with acceptable peaking at gains of +2/–1. As can be seen from the above relationships, at higher closed-loop gains reducing R_F has the effect of increasing closed-loop bandwidth. Table I gives optimum values for R_F and R_G for a variety of gains.

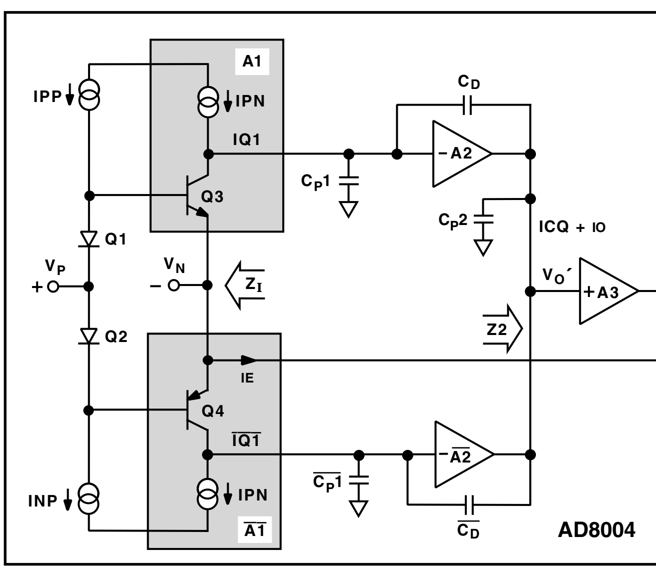


Figure 5. Simplified Block Diagram

DRIVING CAPACITIVE LOADS

The AD8004 was designed primarily to drive nonreactive loads. If driving loads with a capacitive component is desired, best settling response is obtained by the addition of a small series resistance as shown in Figure 6. The accompanying graph shows the optimum value for R_{SERIES} vs. capacitive load. It is worth noting that the frequency response of the circuit when driving large capacitive loads will be dominated by the passive roll-off of R_{SERIES} and C_L.

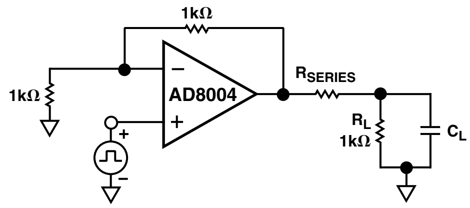


Figure 6. Driving Capacitive Load

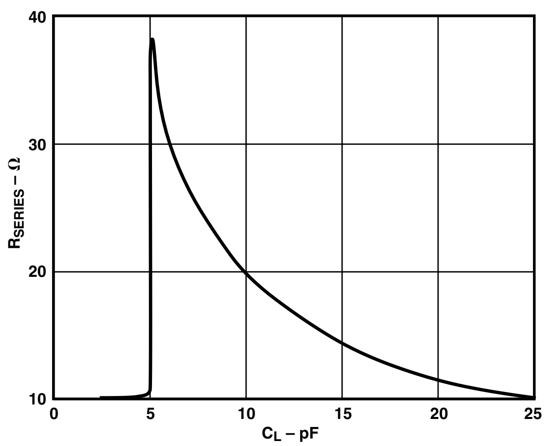


Figure 7. Recommended R_{SERIES} vs. Capacitive Load for ≤ 30 ns Settling to 0.1%

OPTIMIZING FLATNESS

The fine scale gain flatness and –3 dB bandwidth is affected by $R_{FEEDBACK}$ selection as is normal of current feedback amplifiers. With the exception of gain = +1, the AD8004 can be adjusted for either maximal flatness with modest closed-loop bandwidth or for mildly peaked-up frequency response with much more bandwidth. Figure 8 shows the effect of three evenly spaced R_F changes upon gain = +1 and gain = +2. Table I shows the recommended component values for achieving maximally flat frequency response as well as a faster slightly peaked-up frequency response.

Printed circuit board parasitics and device lead frame parasitics also control fine scale gain flatness. The AD8004R package, because of its small lead frame, offers superior parasitics relative to the N package. In the printed circuit board environment, parasitics such as extra capacitance caused by two parallel and vertical flat conductors on opposite PC board sides in the region of the summing junction will cause some bandwidth extension and/or increased peaking. In noninverting gains, the effect of extra capacitance on summing junctions is far more pronounced than with inverting gains. Figure 9 shows an example of this. Note that only 1 pF of added junction capacitance causes about a 70% bandwidth extension and additional peaking on a gain = +2. For an inverting gain = –2, 5 pF of additional summing junction capacitance caused a small 10% bandwidth extension.

Extra output capacitive loading also causes bandwidth extensions and peaking. The effect is more pronounced with less resistive loading from the next stage. Figure 10 shows the effect of direct output capacitive loads for gains of +2 and –2. For both gains C_{LOAD} was set to 10 pF or 0 pF (no extra capacitive loading). For each of the four traces in Figure 10 the resistive loads were 100 Ω. Figure 11 also shows capacitive loading effects with a lighter output resistive load. Note that even though bandwidth is extended 2×, the flatness dramatically suffers.

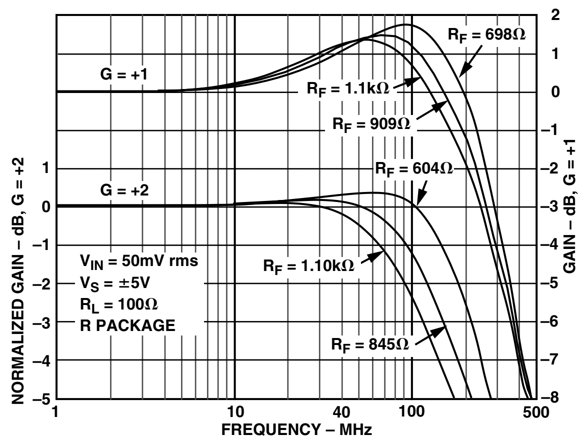


Figure 8. $R_{FEEDBACK}$ vs. Frequency Response, G = +1/+2

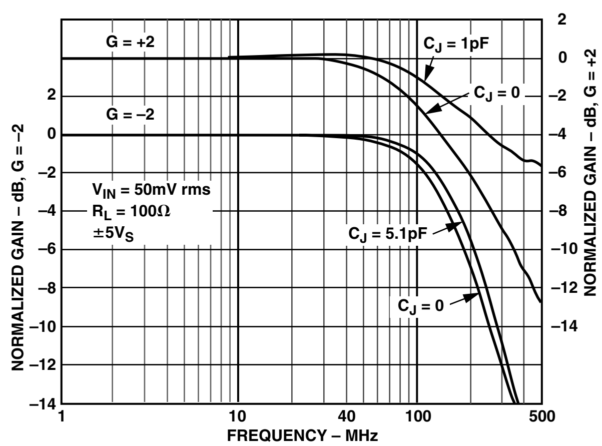


Figure 9. Frequency Response vs. Added Summing Junction Capacitance

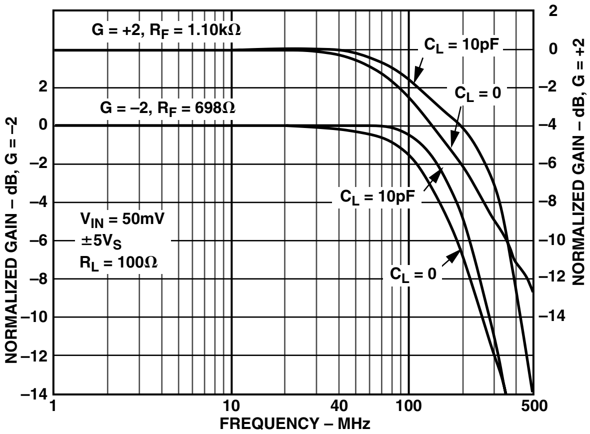


Figure 10. Frequency Response vs. Capacitive Loading, R_L = 100 Ω Output

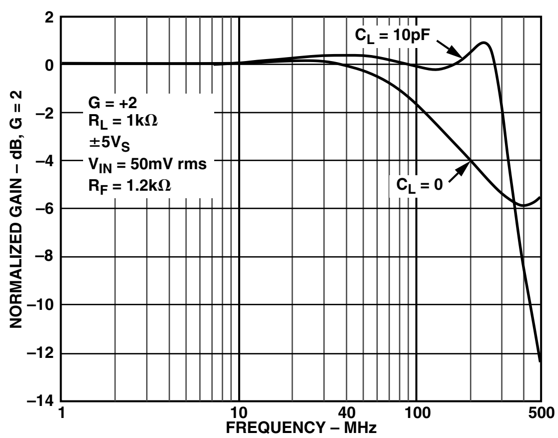


Figure 11. Flatness with 10 pF Capacitive Load

DRIVING A SINGLE-SUPPLY A/D CONVERTER

New CMOS A/D converters are placing greater demands on the amplifiers that drive them. Higher resolutions, faster conversion rates, and input switching irregularities require superior settling characteristics. In addition, these devices run off a single +5 V supply and consume little power, so good single-supply operation with low power consumption is very important. The AD8004 is well positioned for driving this new class of A/D converters.

Figure 12 shows a circuit that uses an AD8004 to drive an AD876, a single supply, 10-bit, 20 MSPS A/D converter that requires only 140 mW. Using the AD8004 for level shifting and driving, the A/D exhibits no degradation in performance compared to when it is driven from a signal generator.

The analog input of the AD876 spans 2 V centered at about 2.6 V. The resistor network and bias voltages provide the level shifting and gain required to convert the 0 V to 1 V input signal to a 3.6 V to 1.6 V range that the AD876 wants to see.

Biasing the noninverting input of the AD8004 at 1.6 V dc forces the inverting input to be at 1.6 V dc for linear operation of the amplifier. When the input is at 0 V, there is 3.2 mA flowing out of the summing junction via R1 (1.6 V/499 Ω). R3 has a current of 1.2 mA flowing into the summing junction (3.6 V – 1.6 V)/ 1.65 kΩ. The difference of these two currents (2 mA) must flow through R2. This current flows toward the summing junction and requires that the output be 2 V higher than the summing junction or at 3.6 V.

When the input is at 1 V, there is 1.2 mA flowing into the summing junction through R3 and 1.2 mA flowing out through R1. These currents balance and leave no current to flow through R2. Thus the output is at the same potential as the inverting input or 1.6 V.

The input of the AD876 has a series MOSFET switch that turns on and off at the sampling rate. This MOSFET is connected to a hold capacitor internal to the device. The on impedance of the MOSFET is about 50 Ω, while the hold capacitor is about 5 pF.

In a worst case condition, the input voltage to the AD876 will change by a full-scale value (2 V) in one sampling cycle. When the input MOSFET turns on, the output of the op amp will be connected to the charged hold capacitor through the series resistance of the MOSFET. Without any other series resistance, the instantaneous current that flows would be 40 mA. This would cause settling problems for the op amp.

The series 100 Ω resistor limits the current that flows instantaneously after the MOSFET turns on to about 13 mA. This resistor cannot be made too large or the high frequency performance will be affected.

The sampling MOSFET of the AD876 is closed for only half of each cycle or for 25 ns. Approximately seven time constants are required for settling to 10 bits. The series 100 Ω resistor along with the 50 Ω on resistance and the hold capacitor, create a 750 ps time constant. These values leave a comfortable margin for settling. Obtaining the same results with the op amp A/D combination as compared to driving with a signal generator indicates that the op amp is settling fast enough.

Overall the AD8004 provides adequate buffering for the AD876 A/D converter without introducing distortion greater than that of the A/D converter by itself.

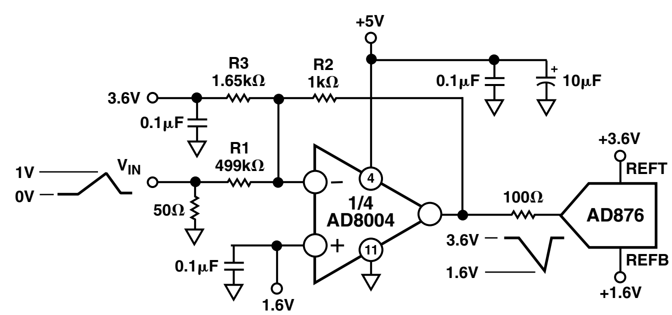


Figure 12. AD8004 Driving the AD876

LAYOUT CONSIDERATIONS

The specified high speed performance of the AD8004 requires careful attention to board layout and component selection. Table I shows the recommended component values for the AD8004 and Figures 14–16 show the layout for the AD8004 evaluation boards (14-lead DIP and SOIC). Proper R_F design techniques and low parasitic component selection are mandatory.

The PCB should have a ground plane covering all unused portions of the component side of the board to provide a low impedance ground path. The ground plane should be removed from the area near the input pins to reduce stray capacitance.

Chip capacitors should be used for supply bypassing (see Figure 13). One end should be connected to the ground plane and the other within 1/8" of each power pin. An additional (4.7 µF to 10 µF) tantalum electrolytic capacitor should be connected in parallel.

The feedback resistor should be located close to the inverting input pin in order to keep the stray capacitance at this node to a minimum. Capacitance greater than 1 pF at the inverting input will significantly affect high speed performance when operating at low noninverting gains. An example of extra inverting input capacitance can be seen on the plot of Figure 10.

Stripline design techniques should be used for long signal traces (greater than about 1"). These should be designed with the proper system characteristic impedance and be properly terminated at each end.

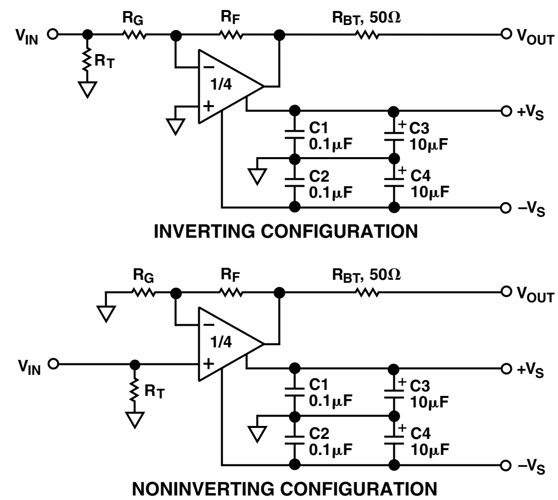
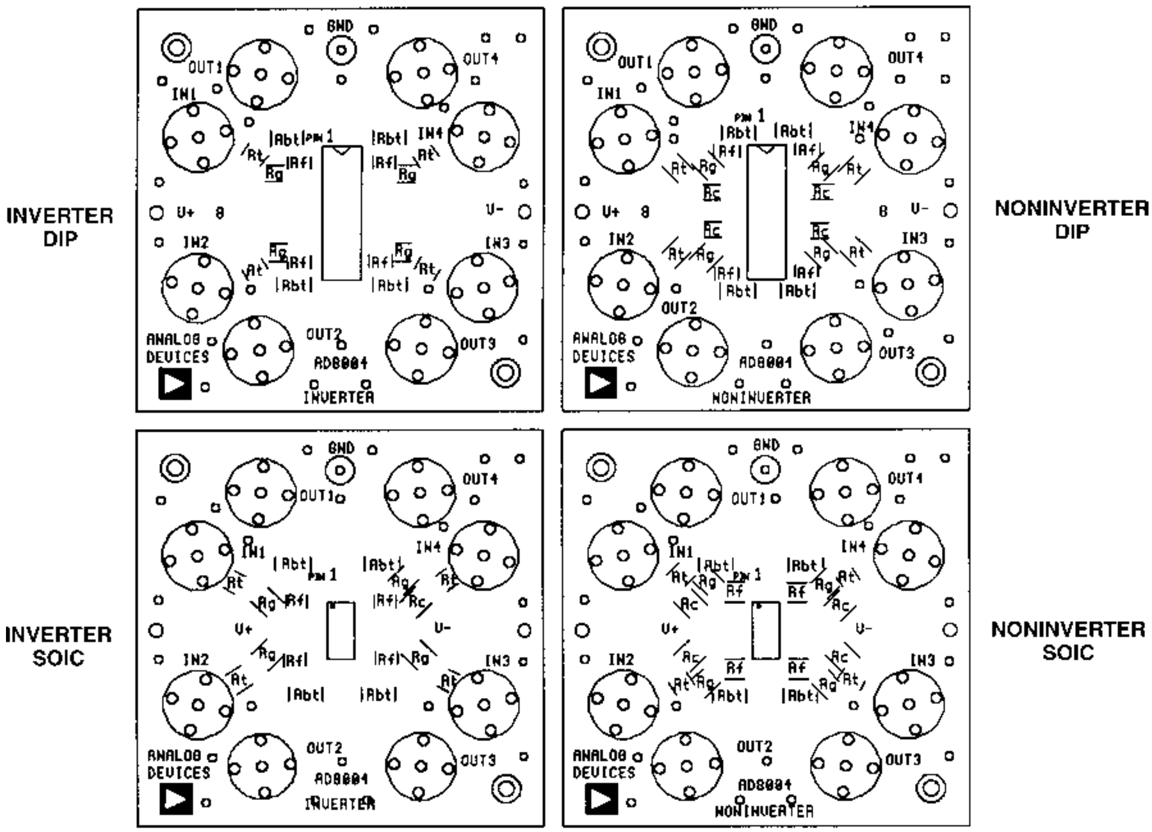


Figure 13. Inverting and Noninverting Configurations

Table I. Recommended Component Values[1] and Typical Bandwidths

Gain	–10	–2	Alternate –2	–1	Alternate –1	+1	Alternate +1	+2	Alternate +2	+10
AD8004 (DIP) PACKAGE TYPE										
R_F (Ω)	499	698	499	649	499	1.21 k	806	1.10 k	698	499
R_G (Ω)	49.9	348	249	649	499			1.10 k	698	54.9
R_T[2] (Ω)	None	57.6	61.9	53.6	54.9	50	50	50	50	50
Small Signal BW @ ±5 V_S (MHz)	155	125	180	135	190	150	250	115	185	135
Peaking @ ±5 V_S	< 0.3 dB	None	0.3 dB	None	0.3 dB	1.3 dB	1.7 dB	< 0.14 dB	0.4 dB	< 0.3 dB
0.1 dB Flatness @ ±5 V_S (MHz)		25		30				35		
Small Signal BW @ +5 V_S (MHz)	135	105	155	120	160	130	200	95	150	120
AD8004 (SOIC) PACKAGE TYPE										
R_F (Ω)	499	698	499	750	499	1.10 k	698	1.10 k	604	499
R_G (Ω)	49.9	348	249	750	499			1.10 k	604	54.9
R_T[2] (Ω)	None	57.6	61.9	53.6	54.9	50	50	50	50	50
Small Signal BW @ ±5 V_S (MHz)	155	130	190	125	195	150	225	110	175	135
Peaking @ ±5 V_S	< 0.7 dB	< 0.1 dB	0.5 dB	None	0.4 dB	1.3 dB	1.8 dB	< 0.1 dB	0.5 dB	< 0.2 dB
0.1 dB Flatness @ ±5 V_S (MHz)		35		25				30		
Small Signal BW @ +5 V_S (MHz)	135	115	175	110	165	130	195	95	155	120

NOTES
[1]Resistor values listed are standard 1% tolerance.
[2]R_T chosen for 50 Ω characteristic input impedance.



NOTES:

1. R_T (INPUT TERMINATION RESISTOR) IS MOUNTED ON BOARD BOTTOMS.
2. R_C (IN SERIES WITH INPUT) IS A SHORT ON AD8004.
3. BYPASS CHIP CAPACITORS ARE MOUNTED ON BOARD BOTTOM WITH 0.1μF BEING CLOSEST TO SUPPLY PINS.
4. ON BOTH INVERTER BOARDS R_G, R_F AND R_{BT} ARE MOUNTED ON BOARD TOP.
5. ON NONINVERTER DIP BOARDS, R_F AND R_{BT} ARE ON BOARD TOP WHILE R_G IS ON BOTTOM. ON NONINVERTER SOIC BOARD, R_{BT} IS ON TOP WHILE R_F AND R_G ARE ON BOARD BOTTOM.

Figure 14. Evaluation Board Silkscreen (Top)

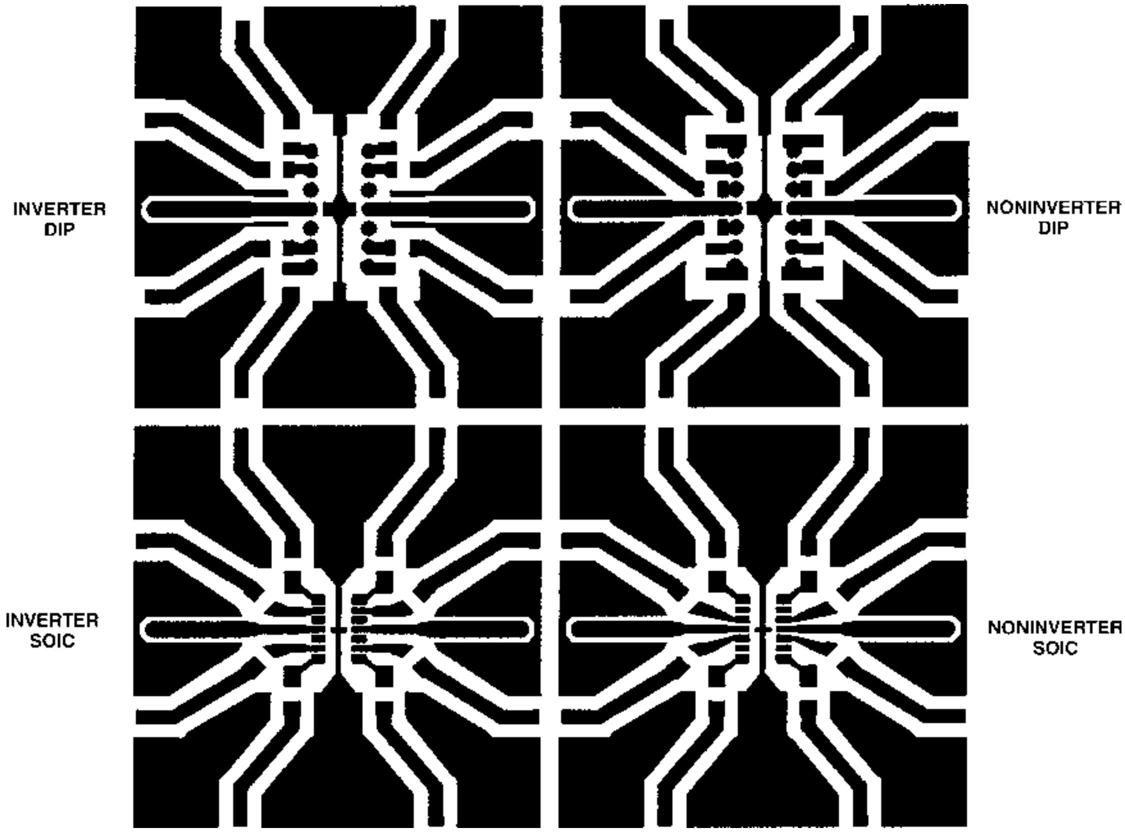


Figure 15 Evaluation Board Layout (Top Side)

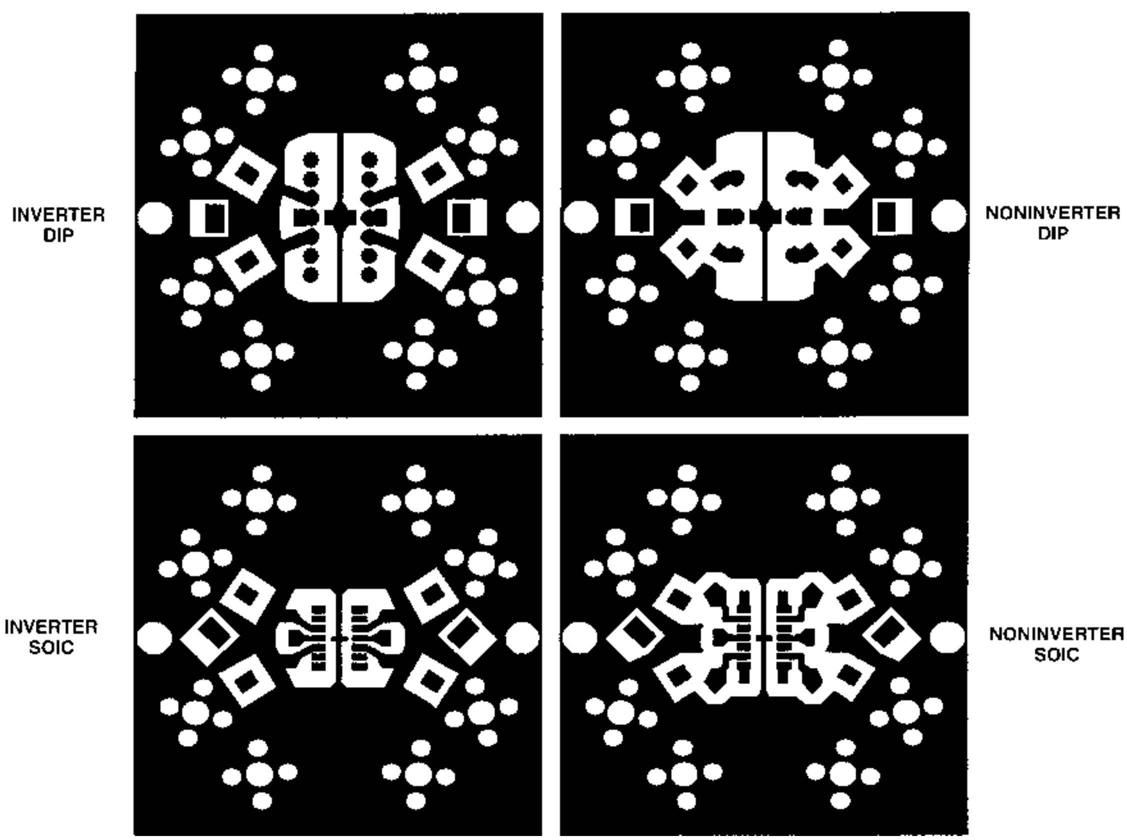
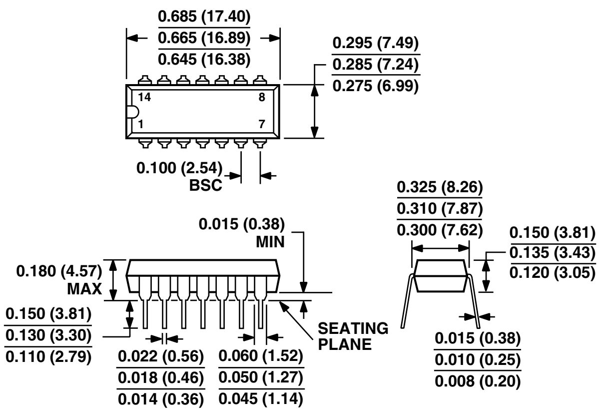


Figure 16. Evaluation Board Layout (Bottom Side, Looking Through the Board)

OUTLINE DIMENSIONS

14-Lead Plastic Dual In-Line Package [PDIP] (N-14)

Dimensions shown in inches and (millimeters)



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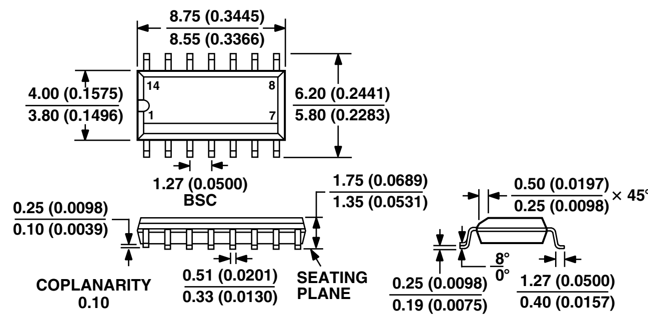
14-Lead Standard Small Outline Package [SOIC] (R-14)

Dimensions shown in millimeters and (inches)



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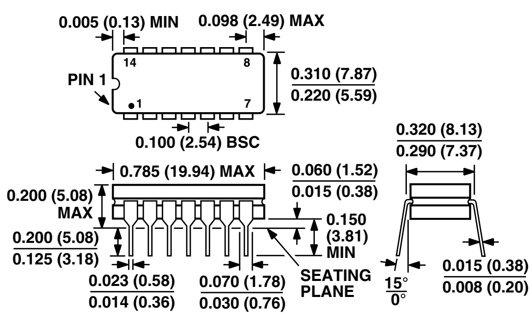
14-Lead Ceramic Dual In-Line Package [CERDIP] (Q-14)

Dimensions shown in inches and (millimeters)



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Revision History

Location	Page
3/03—Data Sheet changed from REV. B to REV. C.	
Updated format	Universal
Added CERDIP (Q) Package	1
Added text to GENERAL DESCRIPTION	1
Changes to SPECIFICATIONS	2
Changes to ABSOLUTE MAXIMUM RATINGS	4
Changes to ORDERING GUIDE	4
Edited MAXIMUM POWER DISSIPATION section	4
Deleted Figure 3	4
Edited Y axis of TPC 13	7
Edited OPTIMIZING FLATNESS section	10
Edits to Figure 13	12
Changes to Table I	12
Updated OUTLINE DIMENSIONS	15

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