

DPDT USB 2.0 High-Speed (480Mbps) and Mobile High-Definition Link (MHL) Switch

Check for Samples: [TS3USB3000](#)

FEATURES

- V_{CC} Range 2.7V to 4.3V
- Mobile Hi-definition Link (MHL) Switch
 - Bandwidth (-3dB) 6.1 GHz
 - Ron (Typ) 5.7 Ω
 - Con (Typ) 1.6 pF
- USB Switch
 - Bandwidth (-3dB) 6.1 GHz
 - Ron (Typ) 4.6 Ω
 - Con (Typ) 1.4 pF
- Current Consumption 30 μ A Typ
- Special Features
 - I_{OFF} Protection Prevents Current Leakage in Powered Down State (V_{CC} and $V_{BUS} = 0$ V)
 - 1.8-V Compatible Control Inputs (SEL, \overline{OE})
 - Over-Voltage Tolerance (OVT) on all I/O Pins up to 5.5V Without External Components
- ESD Performance
 - 3.5 kV Human Body Model (A114B, Class II)
 - 1 kV Charged Device Model (C101)
- 10-pin QFN Package (2.0x1.5 mm, 0.5 mm Pitch)

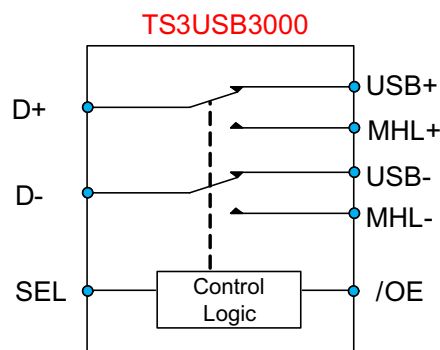
DESCRIPTION

The TS3USB3000 is a double-pole, double throw (DPDT) multiplexer that includes a high speed Mobile High-Definition Link (MHL) switch and an USB 2.0 High-Speed (480Mbps) switches in the same package. These configurations allow the system designer to use a common USB or Mico-USB connector for both MHL video signals and USB data.

The TS3USB3000 has a V_{CC} range of 2.7V to 4.3V and supports over-voltage tolerance (OVT) feature, which allows the I/O pins to withstand over-voltage conditions (up to 5.5V). The power-off protection feature forces all I/O pins to be in high impedance mode when power is not present, allowing full isolation of the signals lines under such condition without excessive leakage current. The select pins of TS3USB3000 are compatible with 1.8V control voltage, allowing them to be directly interfaced with the General Purpose I/O (GPIO) from a mobile processor.

The TS3USB3000 comes with a small 10-pin QFN package with only 2.0mm x 1.5mm is size, which makes it a perfect candidate to be used in mobile applications.

SWITCH DIAGRAM



ORDERING INFORMATION

T_A	PACKAGE		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	QFN- RSE	Tape and reel	TS3USB3000RSER	DSJ

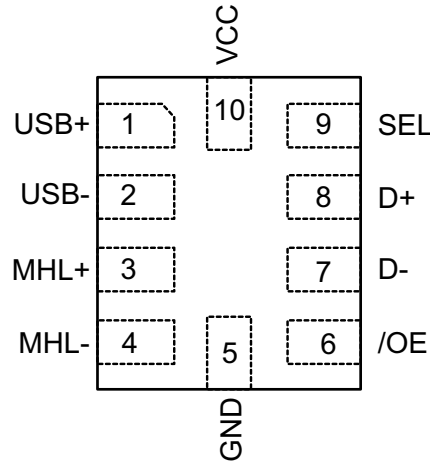


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

PIN DESCRIPTION



Pin Description Table

PIN			DESCRIPTION
NO.	NAME	TYPE	
1	USB+	I/O	USB Data (Differential +)
2	USB-	I/O	USB Data (Differential -)
3	MHL+	I/O	MHL Data (Differential +)
4	MHL-	I/O	MHL Data (Differential -)
5	GND	Ground	Ground
6	\overline{OE}	Input	Output Enable (Active Low)
7	D-	I/O	Data Switch Output (Differential -)
8	D+	I/O	Data Switch Output (Differential +)
9	SEL	Input	Output Select
10	VCC	Power	Supply

FUNCTION TABLE

SEL	\overline{OE}	SWITCH STATUS
X	High	Both USB and MHL switches in High-Z
Low	Low	D+/D- to USB+/USB-
High	Low	D+/D- to MHL+/MHL-

SUMMARY OF TYPICAL CHARACTERISTICS

	MHL PATH	USB PATH
Number of switches	2	2
ON-state resistance (r_{on})	5.7 Ω	4.6 Ω
ON-state resistance match (Δr_{on})	<0.1 Ω	<0.1 Ω
ON-state capacitance ($C_{I/O,on}$)	1.6 pF	1.4 pF
Bandwidth (BW)	6.1 GHz	6.1 GHz

TYPICAL APPLICATION

Figure 1 represents a typical application of the TS3USB3000 MHL switch. The TS3USB3000 is used to switch signals between the USB path, which goes to the baseband or application processor, or the MHL path, which goes to the HDMI to MHL bridge. The TS3USB3000 has internal 6MΩ pull-down resistors on SEL and OE. The pull-down on SEL ensure the USB channel is selected by default. The pull-down on OE enables the switch when power is applied. The TS5A3157 is a separate SPDT switch that is used to switch between MHL's CBUS and the USB ID line that is needed for USB OTG (USB On-The-Go) application.

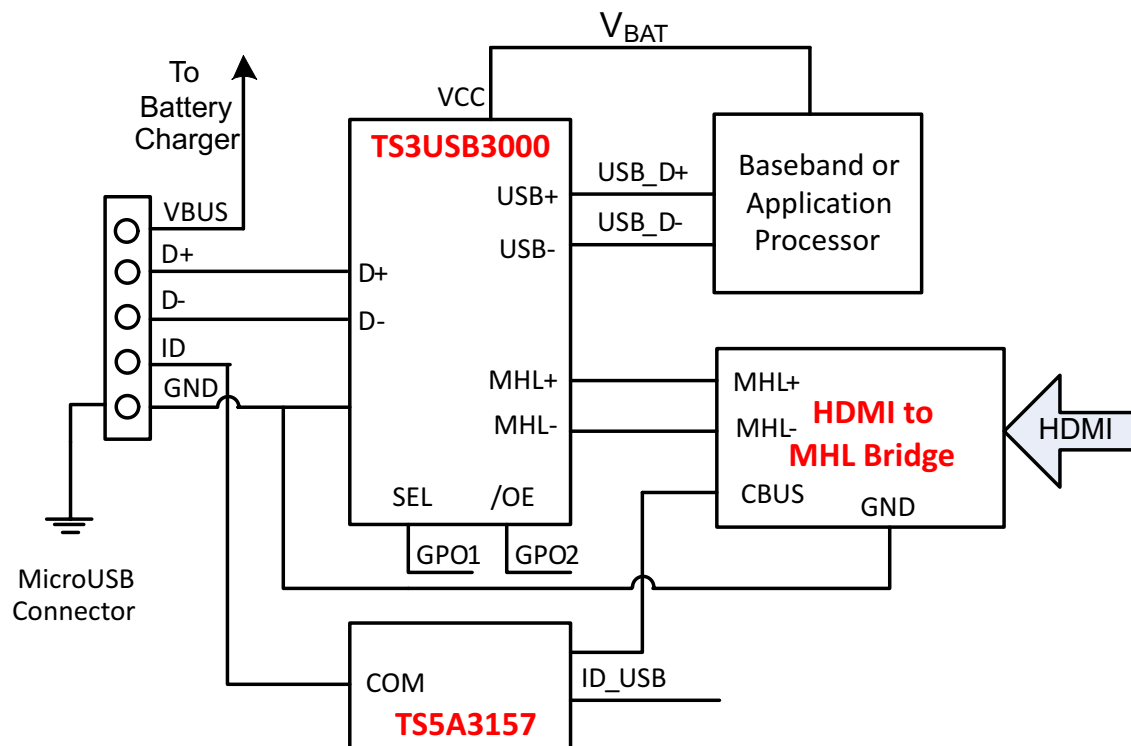


Figure 1. Typical TS3USB3000 Application

ABSOLUTE MAXIMUM RATINGS⁽¹⁾⁽²⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range ⁽³⁾	-0.3	5.5	V
$V_{I/O}$	Input/Output DC voltage range ⁽³⁾	-0.3	5.5	V
I_K	Input/Output port diode current	$V_{I/O} < 0$		mA
V_I	Digital input voltage range (SEL, /OE)	-0.3	5.5	V
I_{IK}	Digital logic input clamp current ⁽³⁾	$V_I < 0$		mA
I_{CC}	Continuous current through VCC		100	mA
I_{GND}	Continuous current through GND	-100		mA
T_{stg}	Storage temperature range	-65	150	°C

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
- (2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
- (3) All voltages are with respect to ground, unless otherwise specified.

PACKAGE THERMAL IMPEDANCE⁽¹⁾

		TYP	UNIT
θ_{JA}	Package thermal impedance	243	°C/W

- (1) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	2.7	4.3	V
$V_{I/O (USB)}$	Analog voltage range	0	3.6	V
$V_{I/O (MHL)}$				
V_I	Digital input voltage range (SEL, \overline{OE})	0	V_{CC}	V
$T_{RAMP (V_{CC})}$	Power supply ramp time requirement (V_{CC})	100	1000	$\mu s/V$
T_A	Operating free-air temperature	-40	85	°C

ELECTRICAL CHARACTERISTICS
 $T_A = -40^{\circ}\text{C}$ to 85°C , Typical values are at $V_{CC} = 3.3\text{V}$, $T_A = 25^{\circ}\text{C}$, (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
MHL SWITCH							
R_{ON}	ON-state resistance	$V_{CC} = 2.7\text{V}$	$V_{I/O} = 1.65\text{V}$, $I_{ON} = -8\text{mA}$	5.7	9.0		Ω
ΔR_{ON}	ON-state resistance match between + and – paths	$V_{CC} = 2.7\text{V}$	$V_{I/O} = 1.65\text{V}$, $I_{ON} = -8\text{mA}$	0.1			Ω
$R_{ON (FLAT)}$	ON-state resistance flatness	$V_{CC} = 2.7\text{V}$	$V_{I/O} = 1.65\text{V}$ to 3.45V , $I_{ON} = -8\text{mA}$	1			Ω
I_{OZ}	OFF leakage current	$V_{CC} = 4.3\text{V}$	Switch OFF, $V_{MHL+/MHL-} = 1.65\text{V}$ to 3.45V , $V_{D+/D-} = 0\text{V}$	-2		2	μA
I_{OFF}	Power-off leakage current	$V_{CC} = 0\text{V}$	Switch ON or OFF, $V_{MHL+/MHL-} = 1.65\text{V}$ to 3.45V , $V_{D+/D-} = \text{NC}$	-10		10	μA
I_{ON}	ON leakage current	$V_{CC} = 4.3\text{V}$	Switch ON, $V_{MHL+/MHL-} = 1.65\text{V}$ to 3.45V , $V_{D+/D-} = \text{NC}$	-2		2	μA
USB SWITCH							
R_{ON}	ON-state resistance	$V_{CC} = 2.7\text{V}$	$V_{I/O} = 0.4\text{V}$, $I_{ON} = -8\text{mA}$	4.6	7.5		Ω
ΔR_{ON}	ON-state resistance match between + and – paths	$V_{CC} = 2.7\text{V}$	$V_{I/O} = 0.4\text{V}$, $I_{ON} = -8\text{mA}$	0.1			Ω
$R_{ON (FLAT)}$	ON-state resistance flatness	$V_{CC} = 2.7\text{V}$	$V_{I/O} = 0\text{V}$ to 0.4V , $I_{ON} = -8\text{mA}$	1			Ω
I_{OZ}	OFF leakage current	$V_{CC} = 4.3\text{V}$	Switch OFF, $V_{USB+/USB-} = 0\text{V}$ to 3.6V , $V_{D+/D-} = 0\text{V}$	-2		2	μA
I_{OFF}	Power-off leakage current	$V_{CC} = 0\text{V}$	Switch ON or OFF, $V_{USB+/USB-} = 0\text{V}$ to 3.6V , $V_{D+/D-} = \text{NC}$	-10		10	μA
I_{ON}	ON leakage current	$V_{CC} = 4.3\text{V}$	Switch ON, $V_{USB+/USB-} = 0\text{V}$ to 3.6V , $V_{D+/D-} = \text{NC}$	-2		2	μA
DIGITAL CONTROL INPUTS (SEL, \overline{OE})							
V_{IH}	Input logic high	$V_{CC} = 2.7\text{V}$ to 4.3V		1.3			V
V_{IL}	Input logic low	$V_{CC} = 2.7\text{V}$ to 4.3V				0.6	V
I_{IN}	Input leakage current	$V_{CC} = 4.3\text{V}$, $V_{I/O} = 0\text{V}$ to 3.6V , $V_{IN} = 0$ to 4.3V		-10		10	μA

DYNAMIC CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
t_{pd}	Propagation Delay				100		ps	
t_{ON}	Turn-on time (SEL to Output)					400	ns	
t_{OFF}	Turn-off time (SEL to Output)					400	ns	
$t_{ZH, ZL (MHL)}$	MHL Enable Time (\overline{OE} to Output)	$V_{IO} = 3.3 \text{ V or } 0 \text{ V}$	$R_L = 50 \Omega,$ $C_L = 5 \text{ pF},$ $V_{CC} = 2.7 \text{ V to } 4.3 \text{ V}$		100		μs	
$t_{HZ, LZ (MHL)}$	MHL Disable Time (\overline{OE} to Output)				200		ns	
$t_{ZH, ZL (USB)}$	USB Enable Time (\overline{OE} to Output)	$V_{IO} = 0.8 \text{ V or } 0 \text{ V}$			100		μs	
$t_{HZ, LZ (USB)}$	USB Disable Time (\overline{OE} to Output)				200		ns	
$t_{SK(P)}$	Skew of opposite transitions of same output					20		ps
$C_{ON(MHL)}$	MHL path ON capacitance	$V_{CC} = 3.3 \text{ V}, V_{IO} = 0 \text{ or } 3.3 \text{ V},$ $f = 240 \text{ MHz}$		Switch ON		1.6	2.0	pF
$C_{ON(USB)}$	USB path ON capacitance		Switch ON		1.4	2.0	pF	
$C_{OFF(MHL)}$	MHL path OFF capacitance	$V_{CC} = 3.3 \text{ V}, V_{IO} = 0 \text{ or } 3.3 \text{ V},$ $f = 240 \text{ MHz}$	Switch OFF		1.4	2.0	pF	
$C_{OFF(USB)}$	USB path OFF capacitance		Switch OFF		1.6	2.0	pF	
C_I	Digital input capacitance	$V_{CC} = 3.3 \text{ V}, V_I = 0 \text{ or } 2 \text{ V}$			2.2		pF	
O_{ISO}	OFF Isolation	$V_{CC} = 2.7 \text{ V to } 4.3 \text{ V}, R_L = 50 \Omega,$ $f = 240 \text{ MHz}$	Switch OFF		-34		dB	
X_{TALK}	Crosstalk	$V_{CC} = 2.7 \text{ V to } 4.3 \text{ V}, R_L = 50 \Omega,$ $f = 240 \text{ MHz}$	Switch ON		-37		dB	
$B_{W(MHL)}$	MHL path -3dB bandwidth	$V_{CC} = 2.7 \text{ V to } 4.3 \text{ V}, R_L = 50 \Omega,$ $f = 240 \text{ MHz}$	Switch ON		6.1		GHz	
$B_{W(USB)}$	USB path -3dB bandwidth	$V_{CC} = 2.7 \text{ V to } 4.3 \text{ V}, R_L = 50 \Omega,$	Switch ON		6.1		GHz	
SUPPLY								
V_{CC}	Power supply voltage			2.7		4.3	V	
I_{CC}	Positive supply current	$V_{CC} = 4.3 \text{ V}, V_{IN} = V_{CC} \text{ or } \text{GND}, V_{IO} = 0 \text{ V},$ Switch ON or OFF			30	50	μA	
$I_{cc, HZ}$	Power supply current in high-Z mode	$V_{CC} = 4.3 \text{ V}, V_{IN} = V_{CC} \text{ or } \text{GND}, V_{IO} = 0 \text{ V},$ Switch ON or OFF, $\overline{OE} = \text{H}$			5	10	μA	

PARAMETER MEASUREMENT INFORMATION

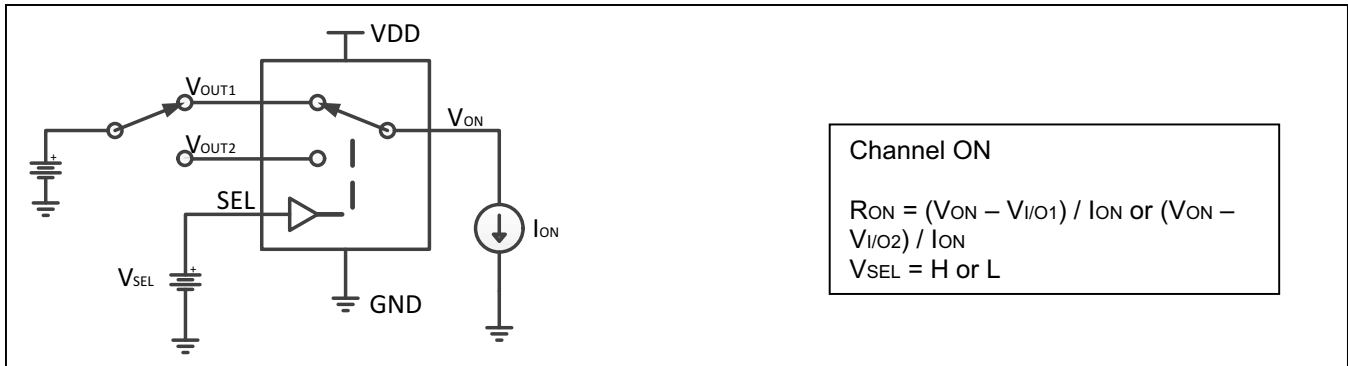


Figure 2. ON State Resistance (R_{ON})

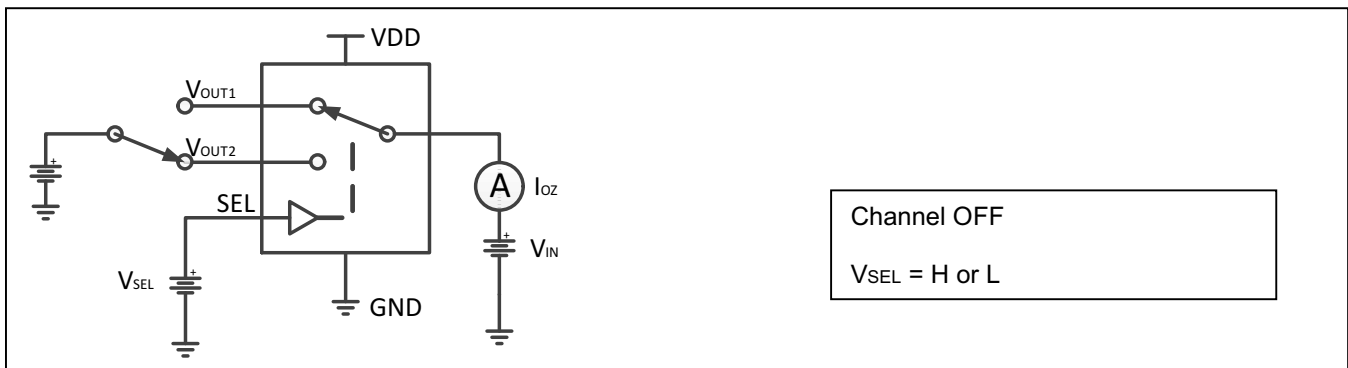


Figure 3. OFF Leakage Current (I_{OZ})

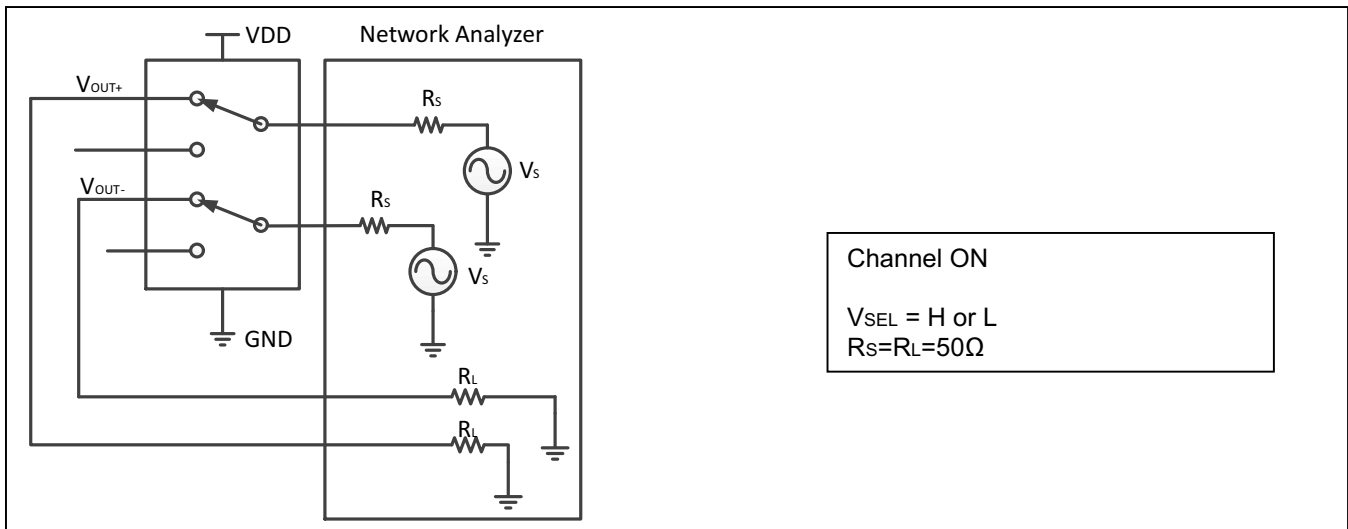


Figure 4. Bandwidth (BW)

TYPICAL CHARACTERISTICS

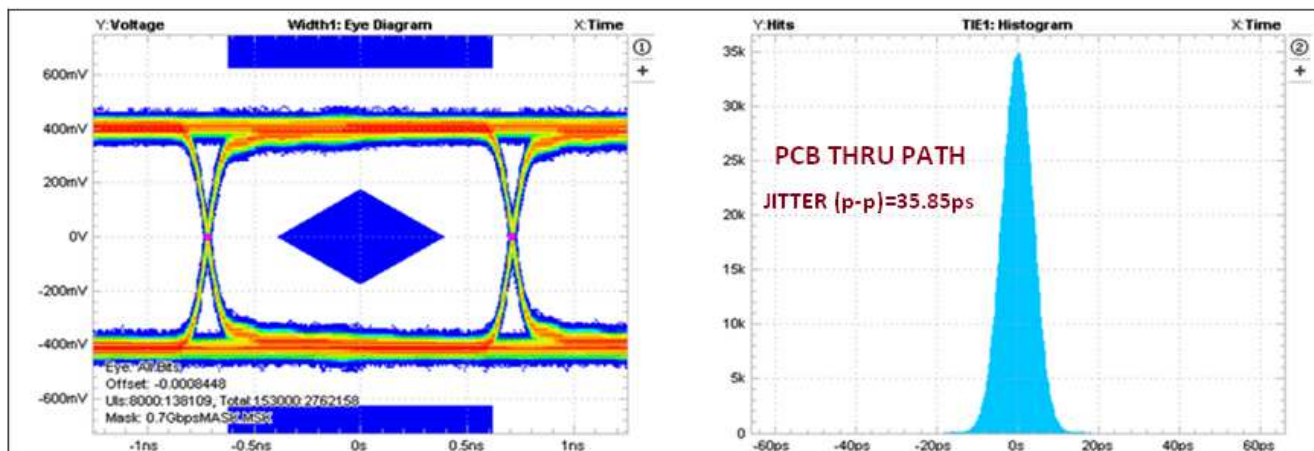
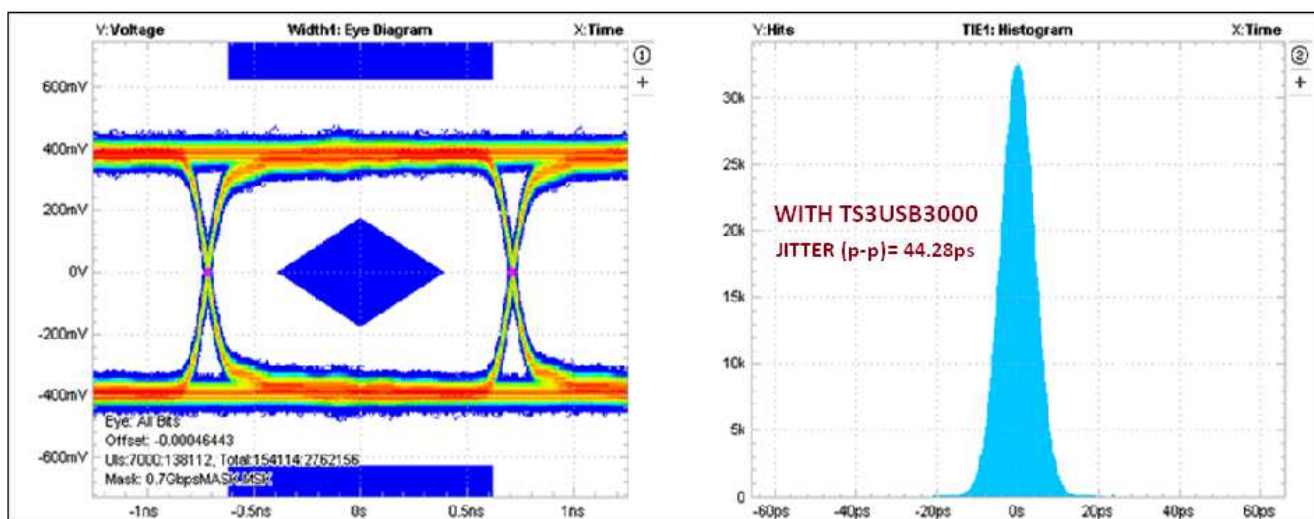


Figure 5. Eye Pattern and Time Interval Error Histogram: 0.7 Gbps With No Device



The TS3USB3000 contributes only 8.4ps of peak-to-peak jitter for 0.7 Gbps data rate.

Figure 6. Eye Pattern and Time Interval Error Histogram: 0.7 Gbps for MHL Switch

TYPICAL CHARACTERISTICS (continued)

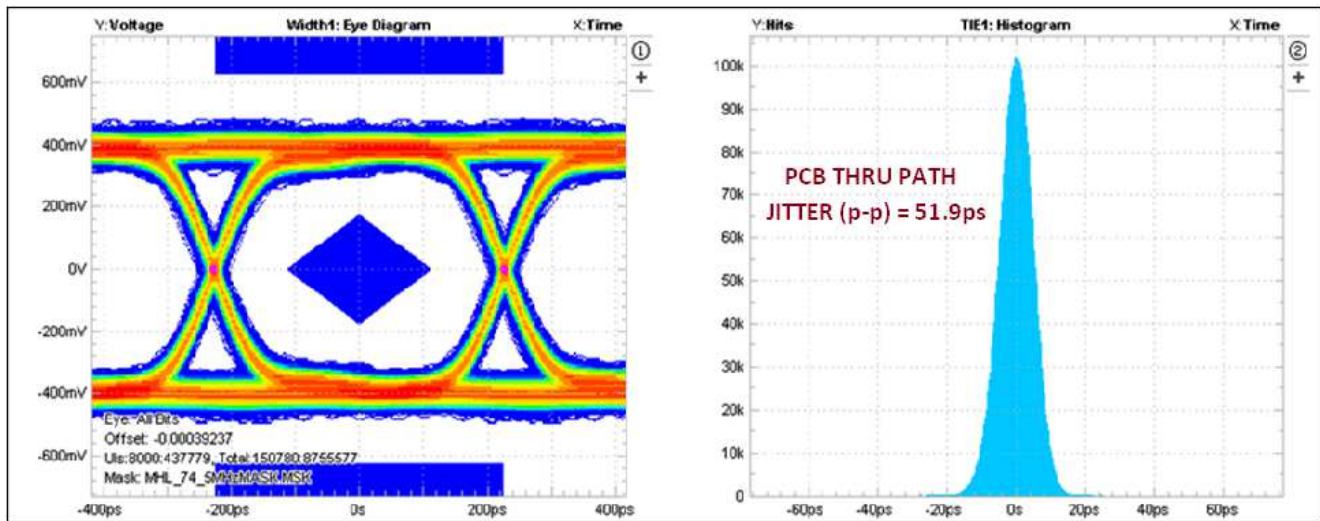
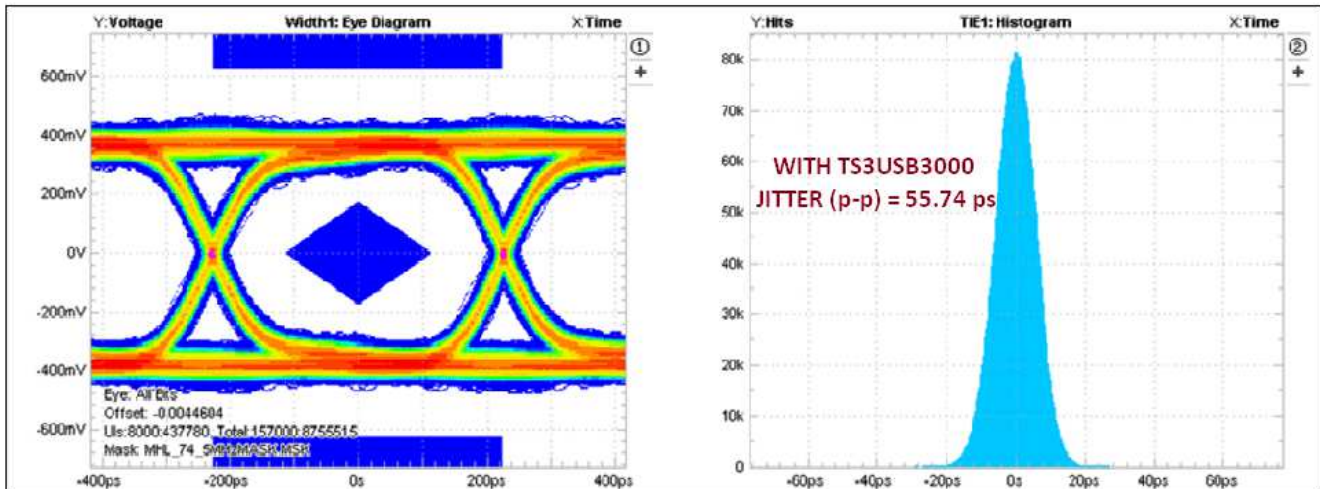


Figure 7. Eye Pattern and Time Interval Error Histogram: 2.2 Gbps With No Device



The TS3USB3000 contributes only 3.8ps of peak-to-peak jitter for 2.2 Gbps data rate.

Figure 8. Eye Pattern and Time Interval Error Histogram: 2.2 Gbps for MHL Switch

TYPICAL CHARACTERISTICS (continued)

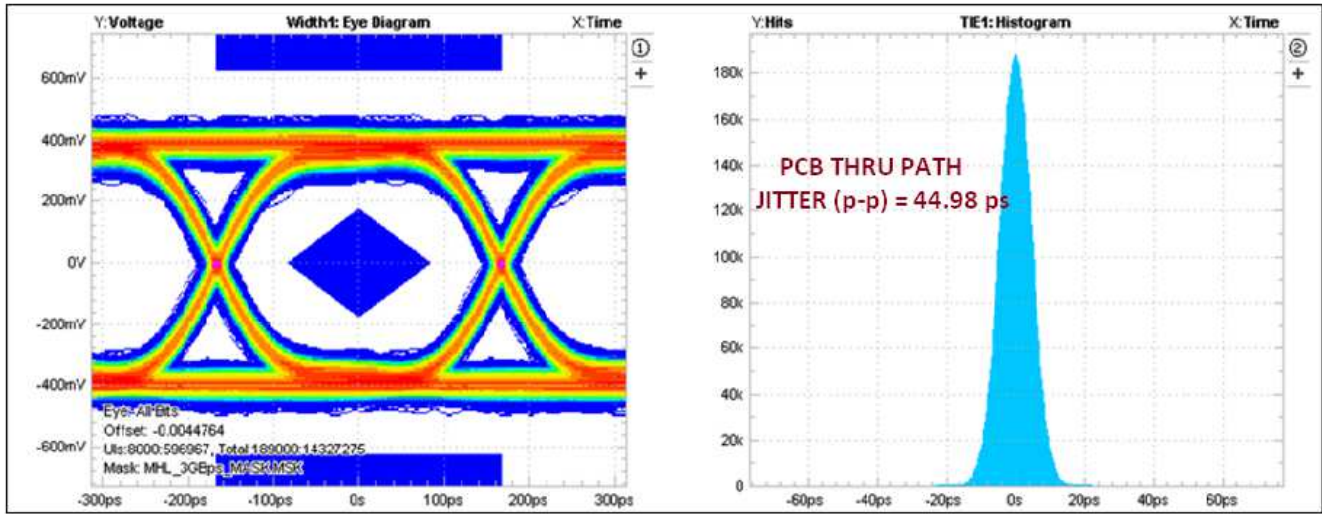
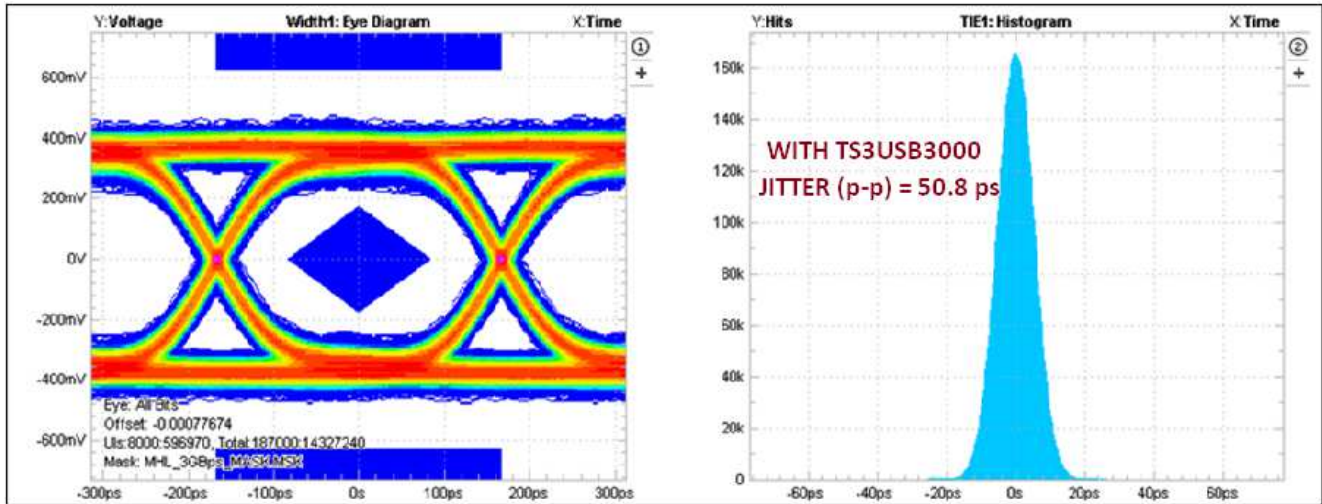


Figure 9. Eye Pattern and Time Interval Error Histogram: 3.0 Gbps With No Device



The TS3USB3000 contributes only 5.8ps of peak-to-peak jitter for 3.0 Gbps data rate.

Figure 10. Eye Pattern and Time Interval Error Histogram: 3.0 Gbps for MHL Switch

TYPICAL CHARACTERISTICS (continued)

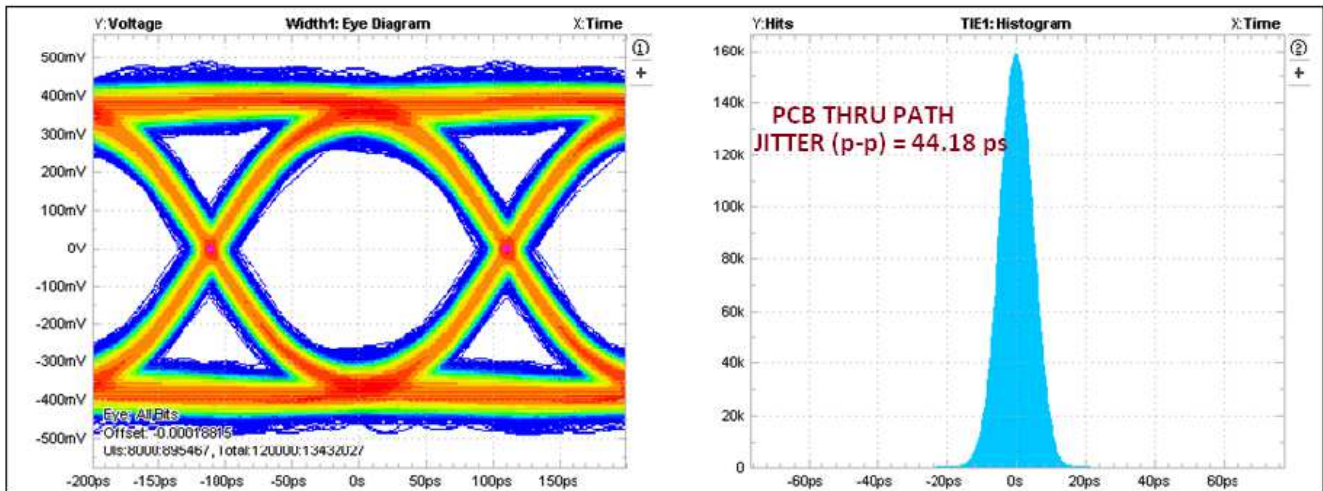
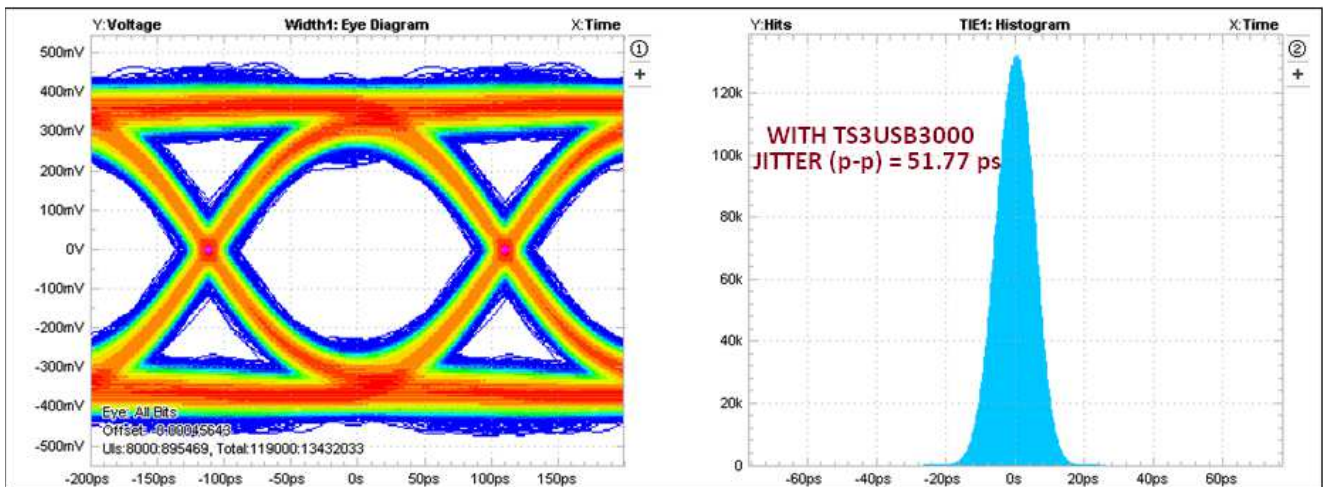


Figure 11. Eye Pattern and Time Interval Error Histogram: 4.5 Gbps With No Device



The TS3USB3000 contributes only 7.6ps of peak-to-peak jitter for 4.5 Gbps data rate.

Figure 12. Eye Pattern and Time Interval Error Histogram: 4.5 Gbps for MHL Switch

TYPICAL CHARACTERISTICS (continued)

USB 2.0 EYE PATTERN

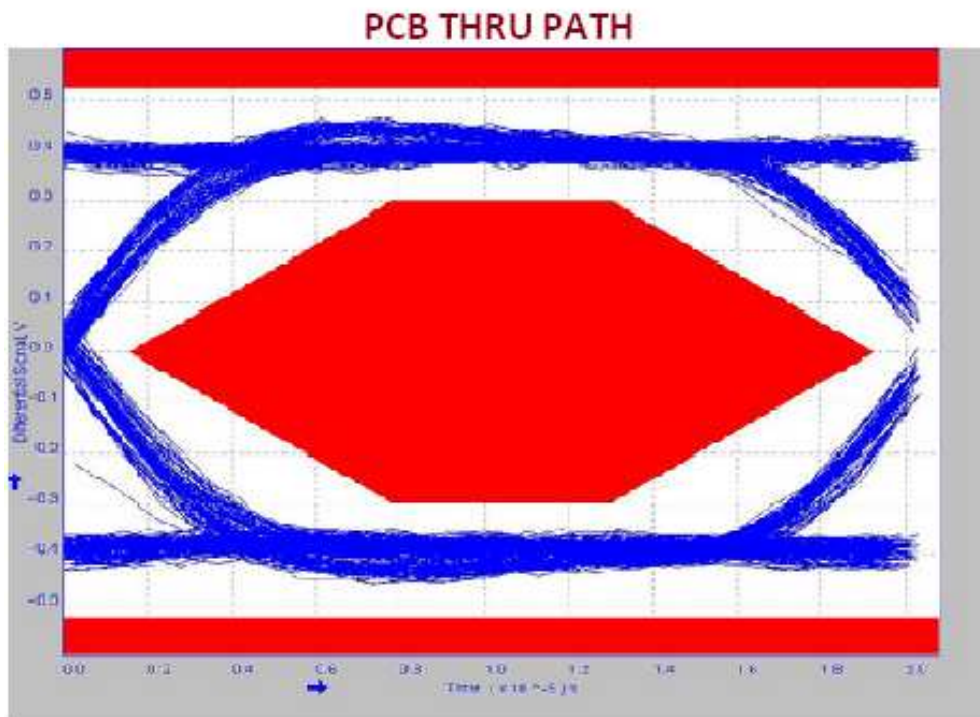


Figure 13. 480-Mbps USB 2.0 Eye Pattern with No Device

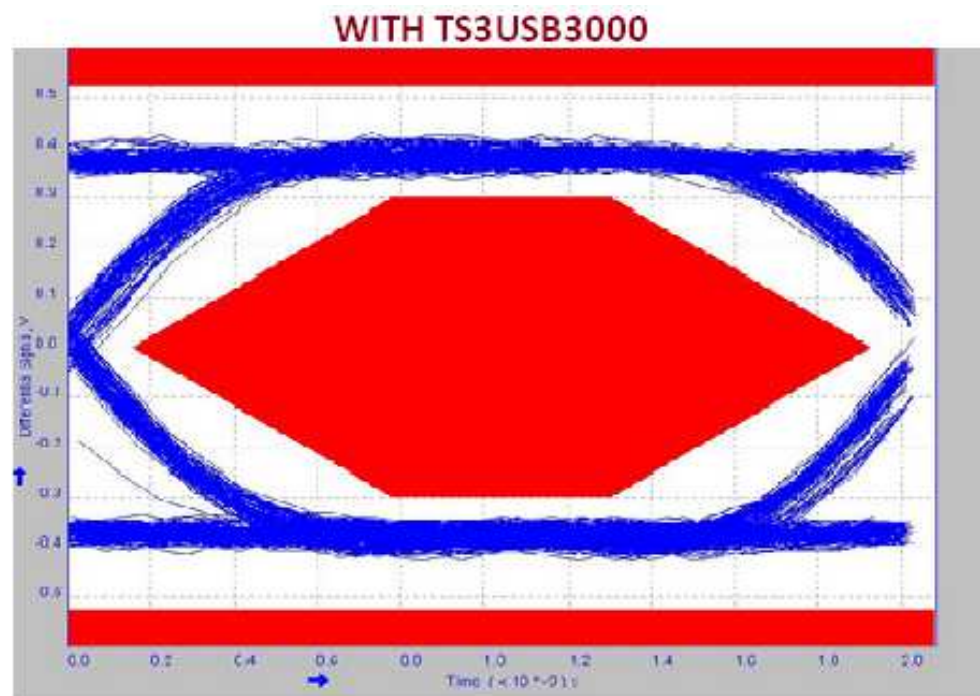


Figure 14. 480-Mbps USB 2.0 Eye Pattern for USB Switch

TYPICAL CHARACTERISTICS (continued)

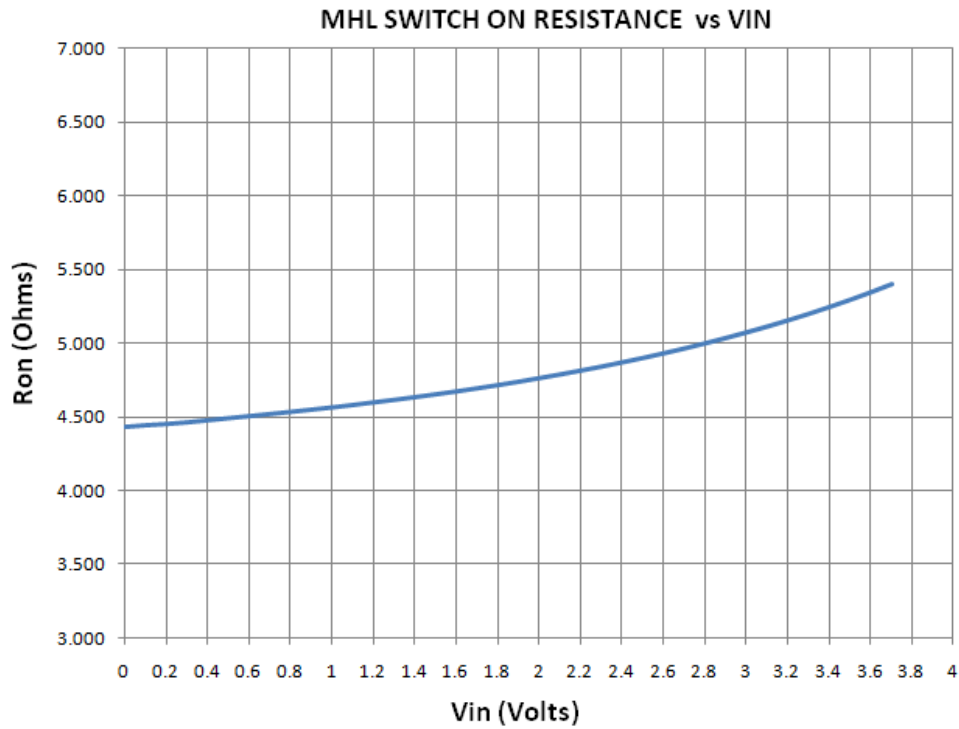


Figure 15. ON-Resistance vs. VI for MHL Switch

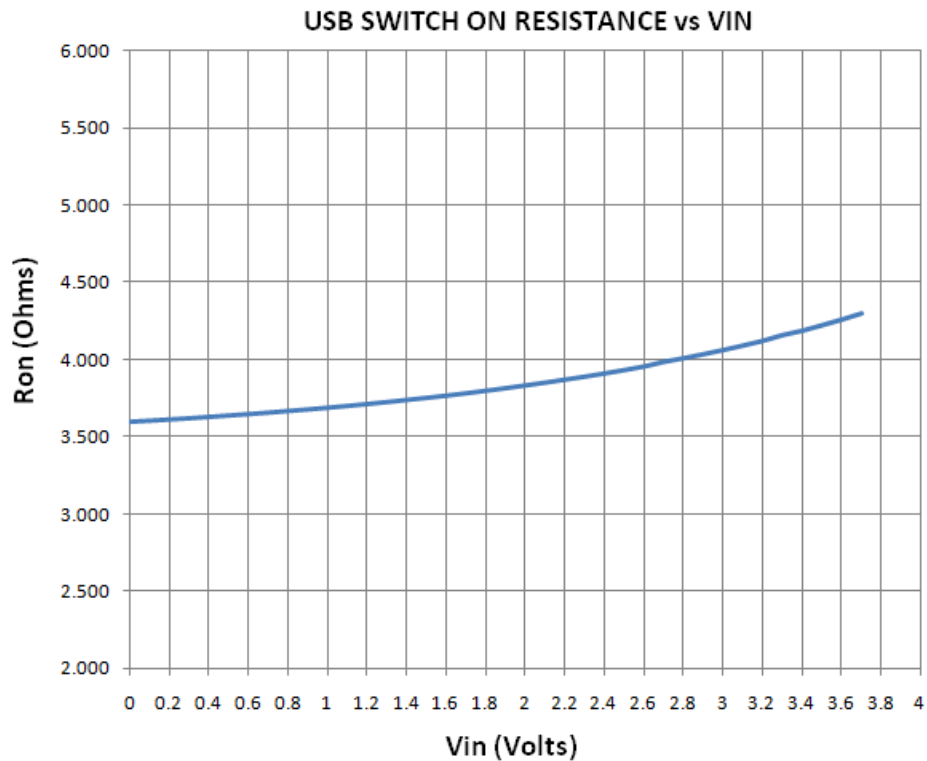


Figure 16. ON-Resistance vs. VI for USB Switch

TYPICAL CHARACTERISTICS (continued)

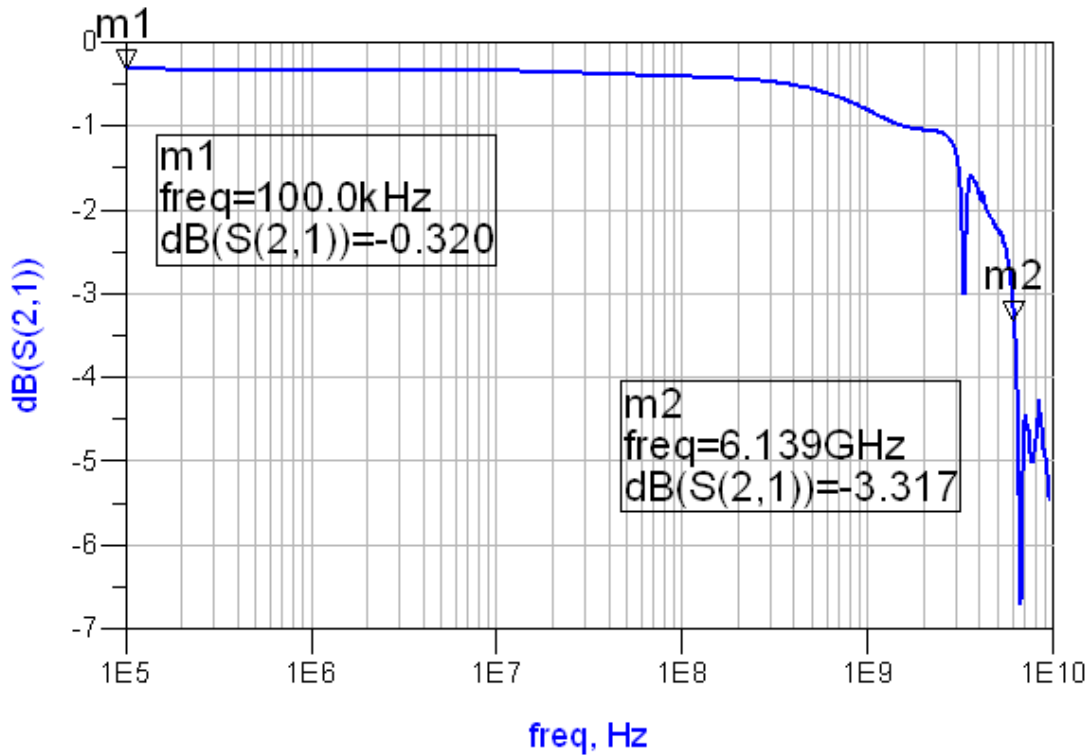


Figure 17. Differential S21 vs. Frequency for MHL Switch

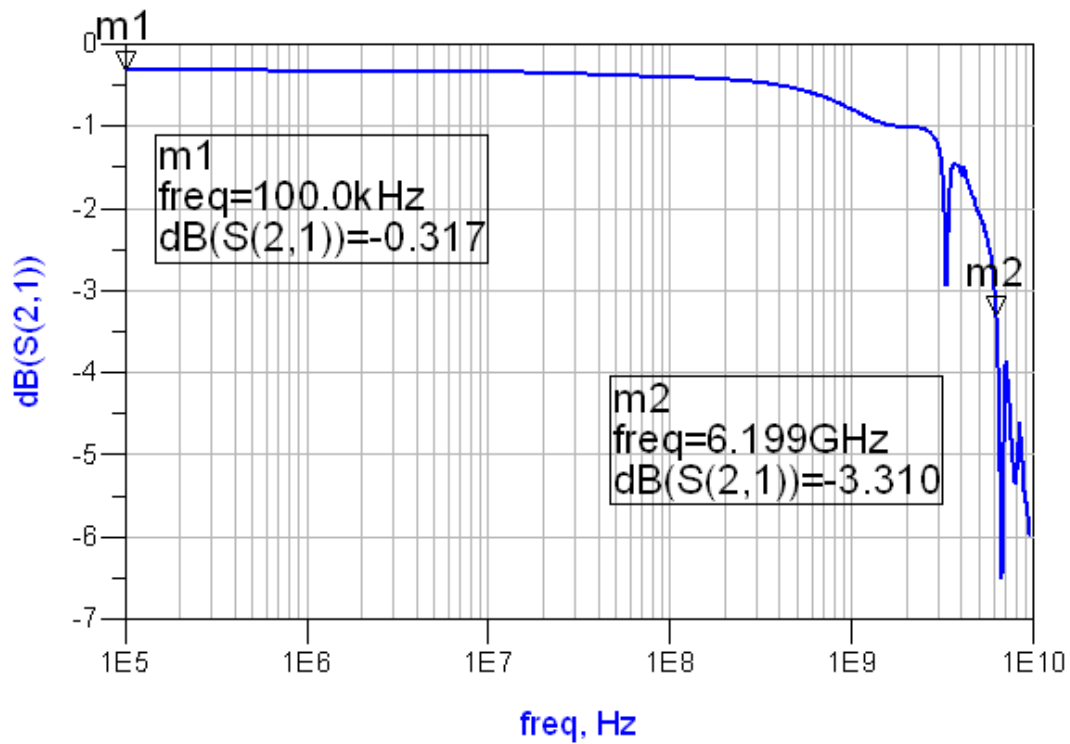


Figure 18. Differential S21 vs. Frequency for USB Switch

TYPICAL CHARACTERISTICS (continued)

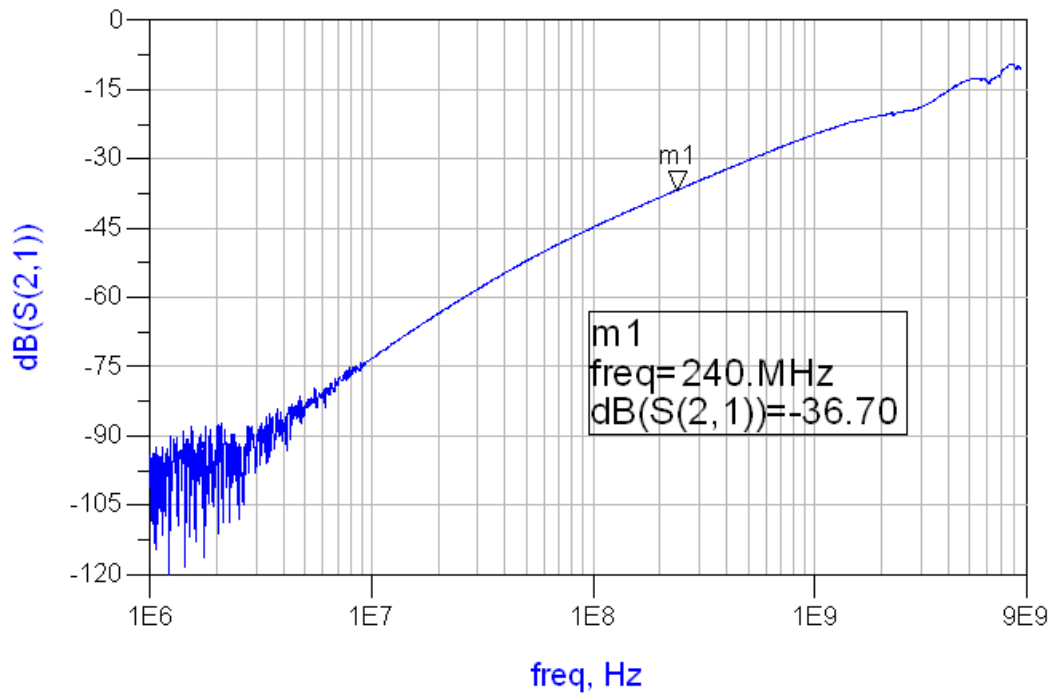


Figure 19. Off Isolation vs. Frequency for MHL Path

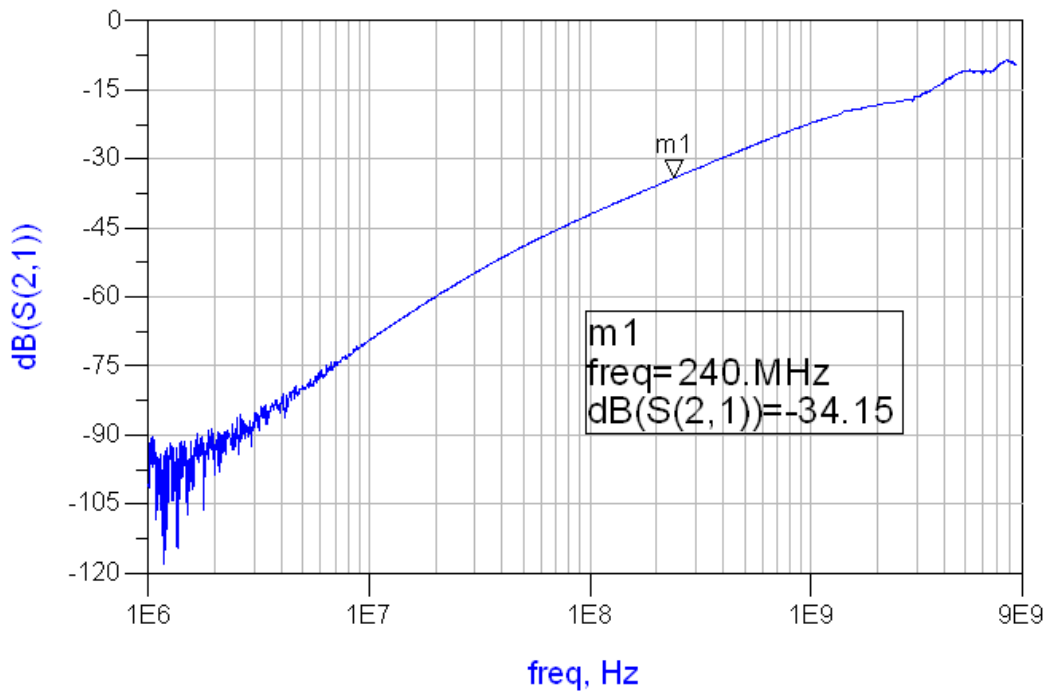


Figure 20. Off Isolation vs. Frequency for USB Path

TYPICAL CHARACTERISTICS (continued)

MHL PATH CROSSTALK

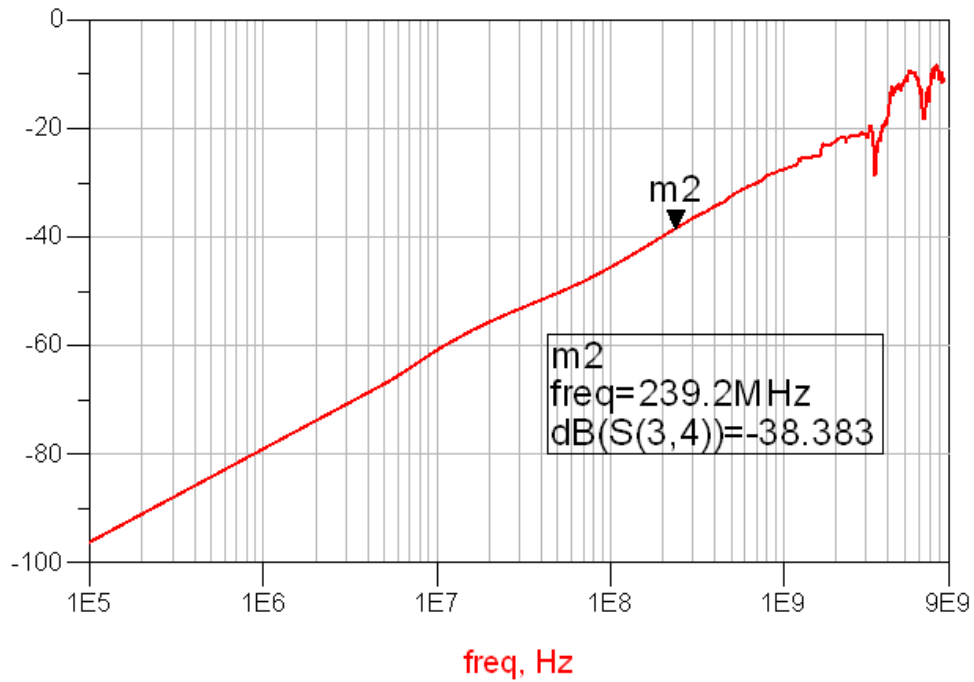


Figure 21. Cross talk vs. Frequency for MHL Path

USB PATH CROSSTALK

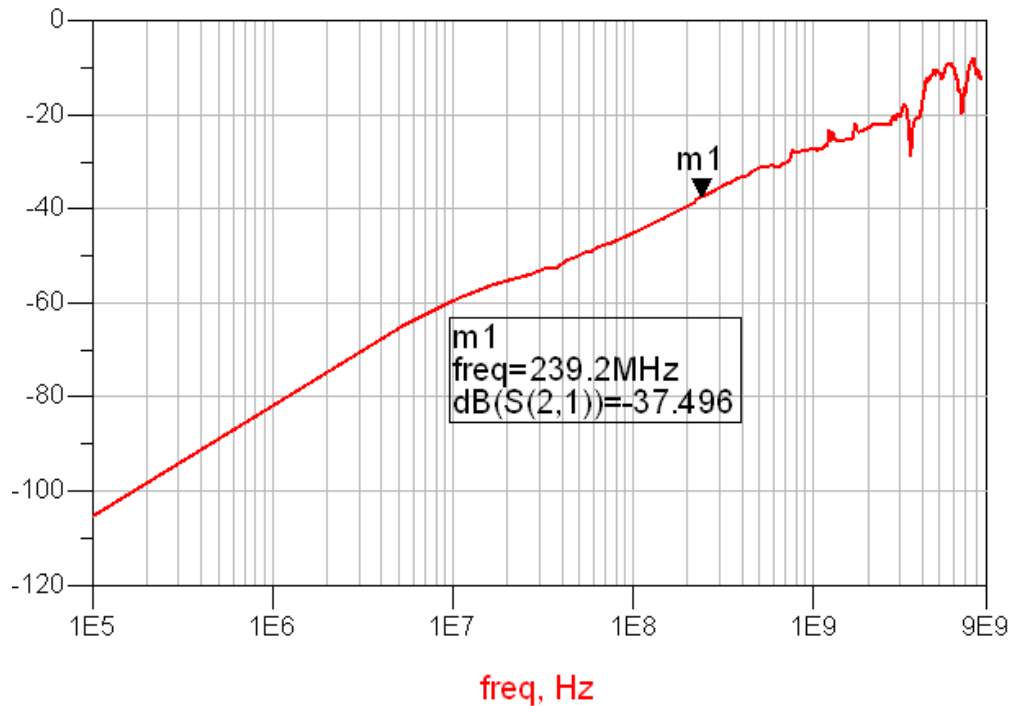



Figure 22. Cross talk vs. Frequency for USB Path

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TS3USB3000RLSR	PREVIEW	UQFN	RLS	10	3000	TBD	Call TI	Call TI	-40 to 85		
TS3USB3000RSER	ACTIVE	UQFN	RSE	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	DSJ	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3USB3000RSER	UQFN	RSE	10	3000	179.0	8.4	1.75	2.25	0.65	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS

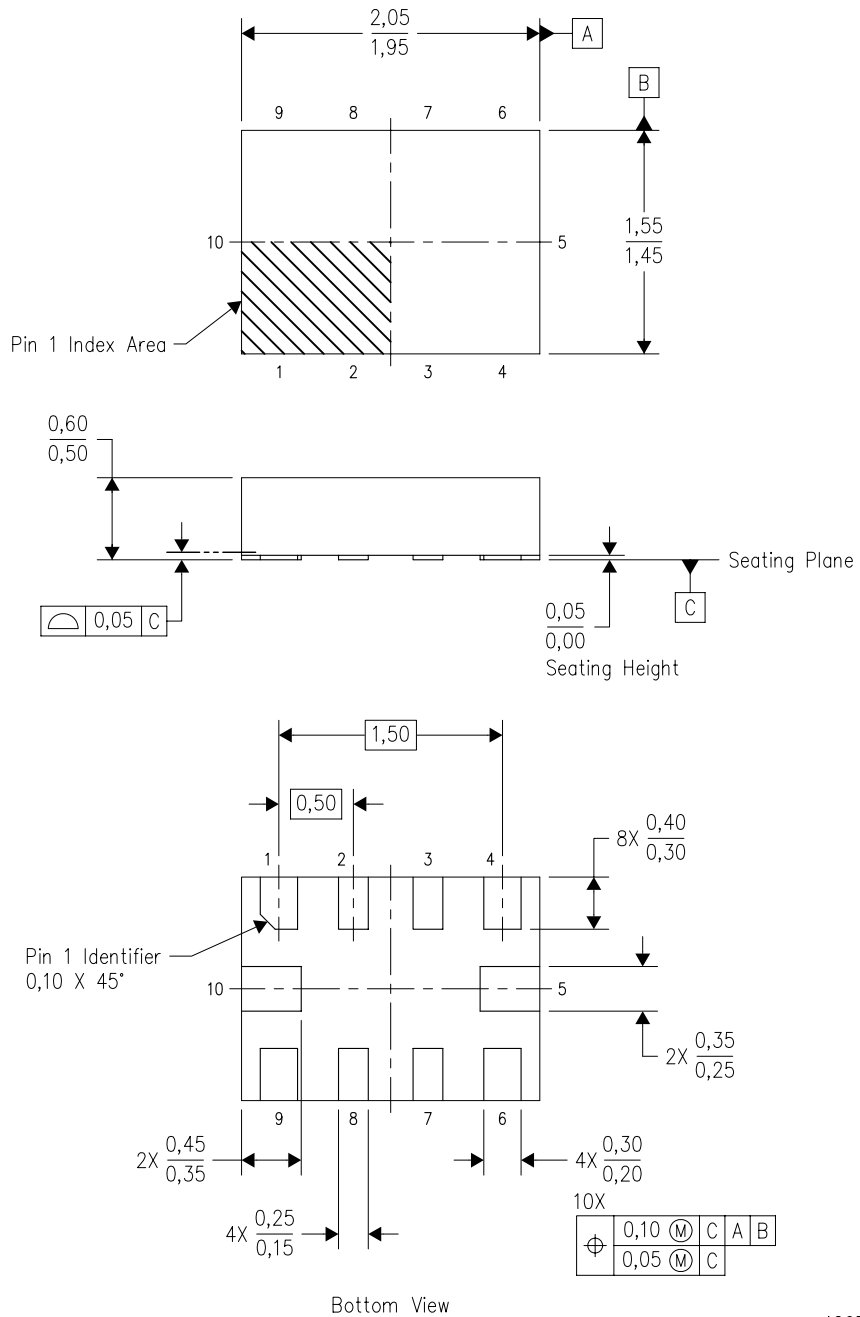


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3USB3000RSER	UQFN	RSE	10	3000	203.0	203.0	35.0

RSE (R-PUQFN-N10)

PLASTIC QUAD FLATPACK NO-LEAD

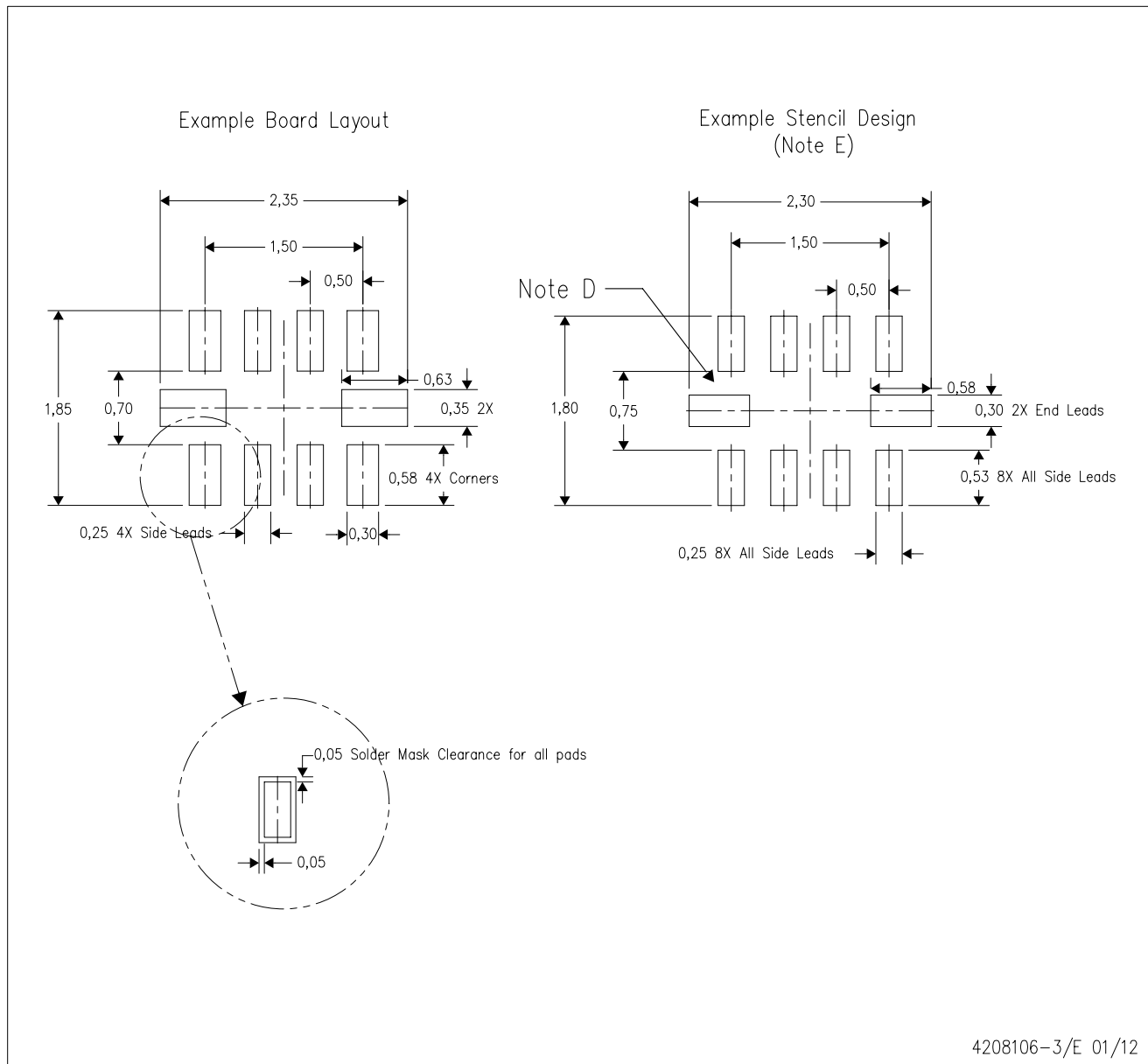


4207268-3/D 01/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) package configuration.
 - D. This package complies to JEDEC MO-288 variation UDFD.

RSE (R-PUQFN-N10)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
 - E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
 - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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