S-8243A/B Series

BATTERY PROTECTION IC FOR 3-SERIAL OR 4-SERIAL CELL PACK

www.sii-ic.com

Rev.3.0_00

The S-8243A/B Series is a protection IC for lithium-ion rechargeable battery. The S-8243A Series protects 3-series, the S-8243B Series protects 4-series cell pack from the overcharge, overdischarge, overcurrent voltages. This IC has a high-accuracy battery protection circuit and a battery monitor amplifier, and also a voltage regulator which operates the microcomputer or gas gauge IC. Combining this IC and a microcomputer or a gas gauge IC allows to display the amount of charge remained in a battery.

■ Features

(1) High-accuracy voltage detection for each cell
- Overcharge detection voltage n (n = 1 to 4)
  3.9 V to 4.4 V (50 mV step) Accuracy ±25 mV
- Hysteresis voltage n (n = 1 to 4) of overcharge detection
  −0.10 V to −0.40 V (50 mV step) or 0 V Accuracy ±50 mV

  (Overcharge release voltage n (= Overcharge detection voltage n + Hysteresis voltage n) can be selected within the range 3.8 V to 4.4 V.)
- Overdischarge detection voltage n (n = 1 to 4)
  2.0 V to 3.0 V (100 mV step) Accuracy ±80 mV
- Hysteresis voltage n (n = 1 to 4) of overdischarge detection
  0.15 V to 0.70 V or 0 V (50 mV step) Accuracy ±100 mV

  (Overdischarge release voltage n (= Overdischarge detection voltage n + Hysteresis voltage n) can be selected within the range 2.0 V to 3.4 V.)

(2) Three-level overcurrent protection including protection for short-circuiting
- Overcurrent detection voltage 1 0.05 V to 0.3 V (50 mV step) Accuracy ±25 mV
- Overcurrent detection voltage 2 0.5 V Accuracy ±100 mV
- Overcurrent detection voltage 3 V_{DD} / 2 Accuracy ±15 %

(3) Delay times for overcharge detection, overdischarge detection and overcurrent detection 1 can be set by external capacitors. (Delay times for overcurrent detection 2 and 3 are fixed internally.)

(4) Charge/discharge operation can be controlled through the control pins.

(5) High-accuracy battery monitor amp GAMP = $V_{BATTERY}$ × 0.2 ±1.0%

(6) Voltage regulator V_{OUT} = 3.3 V ±2.4 % (3 mA max.)

(7) High input-voltage device Absolute maximum rating: 26 V

(8) Wide operating voltage range 6 V to 18 V

(9) Wide operating temperature range: −40°C to +85°C

(10) Low current consumption
- Operation mode 120 μA max.
- Power down mode 0.1 μA max.

(11) Lead-free, Sn 100%, halogen-free[*1]

***1.** Refer to "■ **Product Name Structure**" for details.

■ Applications

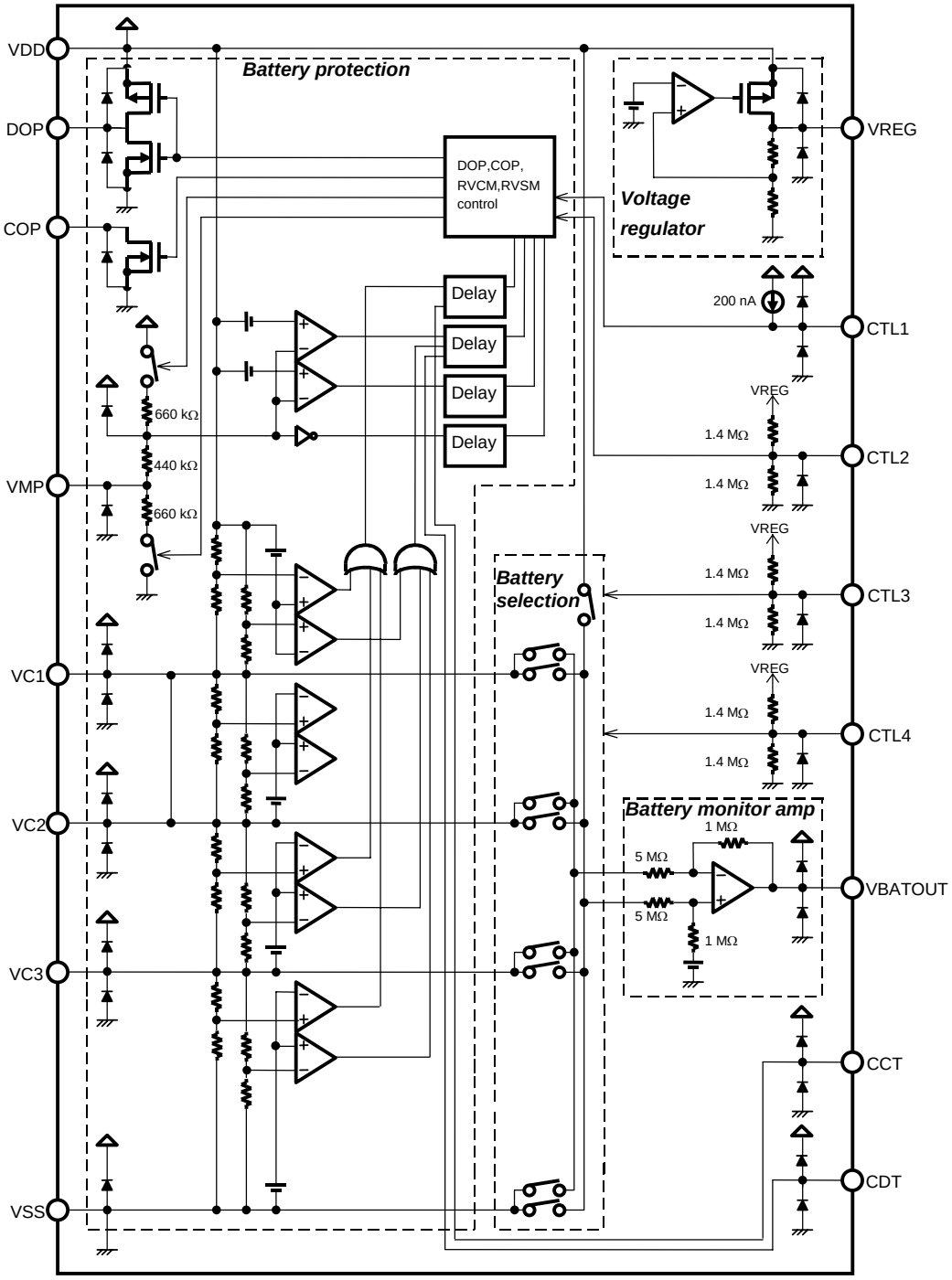
- Lithium-ion rechargeable battery packs
- Lithium polymer rechargeable battery packs

■ Package

- 16-Pin TSSOP

■ Block Diagrams

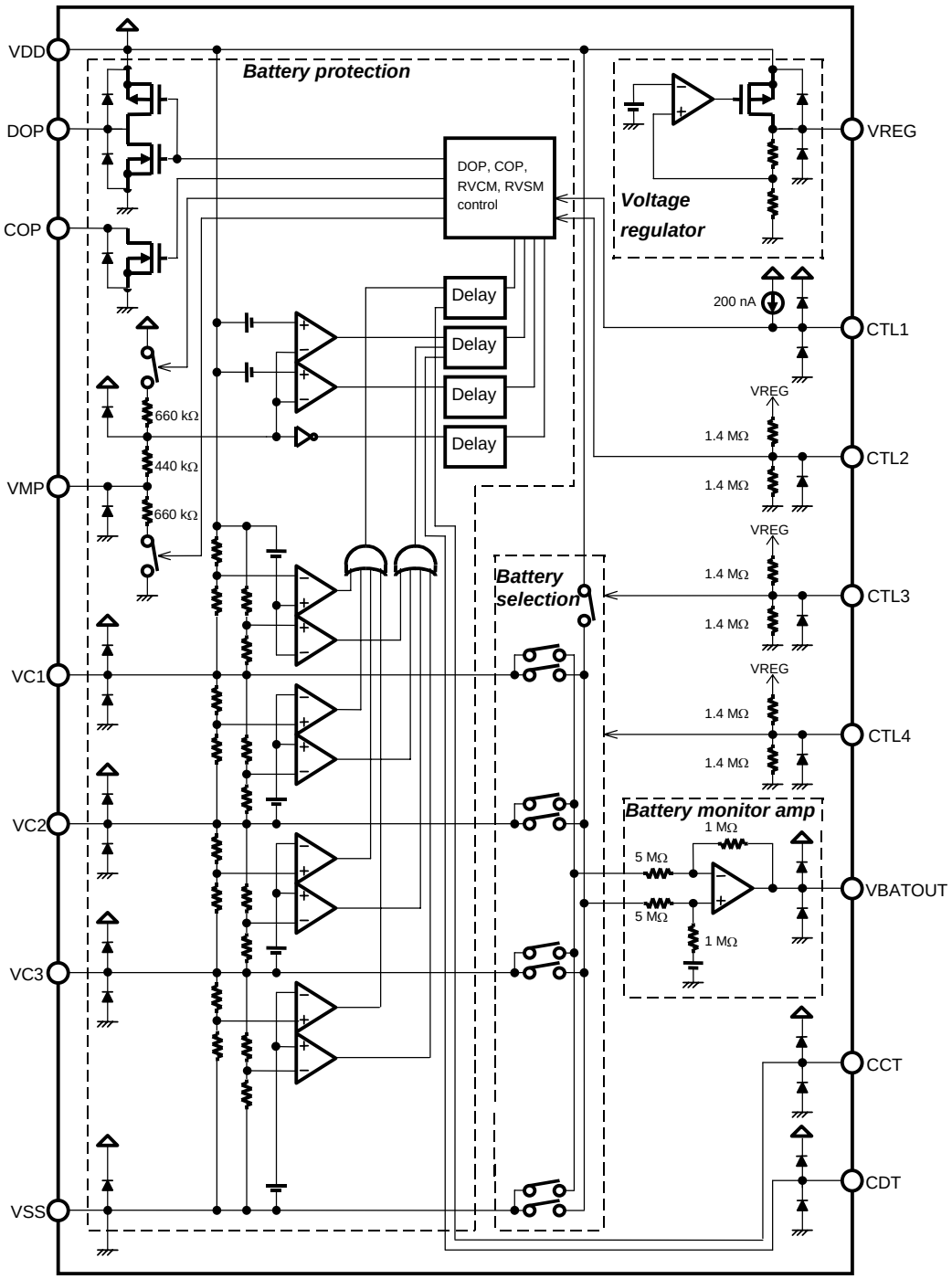
1. S-8243A Series



Remark1. Diodes in the figure are parasitic diodes.
2. Numerical values are typical values.

Figure 1

2. S-8243B Series

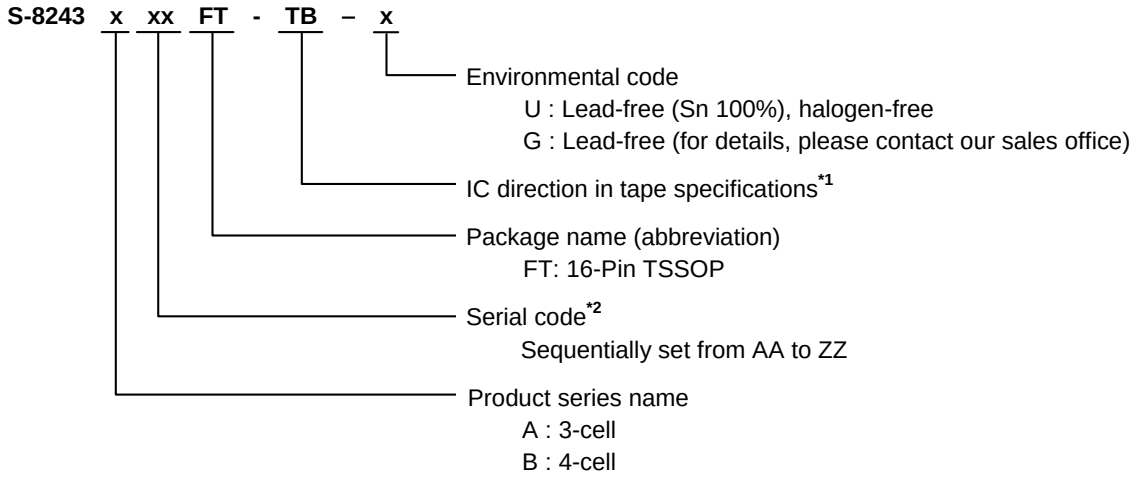


Remark1. Diodes in the figure are parasitic diodes.
2. Numerical values are typical values.

Figure 2

■ Product Name Structure

1. Product Name



***1.** Refer to the tape specifications at the end of this book.
***2.** Refer to the "**3. Product Name List**".

2. Package

Package Name		Drawing Code		
		Package	Tape	Reel
16-Pin TSSOP	Environmental code = G	FT016-A-P-SD	FT016-A-C-SD	FT016-A-R-SD
	Environmental code = U	FT016-A-P-SD	FT016-A-C-SD	FT016-A-R-S1

3. Product Name List

Table 1 S-8243A Series (For 3-Serial Cell)

Product name / Item	Overcharge detection voltage [V_{CU}]	Hysteresis voltage for overcharge detection [V_{HC}]	Overdischarge detection voltage [V_{DL}]	Hysteresis voltage for overdischarge detection [V_{HD}]	Overcurrent detection voltage1 [V_{IOV1}]	0 V battery charging function
S-8243AACFT-TB-x	4.350 ±0.025 V	−0.15 ±0.05 V	2.40 ±0.08 V	0.20 ±0.10 V	0.20 ±0.025 V	Available
S-8243AADFT-TB-x	4.350 ±0.025 V	−0.35 ±0.05 V	2.40 ±0.08 V	0 V	0.20 ±0.025 V	Available

Table 2 S-8243B Series (For 4-Serial Cell)

Product name / Item	Overcharge detection voltage [V_{CU}]	Hysteresis voltage for overcharge detection [V_{HC}]	Overdischarge detection voltage [V_{DL}]	Hysteresis voltage for overdischarge detection [V_{HD}]	Overcurrent detection voltage1 [V_{IOV1}]	0 V battery charging function
S-8243BADFT-TB-x	4.350 ±0.025 V	−0.25 ±0.05 V	2.40 ±0.08 V	0 V	0.25 ±0.025 V	Available
S-8243BAEFT-TB-x	4.350 ±0.025 V	−0.15 ±0.05 V	2.40 ±0.08 V	0.20 ±0.10 V	0.20 ±0.025 V	Available
S-8243BAFFT-TB-x	4.250 ±0.025 V	−0.25 ±0.05 V	2.40 ±0.08 V	0 V	0.20 ±0.025 V	Available
S-8243BAHFT-TB-x	4.315 ±0.025 V	−0.20 ±0.05 V	2.00 ±0.08 V	0.15 ±0.10 V	0.20 ±0.025 V	Available

Remark 1. Change in the detection voltage is available in products other than listed above. Contact our sales office.
2. x: G or U
3. Please select products of environmental code = U for Sn 100%, halogen-free products.

■ Pin Configuration

16-Pin TSSOP
Top view

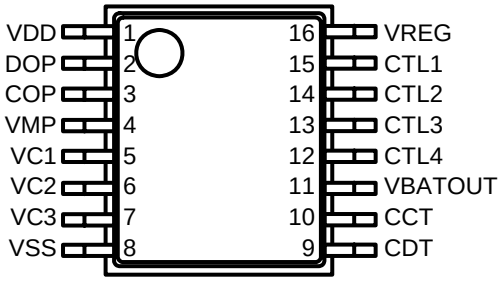


Figure 3

Table 3 Pin description (S-8243A Series)

Pin No.	Symbol	Description
1	VDD	Input pin for positive power supply, Connection pin for battery 1's positive voltage
2	DOP	Connection pin for discharge control FET gate (CMOS output)
3	COP	Connection pin for charge control FET gate (Nch open drain output)
4	VMP	Pin for voltage detection between VDD-VMP pin (Pin for overcurrent detection)
5	VC1	No connection
6	VC2	Connection pin for battery 1's negative voltage, for battery 2's positive voltage
7	VC3	Connection pin for battery 2's negative voltage, for battery 3's positive voltage
8	VSS	Input pin for negative power supply, Connection pin for battery 3's negative voltage
9	CDT	Connection pin to capacitor for overdischarge detection delay, for overcurrent detection delay 1
10	CCT	Connection pin to capacitor for overcharge detection delay
11	VBATOUT	Output pin for battery voltage and offset voltage
12	CTL4	Pin for selecting output from VBATOUT pin
13	CTL3	Pin for selecting output from VBATOUT pin
14	CTL2	Control pin for charge / discharge FET
15	CTL1	Control pin for charge / discharge FET
16	VREG	Output pin for voltage regulator (3.3 V)

Table 4 Pin description (S-8243B Series)

Pin No.	Symbol	Description
1	VDD	Input pin for positive power supply, Connection pin for battery 1's positive voltage
2	DOP	Connection pin for discharge control FET gate (CMOS output)
3	COP	Connection pin for charge control FET gate (Nch open drain output)
4	VMP	Pin for voltage detection between VDD-VMP pin (Pin for overcurrent detection)
5	VC1	Connection pin for battery 1's negative voltage, for battery 2's positive voltage
6	VC2	Connection pin for battery 2's negative voltage, for battery 3's positive voltage
7	VC3	Connection pin for battery 3's negative voltage, for battery 4's positive voltage
8	VSS	Input pin for negative power supply, Connection pin for battery 4's negative voltage
9	CDT	Connection pin to capacitor for overdischarge detection delay, for overcurrent detection delay 1
10	CCT	Connection pin to capacitor for overcharge detection delay
11	VBATOUT	Output pin for battery voltage and offset voltage
12	CTL4	Pin for selecting output from VBATOUT pin
13	CTL3	Pin for selecting output from VBATOUT pin
14	CTL2	Control pin for charge / discharge FET
15	CTL1	Control pin for charge / discharge FET
16	VREG	Output pin for voltage regulator (3.3 V)

■ Absolute Maximum Ratings

Table 5

(Ta = 25°C unless otherwise specified)

Item	Symbol	Applied Pins	Absolute Maximum Ratings	Unit
Input voltage VDD	V_{DS}	–	V_{SS}–0.3 to V_{SS}+26	V
Input voltage	V_{IN}	VC1, VC2, VC3, CCT, CDT	V_{SS}–0.3 to V_{DD}+0.3	V
VMP pin Input voltage	V_{MP}	VMP	V_{SS}–0.3 to V_{SS}+26	V
DOP pin output voltage	V_{DOP}	DOP	V_{SS}–0.3 to V_{DD}+0.3	V
COP pin output voltage	V_{COP}	COP	V_{SS}–0.3 to V_{SS}+26	V
VREG pin output voltage	V_{OUT}	VREG	V_{SS}–0.3 to V_{DD}+0.3	V
CTL1 pin input voltage	V_{CTL1}	CTL1	V_{SS}–0.3 to V_{DD}+0.3	V
CTL2 to CTL4 pin input voltage	V_{CTLn}	CTL2, CTL3, CTL4	V_{SS}–0.3 to V_{OUT}+0.3	V
Cell voltage output voltage	V_{BATOUT}	VBATOUT	V_{SS}–0.3 to V_{OUT}+0.3	V
Power dissipation	P_D	–	300 (When not mounted on board)	mW
		–	1100*1	mW
Operation ambient temperature	T_{opr}	–	–40 to +85	°C
Storage temperature	T_{stg}	–	–40 to +125	°C

***1.** When mounted on board
[Mounted board]
(1) Board size : 114.3 mm × 76.2 mm × t1.6 mm
(2) Board name : JEDEC STANDARD51-7

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

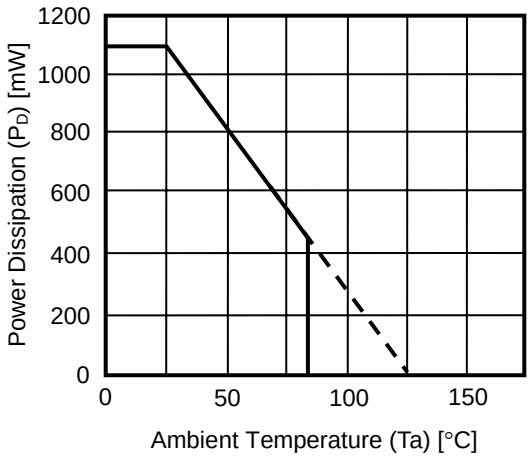


Figure 4 Power Dissipation of Package (When Mounted on Board)

■ Electrical Characteristics

1. S-8243A Series

Table 6 (1 / 2)

(Ta = 25°C unless otherwise specified)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Test circuit
BATTERY PROTECTION							
Overcharge detection voltage n n=1, 2, 3	V_{CUn}	3.9 V to 4.4 V, 50 mV Step	V_{CUn} −0.025	V_{CUn}	V_{CUn} +0.025	V	4
Hysteresis voltage n of overcharge detection n = 1, 2, 3	V_{HCn}	−0.10 V to −0.40 V, and 0 V	V_{HCn} −0.05	V_{HCn}	V_{HCn} +0.05	V	4
Overdischarge detection voltage n = 1, 2, 3	V_{DLn}	2.0 V to 3.0 V, 100 mV Step	V_{DLn} −0.08	V_{DLn}	V_{DLn} +0.08	V	4
Hysteresis voltage n of Overdischarge detection n = 1, 2, 3	V_{HDn}	0.15 V to 0.70 V, and 0 V	V_{HDn} −0.10	V_{HDn}	V_{HDn} +0.10	V	4
Overcurrent detection voltage 1	V_{IOV1}	0.05 V to 0.3 V, 50 mV Step VM voltage based on V_{DD}	V_{IOV1} −0.025	V_{IOV1}	V_{IOV1} +0.025	V	4
Overcurrent detection voltage 2	V_{IOV2}	VM voltage based on V_{DD}	0.40	0.50	0.60	V	4
Overcurrent detection voltage 3	V_{IOV3}	−	V_{DD}×0.425	V_{DD}×0.5	V_{DD}×0.575	V	4
Temperature coefficient for detection and release voltage*1	T_{COE1}	Ta = −5°C to +55°C*3	−1.0	0	1.0	mV/°C	4
Temperature coefficient for overcurrent detection voltage*2	T_{COE2}	Ta = −5°C to +55°C*3	−0.5	0	0.5	mV/°C	4
0 V BATTERY CHARGING FUNCTION (The 0 V battery function is either "0 V battery charging is allowed." or "0 V battery charging is inhibited." depending upon the product type.)							
0 V battery charge starting charger voltage	V_{0CHA}	0 V battery charging available	−	0.8	1.5	V	7
0 V battery charge inhibition battery voltage	V_{0INH}	0 V battery charging unavailable	0.4	0.7	1.1	V	7
INTERNAL RESISTANCE							
Internal resistance between VMP and VDD	R_{VDM}	V1 = V2 = V3 = 3.5 V	500	1100	2400	kΩ	8
Internal resistance between VMP and VSS	R_{VSM}	V1 = V2 = V3 = 1.8 V	300	700	1500	kΩ	8
VOLTAGE REGULATOR							
Output voltage	V_{OUT}	V_{DD} = 14 V, I_{OUT} = 3 mA	3.221	3.300	3.379	V	2
Line regulation	ΔV_{OUT1}	V_{DD} = 6 V→18 V, I_{OUT} = 3 mA	−	5	15	mV	2
Load regulation	ΔV_{OUT2}	V_{DD} = 14 V, I_{OUT} = 5 μA→3 mA	−	15	30	mV	2
BATTERY MONITOR AMP							
Input offset voltage n n = 1, 2, 3	V_{OFFn}	V1 = V2 = V3 = 3.5 V	60	165	270	mV	3
Voltage gain n n = 1, 2, 3	GAMPn	V1 = V2 = V3 = 3.5 V	0.2×0.99	0.2	0.2×1.01	−	3
INPUT VOLTAGE, OPERATING VOLTAGE							
Operating voltage between V_{DD} and V_{SS}	V_{DSOP}	−	6	−	18	V	4
CTL1 input voltage for High	V_{CTL1H}	−	V_{DD}×0.8	−	−	V	6
CTL1 input voltage for Low	V_{CTL1L}	−	−	−	V_{DD}×0.2	V	6
CTLn input voltage for High n = 2, 3, 4	V_{CTLnH}	−	V_{OUT}×0.9	−	V_{OUT}	V	3, 6
CTLn input voltage for Low n = 2, 3, 4	V_{CTLnL}	−	−	−	V_{OUT}×0.1	V	3, 6

Table 6 (2 / 2)

Item	Symbol	Remarks	Min.	Typ.	Max.	Unit	Test circuit
INPUT CURRENT							
Current consumption at not monitoring V_{BATOUT}	I_{OPE}	V1 = V2 = V3 = 3.5 V, $V_{MP} = V_{DD}$	–	65	120	μA	1
Current consumption at power down	I_{PDN}	V1 = V2 = V3 = 1.5 V, $V_{MP} = V_{SS}$	–	–	0.1	μA	1
Current for VCn at not monitoring V_{BATOUT} (n = 2, 3)	I_{VCnN}	V1 = V2 = V3 = 3.5 V	–0.3	0	0.3	μA	3
Current for VC2 at monitoring of V_{BATOUT}	I_{VC2}	V1 = V2 = V3 = 3.5 V	–	2.0	7.2	μA	3
Current for VC3 at monitoring of V_{BATOUT}	I_{VC3}	V1 = V2 = V3 = 3.5 V	–	1.0	4.0	μA	3
Current for CTL1 at Low	I_{CTL1L}	V1 = V2 = V3 = 3.5 V, V_{CTL1} = 0 V	–0.4	–0.2	–	μA	5
Current for CTLn at High n = 2,3,4	I_{CTLnH}	$V_{CTLn} = V_{OUT}$	–	2.5	5	μA	9
Current for CTLn at Low n = 2,3,4	I_{CTLnL}	V_{CTLn} = 0 V	–5	–2.5	–	μA	9
OUTPUT CURRENT							
Leak current COP	I_{COH}	V_{COP} = 24 V	–	–	0.1	μA	9
Sink current COP	I_{COL}	$V_{COP} = V_{SS}$+0.5 V	10	–	–	μA	9
Source current DOP	I_{DOH}	$V_{DOP} = V_{DD}$–0.5 V	10	–	–	μA	9
Sink current DOP	I_{DOL}	$V_{DOP} = V_{SS}$+0.5 V	10	–	–	μA	9
Source current V_{BATOUT}	I_{VBATH}	$V_{BATOUT} = V_{DD}$–0.5 V	100	–	–	μA	9
Sink current V_{BATOUT}	I_{VBATL}	$V_{BATOUT} = V_{SS}$+0.5 V	100	–	–	μA	9

Applied to S-8243AACFT and S-8243AADFT

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Test circuit
DELAY TIME							
Overcharge detection delay time	t_{CU}	C_{CT} = 0.1 μF	0.5	1.0	1.5	s	5
Overdischarge detection delay time	t_{DL}	C_{DT} = 0.1 μF	50	100	150	ms	5
Overcurrent detection delay time 1	t_{IOV1}	C_{DT} = 0.1 μF	5	10	15	ms	5
Overcurrent detection delay time 2	t_{IOV2}	–	1.5	2.5	4.0	ms	4
Overcurrent detection delay time 3	t_{IOV3}	–	100	300	600	μs	4

***1.** Temperature coefficient for detection and release voltage is applied to overcharge detection voltage n, overcharge release voltage n, overdischarge detection voltage n, and overdischarge release voltage n.

***2.** Temperature coefficient for overcurrent detection voltage is applied to over current detection voltage 1 and 2.

***3.** Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

2. S-8243B Series

Table 7 (1 / 2)

(Ta = 25°C unless otherwise specified)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Test circuit
DETECTION VOLTAGE							
Overcharge detection voltage n n = 1, 2, 3, 4	V_{CUn}	3.9 V to 4.4 V, 50 mV Step	V_{CUn} −0.025	V_{Cun}	V_{CUn} +0.025	V	4
Hysteresis voltage n of overcharge detection n = 1, 2, 3, 4	V_{HCn}	−0.10 V to −0.40 V, and 0 V	V_{HCn} −0.05	V_{HCn}	V_{HCn} +0.05	V	4
Overdischarge detection voltage n = 1, 2, 3, 4	V_{DLn}	2.0 V to 3.0 V, 100 mV Step	V_{DLn} −0.08	V_{DLn}	V_{DLn} +0.08	V	4
Hysteresis voltage n of overdischarge detection n = 1, 2, 3, 4	V_{HDn}	0.15 V to 0.70 V, and 0 V	V_{HDn} −0.10	V_{HDn}	V_{HDn} +0.10	V	4
Overcurrent detection voltage 1	V_{IOV1}	0.05 V to 0.3 V, 50 mV Step VM voltage based on V_{DD}	V_{IOV1} −0.025	V_{IOV1}	V_{IOV1} +0.025	V	4
Overcurrent detection voltage 2	V_{IOV2}	VM voltage based on V_{DD}	0.40	0.50	0.60	V	4
Overcurrent detection voltage 3	V_{IOV3}	−	V_{DD} ×0.425	V_{DD} ×0.5	V_{DD} ×0.575	V	4
Temperature coefficient for detection and release voltage*1	T_{COE1}	Ta = −5°C to +55°C*3	−1.0	0	1.0	mV/°C	4
Temperature coefficient for overcurrent detection voltage*2	T_{COE2}	Ta = −5°C to +55°C*3	−0.5	0	0.5	mV/°C	4
0 V BATTERY CHARGING FUNCTION (The 0 V battery function is either "0 V battery charging is allowed." or "0 V battery charging is inhibited." depending upon the product type.)							
0 V battery charge starting charger voltage	V_{0CHA}	0 V battery charging allowed	−	0.8	1.5	V	7
0 V battery charge inhibition battery voltage	V_{0INH}	0 V battery charging inhibited	0.4	0.7	1.1	V	7
INTERNAL RESISTANCE							
Internal resistance between VMP and VDD	R_{VDM}	V1 = V2 = V3 = V4 = 3.5 V	500	1100	2400	kΩ	8
Internal resistance between VMP and VSS	R_{VSM}	V1 = V2 = V3 = V4 = 1.8 V	300	700	1500	kΩ	8
VOLTAGE REGULATOR							
Output voltage	V_{OUT}	V_{DD} = 14V, I_{OUT} = 3 mA	3.221	3.300	3.379	V	2
Line regulation	ΔV_{OUT1}	V_{DD} = 6 V→18 V, I_{OUT} = 3 mA	−	5	15	mV	2
Load regulation	ΔV_{OUT2}	V_{DD} = 14 V, I_{OUT} = 5 μA→3 mA	−	15	30	mV	2
BATTERY MONITOR AMP							
Input offset voltage n n = 1, 2, 3, 4	V_{OFFn}	V1 = V2 = V3 = V4 = 3.5 V	60	165	270	mV	3
Voltage gain n n = 1, 2, 3, 4	GAMPn	V1 = V2 = V3 = V4 = 3.5 V	0.2×0.99	0.2	0.2×1.01	—	3
INPUT VOLTAGE, OPERATING VOLTAGE							
Operating voltage between V_{DD} and V_{SS}	V_{DSOP}	−	6	−	18	V	4
CTL1 input voltage for High	V_{CTL1H}	−	V_{DD}×0.8	−	−	V	6
CTL1 input voltage for Low	V_{CTL1L}	−	−	−	V_{DD}×0.2	V	6
CTLn input voltage for High n = 2, 3, 4	V_{CTLnH}	−	V_{OUT}×0.9	−	V_{OUT}	V	3, 6
CTLn input voltage for Low n = 2, 3, 4	V_{CTLnL}	−	−	−	V_{OUT}×0.1	V	3, 6

Table 7 (2 / 2)

Item	Symbol	Remarks	Min.	Typ.	Max.	Unit	Test circuit
INPUT CURRENT							
Current consumption at not monitoring V_{BATOUT}	I_{OPE}	V1 = V2 = V3 = V4 = 3.5 V, $V_{MP} = V_{DD}$	–	65	120	μA	1
Current consumption at power down	I_{PDN}	V1 = V2 = V3 = V4 = 1.5 V, $V_{MP} = V_{SS}$	–	–	0.1	μA	1
Current for VCn at not monitoring V_{BATOUT} (n = 2, 3)	I_{VCnN}	V1 = V2 = V3 = V4 = 3.5 V	–0.3	0	0.3	μA	3
Current for VC1 at monitoring of V_{BATOUT}	I_{VC1}	V1 = V2 = V3 = V4 = 3.5 V	–	3.2	10.4	μA	3
Current for VC2 at monitoring of V_{BATOUT}	I_{VC2}	V1 = V2 = V3 = V4 = 3.5 V	–	2.0	7.2	μA	3
Current for VC3 at monitoring of V_{BATOUT}	I_{VC3}	V1 = V2 = V3 = V4 = 3.5 V, V_{CTL1} = 0 V	–	1.0	4.0	μA	3
Current for CTL1 at Low	I_{CTL1L}	V1 = V2 = V3 = V4 = 3.5 V, V_{CTL1} = 0 V	–0.4	–0.2	–	μA	5
Current for CTLn at High n = 2, 3, 4	I_{CTLnH}	$V_{CTLn} = V_{OUT}$	–	2.5	5	μA	9
Current for CTLn at Low n = 2, 3, 4	I_{CTLnL}	V_{CTLn} = 0 V	–5	–2.5	–	μA	9
OUTPUT CURRENT							
Leak current COP	I_{COH}	V_{COP} = 24 V	–	–	0.1	μA	9
Sink current COP	I_{COL}	$V_{COP} = V_{SS}$+0.5 V	10	–	–	μA	9
Source current DOP	I_{DOH}	$V_{DOP} = V_{DD}$–0.5 V	10	–	–	μA	9
Sink current DOP	I_{DOL}	$V_{DOP} = V_{SS}$+0.5 V	10	–	–	μA	9
Source current V_{BATOUT}	I_{VBATH}	$V_{BATOUT} = V_{DD}$–0.5 V	100	–	–	μA	9
Sink current V_{BATOUT}	I_{VBATL}	$V_{BATOUT} = V_{SS}$+0.5 V	100	–	–	μA	9

Applied to S-8243BAEFT, S-8243BAFFT, S-8243BAHFT

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Test circuit
DELAY TIME							
Overcharge detection delay time	t_{CU}	C_{CT} = 0.1 μF	0.5	1.0	1.5	s	5
Overdischarge detection delay time	t_{DL}	C_{DT} = 0.1 μF	50	100	150	ms	5
Overcurrent detection delay time 1	t_{IOV1}	C_{DT} = 0.1 μF	5	10	15	ms	5
Overcurrent detection delay time 2	t_{IOV2}	–	1.5	2.5	4.0	ms	4
Overcurrent detection delay time 3	t_{IOV3}	–	100	300	600	μs	4

Applied to S-8243BADFT

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Test circuit
DELAY TIME							
Overcharge detection delay time	t_{CU}	C_{CT} = 0.1 μF	0.5	1.0	1.5	s	5
Overdischarge detection delay time	t_{DL}	C_{DT} = 0.1 μF	55.5	111	222	ms	5
Overcurrent detection delay time 1	t_{IOV1}	C_{DT} = 0.1 μF	3.31	6.62	13.2	ms	5
Overcurrent detection delay time 2	t_{IOV2}	–	1.5	2.5	4.0	ms	4
Overcurrent detection delay time 3	t_{IOV3}	–	100	300	600	μs	4

***1.** Temperature coefficient for detection and release voltage is applied to overcharge detection voltage n, overcharge release voltage n, overdischarge detection voltage n, and overdischarge release voltage n.

***2.** Temperature coefficient for overcurrent detection voltage is applied to over current detection voltage 1 and 2.

***3.** Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

■ Test Circuits

In this chapter test methods are explained for the case of S-8243B series, which is designed for 4-serial cell pack. For the case of S-8243A series, which is designed for 3-serial cell, voltage source V2 should be shorted, V3 should be read as V2, and V4 as V3.

1. Current consumption (Test circuit 1)

Current consumption at not monitoring V_{BATOUT}, I_{OPE}, is a current measured at the VSS pin when V1 = V2 = V3 = V4 = 3.5 V and $V_{MP} = V_{DD}$. Current consumption at power down, I_{PDN}, is a current measured at the VSS pin when V1 = V2 = V3 = V4 = 1.5 V and $V_{MP} = V_{SS}$.

2. Voltage regulator (Test circuit 2)

Output voltage of the regulator V_{OUT} is a voltage measured at the VREG pin when $V_{DD} = V_{MP}$ = 14 V and I_{OUT} = 3 mA.
Line regulation of the voltage regulator ΔV_{OUT1} is defined by the equation $\Delta V_{OUT1} = V_{OUT2} - V_{OUT1}$ where V_{OUT1} is the output voltage when $V_{DD} = V_{MP}$ = 6 V and I_{OUT} = 3 mA, and V_{OUT2} is the output voltage when $V_{DD} = V_{MP}$ = 18 V and I_{OUT} = 3 mA.
Load regulation of the regulator is defined by the equation $\Delta V_{OUT2} = V_{OUT3} - V_{OUT}$ where V_{OUT3} is the output voltage when $V_{DD} = V_{MP}$ = 14 V and I_{OUT} = 5 μA.

3. Battery monitor amp and pin current for VC1 to VC3 (Test circuit 3)

Voltage gain of the battery monitor amp for each cell is defined by the input offset voltage and the measurement result provided from the VBATOUT pin for the combination of the CTL3 pin and CTL4 pin expressed by the following table at the condition where V1 = V2 = V3 = V4 = 3.5 V. Pin current for VC1 to VC3, I_{VCn} and I_{VCnN} are at the same time measured.

Table 8

CTL3 pin status	CTL4 pin status	VBATOUT pin output	VCn (n = 1, 2, 3) pin current
V_{CTL3H} min.	V_{CTL4H} min.	V_{OFF1}	I_{VC1} at VC1 pin
V_{CTL3H} min.	Open	V_{BAT1}	−
V_{CTL3H} min.	V_{CTL4L} max.	V_{OFF2}	I_{VC2} at VC2 pin
Open	V_{CTL4H} min.	V_{BAT2}	−
Open	Open	V_{OFF3}	I_{VC3} at VC3 pin
Open	V_{CTL4L} max.	V_{BAT3}	−
V_{CTL3L} max.	V_{CTL4H} min.	V_{OFF4}	I_{VCnN} at VCn pin (n = 1, 2, 3)
V_{CTL3L} max.	Open	V_{BAT4}	−

Voltage gain of the battery monitor amp for each cell is calculated by the equation
GAMPn = $(V_{BATn} - V_{OFFn}) / Vn$ (n = 1 to 4)

4. Overcharge detection voltages, overcharge detection hysteresis, overdischarge detection voltages, overdischarge detection hysteresis, and overcurrent detection voltages (Test circuit 4)

4. 1 Overcharge detection voltages, hysteresis voltages, and overdischarge detection voltages

In the following $V_{MP} = V_{DD}$ and the CDT pin is open.
The COP pin and the DOP pin should provide "Low", which is a voltage equal to $V_{DD} \times 0.1$ V or lower, in the condition that V1 = V2 = V3 = V4 = 3.5 V.
The overcharge detection voltage V_{CU1} is defined by the voltage at which COP pin voltage becomes "High", which is a voltage equal to VDD $\times$ 0.9 V or higher, when the voltage V1 is gradually increased from the starting condition V1 = 3.5 V. The overcharge release voltage V_{CL1} is defined by the voltage at which COP pin voltage becomes "Low" when the voltage V1 is gradually decreased. The hysteresis voltage of the overcharge detection V_{HC1} is then defined by the difference between the overcharge detection voltage V_{CU1} and the overcharge release voltage V_{CL1}.

The overdischarge detection voltage V_{DL1} is defined by the voltage at which DOP pin voltage becomes "High" when the voltage V1 is gradually decreased from the starting condition V1 = 3.5 V. The overdischarge release voltage V_{DU1} is defined by the voltage at which DOP pin voltage becomes "Low" when the voltage V1 is gradually increased. The hysteresis of the overdischarge detection voltage V_{HD1} is then defined by the difference between the overdischarge release voltage V_{DU1} and the overdischarge detection voltage V_{DL1}.
Other overcharge detection voltage V_{CUn}, hysteresis voltage of overcharge detection V_{HCn}, overdischarge detection voltage V_{DLn}, and hysteresis of the overdischarge detection voltage V_{HDn} (for n = 2 to 4) are defined in the same manner as in the case for n = 1.

4. 2 Overcurrent detection voltages

Starting condition is V1 = V2 = V3 = V4 = 3.5 V, VMP = VDD, and the CDT pin is open. The DOP pin voltage thus provides "Low"
The overcurrent detection voltage 1, VIOV1 is defined by the voltage difference VDD − VMP at which the DOP pin voltage becomes "High" when the voltage of VMP pin is decreased.

Starting condition for measuring the overcurrent detection voltage 2 and 3 is V1 = V2 = V3 = V4 = 3.5 V, $V_{MP} = V_{DD}$ and the CDT pin voltage $V_{CDT} = V_{SS}$. The DOP pin voltage thus provides "Low".
The overcurrent detection voltage 2, V_{IOV2} is defined by the voltage difference V_{DD}–V_{MP} at which the DOP pin voltage becomes "High" when the voltage of VMP pin is decreased.
The overcurrent detection delay time 2, t_{IOV2} is a time needed for the DOP pin to become "High" from "Low" when the VM pin voltage is changed quickly to V_{IOV2} min.–0.2 V from the starting condition $V_{MP} = V_{DD}$.
The overcurrent detection voltage 3, V_{IOV3} is defined by the voltage of the VM pin at which the DOP pin voltage becomes "High" when the voltage of VMP pin is decreased at the speed 10 V / ms.
The overcurrent detection delay time 3, t_{IOV3} is a time needed for the DOP pin to become "High" from "Low" when the VM pin voltage is changed quickly to V_{IOV3} min.–0.2 V from the starting condition $V_{MP} = V_{DD}$.

5. CTL1 pin current, overcharge detection delay, overdischarge detection delay, and overcurrent detection delay 1 (Test circuit 5)

Starting condition is V1 = V2 = V3 = V4 = 3.5 V and $V_{MP} = V_{DD}$.
Current that flows between the CTL1 pin and V_{SS} is the CTL1 pin current I_{CTL1L}.

The overcharge detection delay time t_{CU} is a time needed for the COP pin voltage to change from "Low" to "High" just after the V1 voltage is rapidly increased from 3.5 V to 4.5 V.

The overdischarge detection delay time t_{DL} is a time needed for the DOP pin voltage to change from "Low" to "High" just after the V1 voltage is rapidly decreased from 3.5 V to 1.5 V.

The overcurrent detection delay time 1 is a time needed for the DOP pin voltage to change from "Low" to "High" just after the VMP pin voltage is decreased from V_{DD} to V_{DD}−0.35 V when V1 = 3.5 V.

6. Input voltages for CTL1 and CTL2 (Test circuit 6)

Starting condition is V1 = V2 = V3 = V4 = 3.5 V.
Pin voltages of the COP and the DOP should be "High" when $V_{CTL1} = V_{CTL1H}$ min. and CTL2 is OPEN.
Pin voltages of the COP and the DOP should be "Low" when $V_{CTL1} = V_{CTL1L}$ max. and CTL2 is OPEN.
Pin voltage of the COP is "High" and the pin voltage of the DOP is "Low" when $V_{CTL1} = V_{CTL1L}$ max. and $V_{CTL2} = V_{CTL2H}$ min.
Pin voltage of the COP is "Low" and the pin voltage of the DOP is "High" when $V_{CTL1} = V_{CTL1L}$ max. and $V_{CTL2} = V_{CTL2L}$ max.

7. 0 V battery charge starting charger voltage and 0 V battery charge inhibition battery voltage (Test circuit 7)

One of the 0 V battery charge starting charger voltage and 0 V battery charge inhibition battery voltage is applied to each product according to the 0V battery charging function.

Starting condition is V1 = V2 = V3 = V4 = 0 V for a product in which 0 V battery charging is available.
The COP pin voltage should be lower than V_{0CHA} max.−1 V when the VMP pin voltage $V_{MP} = V_{0CHA}$ max.

Starting condition is V1 = V2 = V3 = V4 = V_{0INH} for a product in which 0 V battery charging is inhibited.
The COP pin voltage should be higher than V_{MP}−1 V when the VMP pin voltage V_{MP} = 24 V.

8. Internal resistance (Test circuit 8)

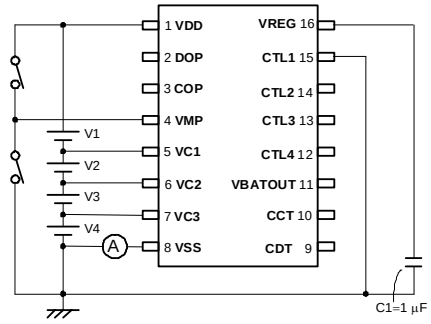
The resistance between VDD and VMP is R_{VDM} and is calculated by the equation $R_{VDM} = V_{DD} / I_{VDM}$ where I_{VDM} is a VMP pin current after V_{MP} is changed to V_{SS} from the starting condition V1 = V2 = V3 = V4 = 3.5 V and $V_{MP} = V_{DD}$.
The resistance between VSS and VMP is R_{VSM} and is calculated by the equation $R_{VSM} = V_{DD} / I_{VSM}$ where I_{VSM} is a VMP pin current at the condition V1 = V2 = V3 = V4 = 1.8 V and $V_{MP} = V_{DD}$.

9. Pin current for CTL2 to CTL4, COP, DOP, VBATOUT (Test circuit 9)

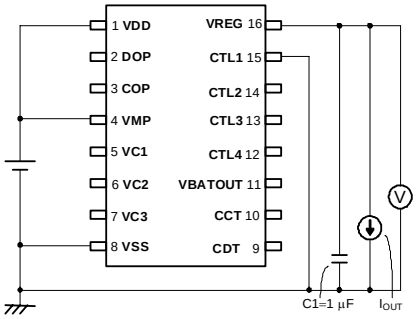
Starting condition is V1 = V2 = V3 = V4 = 3.5 V.
Pin current for CTL2 at "High" is I_{CTL2H} and is obtained by setting $V_{CTL2} = V_{OUT}$.
Pin current for CTL2 at "Low" is I_{CTL2L} and is obtained by setting $V_{CTL2} = V_{SS}$.
Pin current for CTL3 and CTL4 can be obtained in the same manner as in the CTL2.

Pin current for COP at "High" is I_{COH} and is obtained by setting V1 = V2 = V3 = V4 = 6 V, $V_{MP} = V_{DD}$, and $V_{COP} = V_{DD}$. And pin current for COP at "Low" is I_{COL} and is obtained by setting V1 = V2 = V3 = V4 = 3.5 V, $V_{MP} = V_{DD}$, and V_{COP} = 0.5 V.
Pin current for DOP at "Low" is I_{DOL} and is obtained by setting V1 = V2 = V3 = V4 = 3.5 V, $V_{MP} = V_{DD}$, and V_{DOP} = 0.5 V.
And pin current for COP at "High" is I_{COH} and is obtained by setting V1 = V2 = V3 =V4 = 3.5 V, $V_{MP} = V_{DD}$–1 V, and $V_{DOP} = V_{DD}$–0.5 V.

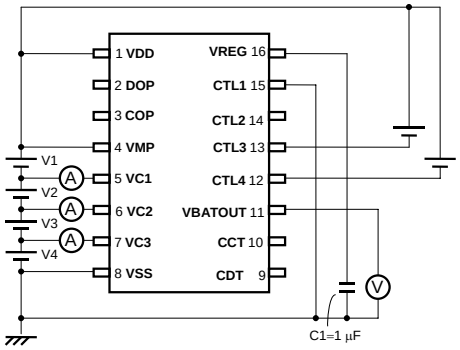
Pin current for VBATOUT at "High" is I_{VBATH} and is obtained by setting CTL3 and CTL4 are open and $V_{BATOUT} = V_{OFF3}$–0.5 V. And pin current for VBATOUT at "Low" is I_{VBATL} and is obtained by setting $V_{BATOUT} = V_{OFF3}$+0.5 V.



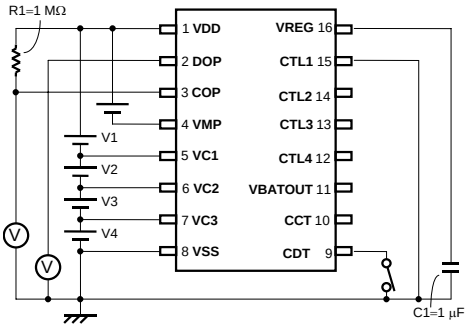
Test circuit 1



Test circuit 2

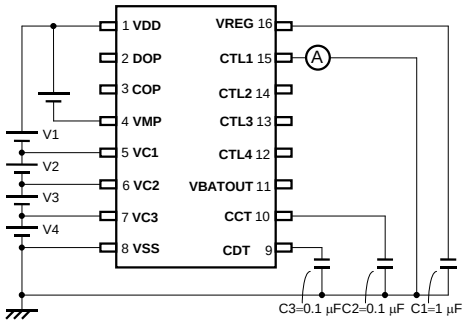


Test circuit 3

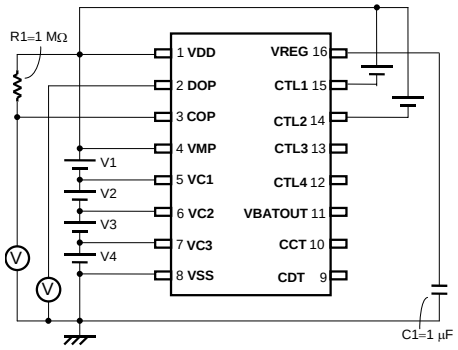


Test circuit 4

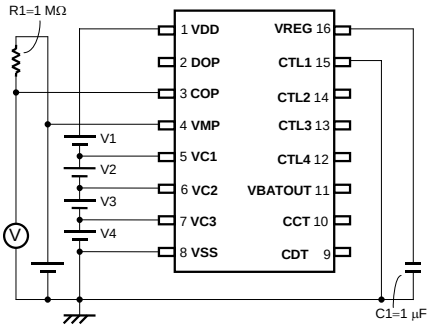
Figure 5 (1 / 2)



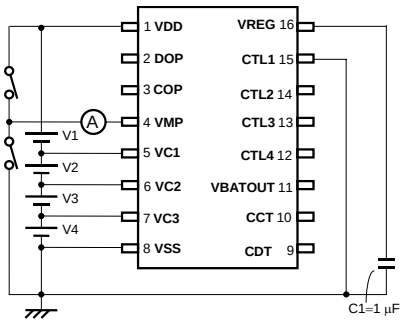
Test circuit 5



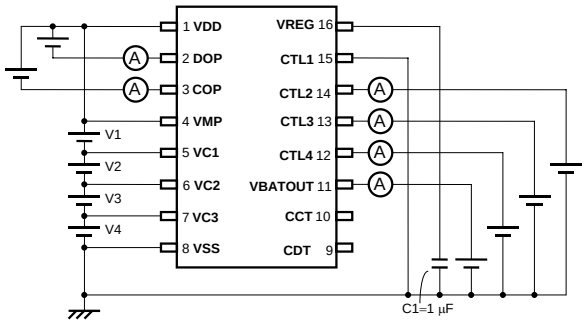
Test circuit 6



Test circuit 7



Test circuit 8



Test circuit 9

Figure 5 (2 / 2)

■ Operation

1. Battery protection circuit

Remark Refer to "■ **Battery Protection IC Connection Example**".

Battery protection protects batteries from overcharge and overdischarge, and also protects external FETs from overcurrent.

1. 1 Normal status

When all of the battery voltages are in the range from V_{DLn} to V_{CUn} and the discharge current is lower than a specified value (the VMP pin voltage is lower than V_{IOV1}), the charging and discharging FETs are turned on.

1. 2 Overcharge status

When any one of the battery voltages becomes higher than V_{CUn} and the state continues for t_{CU} or longer, the COP pin becomes high impedance and is pulled up to EB+ pin voltage by an external resistor, and the charging FET is turned off to stop charging. The overcharge status is released when one of the following two conditions holds.

(a) All battery voltages become lower than $V_{CUn} + V_{HCn}$.

(b) $V_{DD}-V_{MP}>V_{IOV1}$ (A load is connected, and discharging starts.)

1. 3 Overdischarge status

When any one of the battery voltages becomes lower than V_{DLn} and the state continues for t_{DL} or longer, the DOP pin voltage becomes V_{DD} level, and the discharging FET is turned off to stop discharging. This is the overdischarge status.

1. 4 Power down status

After stopping discharging due to overdischarge status, the S-8243 enters power down status. In this status, almost all circuits of the S-8243 are stopped to save current consumption. The current consumption becomes lower than I_{PDN}. In the power down status, the VMP pin is pulled down to V_{SS} level by the internal R_{VSM} resistor. In power down status, output pin voltages are fixed at the following levels.

(a) COP	High-Z	(Charging FET is turned off)
(b) DOP	V_{DD}	(Discharging FET is turned off)
(c) VREG	V_{SS}	(Voltage regulator circuit is off)
(d) VBATOUT	V_{SS}	(Battery voltage monitor amp circuit is off)

The power down status is released when the following condition holds.

(a) $V_{MP}>V_{IOV3}$ (A charger is connected, and charging starts.)

The overdischarging status is released when the following condition holds.

(a) All of the battery voltages are V_{DLn} or higher, and the VMP pin voltage is VDD / 2 or higher. (A charger is connected.)

1. 5 Overcurrent status

The S-8243 has three overcurrent detection levels (V_{IOV1}, V_{IOV2} and V_{IOV3}) and three overcurrent detection delay times (t_{IOV1}, t_{IOV2} and t_{IOV3}) corresponding to each overcurrent detection levels. When the discharging current becomes higher than a specified value (the voltage between V_{DD} and V_{MP} is greater than V_{IOV1}) and the state continues for t_{IOV1} or longer, the S-8243 enters the overcurrent status in which the DOP pin voltage becomes V_{DD} level to turn off the discharging FET to stop discharging, the COP pin becomes high impedance and is pulled up to EB+ pin voltage by an external resistor to turn off the charging FET to stop charging, and the VMP pin is pulled up to V_{DD} voltage by the internal resistor R_{VDM}. Operation of two other overcurrent detection levels (V_{IOV2} and V_{IOV3}) and overcurrent detection delay times (t_{IOV2} and t_{IOV3}) is the same as that for V_{IOV1} and t_{IOV1}.

The overcurrent status is released when the following condition holds.

(a) $V_{MP}> \{V_{IOV3} / (1-V_{IOV3}) \times 3 / 5-2 / 5\} \times R_{VDM}$ (A load is released, and the impedance between the EB− and EB+ pin becomes higher.)

1. 6 0 V battery charging function

Regarding the charging of a self-discharged battery (0 V battery) the S-8243 has two functions from which one should be selected.

(a) 0 V battery charging is allowed (0 V battery charging is available)
When a charger voltage is higher than V_{0CHA}, 0 V battery can be charged.

(b) 0 V battery charging is forbidden (0 V battery charging is impossible)
When one of the battery voltages is lower than V_{0INH}, 0 V battery can not be charged.

Caution When the VDD pin voltage is lower than minimum of V_{DSOP}, the operation of S-8243 series is not guaranteed.

1. 7 Delay time setting

Overcharge detection delay times (t_{CU1} to t_{CU4}) are determined by the external capacitor at the CCT pin. Overdischarge detection delay times (t_{DL1} to t_{DL4}) and overcurrent detection delay time 1 (t_{IOV1}) are determined by the external capacitor at CDT pin. Overcurrent detection delay time 2,3 (t_{IOV2}, t_{IOV3}) are fixed internally.

S-8243AAC, S-8243AAD, S-8243BAE, S-8243BAF, S-8243BAH

		min.	typ.	max.	
t_{CU} [s]	= Delay factor (	5	10	15	) × C_{CT} [μF]
t_{DL} [ms]	= Delay factor (	500	1000	1500	) × C_{DT} [μF]
t_{IOV1} [ms]	= Delay factor (	50	100	150	) × C_{DT} [μF]

S-8243BAD

		min.	typ.	max.	
t_{CU} [s]	= Delay factor (	5	10	15	) × C_{CT} [μF]
t_{DL} [ms]	= Delay factor (	555	1110	2220	) × C_{DT} [μF]
t_{IOV1} [ms]	= Delay factor (	33.1	66.2	132	) × C_{DT} [μF]

2. Voltage regulator circuit

Built-in voltage regulator can be used to drive a micro computer, etc. The voltage regulator supplies voltage of 3.3 V (3 mA maximum) and an external capacitor is needed.

Caution In the power down status the voltage regulator output is pulled down to the V_{SS} level by an internal resistor.

3. Battery monitor amp circuit

Battery monitor amp sends information of the batteries to a microcomputer. The battery monitor amp output is controlled and selected by CTL3 and CTL4 pins to give the following two voltages.

(a) V_{BATn} = GAMPn × $V_{BATTERYn}$ + V_{OFFn} where GAMPn is the n-th voltage gain of the amp, $V_{BATTERYn}$ is the n-th battery voltage, and V_{OFFn} is the n-th offset voltage of the amp.

(b) N-th offset voltage V_{OFFn}
Each battery voltage **$V_{BATTERYn}$** (n = 1 to 4) is thus calculated by following equation.
$V_{BATTERYn}$ = (V_{BATn} − V_{OFFn}) / GAMPn (n = 1, 2, 3, 4)

After the state of CTL3 and CTL4 are changed, a time between 25 μs and 250 μs is needed for the battery monitor amp to become stable.

Caution In the power down status the battery monitor amp output is the V_{SS} level.

4. CTL pins

The S-8243 has four control pins. The CTL1 and CTL2 pins are used to control the COP and DOP pin output voltages. CTL1 takes precedence over CTL2. CTL2 takes precedence over the battery protection circuit. The CTL3 and CTL4 pins are used to control the VBATOUT pin output voltage.

Table 9 CTL1 and CTL2 Mode

Input		Output	
CTL1 pin	CTL2 pin	External discharging FET	External charging FET
High	High	OFF	OFF
High	Open	OFF	OFF
High	Low	OFF	OFF
Open	High	OFF	OFF
Open	Open	OFF	OFF
Open	Low	OFF	OFF
Low	High	Normal*1	OFF*2
Low	Open	Normal*1	Normal*1
Low	Low	OFF	Normal*1

***1.** States are controlled by voltage detection circuit.
***2.** Off state is brought after the overcharge detection delay time t_{CU}.

Table 10 CTL3 and CTL4 Mode

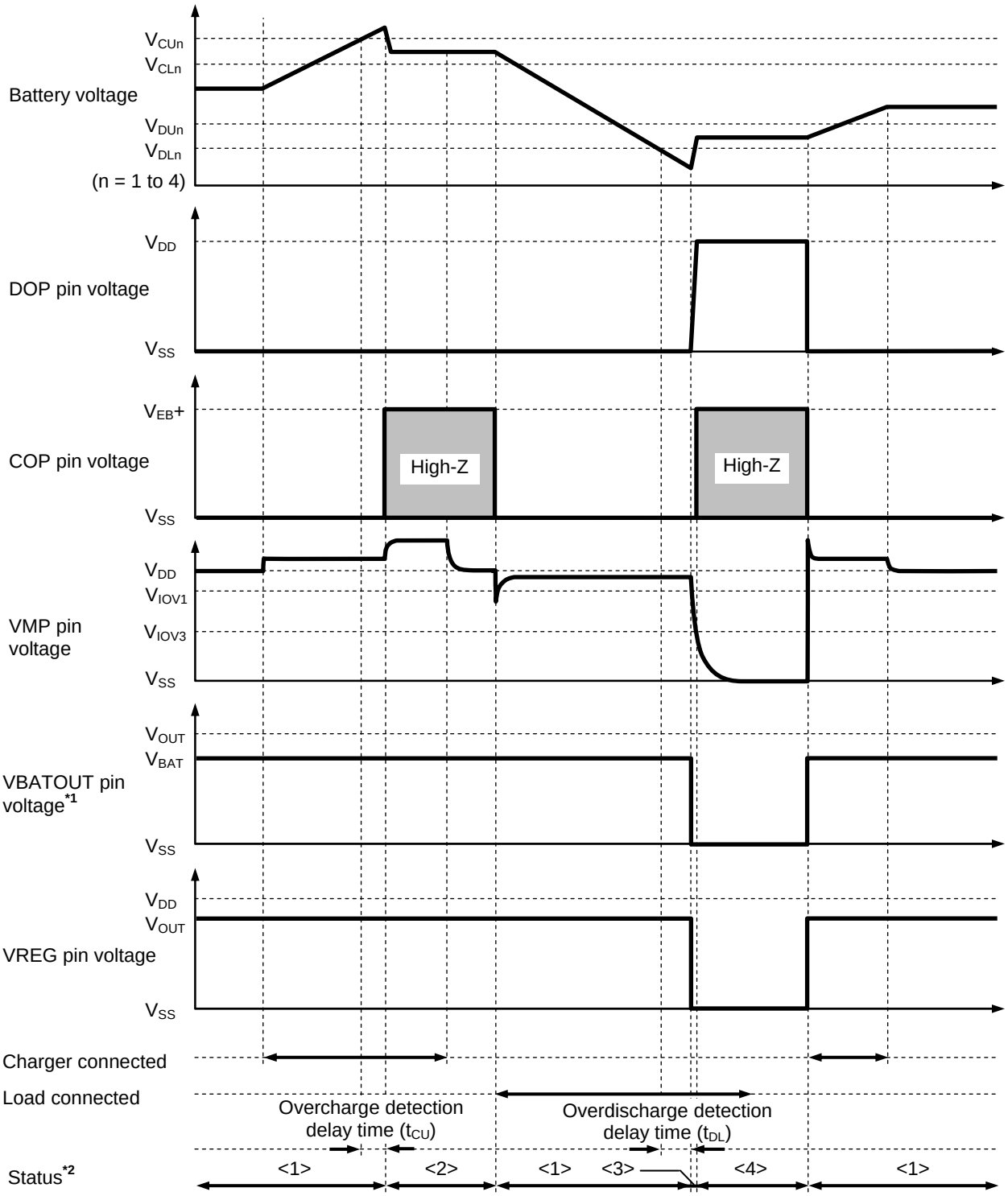
Input		Output	
CTL3 pin	CTL4 pin	V_{BATOUT} (A series)	V_{BATOUT} (B series)
High	High	V1 Offset	V1 Offset
High	Open	V1 × 0.2 + V1 Offset	V1 × 0.2 + V1 Offset
High	Low	Don't use.	V2 Offset
Open	High	Don't use.	V2 × 0.2 + V2 Offset
Open*1	Open*1	V2 Offset	V3 Offset
Open	Low	V2 × 0.2 + V2 Offset	V3 × 0.2 + V3 Offset
Low	High	V3 Offset	V4 Offset
Low	Open	V3 × 0.2 + V3 Offset	V4 × 0.2 + V4 Offset
Low	Low	Don't use.	Don't use.

***1.** CTL3 and CTL4 pins should be open when a microcomputer is not used.

Caution Please note unexpected behavior might occur when electrical potential difference between the CTL pin ("L" level) aMSS is generated through the external filter (R_{VSS} and C_{VSS}) as a result of input voltage fluctuations.

■ Timing Charts

1. Overcharge detection, Over discharge detection

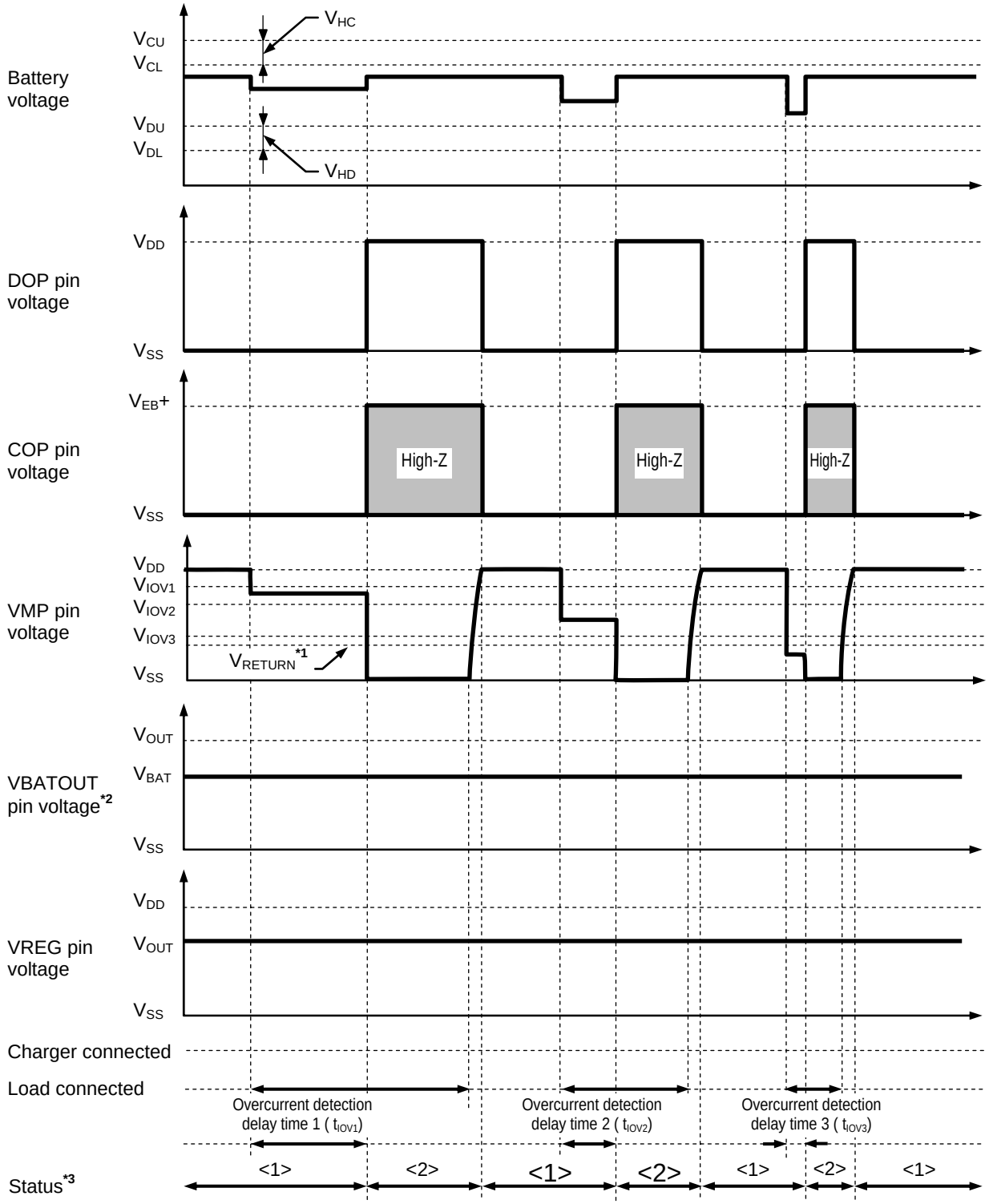


***1.** State depends on CTL3 and CTL4 input levels. Refer to **Figure 9**.
***2.** <1>: Normal status, <2>: Overcharge status, <3>: Overdischarge status, <4>: Power down status

Remark The charger is assumed to charge with a constant current. V_{EB}+ indicates the open voltage of the charger.

Figure 6

2. Overcurrent detection

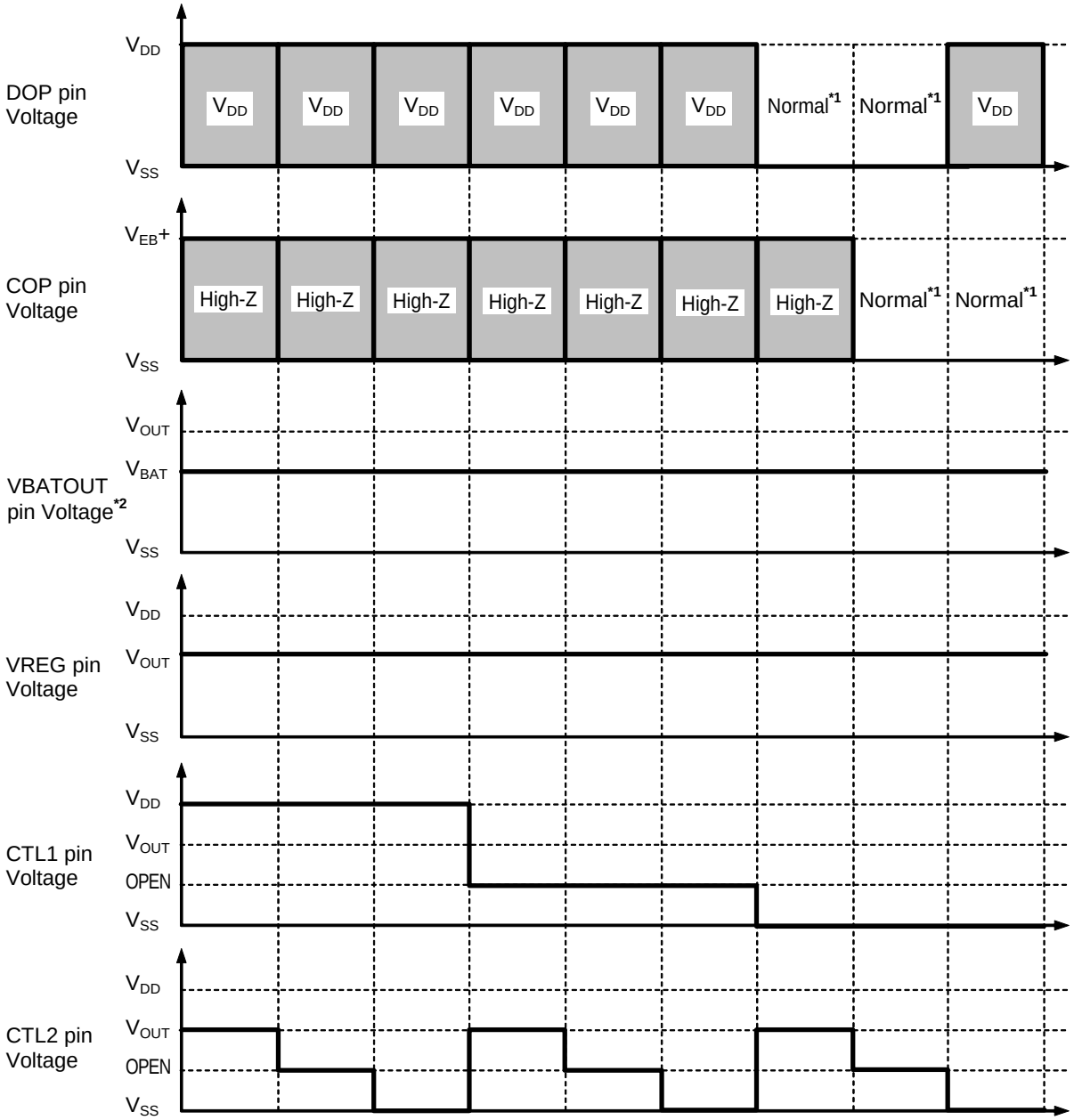


***1.** $V_{RETURN} = V_{DD} / 6$ (typ.)
***2.** State depends on CTL3 and CTL4 input levels. Refer to **Figure 9**.
***3.** <1>: Normal status, <2>: Overcurrent status

Remark The charger is assumed to charge with a constant current. V_{EB}+ indicates the open voltage of the charger.

Figure 7

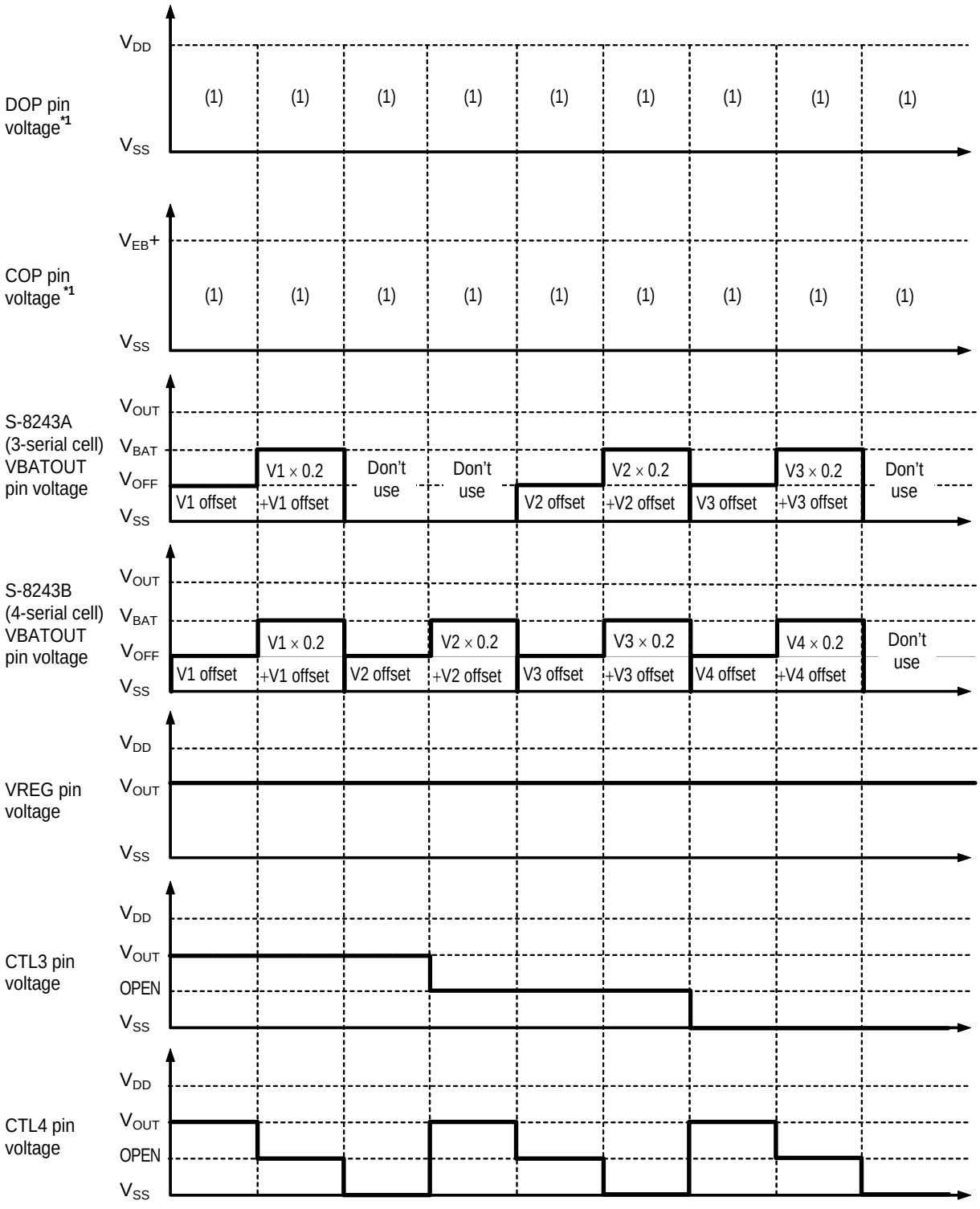
3. CTL1, CTL2 pin voltage



***1.** State depends on each battery voltage and the VMP pin voltage.
***2.** State depends on CTL3 and CTL4 input levels. Refer to **Figure 9**.

Figure 8

4. CTL3, TL4 pin voltage



***1.** State depends on CTL1 and CTL2 and each battery voltage and the VMP pin voltage. Refer to **Figure 6** to **8**.

Figure 9

■ Battery Protection IC Connection Example

1. S-8243A Series

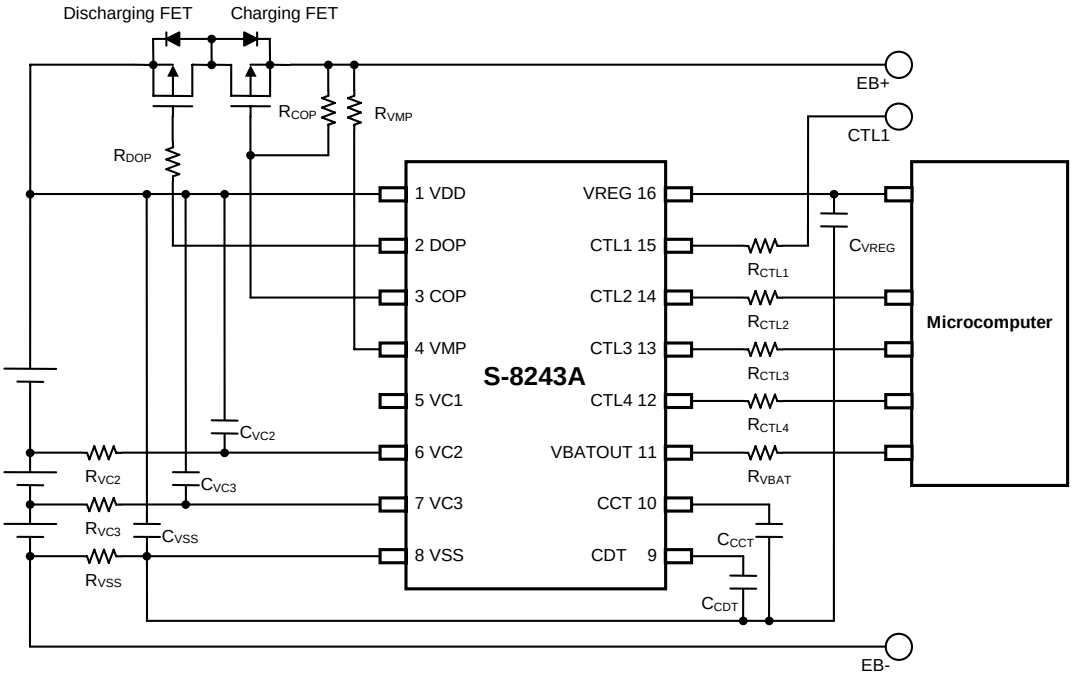


Figure 10

Table 11 Constants for External Components

No.	Part	Typ.	Range	Unit
1	R_{VC2}	1	0.51 to 1[*1]	kΩ
2	R_{VC3}	1	0.51 to 1[*1]	kΩ
3	R_{VSS}	10	2.2 to 10[*1]	Ω
4	R_{DOP}	5.1	2 to 10	kΩ
5	R_{COP}	1	0.1 to 1	MΩ
6	R_{VMP}	5.1	1 to 10	kΩ
7	R_{CTL1}	1	1 to 100	kΩ
8	R_{CTL2}	1	1 to 10	kΩ
9	R_{CTL3}	1	1 to 10	kΩ
10	R_{CTL4}	1	1 to 10	kΩ
11	R_{VBAT}	0	0 to 100	kΩ
12	C_{VC2}	0.047	0.047 to 0.22[*1]	μF
13	C_{VC3}	0.047	0.047 to 0.22[*1]	μF
14	C_{VSS}	4.7	2.2 to 10[*1]	μF
15	C_{CCT}	0.1	More than 0.01	μF
16	C_{CDT}	0.1	More than 0.02	μF
17	C_{VREG}	4.7	0.68 to 10	μF

***1.** Please set up a filter constant to be $R_{VSS} \times C_{VSS} \geq 22\ \mu F \bullet \Omega$ and to be
$R_{VC2} \times C_{VC2} = R_{VC3} \times C_{VC3} = R_{VSS} \times C_{VSS}$.

Caution1. No resistance should be inserted in the power supply pin VDD.
2. The above constants are subject to change without prior notice.
3. It has not been confirmed whether the operation is normal or not in circuits other than the above example of connection. In addition, the example of connection shown above and the constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.

2. S-8243B Series

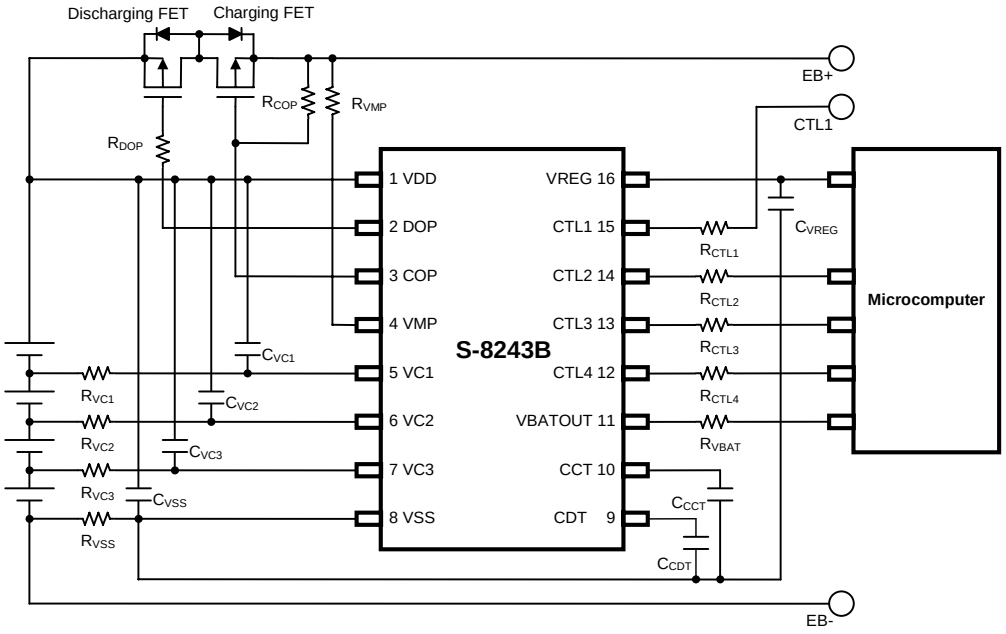


Figure 11

Table 12 Constants for External Components

No.	Part	Typ.	Range	Unit
1	R_{VC1}	1	0.51 to 1*1	kΩ
2	R_{VC2}	1	0.51 to 1*1	kΩ
3	R_{VC3}	1	0.51 to 1*1	kΩ
4	R_{VSS}	10	2.2 to 10*1	Ω
5	R_{DOP}	5.1	2 to 10	kΩ
6	R_{COP}	1	0.1 to 1	MΩ
7	R_{VMP}	5.1	1 to 10	kΩ
8	R_{CTL1}	1	1 to 100	kΩ
9	R_{CTL2}	1	1 to 10	kΩ
10	R_{CTL3}	1	1 to 10	kΩ
11	R_{CTL4}	1	1 to 10	kΩ
12	R_{VBAT}	0	0 to 100	kΩ
13	C_{VC1}	0.047	0.047 to 0.22*1	μF
14	C_{VC2}	0.047	0.047 to 0.22*1	μF
15	C_{VC3}	0.047	0.047 to 0.22*1	μF
16	C_{VSS}	4.7	2.2 to 10*1	μF
17	C_{CCT}	0.1	More than 0.01	μF
18	C_{CDT}	0.1	More than 0.02	μF
19	C_{VREG}	4.7	0.68 to 10	μF

***1.** Please set up a filter constant to be $R_{VSS} \times C_{VSS} \geq 22\ \mu F \bullet \Omega$ and to be
$R_{VC1} \times C_{VC1} = R_{VC2} \times C_{VC2} = R_{VC3} \times C_{VC3} = R_{VSS} \times C_{VSS}$.

Caution1. No resistance should be inserted in the power supply pin VDD.
2. The above constants are subject to change without prior notice.
3. It has not been confirmed whether the operation is normal or not in circuits other than the above example of connection. In addition, the example of connection shown above and the constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.

■ Precautions

- Pay attention to the operating conditions for input/output voltage and load current so that the power loss in the IC does not exceed the package power dissipation.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- Seiko Instruments Inc. shall not be responsible for any patent infringement by products including the S-8243 series, the method of using the S-8243 series in such products, the product specifications or the country of destination thereof.

■ The Example of Application Circuit

1. S-8243A Series

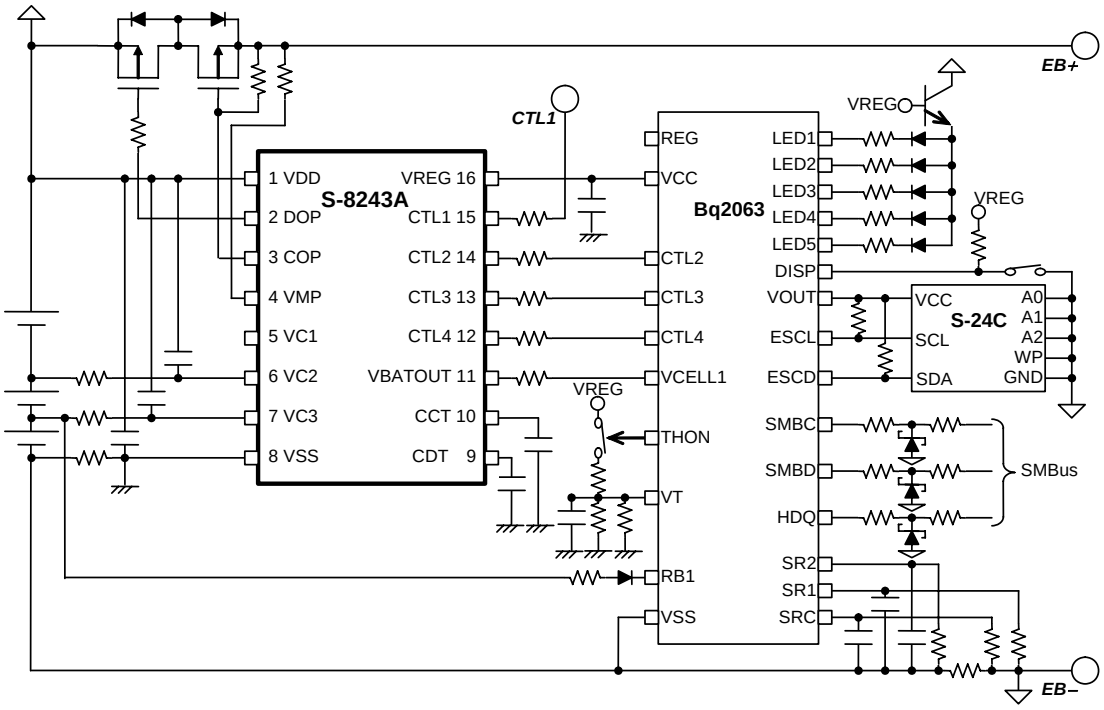


Figure 12

2. S-8243B Series

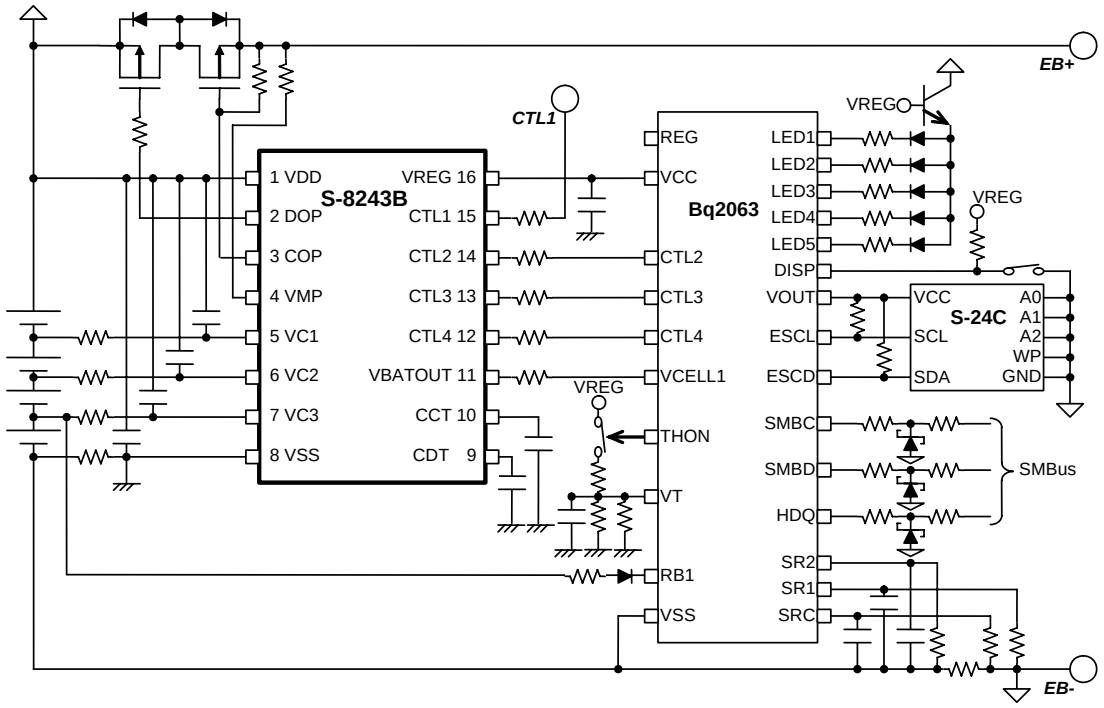


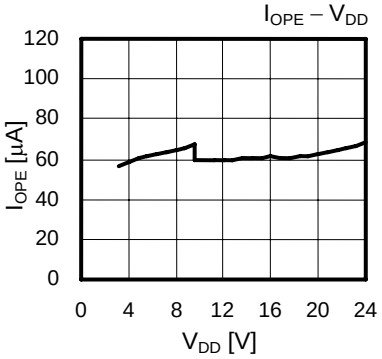
Figure 13

Caution The above connection example will not guarantee successful operation. Perform thorough evaluation using the actual application.

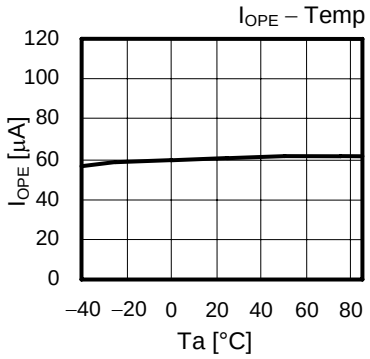
■ Characteristics (Typical Data)

1. Current consumption

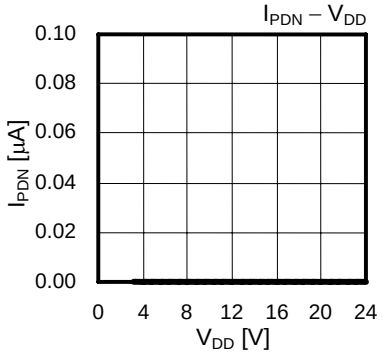
S-8243BAF



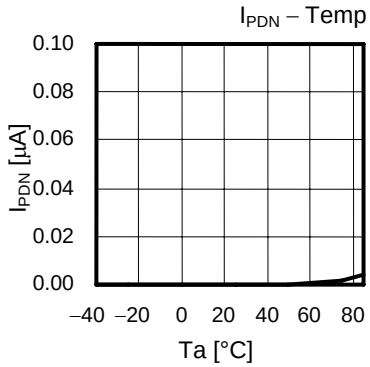
S-8243BAF



S-8243BAF

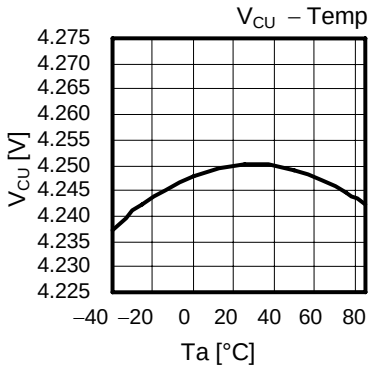


S-8243BAF

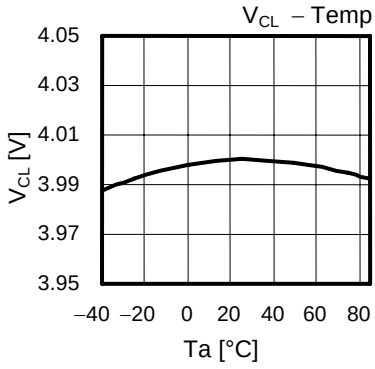


2. Overcharge detection/release voltage, overdischarge detection/release voltage, overcurrent detection voltages, and delay times

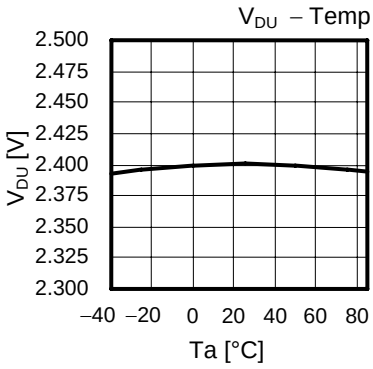
S-8243BAF



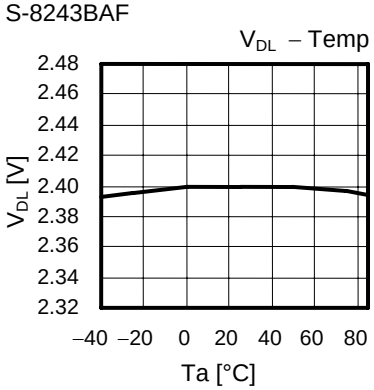
S-8243BAF



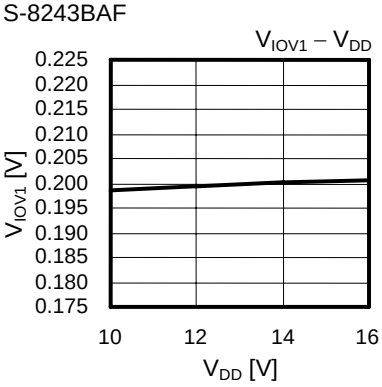
S-8243BAF



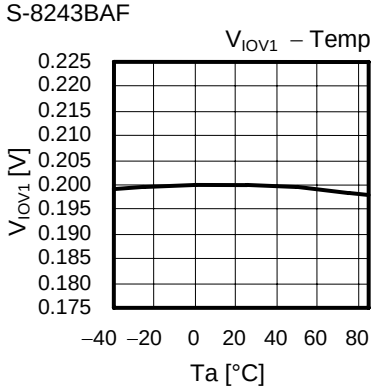
S-8243BAF



S-8243BAF

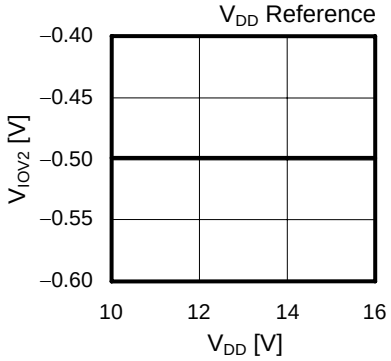


S-8243BAF



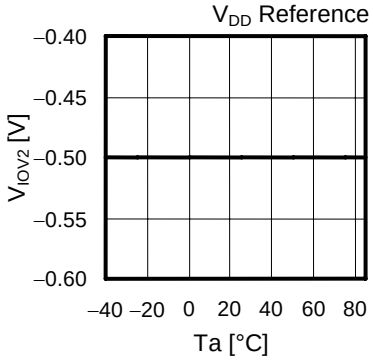
S-8243BAF

V_{IOV2} – V_{DD}
V_{DD} Reference



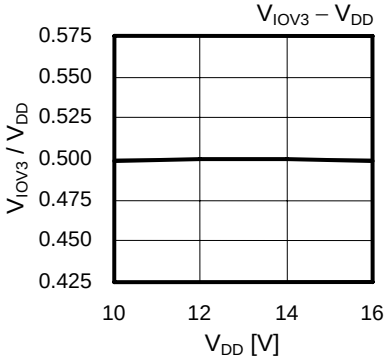
S-8243BAF

V_{IOV2} – Temp
V_{DD} Reference



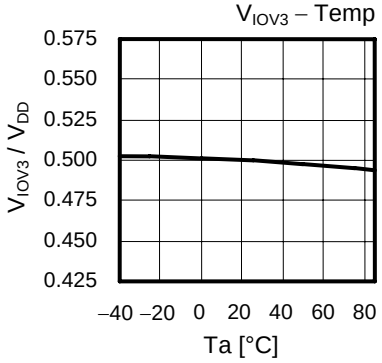
S-8243BAF

V_{IOV3} – V_{DD}



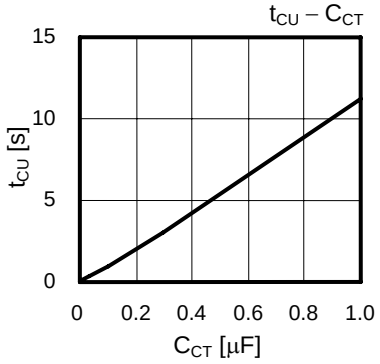
S-8243BAF

V_{IOV3} – Temp



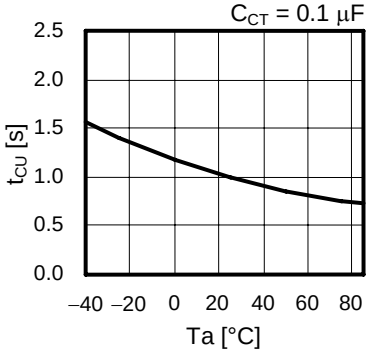
S-8243BAF

t_{CU} – C_{CT}



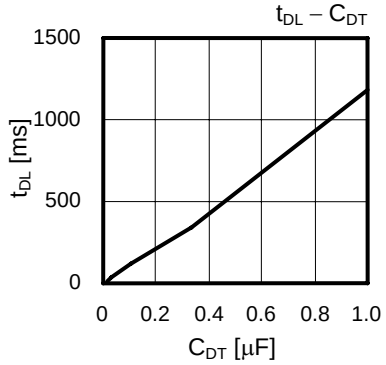
S-8243BAF

t_{CU} – Temp
C_{CT} = 0.1 µF



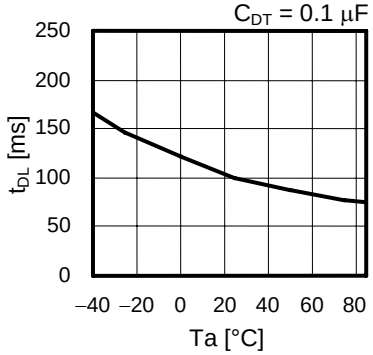
S-8243BAF

t_{DL} – C_{DT}



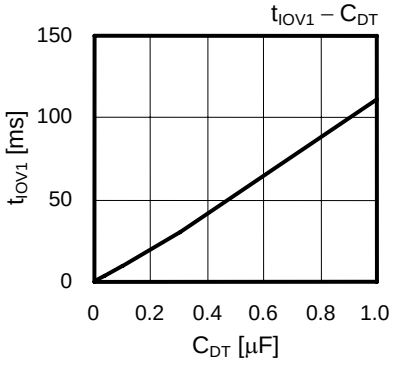
S-8243BAF

t_{DL} – Temp
C_{DT} = 0.1 µF



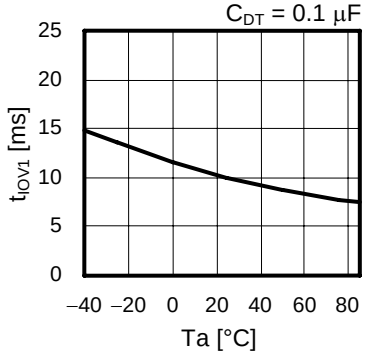
S-8243BAF

t_{IOV1} – C_{DT}



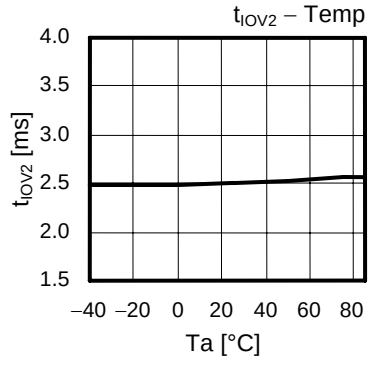
S-8243BAF

t_{IOV1} – Temp
C_{DT} = 0.1 µF



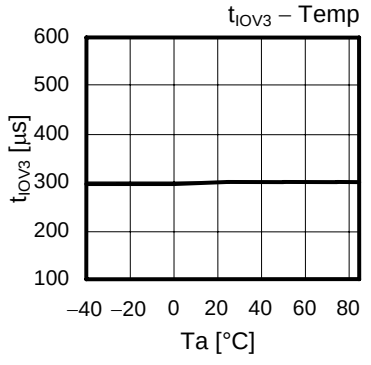
S-8243BAF

t_{IOV2} – Temp



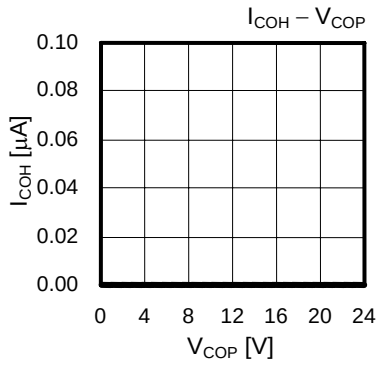
S-8243BAF

t_{IOV3} – Temp

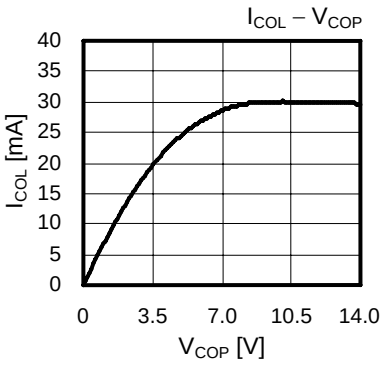


3. COP / DOP pin current

S-8243BAF



S-8243BAF



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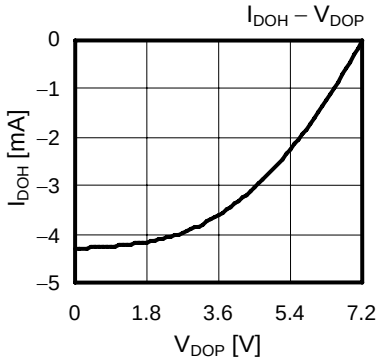
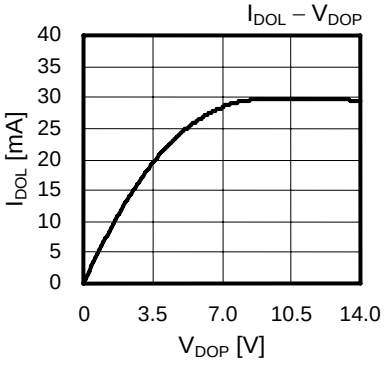
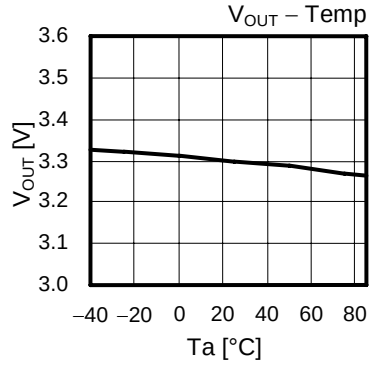


S-8243BAF



4. Voltage regulator

S-8243BAF



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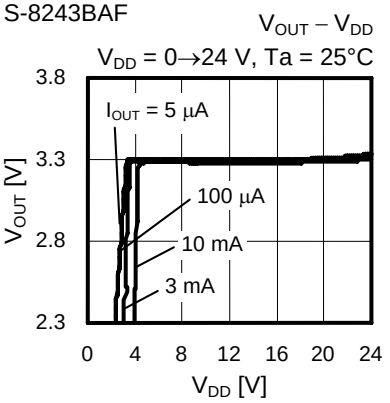

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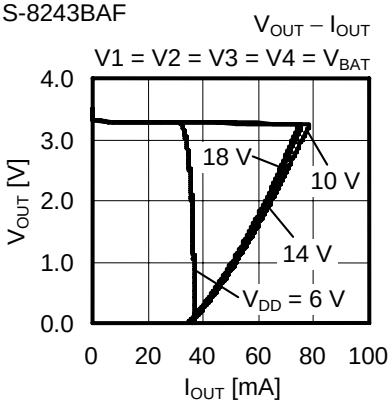
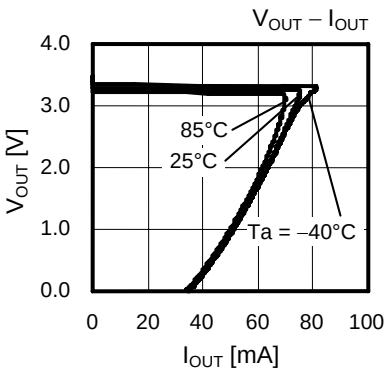


S-8243BAF

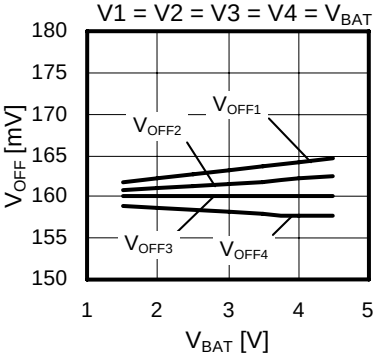


5. Battery monitor amp

S-8243BAF

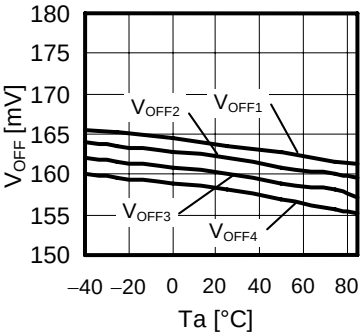
$V_{OFF} - V_{BAT}$

V1 = V2 = V3 = V4 = V_{BAT}



S-8243BAF

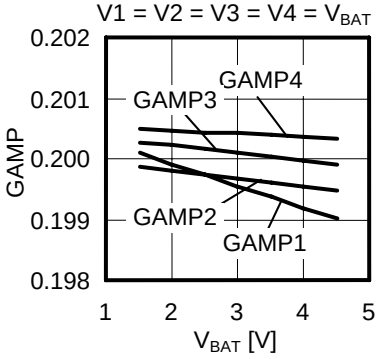
V_{OFF} – Temp



S-8243BAF

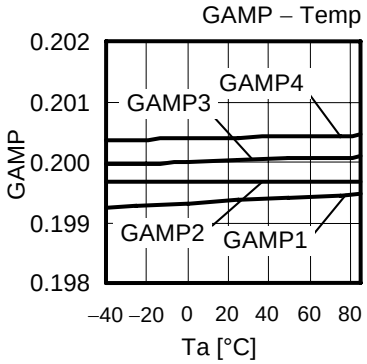
GAMP – V_{BAT}

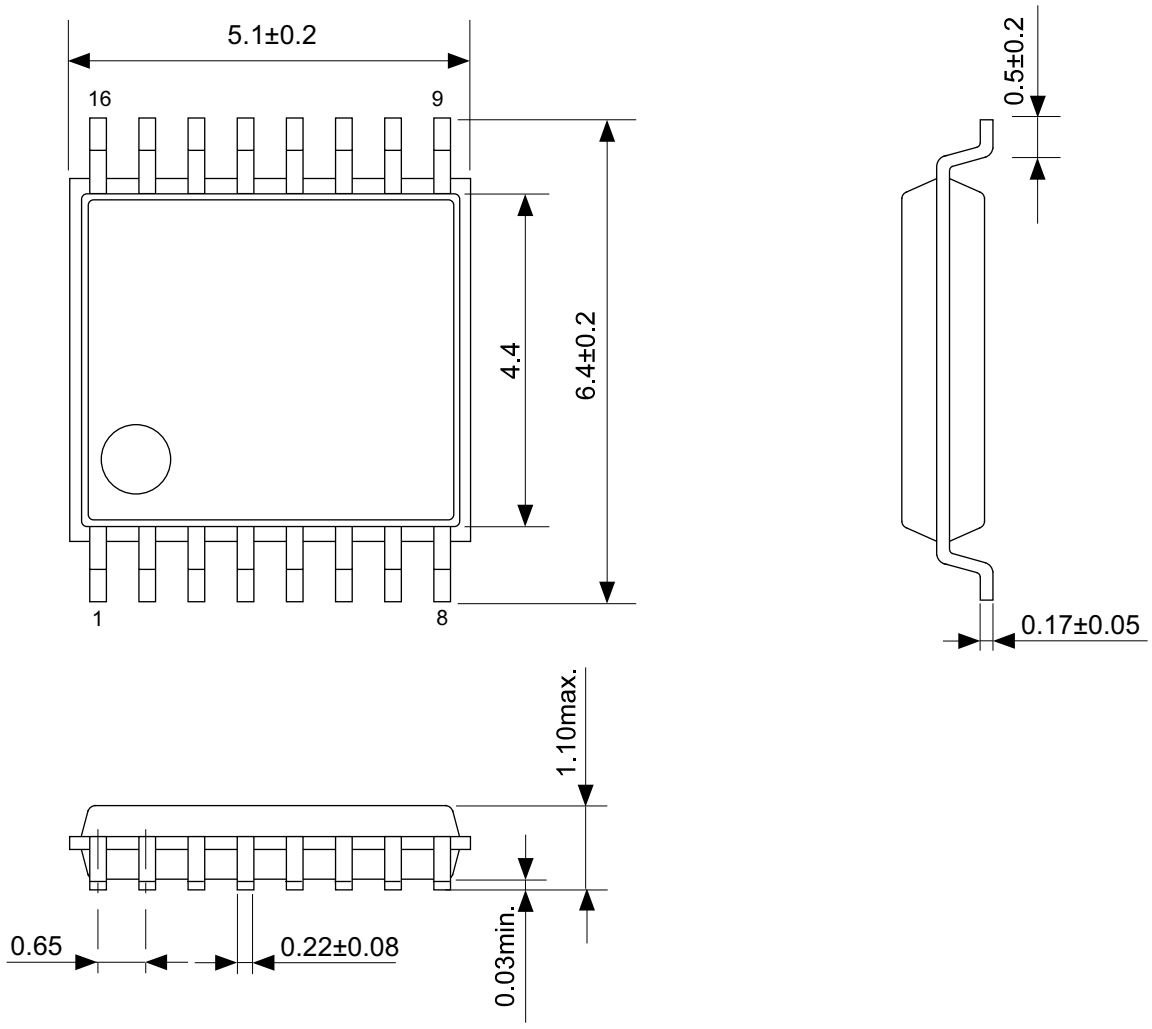
V1 = V2 = V3 = V4 = V_{BAT}



S-8243BAF

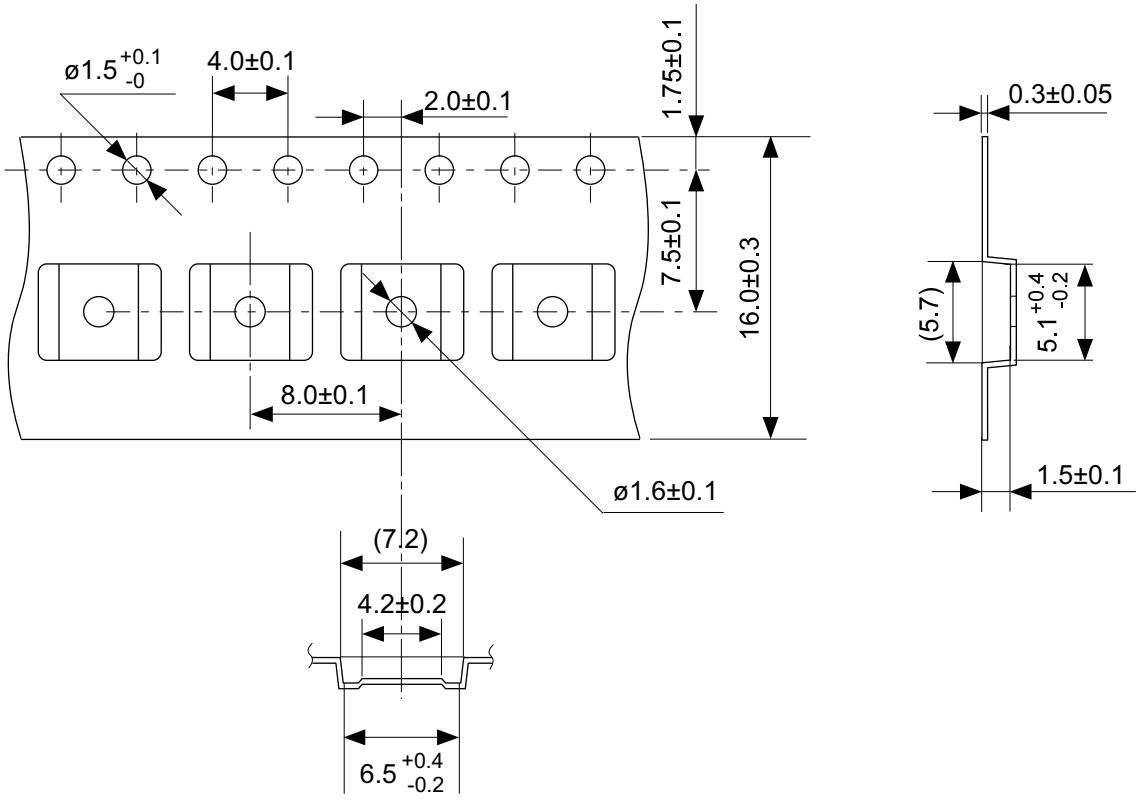
GAMP – Temp

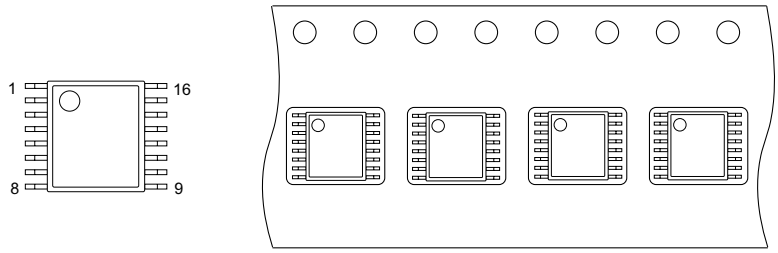




No. FT016-A-P-SD-1.1

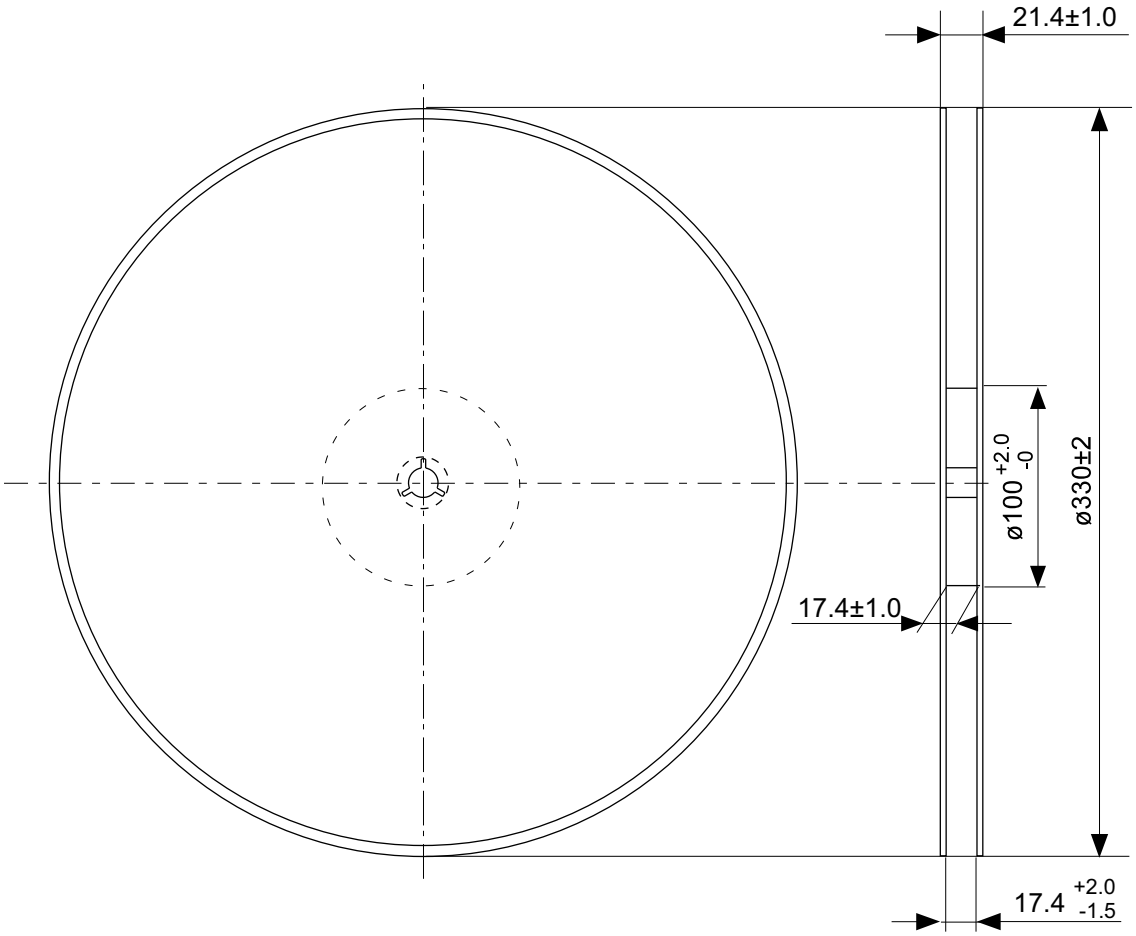
TITLE	TSSOP16-A-PKG Dimensions
No.	FT016-A-P-SD-1.1
SCALE	
UNIT	mm
Seiko Instruments Inc.	



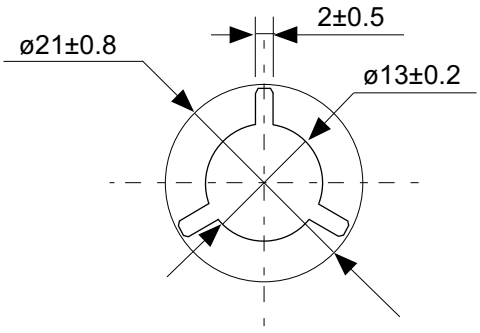


No. FT016-A-C-SD-1.1

TITLE	TSSOP16-A-Carrier Tape
No.	FT016-A-C-SD-1.1
SCALE	
UNIT	mm
Seiko Instruments Inc.	

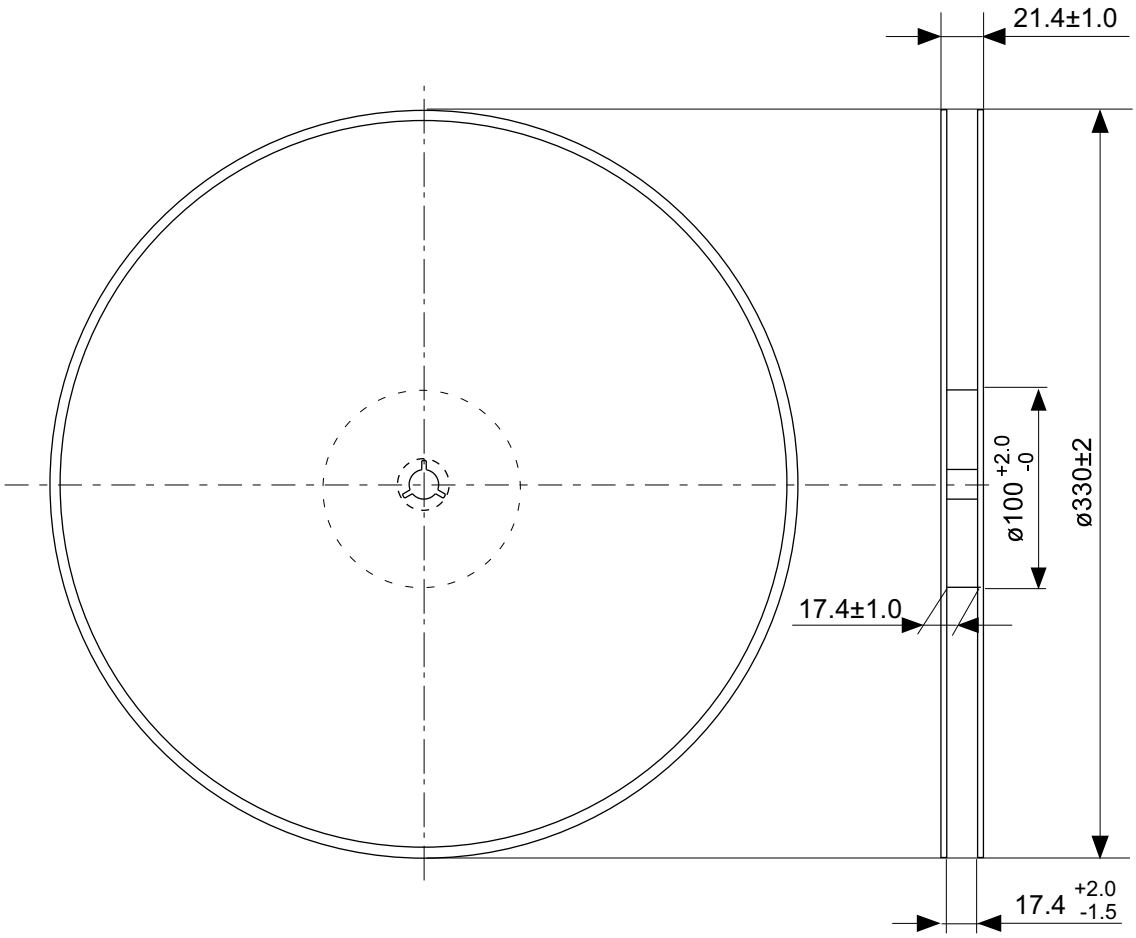


Enlarged drawing in the central part

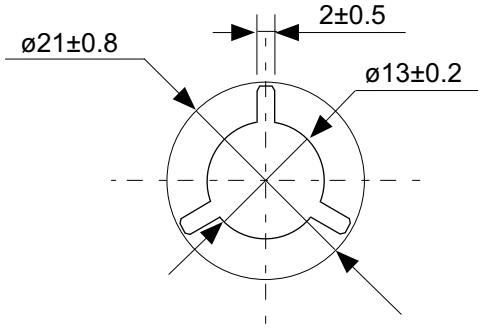


No. FT016-A-R-SD-2.0

TITLE	TSSOP16-A- Reel		
No.	FT016-A-R-SD-2.0		
SCALE		QTY.	2,000
UNIT	mm		
Seiko Instruments Inc.			



Enlarged drawing in the central part



No. FT016-A-R-S1-1.0

TITLE	TSSOP16-A- Reel		
No.	FT016-A-R-S1-1.0		
SCALE		QTY.	4,000
UNIT	mm		
Seiko Instruments Inc.			

Seiko Instruments Inc.
www.sii-ic.com

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Стандарт Электрон Связь

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