

# FDU5N50NZTU

## Power MOSFET, N-Channel, UniFET™ II

500 V, 4 A, 1.5 Ω

UniFET II MOSFET is ON Semiconductor's high voltage MOSFET family based on advanced planar stripe and DMOS technology. This advanced MOSFET family has the smallest on-state resistance among the planar MOSFET, and also provides superior switching performance and higher avalanche energy strength. In addition, internal gate-source ESD diode allows UniFET II MOSFET to withstand over 2 kV HBM surge stress. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.

### Features

- $R_{DS(on)} = 1.38 \Omega$  (Typ.) @  $V_{GS} = 10$  V,  $I_D = 2$  A
- Low Gate Charge (Typ. 9 nC)
- Low  $C_{rss}$  (Typ. 4 pF)
- 100% Avalanche Tested
- Improved dv/dt Capability
- ESD Improved Capability
- These Devices are Pb-Free and are RoHS Compliant

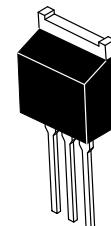
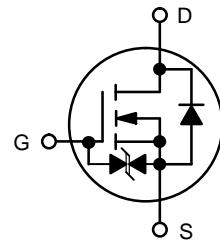
### Applications

- LCD / LED TV
- Lighting
- Charger / Adapter



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IPAK3  
CASE 369AR

### ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 2 of this data sheet.

# FDU5N50NZTU

## MAXIMUM RATINGS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Value	Unit
$V_{DSS}$	Drain-to-Source Voltage	500	V
$V_{GSS}$	Gate-to-Source Voltage	$\pm 25$	V
$I_D$	Drain Current	Continuous ( $T_C = 25^\circ\text{C}$ )	4
		Continuous ( $T_C = 100^\circ\text{C}$ )	2.4
$I_{DM}$	Drain Current	Pulsed (Note 1)	A
$E_{AS}$	Single Pulse Avalanche Energy (Note 2)	304	mJ
$I_{AR}$	Avalanche Current (Note 1)	4	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	6.2	mJ
$dv/dt$	Peak Diode Recovery (Note 3)	10	V/ns
$P_D$	Power Dissipation	$T_C = 25^\circ\text{C}$	62
		Derate Above $25^\circ\text{C}$	0.5 W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering Purposes (1/8" from case for 5 seconds)	300	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2.  $I_{AS} = 4 \text{ A}$ ,  $V_{DD} = 50 \text{ V}$ ,  $L = 38 \text{ mH}$ ,  $R_G = 25 \Omega$ , starting  $T_J = 25^\circ\text{C}$ .
3.  $I_{SD} \leq 4 \text{ A}$ ,  $di/dt \leq 200 \text{ A}/\mu\text{s}$ ,  $V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$ .

## THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	2.0	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	90	

## PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDU5N50NZTU	FDU5N50NZ	IPAK	Tube	N/A	N/A	75 units

# FDU5N50NZTU

**ELECTRICAL CHARACTERISTICS** ( $T_C = 25^\circ\text{C}$  unless otherwise specified)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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## OFF CHARACTERISTICS

$\text{BV}_{\text{DSS}}$	Drain-to-Source Breakdown Voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0 \text{ V}, T_J = 25^\circ\text{C}$	500	—	—	V
$\Delta \text{BV}_{\text{DSS}/\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$ , Referenced to $25^\circ\text{C}$	—	0.5	—	$^\circ\text{C}$
$I_{\text{DSS}}$	Zero Gate Voltage Drain Current	$V_{DS} = 500 \text{ V}, V_{GS} = 0 \text{ V}$	—	—	1	$\mu\text{A}$
		$V_{DS} = 400 \text{ V}, T_C = 125^\circ\text{C}$	—	—	10	
$I_{\text{GSS}}$	Gate-to-Body Leakage Current	$V_{GS} = \pm 25 \text{ V}, V_{DS} = 0 \text{ V}$	—	—	$\pm 10$	nA

## ON CHARACTERISTICS

$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu\text{A}$	3.0	—	5.0	V
$R_{DS(\text{on})}$	Static Drain-to-Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 2 \text{ A}$	—	1.38	1.5	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 20 \text{ V}, I_D = 2 \text{ A}$	—	3.54	—	S

## DYNAMIC CHARACTERISTICS

$C_{\text{iss}}$	Input Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	—	330	440	pF
$C_{\text{oss}}$	Output Capacitance		—	50	70	
$C_{\text{rss}}$	Reverse Transfer Capacitance		—	4	6	
$Q_{\text{g(tot)}}$	Total Gate Charge at 10 V	$V_{DS} = 400 \text{ V}, I_D = 4 \text{ A}, V_{GS} = 10 \text{ V}$ (Note 4)	—	9	12	nC
$Q_{\text{gs}}$	Gate-to-Source Gate Charge		—	2	—	
$Q_{\text{gd}}$	Gate-to-Drain "Miller" Charge		—	4	—	

## SWITCHING CHARACTERISTICS

$t_{d(\text{on})}$	Turn-On Delay Time	$V_{DD} = 250 \text{ V}, I_D = 4 \text{ A}, V_{GS} = 10 \text{ V}, R_G = 25 \Omega$ (Note 4)	—	12	35	ns
$t_r$	Turn-On Rise Time		—	22	55	
$t_{d(\text{off})}$	Turn-Off Delay Time		—	28	65	
$t_f$	Turn-Off Fall Time		—	21	50	

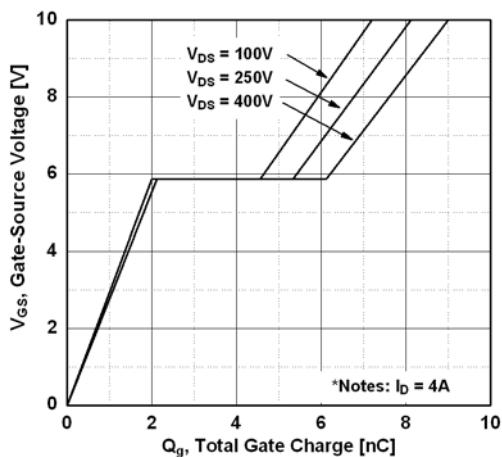
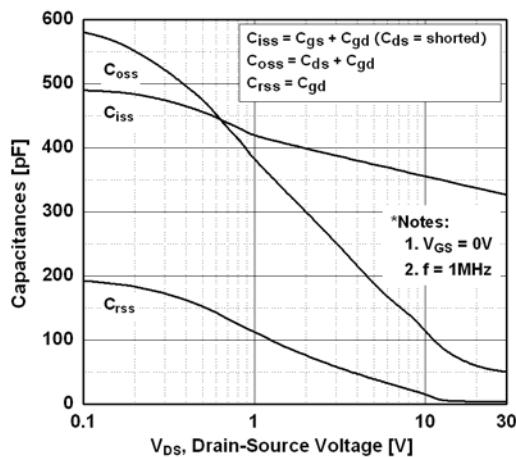
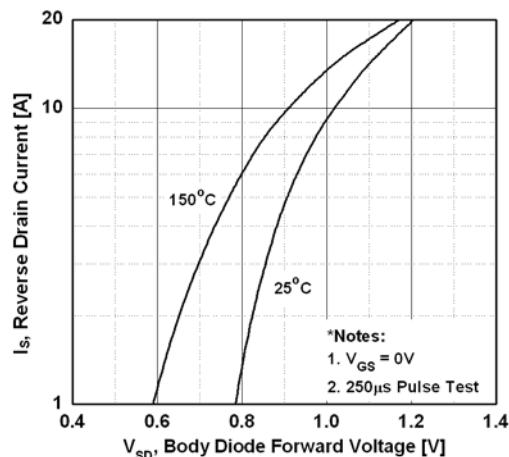
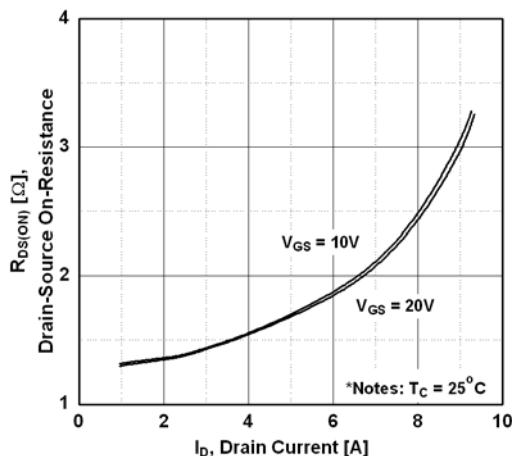
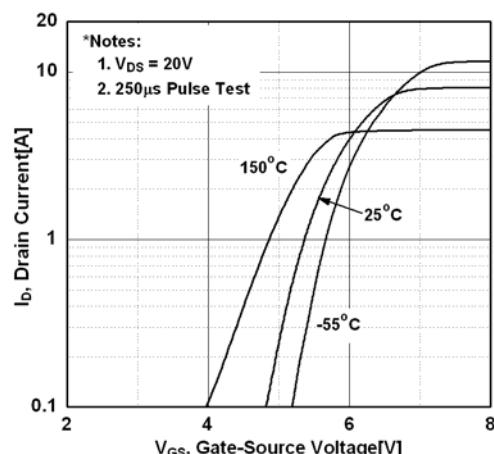
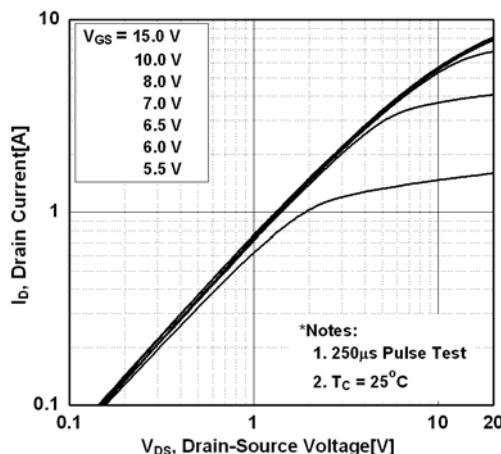
## DRAIN-SOURCE DIODE CHARACTERISTICS

$I_S$	Maximum Continuous Drain to Source Diode Forward Current	$V_{GS} = 0 \text{ V}, I_{SD} = 4 \text{ A}$	—	—	4	A
$I_{SM}$	Maximum Pulsed Drain to Source Diode Forward Current		—	—	16	
$V_{SD}$	Drain to Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{SD} = 4 \text{ A}$	—	—	1.4	V
$t_{rr}$	Reverse Recovery Time		—	210	—	
$Q_{rr}$	Reverse Recovery Charge	$V_{GS} = 0 \text{ V}, I_{SD} = 4 \text{ A}, dI_F/dt = 100 \text{ A}/\mu\text{s}$	—	1.1	—	$\mu\text{C}$

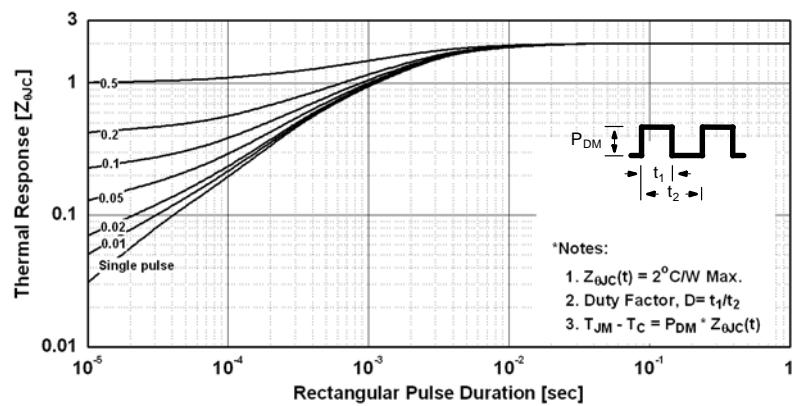
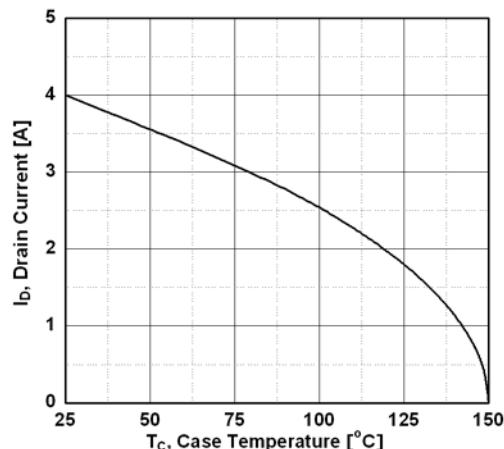
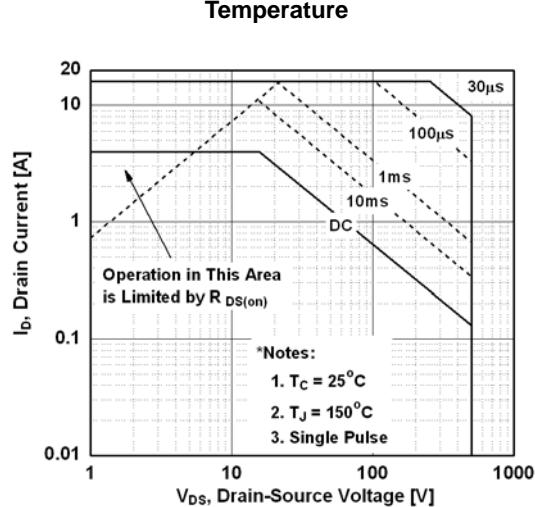
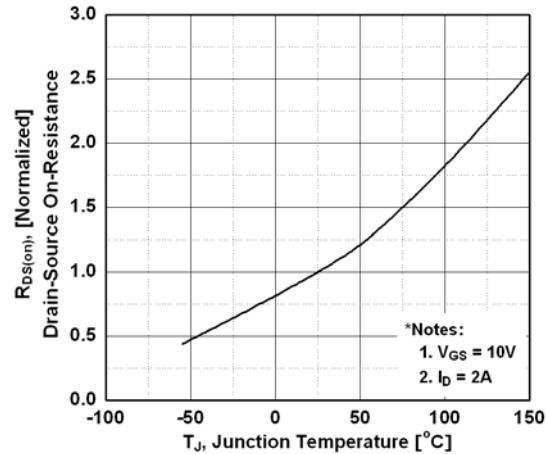
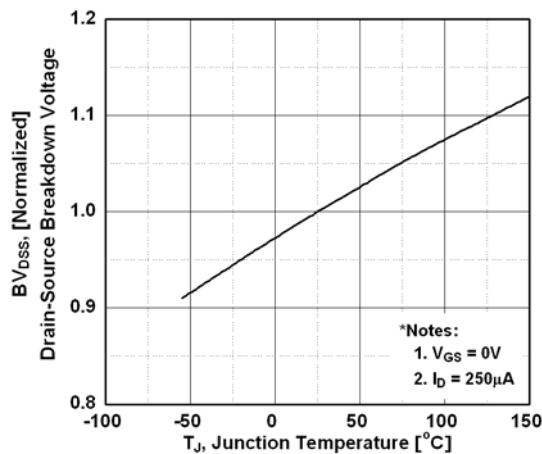
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of Operating Temperature Typical Characteristics.

## TYPICAL CHARACTERISTICS



**TYPICAL CHARACTERISTICS**



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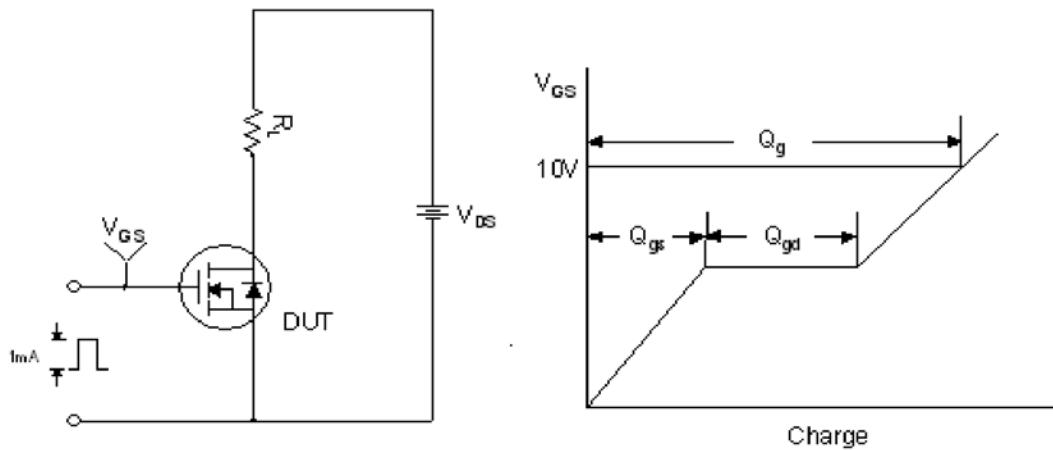


Figure 12. Gate Charge Test Circuit & Waveform

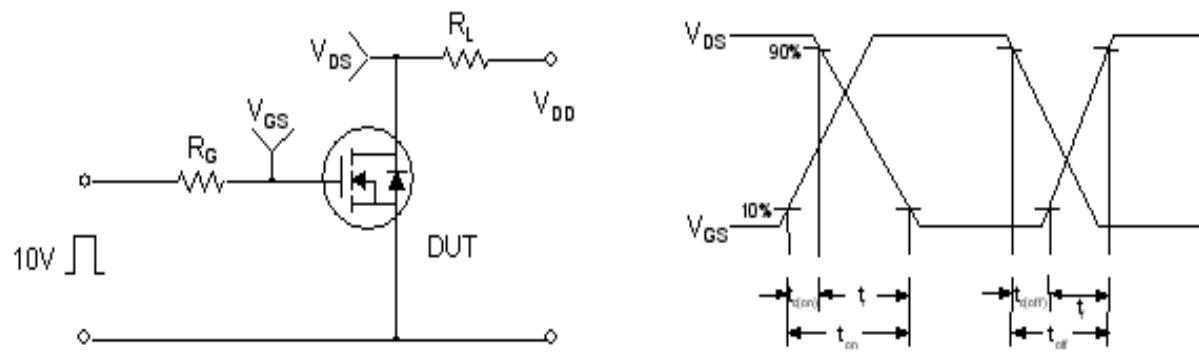


Figure 13. Resistive Switching Test Circuit & Waveforms

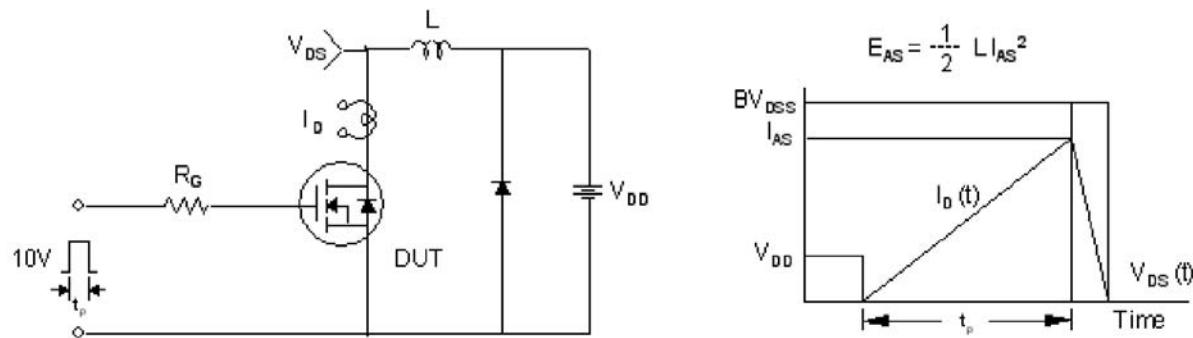


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

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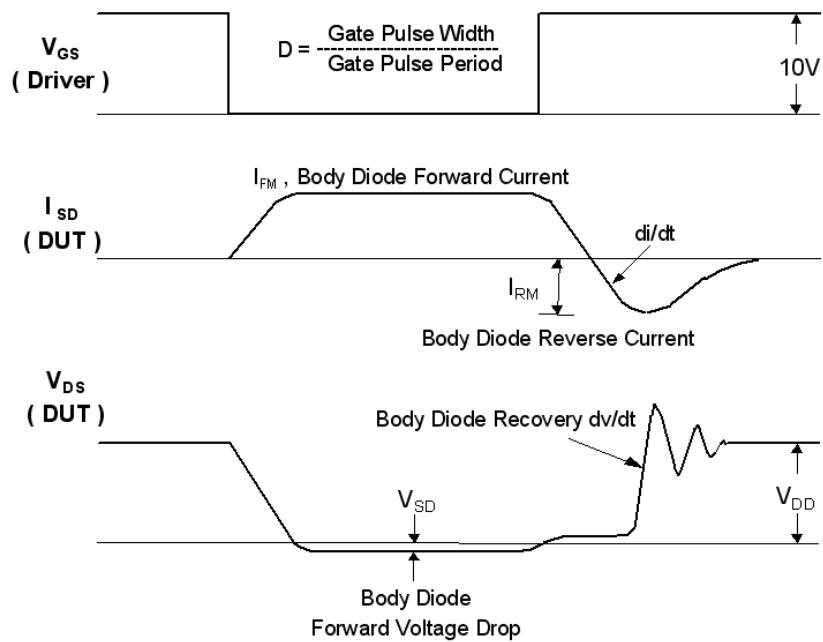
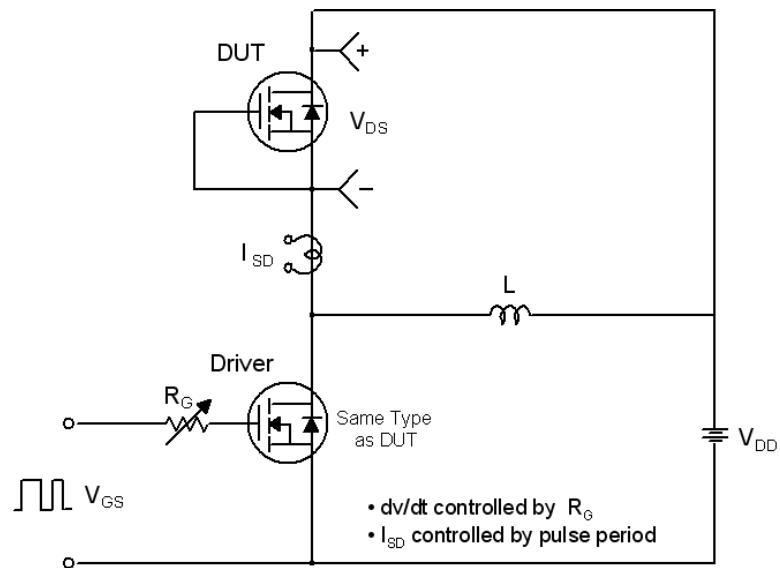
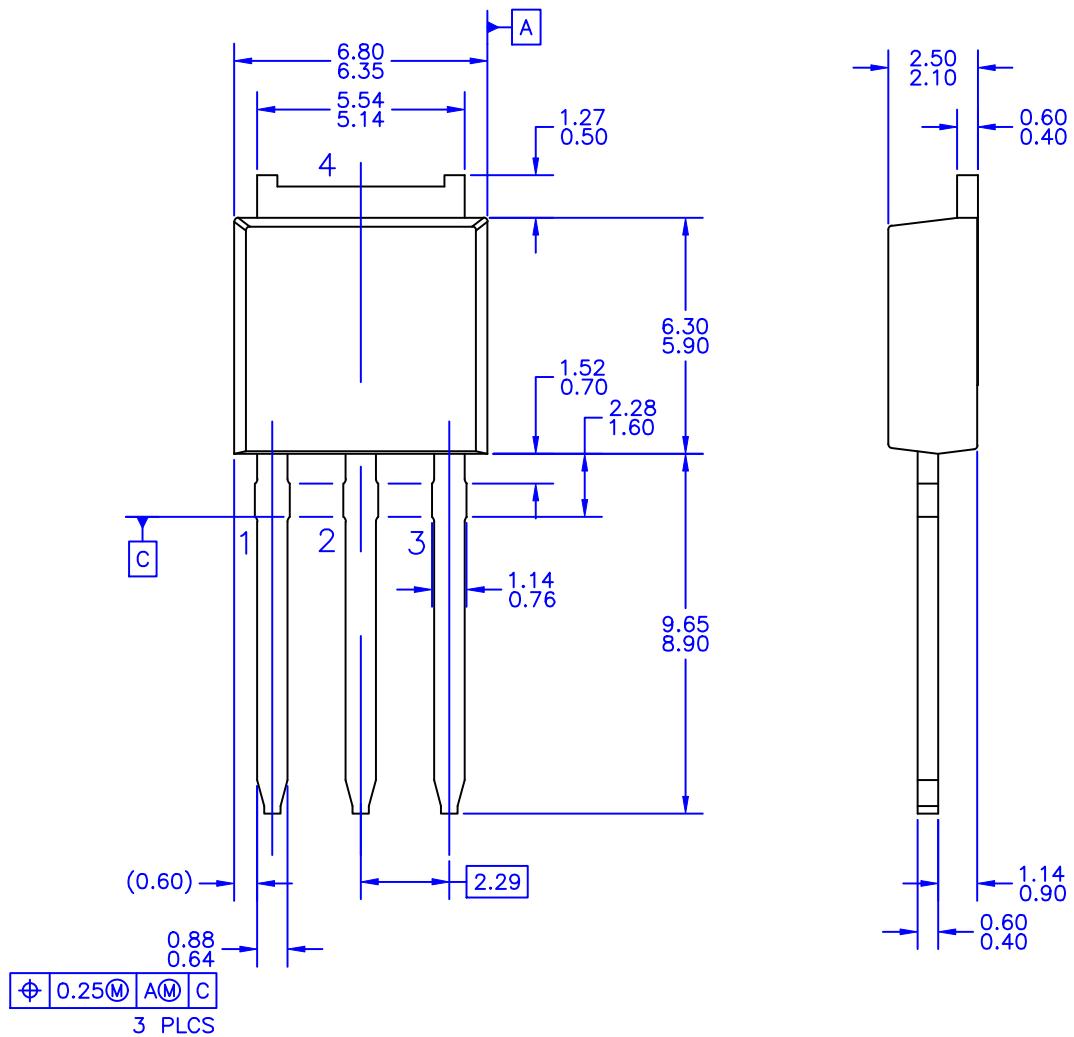


Figure 15. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms

**FDU5N50NZTU**

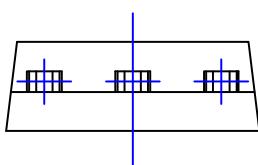
## PACKAGE DIMENSIONS

**DPAK3 (IPAK)  
CASE 369AR  
ISSUE O**



NOTES: UNLESS OTHERWISE SPECIFIED

- A) ALL DIMENSIONS ARE IN MILLIMETERS.
  - B) THIS PACKAGE CONFORMS TO JEDEC, TO-251,  
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  - C) DIMENSIONING AND TOLERANCING PER  
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