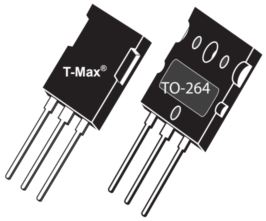
APT48M80B2
APT48M80L

800V, 49A, 0.19Ω Max

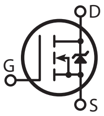
N-Channel MOSFET

Power MOS 8™ is a high speed, high voltage N-channel switch-mode power MOSFET. A proprietary planar strip design yields excellent reliability and manufacturability. Low switching loss is achieved with low input capacitance and ultra low C_{rss} "Miller" capacitance. The intrinsic gate resistance and capacitance of the poly-silicon gate structure help control slew rates during switching, resulting in low EMI and reliable paralleling, even when switching at very high frequency. Reliability in flyback, boost, forward, and other circuits is enhanced by the high avalanche energy capability.



APT48M80B2 **APT48M80L**

Single die MOSFET



FEATURES

- **Fast switching with low EMI/RFI**
- **Low $R_{DS(on)}$**
- **Ultra low C_{rss} for improved noise immunity**
- **Low gate charge**
- **Avalanche energy rated**
- **RoHS compliant**

TYPICAL APPLICATIONS

- **PFC and other boost converter**
- **Buck converter**
- **Two switch forward (asymmetrical bridge)**
- **Single switch forward**
- **Flyback**
- **Inverters**

Absolute Maximum Ratings

Symbol	Parameter	Ratings	Unit
I_D	Continuous Drain Current @ T_C = 25°C	49	A
	Continuous Drain Current @ T_C = 100°C	30	
I_{DM}	Pulsed Drain Current①	173	
V_{GS}	Gate - Source Voltage	±30	V
E_{AS}	Single Pulse Avalanche Energy②	1979	mJ
I_{AR}	Avalanche Current, Repetitive or Non-Repetitive	24	A

Thermal and Mechanical Characteristics

Symbol	Characteristic	Min	Typ	Max	Unit
P_D	Total Power Dissipation @ T_C = 25°C	-	-	1135	W
$R_{\theta JC}$	Junction to Case Thermal Resistance	-	-	0.11	°C/W
$R_{\theta CS}$	Case to Sink Thermal Resistance, Flat, Greased Surface	-	0.11	-	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55	-	150	°C
T_L	Soldering Temperature for 10 Seconds (1.6mm from case)	-	-	300	
W_T	Package Weight	-	0.22	-	oz
		-	6.2	-	g
Torque	Mounting Torque (TO-264 Package), 4-40 or M3 screw	-	-	10	in·lbf
		-	-	1.1	N·m

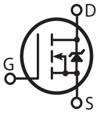
Static Characteristics T_J = 25°C unless otherwise specified APT48M80B2_L

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
$V_{BR(DSS)}$	Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250μA		800			V
$\Delta V_{BR(DSS)}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	Reference to 25°C, I_D = 250μA			0.87		V/°C
$R_{DS(on)}$	Drain-Source On Resistance③	V_{GS} = 10V, I_D = 24A			0.17	0.19	Ω
$V_{GS(th)}$	Gate-Source Threshold Voltage	$V_{GS} = V_{DS}$, I_D = 2.5mA		3	4	5	V
$\Delta V_{GS(th)}/\Delta T_J$	Threshold Voltage Temperature Coefficient				-10		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 800V V_{GS} = 0V	T_J = 25°C			100	μA
			T_J = 125°C			500	
I_{GSS}	Gate-Source Leakage Current	V_{GS} = ±30V				±100	nA

Dynamic Characteristics T_J = 25°C unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
g_{fs}	Forward Transconductance	V_{DS} = 50V, I_D = 24A		43		S
C_{iss}	Input Capacitance	V_{GS} = 0V, V_{DS} = 25V f = 1MHz		9330		pF
C_{rss}	Reverse Transfer Capacitance			160		
C_{oss}	Output Capacitance			930		
$C_{o(cr)}$ ④	Effective Output Capacitance, Charge Related	V_{GS} = 0V, V_{DS} = 0V to 533V		440		
$C_{o(er)}$ ⑤	Effective Output Capacitance, Energy Related			220		
Q_g	Total Gate Charge	V_{GS} = 0 to 10V, I_D = 24A, V_{DS} = 400V		305		nC
Q_{gs}	Gate-Source Charge			51		
Q_{gd}	Gate-Drain Charge			155		
$t_{d(on)}$	Turn-On Delay Time	**Resistive Switching** V_{DD} = 400V, I_D = 24A R_G = 2.2Ω⑥, V_{GG} = 15V		55		ns
t_r	Current Rise Time			75		
$t_{d(off)}$	Turn-Off Delay Time			230		
t_f	Current Fall Time			70		

Source-Drain Diode Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_S	Continuous Source Current (Body Diode)	MOSFET symbol showing the integral reverse p-n junction diode (body diode) 			49	A
I_{SM}	Pulsed Source Current (Body Diode)①				173	
V_{SD}	Diode Forward Voltage	I_{SD} = 24A, T_J = 25°C, V_{GS} = 0V		0.8	1.0	V
t_{rr}	Reverse Recovery Time	I_{SD} = 24A③ di_{SD}/dt = 100A/μs, T_J = 25°C		970		nS
Q_{rr}	Reverse Recovery Charge			22		μC
dv/dt	Peak Recovery dv/dt	I_{SD} ≤ 24A, di/dt ≤1000A/μs, V_{DD} = 533V, T_J = 125°C			10	V/ns

① Repetitive Rating: Pulse width and case temperature limited by maximum junction temperature.

② Starting at T_J = 25°C, L = 6.9mH, R_G = 25Ω, I_{AS} = 24A.

③ Pulse test: Pulse Width < 380μs, duty cycle < 2%.

④ $C_{o(cr)}$ is defined as a fixed capacitance with the same stored charge as C_{OSS} with V_{DS} = 67% of $V_{(BR)DSS}$.

⑤ $C_{o(er)}$ is defined as a fixed capacitance with the same stored energy as C_{OSS} with V_{DS} = 67% of $V_{(BR)DSS}$. To calculate $C_{o(er)}$ for any value of V_{DS} less than $V_{(BR)DSS}$, use this equation: $C_{o(er)} = -8.32E-8/V_{DS}\text{^}2 + 3.49E-8/V_{DS} + 1.30E-10$.

⑥ R_G is external gate resistance, not including internal gate resistance or gate driver impedance. (MIC4452)

Microsemi reserves the right to change, without notice, the specifications and information contained herein.

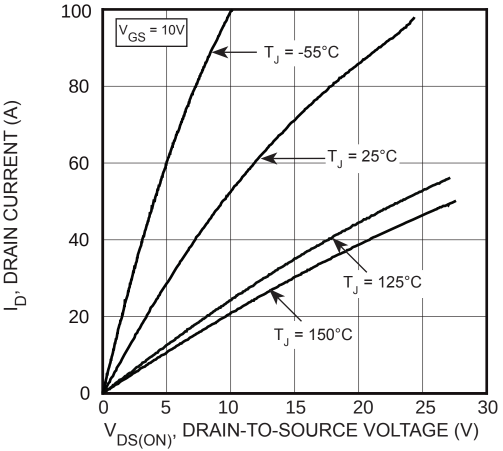


Figure 1, Output Characteristics

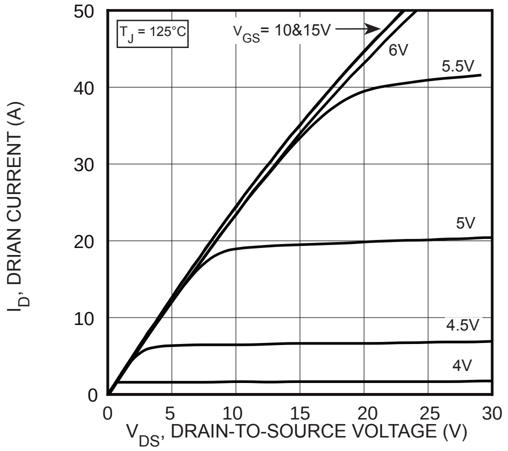


Figure 2, Output Characteristics

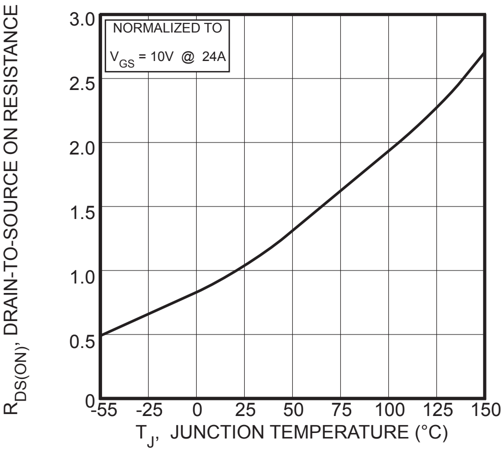


Figure 3, $R_{DS(ON)}$ vs Junction Temperature

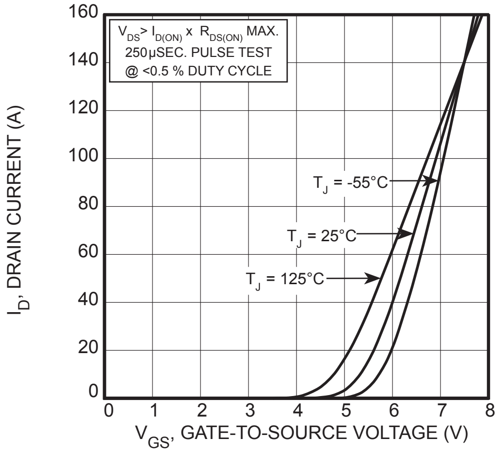


Figure 4, Transfer Characteristics

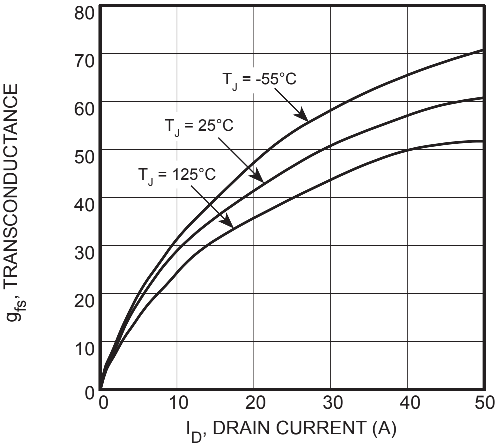


Figure 5, Gain vs Drain Current

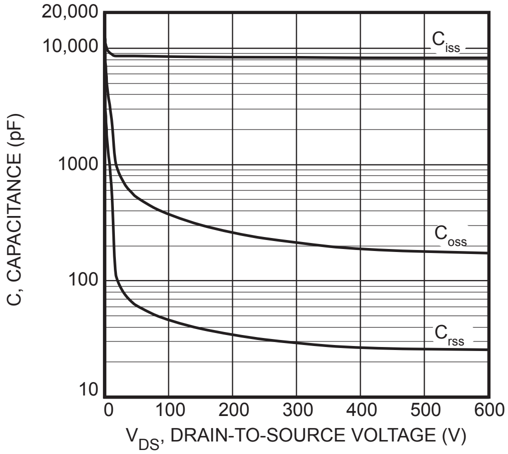


Figure 6, Capacitance vs Drain-to-Source Voltage

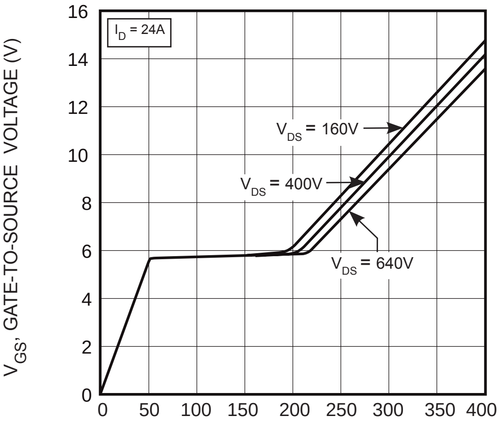


Figure 7, Gate Charge vs Gate-to-Source Voltage

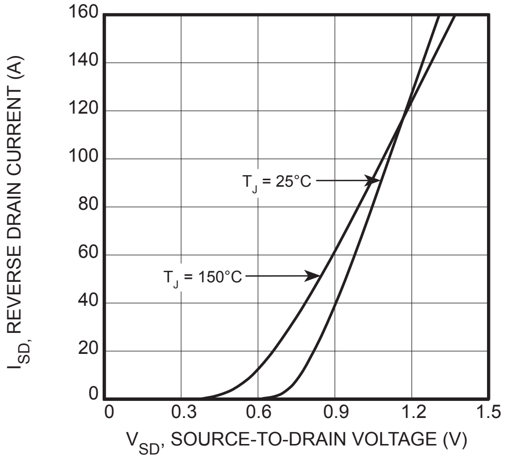


Figure 8, Reverse Drain Current vs Source-to-Drain Voltage

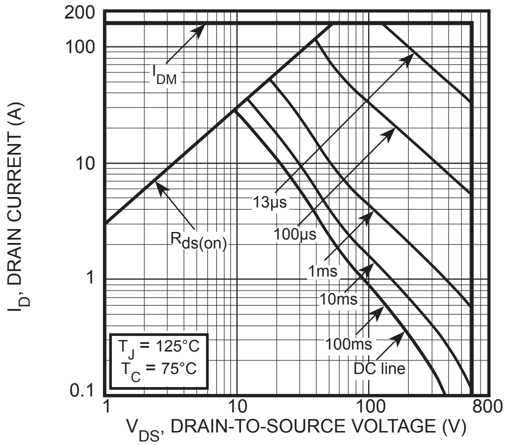


Figure 9, Forward Safe Operating Area

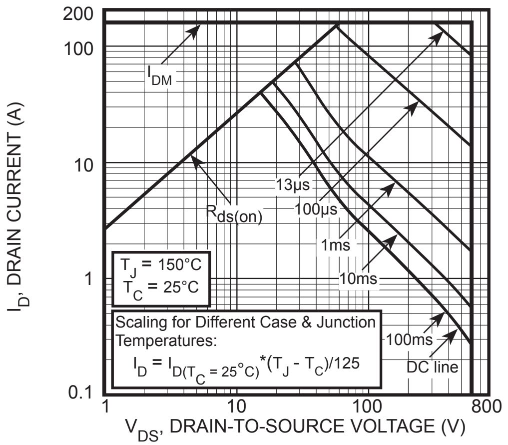


Figure 10, Maximum Forward Safe Operating Area

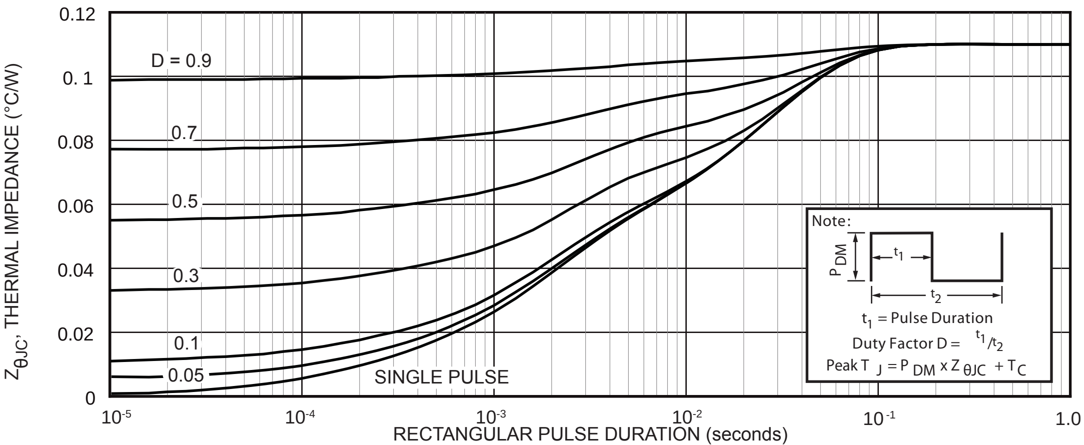
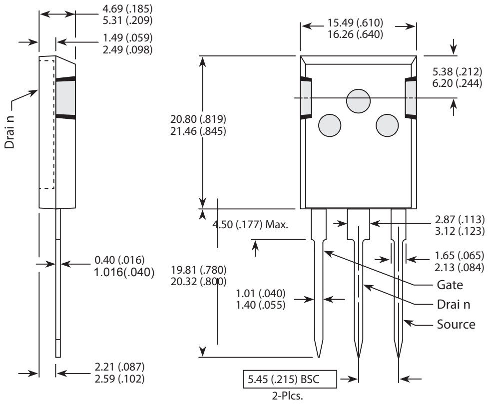


Figure 11. Maximum Effective Transient Thermal Impedance Junction-to-Case vs Pulse Duration

T-MAX® (B2) Package Outline

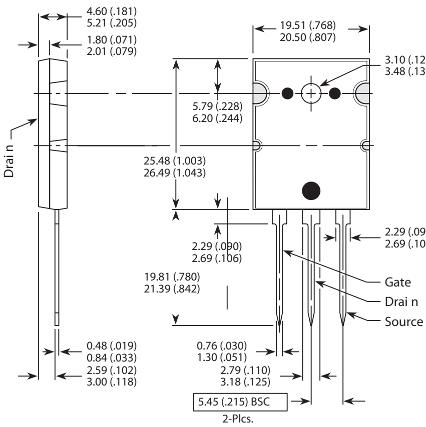
TO-264 (L) Package Outline

e3 100% Sn Plated



These dimensions are equal to the TO-247 without the mounting hole.

Dimensions in Millimeters and (Inches)



Dimensions in Millimeters and (Inches)

Стандарт
Электрон
Связь

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