BIDIRECTIONAL I²C ISOLATORS WITH UNIDIRECTIONAL DIGITAL CHANNELS

Features

- Independent, bidirectional SDA and SCL isolation channels
  - Open drain outputs with 35 mA sink current
  - Supports I^2C clocks up to 1.7 MHz
- Unidirectional isolation channels support additional system signals (Si8605, Si8606)
- Up to 5000 V_{RMS} isolation
- UL, CSA, VDE, CQC recognition
- 60-year life at rated working voltage
- High electromagnetic immunity
- Wide operating supply voltage
  - 3.0 to 5.5 V
- Wide temperature range
  - –40 to +125 °C
- Transient immunity 50 kV/µs
- AEC-Q100 qualification
- RoHS-compliant packages
  - SOIC-8 narrow body
  - SOIC-16 wide body
  - SOIC-16 narrow body

Ordering Information:
See page 27.

Applications

- Isolated I^2C, PMBus, SMBus
- Power over Ethernet
- Motor Control Systems
- Hot-swap applications
- Intelligent Power systems
- Isolated SMPS systems with PMBus interfaces

Description

The Si860x series of isolators are single-package galvanic isolation solutions for I^2C and SMBus serial port applications. These products are based on Silicon Labs proprietary RF isolation technology and offer shorter propagation delays, lower power consumption, smaller installed size, and more stable operation with temperature and age versus opto couplers or other digital isolators.

All devices in this family include hot-swap, bidirectional SDA and/or SCL isolation channels with open-drain, 35 mA sink capability that operate to a maximum frequency of 1.7 MHz. The 8-pin version (Si8600) supports bidirectional SDA and SCL isolation; the Si8602 supports bidirectional SDA and unidirectional SCL isolation, and the 16-pin versions (Si8605, Si8606) feature two unidirectional isolation channels to support additional system signals, such as interrupts or resets. All versions contain protection circuits to guard against data errors when an unpowered device is inserted into a powered system.

Small size, low installed cost, low power consumption, and short propagation delays make the Si860x family the optimum solution for isolating I^2C and SMBus serial ports.

Safety Regulatory Approval

- UL 1577 recognized
  - Up to 5000 V_{RMS} for 1 minute
- CSA component notice 5A approval
  - IEC 60950-1, 61010-1, 60601-1 (reinforced insulation)
- VDE certification conformity
  - IEC 60747-5-2 (VDE0884 Part 2)
  - EN60950-1 (reinforced insulation)
- CQC certification approval
  - GB4943.1

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1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Ambient Operating Temperature*	T_A	–40	25	125*	°C
Supply Voltage	AVDD	3.0	—	5.5	V
	BVDD	3.0	—	5.5	V
***Note:** The maximum ambient temperature is dependent on data frequency, output loading, number of operating channels, and supply voltage.					

Table 2. Si860x Power Characteristics*

3.0 V < VDD < 5.5 V. TA = –40 to +125 °C. Typical specs at 25 °C (See Figures 2 and 10 for test diagrams.)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si8600 Supply Current						
AVDD Current BVDD Current	Idda Iddb	All channels = 0 dc	— —	5.4 4.3	7.6 6.5	mA mA
AVDD Current BVDD Current	Idda Iddb	All channels = 1 dc	— —	2.6 1.9	3.9 2.9	mA mA
AVDD Current BVDD Current	Idda Iddb	All channels = 1.7 MHz	— —	3.3 2.6	5.0 3.9	mA mA
Si8602 Supply Current						
AVDD Current BVDD Current	Idda Iddb	All channels = 0 dc	— —	1.8 1.8	2.7 2.7	mA mA
AVDD Current BVDD Current	Idda Iddb	All channels = 1 dc	— —	4.7 3.1	7.1 4.7	mA mA
AVDD Current BVDD Current	Idda Iddb	All channels = 1.7 MHz	— —	2.5 2.1	3.8 3.2	mA mA
Si8605 Supply Current						
AVDD Current BVDD Current	Idda Iddb	All non-I^2C channels = 0 All I^2C channels = 1	— —	3.4 2.7	5.1 4.1	mA mA
AVDD Current BVDD Current	Idda Iddb	All non-I^2C channels = 1 All I^2C channels = 0	— —	7.2 6.2	10.1 8.7	mA mA
AVDD Current BVDD Current	Idda Iddb	All non-I^2C channels = 5 MHz All I^2C channels = 1.7 MHz	— —	4.2 3.6	6.3 5.4	mA mA
***Note:** All voltages are relative to respective ground.						

Table 2. Si860x Power Characteristics* (Continued)

3.0 V < VDD < 5.5 V. TA = –40 to +125 °C. Typical specs at 25 °C (See Figures 2 and 10 for test diagrams.)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si8606 Supply Current						
AVDD Current BVDD Current	Idda Iddb	All non-I^2C channels = 0 All I^2C channels = 1	— —	2.8 3.0	4.2 4.5	mA mA
AVDD Current BVDD Current	Idda Iddb	All non-I^2C channels = 1 All I^2C channels = 0	— —	8.3 5.5	11.6 7.7	mA mA
AVDD Current BVDD Current	Idda Iddb	All non-I^2C channels = 5 MHz All I^2C channels = 1.7 MHz	— —	4.1 3.5	6.2 5.3	mA mA
***Note:** All voltages are relative to respective ground.						

Table 3. Si8600/02/05/06 Electrical Characteristics for Bidirectional I^2C Channels[1]

3.0 V < VDD < 5.5 V. TA = –40 to +125 °C. Typical specs at 25 °C unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Logic Levels Side A Logic Input Threshold[2] Logic Low Output Voltages Input/Output Logic Low Level Difference[3]	 I^2CV_T (Side A) I^2CV_{OL} (Side A) $I^2C\Delta V$ (Side A)	 ISDAA, ISCLA (>0.5 mA, <3.0 mA)	 410 540 50	 — — —	 540 800 —	 mV mV mV mV
Logic Levels Side B Logic Low Input Voltage Logic High Input Voltage Logic Low Output Voltage	 I^2CV_{IL} (Side B) I^2CV_{IH} (Side B) I^2CV_{OL} (Side B)	 ISCLB = 35 mA	 — 2.0 —	 — — —	 0.8 — 500	 V V mV
SCL and SDA Logic High Leakage	Isdaa, Isdab Iscla, Isclb	SDAA, SCLA = VSSA SDAB, SCLB = VSSB	—	2.0	10	µA
Pin Capacitance SDAA, SCLA, SDAB, SDBB	CA CB		— —	10 10	— —	pF pF

Notes:
1. All voltages are relative to respective ground.
2. V_{IL} < 0.410 V, V_{IH} > 0.540 V.
3. $I^2C\Delta V$ (Side A) = I^2CV_{OL} (Side A) – I^2CV_T (Side A). To ensure no latch-up on a given bus, $I^2C\Delta V$ (Side A) is the minimum difference between the output logic low level of the driving device and the input logic threshold.
4. Side A measured at 0.6 V.

Table 3. Si8600/02/05/06 Electrical Characteristics for Bidirectional I^2C Channels[1] (Continued)
3.0 V < VDD < 5.5 V. TA = –40 to +125 °C. Typical specs at 25 °C unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Timing Specifications (Measured at 1.40 V Unless Otherwise Specified)						
Maximum I^2C Bus Frequency	Fmax		—	—	1.7	MHz
Propagation Delay						
5 V Operation						
Side A to Side B Rising[4]	Tphab	No bus capacitance,	—	38	45	ns
Side A to Side B Falling[4]	Tplab	R1 = 1400,	—	15	26	ns
Side B to Side A Rising	Tphba	R2 = 499,	—	33	46	ns
Side B to Side A Falling	Tplba	See Figure 2	—	11	22	ns
3.3 V Operation						
Side A to Side B Rising[4]	Tphab		—	44	55	ns
Side A to Side B Falling[4]	Tplab	R1 = 806	—	17	29	ns
Side B to Side A Rising	Tphba	R2 = 499	—	30	40	ns
Side B to Side A Falling	Tplba		—	14	27	ns
Pulse Width Distortion		No bus capacitance,				
5 V		R1 = 1400,				
Side A Low to Side B Low[4]	PWDAB	R2 = 499,	—	22	32	ns
Side B Low to Side A Low	PWDBA	See Figure 2	—	21	32	ns
3.3 V						
Side A Low to Side B Low[4]	PWDAB	R1 = 806,	—	27	35	ns
Side B Low to Side A Low	PWDBA	R2 = 499	—	15	25	ns

Notes:
1. All voltages are relative to respective ground.
2. V_{IL} < 0.410 V, V_{IH} > 0.540 V.
3. $I^2C\Delta V$ (Side A) = I^2CV_{OL} (Side A) – I^2CV_T (Side A). To ensure no latch-up on a given bus, $I^2C\Delta V$ (Side A) is the minimum difference between the output logic low level of the driving device and the input logic threshold.
4. Side A measured at 0.6 V.

Table 4. Electrical Characteristics for Unidirectional Non-I^{2}C Digital Channels (Si8602/05/06)
3.0 V < VDD < 5.5 V. TA = –40 to +125 °C. Typical specs at 25 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Positive-Going Input Threshold	VT+	All inputs rising	1.4	1.67	1.9	V
Negative-Going Input Threshold	VT–	All inputs falling	1.0	1.23	1.4	V
Input Hysteresis	V_{HYS}		0.38	0.44	0.50	V
High Level Input Voltage	V_{IH}		2.0	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	Ioh = –4 mA	AVDD, BVDD –0.4	4.8	—	V
Low Level Output Voltage	V_{OL}	Iol = 4 mA	—	0.2	0.4	V
Input Leakage Current	I_L		—	—	±10	µA
Output Impedance[1]	Z_O		—	50	—	Ω
Timing Characteristics						
Maximum Data Rate			0	—	10	Mbps
Minimum Pulse Width			—	—	40	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 1	—	—	20	ns
Pulse Width Distortion $\lvert t_{PLH} – t_{PHL} \rvert$	PWD	See Figure 1	—	—	12	ns
Propagation Delay Skew[2]	$t_{PSK(P-P)}$		—	—	20	ns
Channel-Channel Skew	t_{PSK}		—	—	10	ns
Output Rise Time	t_r	C_3 = 15 pF See Figure 1 and Figure 2	—	2.5	4.0	ns
Output Fall Time	t_f	C_3 = 15 pF See Figure 1 and Figure 2	—	2.5	4.0	ns
Peak Eye Diagram Jitter	$t_{JIT(PK)}$		—	350	—	ps

Notes:
1. The nominal output impedance of a non-I^{2}C isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.

Table 5. Electrical Characteristics for All I²C and Non-I²C Channels
3.0 V < VDD < 5.5 V. TA = –40 to +125 °C. Typical specs at 25 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VDD Undervoltage Threshold	VDDUV+	V_{DD1}, V_{DD2} rising	1.95	2.24	2.375	V
VDD Undervoltage Threshold	VDDUV–	V_{DD1}, V_{DD2} falling	1.88	2.16	2.325	V
VDD Undervoltage Hysteresis	VDD_{HYS}		50	70	95	mV
Common Mode Transient Immunity	CMTI	$V_I = V_{DD}$ or 0 V V_{CM} = 1500 V (see Figure 3)	35	50	—	kV/µs
Shut Down Time from UVLO	t_{SD}		—	3.0	—	µs
Start-up Time*	t_{START}		—	15	40	µs
***Note:** Start-up time is the time period from the application of power to valid data at the output.						

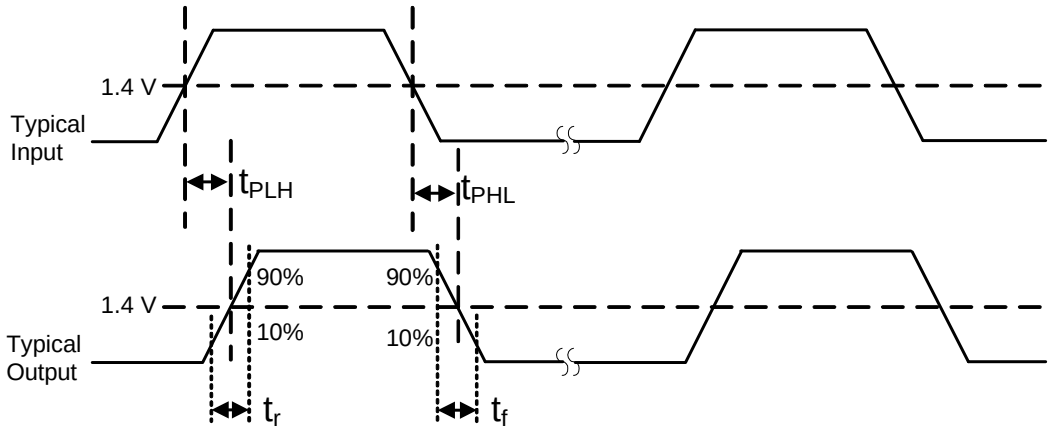


Figure 1. Propagation Delay Timing (Non-I²C Channels)

1.1. Test Circuits

Figure 2 depicts the timing test diagram; Figure 3 depicts the CMTI test diagram.

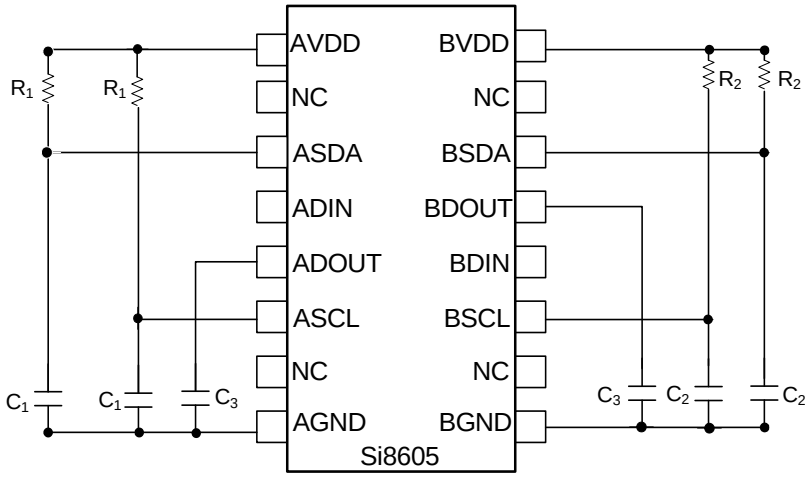


Figure 2. Simplified Timing Test Diagram

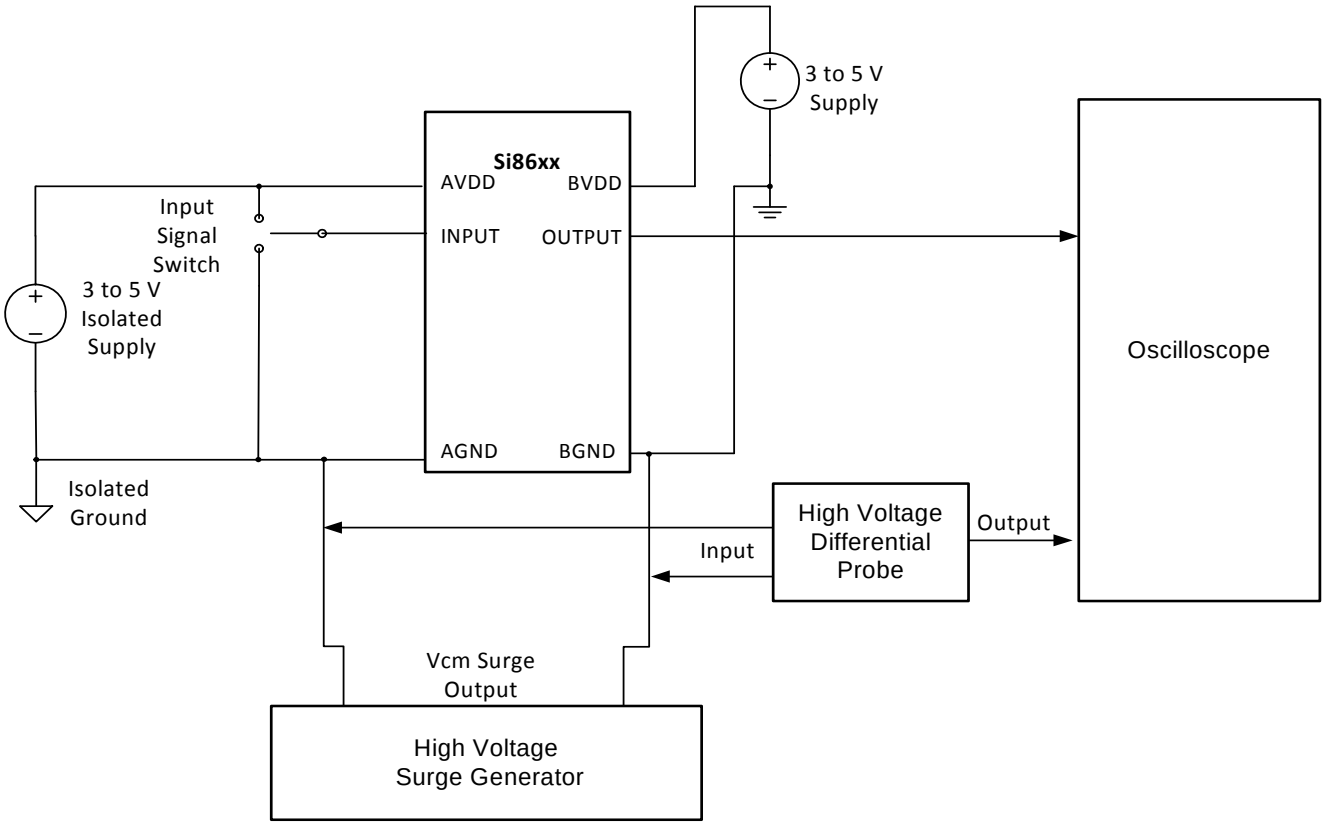


Figure 3. Common Mode Transient Immunity Test Circuit

Table 6. Regulatory Information*

CSA
The Si860x is certified under CSA Component Acceptance Notice 5A. For more details, see File 232873.
61010-1: Up to 600 V_{RMS} reinforced insulation working voltage; up to 600 V_{RMS} basic insulation working voltage.
60950-1: Up to 600 V_{RMS} reinforced insulation working voltage; up to 1000 V_{RMS} basic insulation working voltage.
60601-1: Up to 125 V_{RMS} reinforced insulation working voltage; up to 380 V_{RMS} basic insulation working voltage.
VDE
The Si860x is certified according to IEC 60747-5-2. For more details, see File 5006301-4880-0001.
60747-5-2: Up to 1200 V_{peak} for basic insulation working voltage.
60950-1: Up to 600 V_{RMS} reinforced insulation working voltage; up to 1000 V_{RMS} basic insulation working voltage.
UL
The Si860x is certified under UL1577 component recognition program. For more details, see File E257455.
Rated up to 5000 V_{RMS} isolation voltage for basic protection.
CQC
The Si860x is certified under GB4943.1-2011. For more details, see File V2012CQC001041.
Rated up to 600 V_{RMS} reinforced insulation working voltage; up to 1000 V_{RMS} basic insulation working voltage.
***Note:** Regulatory Certifications apply to 2.5 kV_{RMS} rated devices which are production tested to 3.0 kV_{RMS} for 1 sec. Regulatory Certifications apply to 3.75 kV_{RMS} rated devices which are production tested to 4.5 kV_{RMS} for 1 sec. Regulatory Certifications apply to 5.0 kV_{RMS} rated devices which are production tested to 6.0 kV_{RMS} for 1 sec. For more information, see "6.Ordering Guide" on page 27.

Table 7. Insulation and Safety-Related Specifications

Parameter	Symbol	Test Condition	Value			Unit
			NB SOIC-8	NB SOIC-16	WB SOIC-16	
Nominal Air Gap (Clearance)[1]	L(1O1)		4.9	4.9	8.0	mm
Nominal External Tracking (Creepage)[1]	L(1O2)		4.01	4.01	8.0	mm
Minimum Internal Gap (Internal Clearance)			0.014	0.014	0.014	mm
Tracking Resistance (Proof Tracking Index)	PTI	IEC60112	600	600	600	V_{RMS}
Erosion Depth	ED		0.040	0.019	0.019	mm
Resistance (Input-Output)[2]	R_{IO}		10^{12}	10^{12}	10^{12}	Ω
Capacitance (Input-Output)[2]	C_{IO}	f = 1 MHz	1.0	2.0	2.0	pF
Input Capacitance[3]	C_I	Non-I^2C Channel	4.0	4.0	4.0	pF
		I^2C Channel	10	10	10	pF

Notes:
1. VDE certifies the clearance and creepage limits as 4.7 mm minimum for the NB SOIC-8 and SOIC-16 packages and 8.5 mm minimum for the WB SOIC-16 package. UL does not impose a clearance and creepage minimum for component level certifications. CSA certifies the clearance and creepage limits as 3.9 mm minimum for the NB SOIC-8 and SOIC-16 packages and 7.6 mm minimum for the WB SOIC-16 package.
2. To determine resistance and capacitance, the Si860x, SO-16, is converted into a 2-terminal device. Pins 1–8 (1–4, SO-8) are shorted together to form the first terminal and pins 9–16 (5–8, SO-8) are shorted together to form the second terminal. The parameters are then measured between these two terminals.
3. Measured from input pin to ground.

Table 8. IEC 60664-1 (VDE 0844 Part 2) Ratings

Parameter	Test Conditions	Specification	
		NB SOIC-8 SOIC-16	WB SOIC-16
Basic Isolation Group	Material Group	I	I
Installation Classification	Rated Mains Voltages ≤ 150 V_{RMS}	I-IV	I-IV
	Rated Mains Voltages ≤ 300 V_{RMS}	I-III	I-IV
	Rated Mains Voltages ≤ 400 V_{RMS}	I-II	I-III
	Rated Mains Voltages ≤ 600 V_{RMS}	I-II	I-III

Table 9. IEC 60747-5-2 Insulation Characteristics for Si86xxxx*

Parameter	Symbol	Test Condition	Characteristic		Unit
			WB SOIC-16	NB SOIC-8 SOIC-16	
Maximum Working Insulation Voltage	V_{IORM}		1200	630	Vpeak
Input to Output Test Voltage	V_{PR}	Method b1 (V_{IORM} x 1.875 = V_{PR}, 100% Production Test, t_m = 1 sec, Partial Discharge < 5 pC)	2250	1182	Vpeak
Transient Overvoltage	V_{IOTM}	t = 60 sec	6000	6000	Vpeak
Pollution Degree (DIN VDE 0110, Table 1)			2	2	
Insulation Resistance at T_S, V_{IO} = 500 V	R_S		$>10^9$	$>10^9$	Ω

***Note:** Maintenance of the safety data is ensured by protective circuits. The Si86xxxx provides a climate classification of 40/125/21.

Table 10. IEC Safety Limiting Values[1]

Parameter	Symbol	Test Condition	NB SOIC-8	NB SOIC-16	WB SOIC-16	Unit
Case Temperature	T_S		150	150	150	°C
Safety Input Current	I_S	θ_{JA} = 100 °C/W (WB SOIC-16), 105 °C/W (NB SOIC-16), 140 °C/W (NB SOIC-8) AVDD, BVDD = 5.5 V, T_J = 150 °C, T_A = 25 °C	160	210	220	mA
Device Power Dissipation[2]	P_D		220	275	275	W

Notes:
1. Maximum value allowed in the event of a failure. Refer to the thermal derating curve in Figures 4, 5, and 6.
2. The Si86xx is tested with AVDD, BVDD = 5.5 V; T_J = 150 ºC; C_1, C_2 = 0.1 µF; C_3 = 15 pF; R1, R2 = 3kΩ; input 1 MHz 50% duty cycle square wave.

Table 11. Thermal Characteristics

Parameter	Symbol	NB SOIC-8	NB SOIC-16	WB SOIC-16	Unit
IC Junction-to-Air Thermal Resistance	θ_{JA}	140	105	100	°C/W

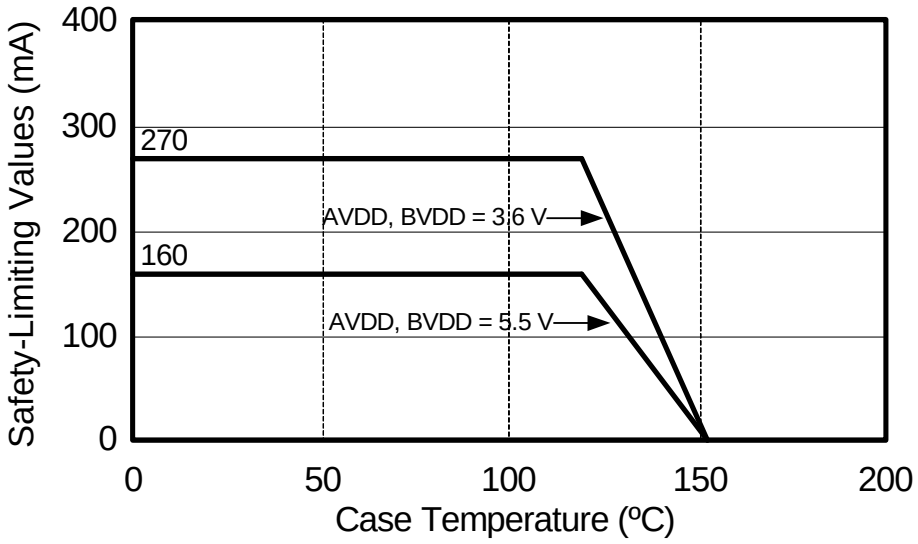


Figure 4. NB SOIC-8 Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-2

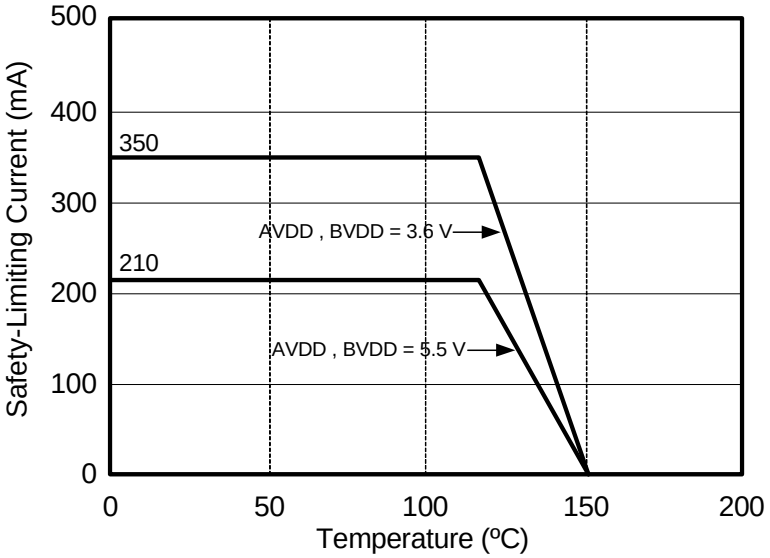


Figure 5. NB SOIC-16 Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-2

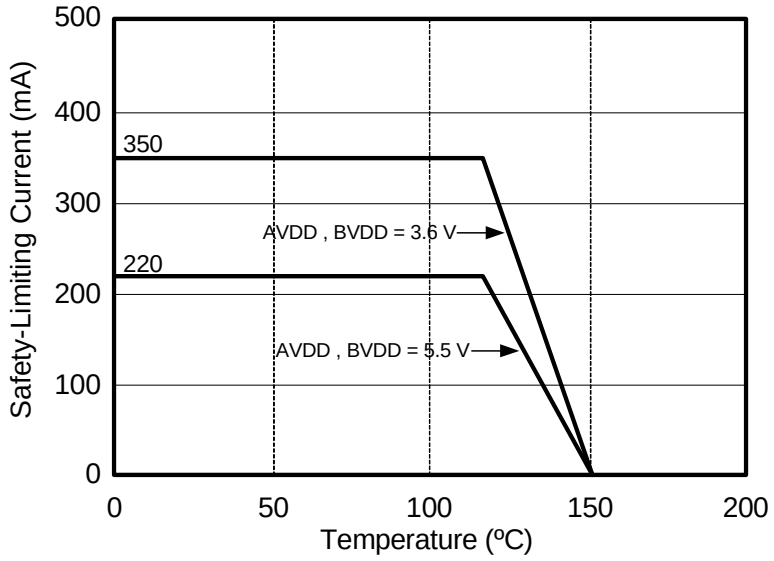


Figure 6. WB SOIC-16 Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-2

Table 12. Absolute Maximum Ratings[1]

Parameter	Symbol	Min	Typ	Max	Unit
Storage Temperature[2]	T_{STG}	–65	—	150	ºC
Ambient Temperature Under Bias	T_A	–40	—	125	ºC
Junction Temperature	T_J	—	—	150	°C
Supply Voltage	V_{DD}	–0.5	—	7.0	V
Input Voltage	V_I	–0.5	—	V_{DD} + 0.5	V
Output Voltage	V_O	–0.5	—	V_{DD} + 0.5	V
Output Current Drive (non-I^2C channels)	I_O	—	—	±10	mA
Side A output current drive (I^2C channels)	I_O	—	—	±15	mA
Side B output current drive (I^2C channels)	I_O	—	—	±75	mA
Lead Solder Temperature (10 s)		—	—	260	ºC
Maximum Isolation (Input to Output) (1 sec) NB SOIC-8, SOIC-16		—	—	4500	V_{RMS}
Maximum Isolation (Input to Output) (1 sec) WB SOIC-16		—	—	6500	V_{RMS}

Notes:
1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to conditions as specified in the operational sections of this data sheet.
2. VDE certifies storage temperature from –40 to 150 °C.

2. Functional Description

2.1. Theory of Operation

The operation of an Si86xx channel is analogous to that of an opto coupler, except an RF carrier is modulated instead of light. This simple architecture provides a robust isolated data path and requires no special considerations or initialization at start-up. A simplified block diagram for a single unidirectional Si86xx channel is shown in Figure 7.

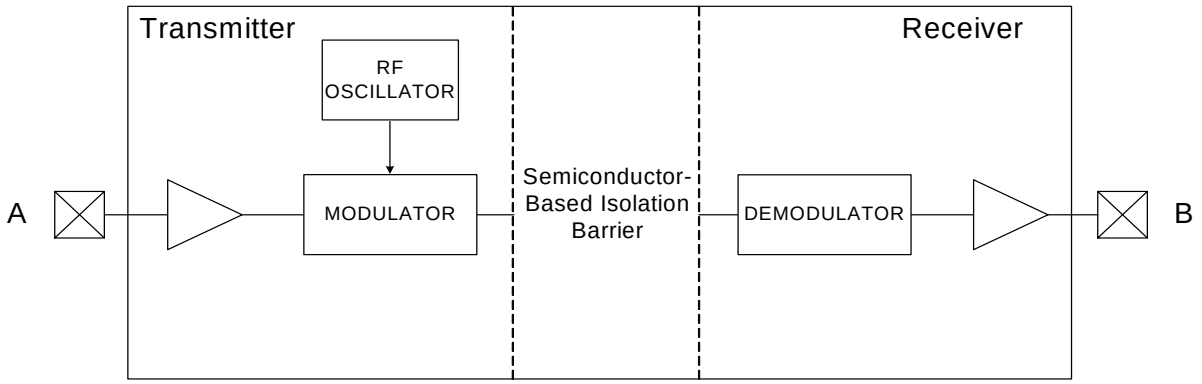


Figure 7. Simplified Channel Diagram

A channel consists of an RF Transmitter and RF Receiver separated by a semiconductor-based isolation barrier. Referring to the Transmitter, input A modulates the carrier provided by an RF oscillator using on/off keying. The Receiver contains a demodulator that decodes the input state according to its RF energy content and applies the result to output B via the output driver. This RF on/off keying scheme is superior to pulse code schemes as it provides best-in-class noise immunity, low power consumption, and better immunity to magnetic fields. See Figure 8 for more details.

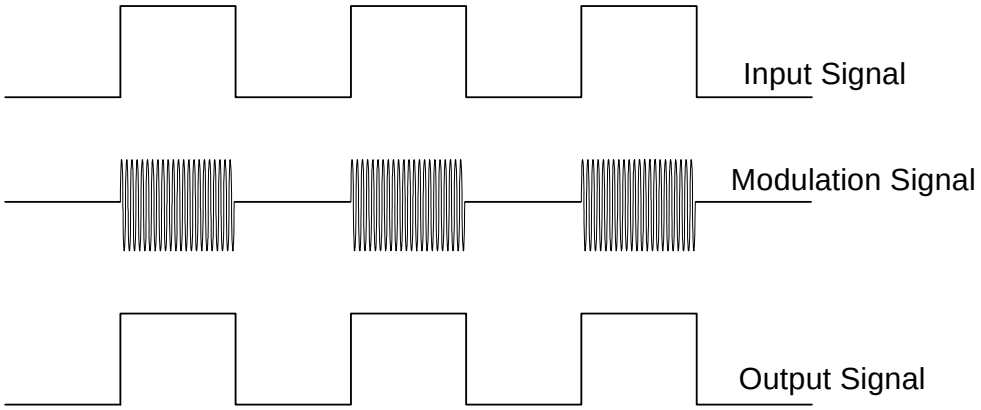


Figure 8. Modulation Scheme

3. Typical Application Overview

3.1. I²C Background

In many applications, I²C, SMBus, and PMBus interfaces require galvanic isolation for safety or ground loop elimination. For example, Power over Ethernet (PoE) applications typically use an I²C interface for communication between the PoE power sourcing device (PSE), and the earth ground referenced system controller. Galvanic isolation is required both by standard and also as a practical matter to prevent ground loops in Ethernet connected equipment.

The physical interface consists of two wires: serial data (SDA) and serial clock (SCL). These wires are connected to open collector drivers that serve as both inputs and outputs. At first glance, it appears that SDA and SCL can be isolated simply by placing two unidirectional isolators in parallel, and in opposite directions. However, this technique creates feedback that latches the bus line low when a logic low asserted by either master or slave. This problem can be remedied by adding anti-latch circuits, but results in a larger and more expensive solution. The Si860x products offer a single-chip, anti-latch solution to the problem of isolating I²C/SMBus applications and require no external components except the I²C/SMBus pull-up resistors. In addition, they provide isolation to a maximum of 5.0 kV_{RMS}, support I²C clock stretching, and operate to a maximum I²C bus speed of 1.7 Mbps.

3.2. I²C Isolator Operation

Without anti-latch protection, bidirectional I²C isolators latch when an isolator output logic low propagates back through an adjacent isolator channel creating a stable latched low condition on both sides. Anti-latch protection is typically added to one side of the isolator to avoid this condition (the “A” side for the Si8600/02/05/06).

The following examples illustrate typical circuit configurations using the Si8600/02/05/06.

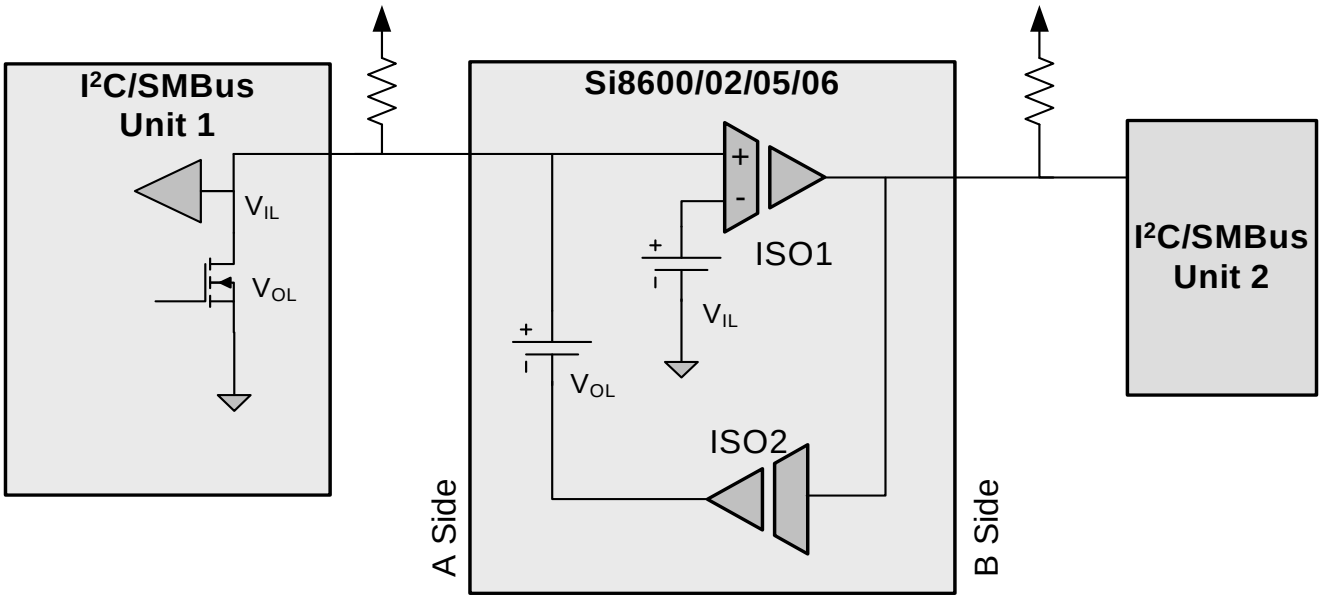


Figure 9. Isolated Bus Overview (I²C Channels Only)

The “A side” output low (V_{OL}) and input low (V_{IL}) levels are designed such that the isolator V_{OL} is greater than the isolator V_{IL} to prevent the latch condition.

3.3. I²C Isolator Design Constraints

Table 13 lists the I²C isolator design constraints.

Table 13. Design Constraints

Design Constraint	Data Sheet Values	Effect of Bus Pull-up Strength and Temperature
To prevent the latch condition, the isolator output low level must be greater than the isolator input low level.	Isolator V_{OL} 0.7 V typical Isolator V_{IL} 0.5 V typical Input/Output Logic Low Level Difference ΔVSDA1, ΔVSCL1 = 50 mV minimum	This is normally guaranteed by the isolator data sheet. However, if the pull up strength is too weak, the output low voltage will fall and can get too close to the input low logic level. These track over temperature.
The bus output low must be less than the isolator input low logic level.	Bus V_{OL} = 0.4 V maximum Isolator V_{IL} = 0.41 V minimum	If the pull up strength is too large, the devices on the bus might not pull the voltage below the input low range. These have opposite temperature coefficients. Worst case is hot temperature.
The isolator output low must be less than the bus input low.	Bus V_{IL} 0.3 x V_{DD} = 1.0 V minimum for V_{DD} = 3.3 V Isolator V_{OL} = 0.8 V maximum	If the pull up strength is too large, the isolator might not pull below the bus input low voltage. Si8600/02/05/06 Vol: –1.8 mV/C CMOS buffer: –0.6 mV/C This provides some temperature tracking, but worst case is cold temperature.

3.4. I²C Isolator Design Considerations

The first step in applying an I²C isolator is to choose which side of the bus will be connected to the isolator A side. Ideally, it should be the side which:

1. Is compatible with the range of bus pull up specified by the manufacturer. For example, the Si8600/02/05/06 isolators are normally used with a pull up of 0.5 mA to 3 mA.
2. Has the highest input low level for devices on the bus. Some devices may specify an input low of 0.9 V and other devices might require an input low of 0.3 x Vdd. Assuming a 3.3 V minimum power supply, the side with an input low of 0.3 x Vdd is the better side because this side has an input low level of 1.0 V.
3. Have devices on the bus that can pull down below the isolator input low level. For example, the Si860x input level is 0.41 V. As most CMOS devices can pull to within 0.4 V of GND this is generally not an issue.
4. Has the lowest noise. Due to the special logic levels, noise margins can be as low as 50 mV.

3.5. Typical Application Schematics

Figures 10 through 15 illustrate typical circuit configurations using the Si8600, Si8602, Si8605, and Si8606.

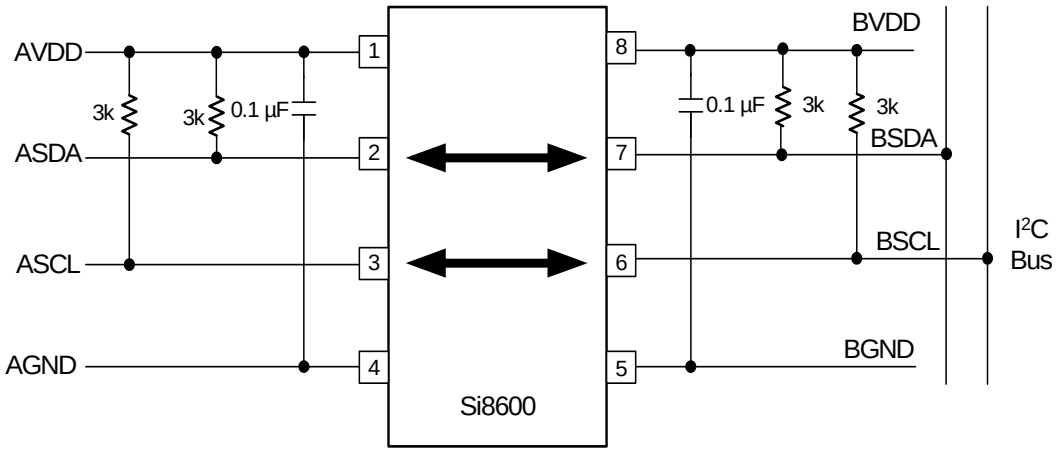


Figure 10. Typical Si8600 Application Diagram

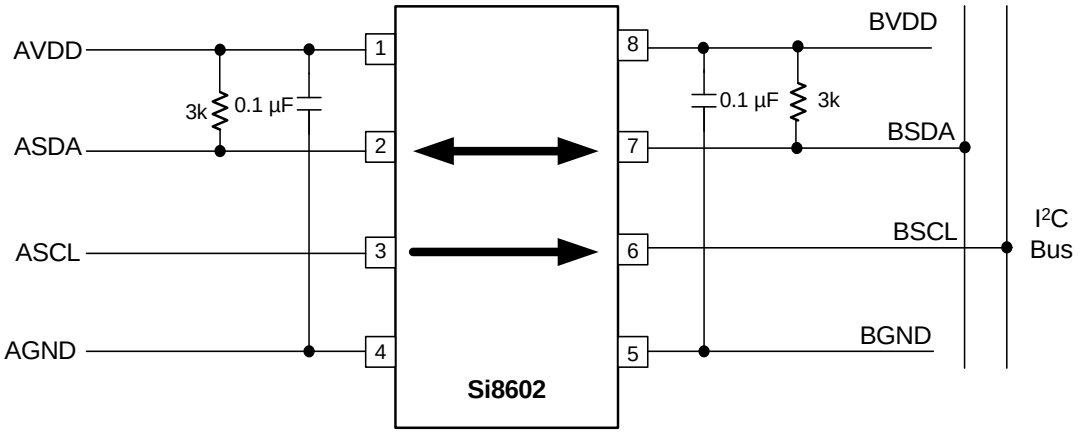


Figure 11. Typical Si8602 Application Diagram

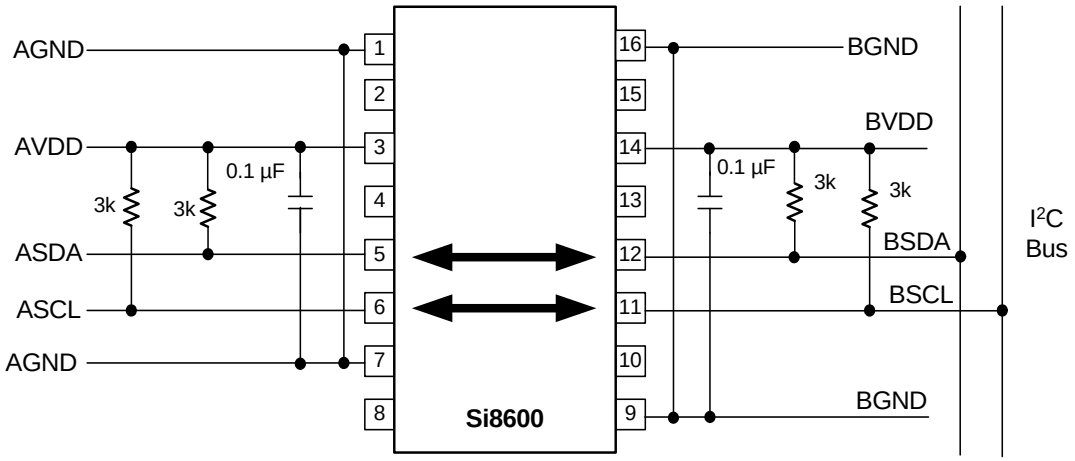


Figure 12. Typical Si8600 Application Diagram

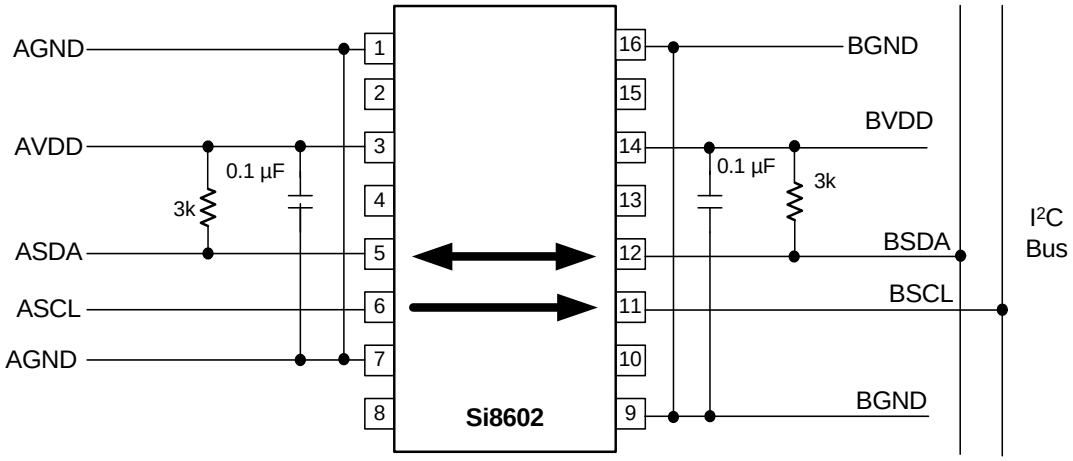


Figure 13. Typical Si8602 Application Diagram

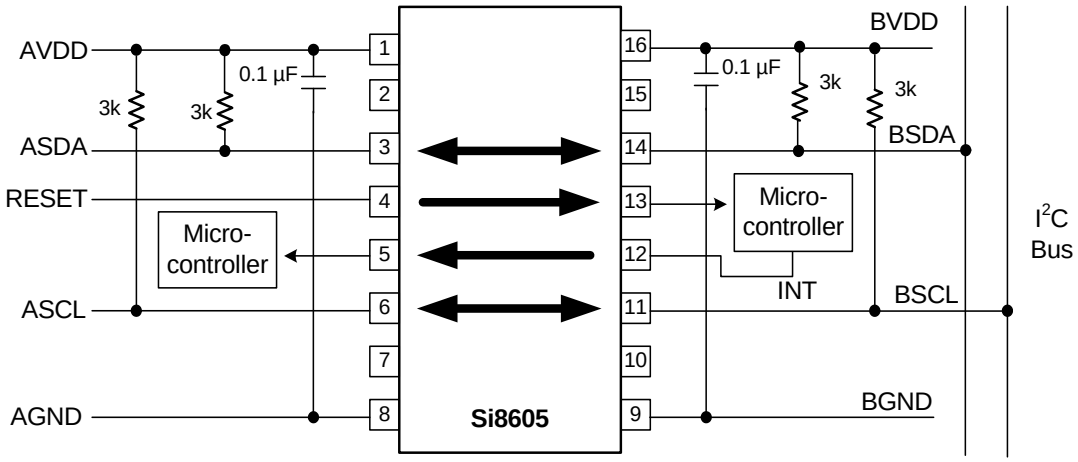


Figure 14. Typical Si8605 Application Diagram

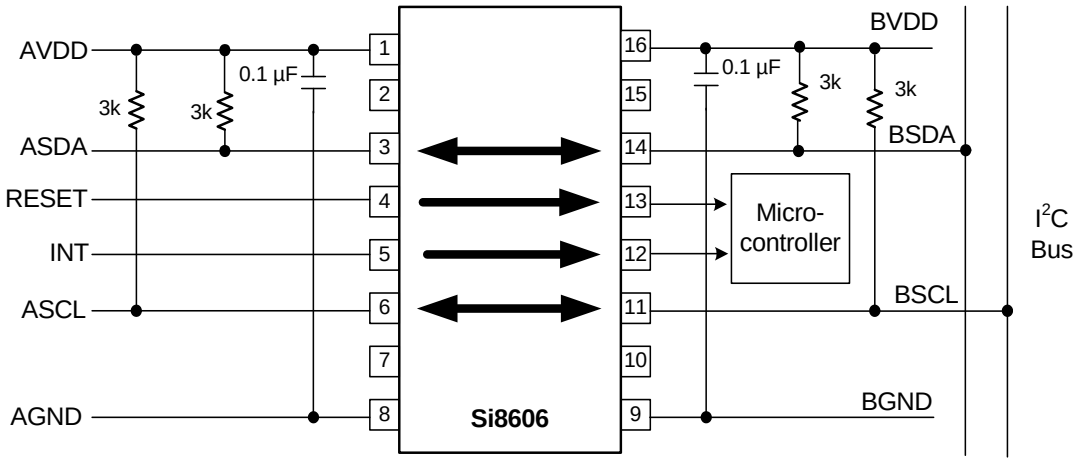


Figure 15. Typical Si8606 Application Diagram

4. Device Operation

Device behavior during start-up, normal operation, and shutdown is shown in Figure 16, where UVLO+ and UVLO- are the positive-going and negative-going thresholds respectively. Refer to Table 14 to determine outputs when power supply (VDD) is not present.

4.1. Device Startup

Outputs are held low during powerup until VDD is above the UVLO threshold for time period tSTART. Following this, the outputs follow the states of inputs.

4.2. Undervoltage Lockout

Undervoltage Lockout (UVLO) is provided to prevent erroneous operation during device startup and shutdown or when VDD is below its specified operating circuits range. Both Side A and Side B each have their own undervoltage lockout monitors. Each side can enter or exit UVLO independently. For example, Side A unconditionally enters UVLO when AVDD falls below $AVDD_{UVLO-}$ and exits UVLO when AVDD rises above $AVDD_{UVLO+}$. Side B operates the same as Side A with respect to its BVDD supply.

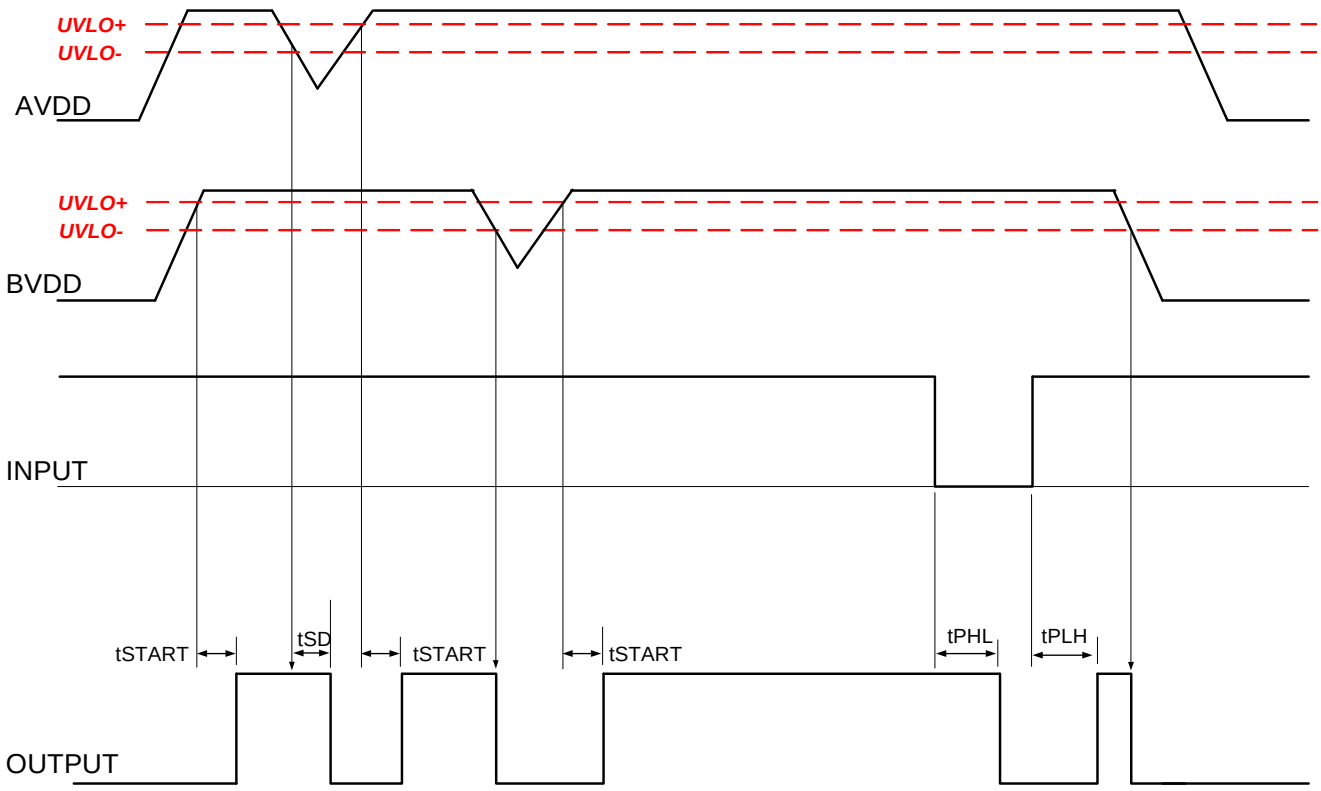


Figure 16. Device Behavior during Normal Operation

4.3. Input and Output Characteristics for Non-I^{2}C Digital Channels

The unidirectional Si86xx inputs and outputs are standard CMOS drivers/receivers. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces. Table 14 details powered and unpowered operation of the Si86xx's non-I^{2}C digital channels.

Table 14. Si86xx Operation Table

V_I Input[1,4]	VDDI State[1,2,3]	VDDO State[1,2,3]	V_O Output[1,4]	Comments
H	P	P	H	Normal operation.
L	P	P	L	
X[5]	UP	P	L[6]	Upon transition of VDDI from unpowered to powered, V_O returns to the same state as V_I in less than 1 µs.
X[5]	P	UP	Undetermined	Upon transition of VDDO from unpowered to powered, V_O returns to the same state as V_I within 1 µs.

Notes:
1. VDDI and VDDO are the input and output power supplies. V_I and V_O are the respective input and output terminals.
2. Powered (P) state is defined as 3.0 V < VDD < 5.5 V.
3. Unpowered (UP) state is defined as VDD = 0 V.
4. X = not applicable; H = Logic High; L = Logic Low.
5. Note that an I/O can power the die for a given side through an internal diode if its source has adequate current.
6. For I^{2}C channels, the outputs for a given side go to Hi-Z when power is lost on the opposite side.

4.4. Layout Recommendations

To ensure safety in the end user application, high voltage circuits (i.e., circuits with >30 V_{AC}) must be physically separated from the safety extra-low voltage circuits (SELV is a circuit with <30 V_{AC}) by a certain distance (creepage/clearance). If a component, such as a digital isolator, straddles this isolation barrier, it must meet those creepage/clearance requirements and also provide a sufficiently large high-voltage breakdown protection rating (commonly referred to as working voltage protection). Table 6 on page 10 and Table 7 on page 11 detail the working voltage and creepage/clearance capabilities of the Si86xx. These tables also detail the component standards (UL1577, IEC60747, CSA 5A), which are readily accepted by certification bodies to provide proof for end-system specifications requirements. Refer to the end-system specification (61010-1, 60950-1, 60601-1, etc.) requirements before starting any design that uses a digital isolator.

4.4.1. Supply Bypass

The Si860x family requires a 0.1 µF bypass capacitor between AVDD and AGND and BVDD and BGND. The capacitor should be placed as close as possible to the package. To enhance the robustness of a design, the user may also include resistors (50–300 Ω) in series with the inputs and outputs if the system is excessively noisy.

4.4.2. Output Pin Termination

The nominal output impedance of an non-I^2C isolator channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.

4.5. Typical Performance Characteristics

The typical performance characteristics depicted in the following diagrams are for information purposes only. Refer to Tables 2, 3, 4, and 5 for actual specification limits.

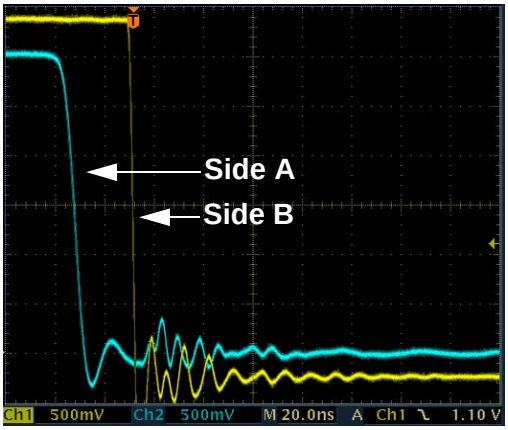


Figure 17. I²C Side A Pulling Down (1100 Ω Pull-Up)

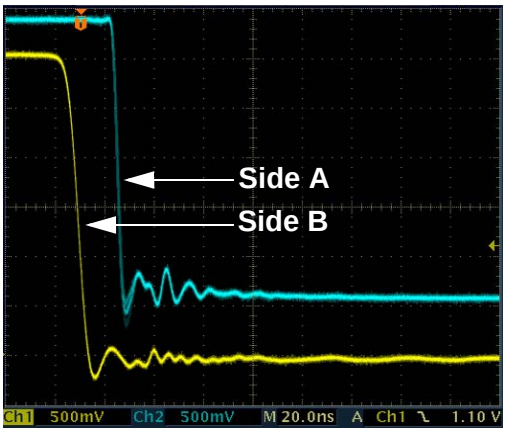


Figure 18. I²C Side B Pulling Down

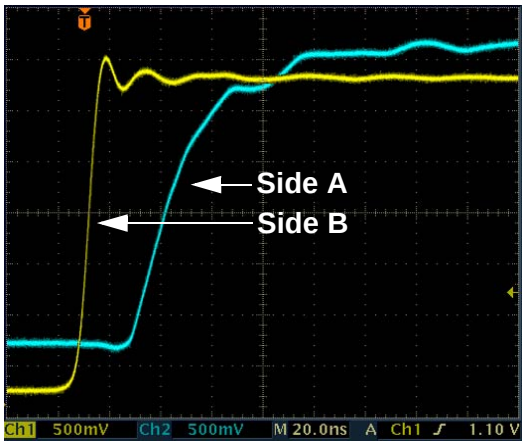


Figure 19. I²C Side B Pulling Up, Side A Following

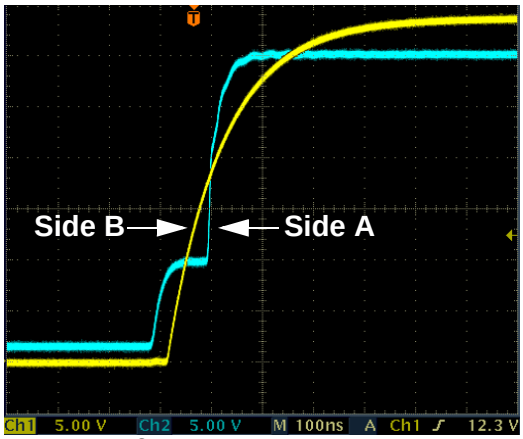


Figure 20. I²C Side A Pulling Up, Side B Following

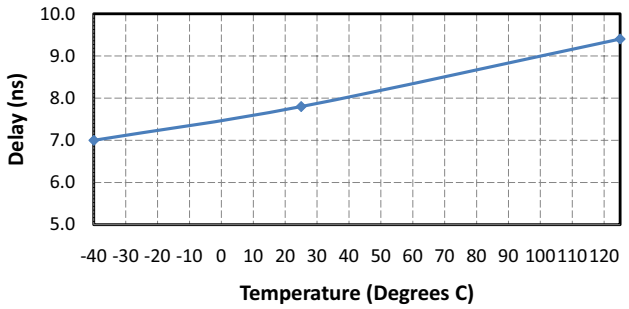


Figure 21. Non I²C Channel Propagation Delay vs. Temperature

5. Pin Descriptions

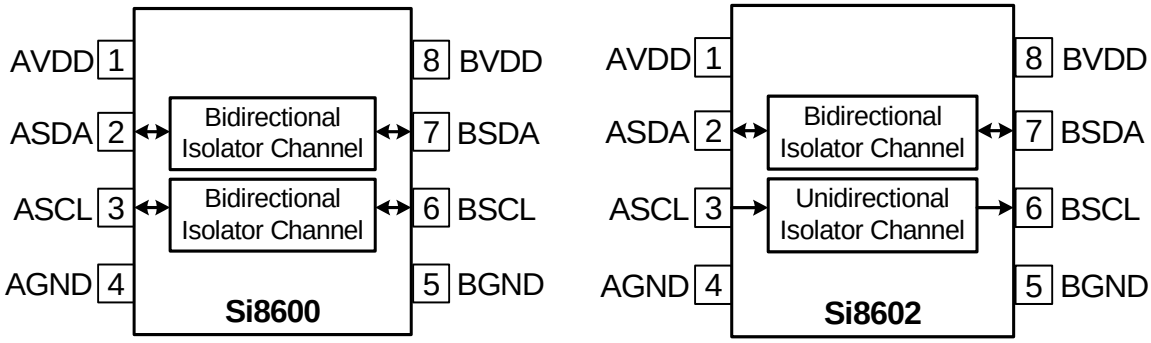
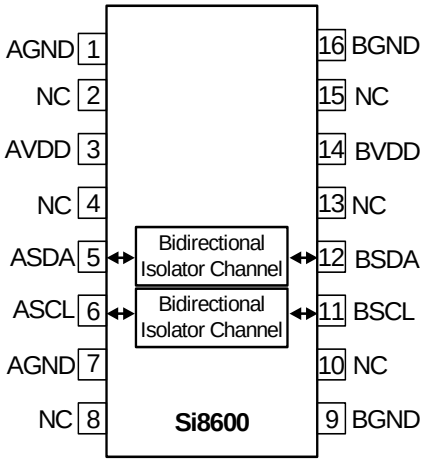


Table 15. Si8600/02 in SOIC-8 Package

Pin	Name	Description
1	AVDD	Side A power supply terminal; connect to a source of 3.0 to 5.5 V.
2	ASDA	Side A data (open drain) input or output.
3	ASCL	Side A clock input or output. Open drain I/O for Si8600. Standard CMOS input for Si8602.
4	AGND	Side A ground terminal.
5	BGND	Side B ground terminal.
6	BSCL	Side B clock input or output. Open drain I/O for Si8600. Push-pull output for Si8602.
7	BSDA	Side B data (open drain) input or output.
8	BVDD	Side B power supply terminal; connect to a source of 3.0 to 5.5 V.



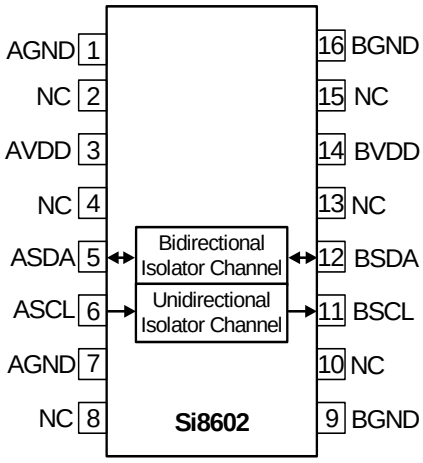
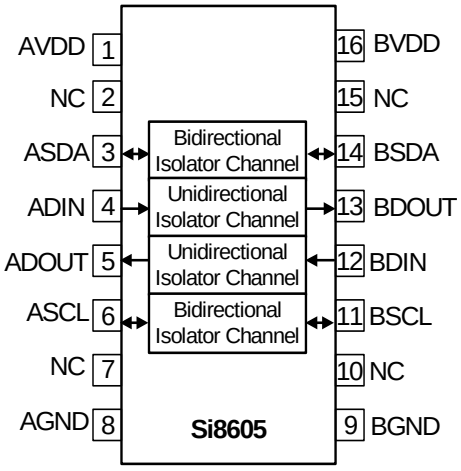


Table 16. Si8600/02 in Narrow and Wide-Body SOIC-16 Packages

Pin	Name	Description
1	AGND	Side A Ground Terminal.
2	NC	No connection.
3	AVDD	Side A power supply terminal. Connect to a source of 3.0 to 5.5 V.
4	NC	No connection.
5	ASDA	Side A data open drain input or output.
6	ASCL	Side A data open drain input or output.
7	AGND	Side A Ground Terminal.
8	NC	No connection.
9	BGND	Side B Ground Terminal.
10	NC	No connection.
11	BSCL	Side B data open drain input or output.
12	BSDA	Side B data open drain input or output.
13	NC	No connection.
14	BVDD	Side B power supply terminal. Connect to a source of 3.0 to 5.5 V.
15	NC	No connection.
16	BGND	Side B Ground Terminal.



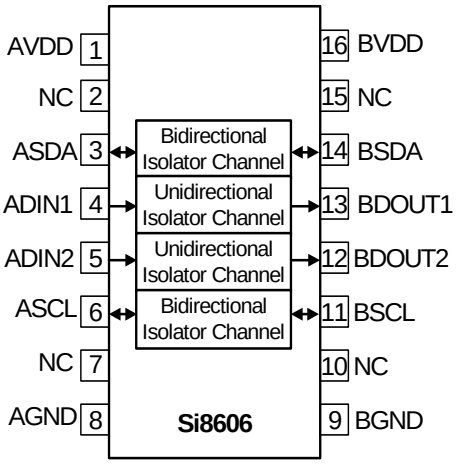


Table 17. Si8605/06 in Narrow and Wide-Body SOIC-16 Packages

Pin	Name	Description
1	AVDD	Side A power supply terminal. Connect to a source of 3.0 to 5.5 V.
2	NC	No connection.
3	ASDA	Side A data (open drain) input or output.
4	ADIN/ADIN1	Side A standard CMOS digital input (non I^2C).
5	ADOUT/ADIN2	Side A digital input/output (non I^2C) Standard CMOS digital input for Si8606. Push-Pull output for Si8605.
6	ASCL	Side A clock input or output. Open drain I/O for Si8605/06.
7	NC	No connection.
8	AGND	Side A Ground Terminal.
9	BGND	Side B Ground Terminal.
10	NC	No connection.
11	BSCL	Side B clock input or output. Open drain I/O for Si8605/06.
12	BDIN/BDOUT2	Side B digital input/output (non I^2C) Standard CMOS digital input for Si8605. Push-Pull output for Si8606.
13	BDOUT/BDOUT1	Side B digital push-pull output (non I^2C).
14	BSDA	Side B data open drain input or output.
15	NC	No connection.
16	BVDD	Side B power supply terminal. Connect to a source of 3.0 to 5.5 V.

6. Ordering Guide

Table 18. Ordering Guide[1,2,3]

Ordering Part Number (OPN)	Number of Bidirectional I^2C Channels	Max I^2C Bus Speed (MHz)	Number of Unidirectional Non-I^2C Channels	Max Data Rate of Non-I^2C Unidirectional Channels (Mbps)	Isolation Ratings (kVrms)	Temp Range (°C)	Package
Si8600AB-B-IS	2	1.7	0	—	2.5	–40 to 125	NB SOIC-8
Si8600AC-B-IS	2	1.7	0	—	3.75	–40 to 125	NB SOIC-8
Si8600AD-B-IS	2	1.7	0	—	5.0	–40 to 125	WB SOIC-16
Si8602AB-B-IS	1	1.7	1	10	2.5	–40 to 125	NB SOIC-8
Si8602AC-B-IS	1	1.7	1	10	3.75	–40 to 125	NB SOIC-8
Si8602AD-B-IS	1	1.7	1	10	5.0	–40 to 125	WB SOIC-16
Si8605AB-B-IS1	2	1.7	1 Forward 1 Reverse	10	2.5	–40 to 125	NB SOIC-16
Si8605AC-B-IS1	2	1.7	1 Forward 1 Reverse	10	3.75	–40 to 125	NB SOIC-16
Si8605AD-B-IS	2	1.7	1 Forward 1 Reverse	10	5.0	–40 to 125	WB SOIC-16
Si8606AC-B-IS1	2	1.7	2 Forward	10	3.75	–40 to 125	NB SOIC-16
Si8606AD-B-IS	2	1.7	2 Forward	10	5.0	–40 to 125	WB SOIC-16

Notes:

1. All packages are RoHS-compliant with peak reflow temperature of 260 °C according to the JEDEC industry standard classifications and peak solder temperature.
   Moisture sensitivity level is MSL3 for wide-body SOIC-16 packages.
   Moisture sensitivity level is MSL2A for narrow-body SOIC-16 packages.
   Moisture sensitivity level is MSL2A for narrow-body SOIC-8 packages.
2. All devices >1 kV_{RMS} are AEC-Q100 qualified.
3. “Si” and “SI” are used interchangeably.

7. Package Outline: 16-Pin Wide Body SOIC

Figure 22 illustrates the package details for the Si860x Digital Isolator. Table 19 lists the values for the dimensions shown in the illustration.

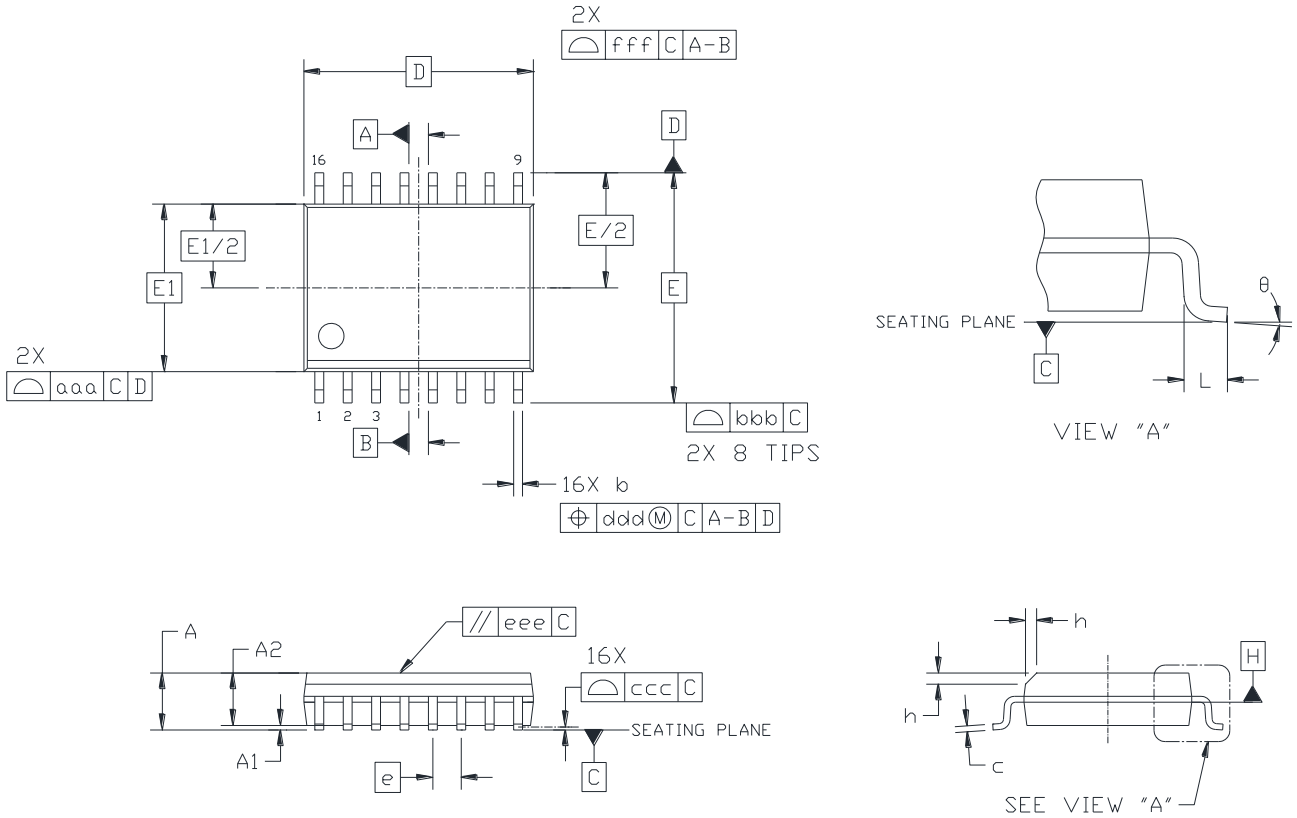


Figure 22. 16-Pin Wide Body SOIC

Table 19. Package Diagram Dimensions

Dimension	Min	Max
A	—	2.65
A1	0.10	0.30
A2	2.05	—
b	0.31	0.51
c	0.20	0.33
D	10.30 BSC	
E	10.30 BSC	
E1	7.50 BSC	
e	1.27 BSC	
L	0.40	1.27
h	0.25	0.75
θ	0°	8°
aaa	—	0.10
bbb	—	0.33
ccc	—	0.10
ddd	—	0.25
eee	—	0.10
fff	—	0.20

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Outline MS-013, Variation AA.
4. Recommended reflow profile per JEDEC J-STD-020C specification for small body, lead-free components.

8. Land Pattern: 16-Pin Wide-Body SOIC

Figure 23 illustrates the recommended land pattern details for the Si860x in a 16-pin wide-body SOIC. Table 20 lists the values for the dimensions shown in the illustration.

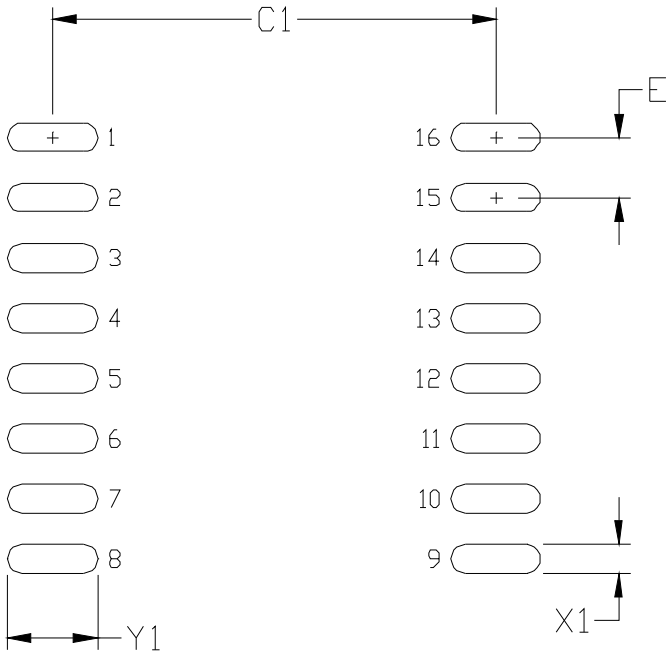


Figure 23. 16-Pin SOIC Land Pattern

Table 20. 16-Pin Wide Body SOIC Land Pattern Dimensions

Dimension	Feature	(mm)
C1	Pad Column Spacing	9.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.90

Notes:
1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P1032X265-16AN for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

9. Package Outline: 8-Pin Narrow Body SOIC

Figure 24 illustrates the package details for the Si860x in an 8-pin SOIC (SO-8). Table 21 lists the values for the dimensions shown in the illustration.

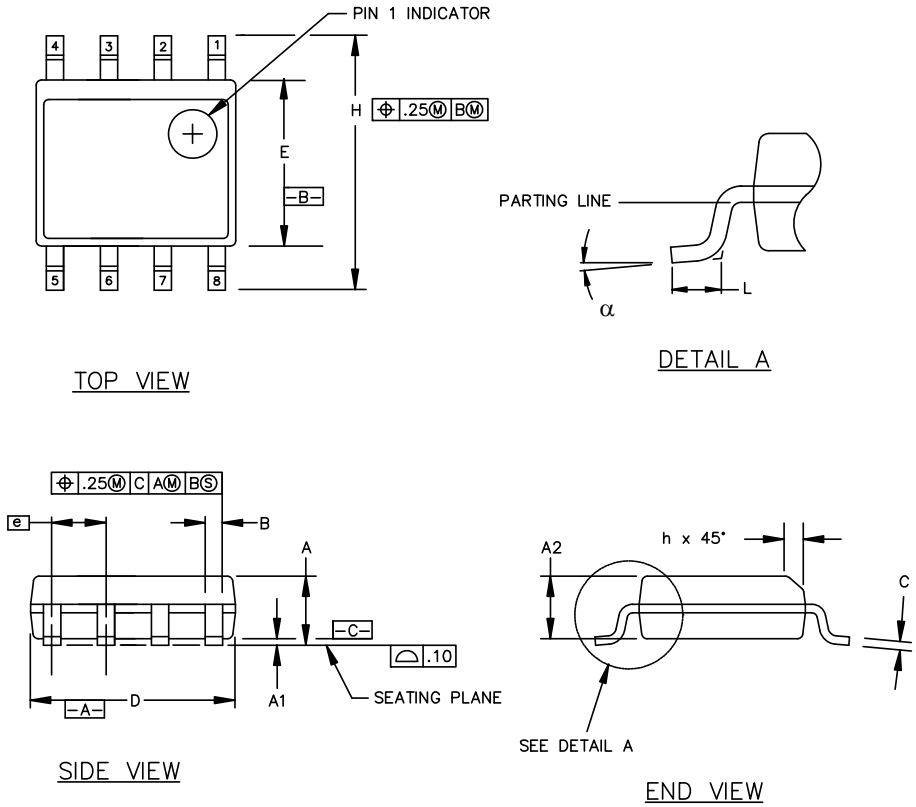


Figure 24. 8-pin Small Outline Integrated Circuit (SOIC) Package

Table 21. Package Diagram Dimensions

Symbol	Millimeters	
	Min	Max
A	1.35	1.75
A1	0.10	0.25
A2	1.40 REF	1.55 REF
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
∝	0°	8°

10. Land Pattern: 8-Pin Narrow Body SOIC

Figure 25 illustrates the recommended land pattern details for the Si860x in an 8-pin narrow-body SOIC. Table 22 lists the values for the dimensions shown in the illustration.

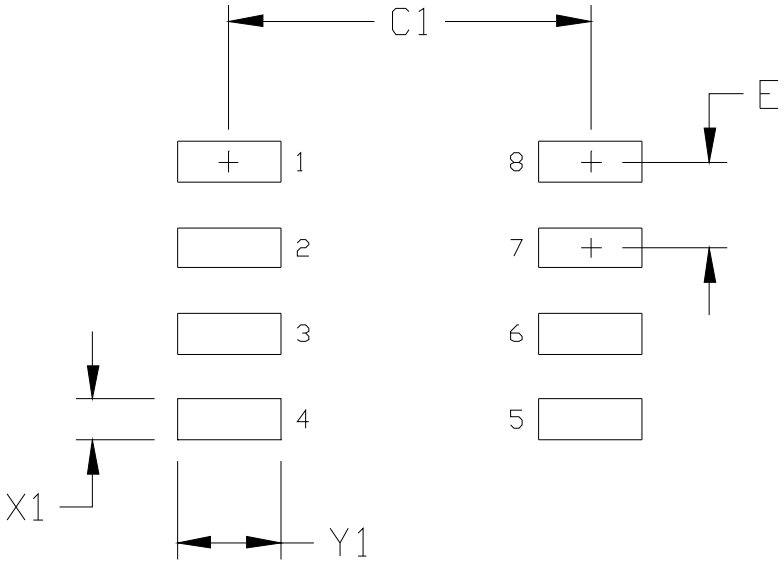


Figure 25. PCB Land Pattern: 8-Pin Narrow Body SOIC

Table 22. PCM Land Pattern Dimensions (8-Pin Narrow Body SOIC)

Dimension	Feature	(mm)
C1	Pad Column Spacing	5.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.55

Notes:
1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P600X173-8N for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

11. Package Outline: 16-Pin Narrow Body SOIC

Figure 26 illustrates the package details for the Si860x in a 16-pin narrow-body SOIC (SO-16). Table 23 lists the values for the dimensions shown in the illustration.

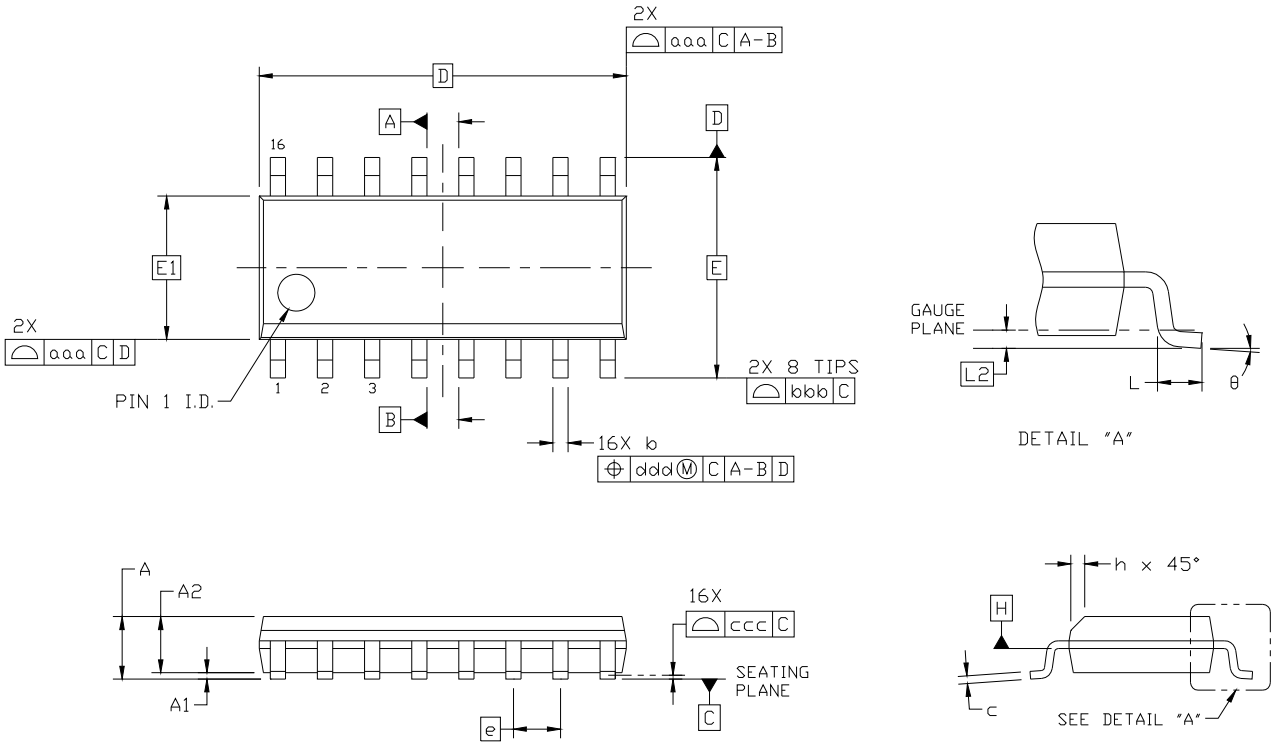


Figure 26. 16-pin Small Outline Integrated Circuit (SOIC) Package

Table 23. Package Diagram Dimensions

Dimension	Min	Max
A	—	1.75
A1	0.10	0.25
A2	1.25	—
b	0.31	0.51
c	0.17	0.25
D	9.90 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
L	0.40	1.27
L2	0.25 BSC	
h	0.25	0.50
θ	0°	8°
aaa	0.10	
bbb	0.20	
ccc	0.10	
ddd	0.25	

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MS-012, Variation AC.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

12. Land Pattern: 16-Pin Narrow Body SOIC

Figure 27 illustrates the recommended land pattern details for the Si860x in a 16-pin narrow-body SOIC. Table 24 lists the values for the dimensions shown in the illustration.

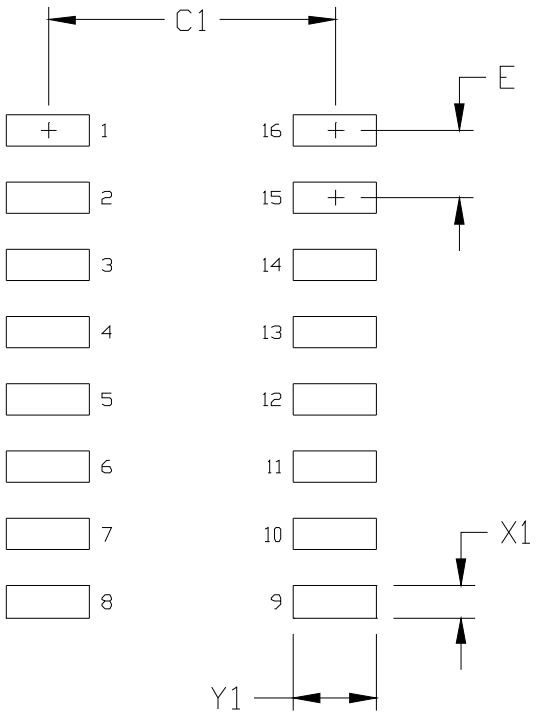


Figure 27. 16-Pin Narrow Body SOIC PCB Land Pattern

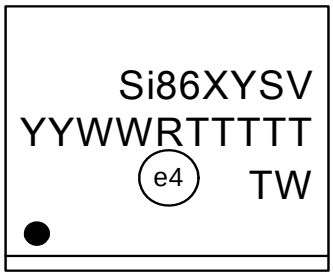
Table 24. 16-Pin Narrow Body SOIC Land Pattern Dimensions

Dimension	Feature	(mm)
C1	Pad Column Spacing	5.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.55

Notes:
1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P600X165-16N for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

13. Top Markings

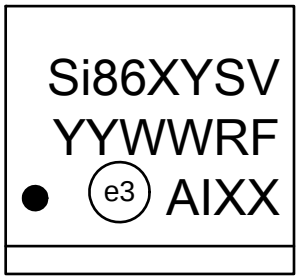
13.1. Si860x Top Marking (16-Pin Wide Body SOIC)



13.2. Top Marking Explanation (16-Pin Wide Body SOIC)

Line 1 Marking:	Base Part Number Ordering Options (See Ordering Guide for more information).	Si86 = Isolator product series XY = Channel Configuration 05 = Bidirectional SCL, SDA; 1- forward and 1-reverse unidirectional channel 06 = Bidirectional SCL, SDA; 2- forward unidirectional channels S = Speed Grade A = 1.7 Mbps V = Isolation rating A = 1 kV; B = 2.5 kV; C = 3.75 kV; D = 5.0 kV
Line 2 Marking:	YY = Year WW = Workweek	Assigned by assembly subcontractor. Corresponds to the year and workweek of the mold date.
	RTTTTT = Mfg Code	Manufacturing code from assembly house “R” indicates revision
Line 3 Marking:	Circle = 1.7 mm Diameter (Center-Justified)	“e4” Pb-Free Symbol
	Country of Origin ISO Code Abbreviation	TW = Taiwan

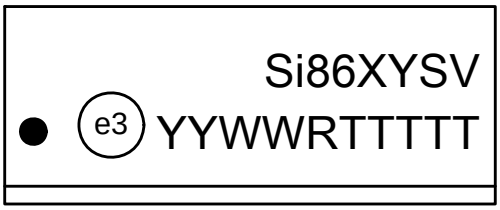
13.3. Si860x Top Marking (8-Pin Narrow Body SOIC)



13.4. Top Marking Explanation (8-Pin Narrow Body SOIC)

Line 1 Marking:	Base Part Number Ordering Options (See Ordering Guide for more information).	Si86 = Isolator I^2C Product Series: XY = Channel Configuration 00 = Bidirectional SCL and SDA channels 02 = Bidirectional SDA channel; Unidirectional SCL channel S = Speed Grade A = 1.7 Mbps V = Isolation rating A = 1 kV; B = 2.5 kV; C = 3.75 kV
Line 2 Marking:	YY = Year WW = Work week	Assigned by assembly contractor. Corresponds to the year and work week of the mold date.
	R = Product Rev F = Wafer Fab	First two characters of the manufacturing code from Assembly.
Line 3 Marking:	Circle = 1.1 mm Diameter Left-Justified	“e3” Pb-Free Symbol
	A = Assembly Site I = Internal Code XX = Serial Lot Number	Last four characters of the manufacturing code from assembly.

13.5. Si860x Top Marking (16-Pin Narrow Body SOIC)



13.6. Top Marking Explanation (16-Pin Narrow Body SOIC)

Line 1 Marking:	Base Part Number Ordering Options	Si86 = Isolator product series XY = Channel Configuration 05 = Bidirectional SCL, SDA; 1- forward and 1-reverse unidirectional channel 06 = Bidirectional SCL, SDA; 2- forward unidirectional channels S = Speed Grade A = 1.7 Mbps V = Isolation rating A = 1 kV; B = 2.5 kV; C = 3.75 kV
Line 2 Marking:	Circle = 1.2 mm Diameter	“e3” Pb-Free Symbol
	YY = Year WW = Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the mold date.
	RTTTTT = Mfg Code	Manufacturing code from assembly house “R” indicates revision
	Circle = 1.2 mm diameter	“e3” Pb-Free Symbol.

DOCUMENT CHANGE LIST

Revision 0.1 to Revision 0.2

- Si8601 replaced by Si8602 throughout.
- Added chip graphics on page 1.
- Moved Table 12 to page 14.
- Updated Table 3, “Si8600/02/05/06 Electrical Characteristics for Bidirectional I2C Channels[1],” on page 5.
- Updated Table 7, “Insulation and Safety-Related Specifications,” on page 11.
- Updated Table 9, “IEC 60747-5-2 Insulation Characteristics for Si86xxxx*,” on page 12.
- Moved “3. Typical Application Overview” to page 16.
- Moved “Typical Performance Characteristics” to page 23.
- Updated "5.Pin Descriptions" on page 24.
- Updated "6.Ordering Guide" on page 27.

Revision 0.2 to Revision 0.3

- Added chip graphics on page 1.
- Moved Tables 1 and 2 to page 4.
- Updated Table 7, “Insulation and Safety-Related Specifications,” on page 11.
- Updated Table 9, “IEC 60747-5-2 Insulation Characteristics for Si86xxxx*,” on page 12.
- Moved Table 13 to page 17.
- Moved Table 14 to page 21.
- Updated "5.Pin Descriptions" on page 24.
- Updated "6.Ordering Guide" on page 27.

Revision 0.3 to Revision 1.0

- Reordered spec tables to conform to new convention.
- Removed “pending” throughout document.

Revision 1.0 to Revision 1.1

- Updated Figures 12 and 13.
  - Updated Pin 7 AGND connection.
- Updated "6.Ordering Guide" on page 27 to include MSL2A.

Revision 1.1 to Revision 1.2

- Updated Table 12 on page 14.
  - Added junction temperature spec.
- Updated "4.4.1.Supply Bypass" on page 22.
- Updated "6.Ordering Guide" on page 27.
  - Removed Rev A devices.
- Updated "7.Package Outline: 16-Pin Wide Body SOIC" on page 28.
- Updated Top Marks.
  - Added revision description.

Revision 1.2 to Revision 1.3

- Added Figure 3, “Common Mode Transient Immunity Test Circuit,” on page 9.
- Added references to CQC throughout.
- Added references to 2.5 kV_{RMS} devices throughout.
- Removed Fail-safe operating mode throughout.
- Updated "6.Ordering Guide" on page 27.
- Updated "13.1.Si860x Top Marking (16-Pin Wide Body SOIC)" on page 36.

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