

## Product Specification

### 40BASE-SR4 QSFP+ Gen2 E-Temp Optical Transceiver Module

#### FTL410QE2N

#### PRODUCT FEATURES

- Four-channel full-duplex transceiver module
- Hot Pluggable QSFP+ form factor
- Maximum link length of 100m on OM3 Multimode Fiber (MMF) and 150m on OM4 MMF
- Multirate capability: 1.06Gb/s to 10.5Gb/s per channel
- Unretimed XLPP electrical interface
- Maximum power dissipation <1.5W
- Reliable VCSEL array technology
- Extended operating case temperature range: -5°C to 85°C
- Single 1x12 MPO receptacle
- RoHS-6 Compliant



#### APPLICATIONS

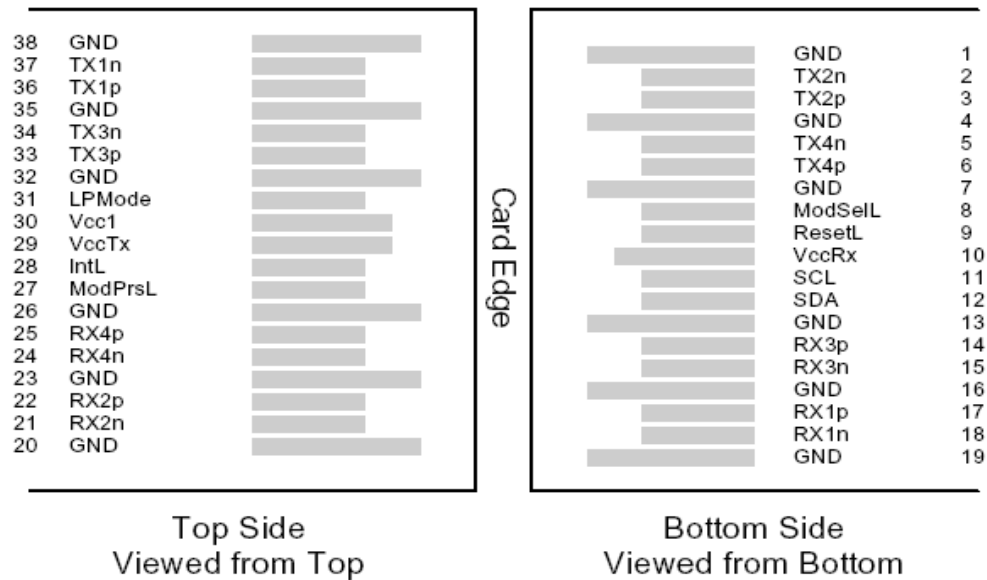
- 40GBASE-SR4 40G Ethernet
- Breakout to 10GBASE-SR Ethernet
- Proprietary interconnections

Finisar's FTL410QE2N QSFP+ transceiver modules are designed for use in 40 Gigabit per second links over multimode fiber. They are compliant with the QSFP+ MSA<sup>1,2</sup> and IEEE 802.3ba 40GBASE-SR4<sup>3</sup>. Module-level digital diagnostic functions are available via an I2C interface, as specified by the QSFP+ MSA. The optical transceiver is compliant per the RoHS Directive 2011/65/EU<sup>4</sup>. See Finisar Application Note AN-2038 for more details<sup>5</sup>.

#### PRODUCT SELECTION

|                   |
|-------------------|
| <b>FTL410QE2N</b> |
|-------------------|

## I. Pin Descriptions



**Figure 1 – QSFP+ MSA-compliant 38-pin connector**

| Pin | Symbol  | Name/Description                    | Notes |
|-----|---------|-------------------------------------|-------|
| 1   | GND     | Ground                              | 1     |
| 2   | Tx2n    | Transmitter Inverted Data Input     |       |
| 3   | Tx2p    | Transmitter Non-Inverted Data Input |       |
| 4   | GND     | Ground                              | 1     |
| 5   | Tx4n    | Transmitter Inverted Data Input     |       |
| 6   | Tx4p    | Transmitter Non-Inverted Data Input |       |
| 7   | GND     | Ground                              | 1     |
| 8   | ModSelL | Module Select                       |       |
| 9   | ResetL  | Module Reset                        |       |
| 10  | Vcc Rx  | +3.3 V Power supply receiver        |       |
| 11  | SCL     | 2-wire serial interface clock       |       |
| 12  | SDA     | 2-wire serial interface data        |       |
| 13  | GND     | Ground                              | 1     |
| 14  | Rx3p    | Receiver Non-Inverted Data Output   |       |
| 15  | Rx3n    | Receiver Inverted Data Output       |       |
| 16  | GND     | Ground                              | 1     |
| 17  | Rx1p    | Receiver Non-Inverted Data Output   |       |
| 18  | Rx1n    | Receiver Inverted Data Output       |       |
| 19  | GND     | Ground                              | 1     |
| 20  | GND     | Ground                              | 1     |
| 21  | Rx2n    | Receiver Inverted Data Output       |       |
| 22  | Rx2p    | Receiver Non-Inverted Data Output   |       |
| 23  | GND     | Ground                              | 1     |
| 24  | Rx4n    | Receiver Inverted Data Output       |       |
| 25  | Rx4p    | Receiver Non-Inverted Data Output   |       |
| 26  | GND     | Ground                              | 1     |

|    |         |                                     |   |
|----|---------|-------------------------------------|---|
| 27 | ModPrsL | Module Present                      |   |
| 28 | IntL    | Interrupt                           |   |
| 29 | Vcc Tx  | +3.3 V Power supply transmitter     |   |
| 30 | Vcc1    | +3.3 V Power Supply                 |   |
| 31 | LPMode  | Low Power Mode                      |   |
| 32 | GND     | Ground                              | 1 |
| 33 | Tx3p    | Transmitter Non-Inverted Data Input |   |
| 34 | Tx3n    | Transmitter Inverted Data Input     |   |
| 35 | GND     | Ground                              | 1 |
| 36 | Tx1p    | Transmitter Non-Inverted Data Input |   |
| 37 | Tx1n    | Transmitter Inverted Data Input     |   |
| 38 | GND     | Ground                              | 1 |

Notes

1. Circuit ground is internally isolated from chassis ground.

## II. General Product Characteristics

| Parameter                         | Value                                                                           | Unit  | Notes                                                                     |
|-----------------------------------|---------------------------------------------------------------------------------|-------|---------------------------------------------------------------------------|
| Module Form Factor                | QSFP+                                                                           |       |                                                                           |
| Number of Lanes                   | 4 Tx and 4 Rx                                                                   |       |                                                                           |
| Maximum Aggregate Data Rate       | 42.0                                                                            | Gb/s  |                                                                           |
| Maximum Data Rate per Lane        | 10.5                                                                            | Gb/s  | Higher bit rates may be supported. Please contact Finisar.                |
| Protocols Supported               | Typical applications include 40G Ethernet, Infiniband, Fibre Channel, SATA/SAS3 |       |                                                                           |
| Operating Case Temperature        | -5 to +85                                                                       | C     |                                                                           |
| Electrical Interface and Pin-out  | 38-pin edge connector                                                           |       | Pin-out as defined by the QSFP+ MSA                                       |
| Maximum Power Consumption per End | 1.5                                                                             | Watts | Varies with output voltage swing and pre-emphasis settings (see Figure 2) |
| Management Interface              | Serial, I2C-based, 400 kHz maximum frequency                                    |       | As defined by the QSFP+ MSA                                               |

| Data Rate Specifications | Symbol | Min  | Typ | Max        | Units  | Ref. |
|--------------------------|--------|------|-----|------------|--------|------|
| Bit Rate per Lane        | BR     | 1062 |     | 10500      | Mb/sec | 1    |
| Bit Error Ratio          | BER    |      |     | $10^{-12}$ |        | 2    |
| Link distance on OM3 MMF | d      |      |     | 100        | meters | 3    |
| Link distance on OM4 MMF | d      |      |     | 150        | meters | 3    |

Notes:

1. Compliant with 40G Ethernet. Compatible with 1/10 Gigabit Ethernet and 1/2/4/8/10G Fibre Channel.
2. Tested with a PRBS  $2^{31}-1$  test pattern.
3. Per 40GBASE-SR4, IEEE 802.3ba

### III. Absolute Maximum Ratings

| Parameter                  | Symbol                                                         | Min  | Typ | Max | Unit | Ref. |
|----------------------------|----------------------------------------------------------------|------|-----|-----|------|------|
| Maximum Supply Voltage     | V <sub>cc1</sub> ,<br>V <sub>ccTx</sub> ,<br>V <sub>ccRx</sub> | -0.5 |     | 3.6 | V    |      |
| Storage Temperature        | T <sub>s</sub>                                                 | -40  |     | 85  | °C   |      |
| Case Operating Temperature | T <sub>OP</sub>                                                | -5   |     | 85  | °C   |      |
| Relative Humidity          | RH                                                             | 0    |     | 85  | %    | 1    |
| Damage Threshold, per Lane | DT                                                             | 3.4  |     |     | dBm  |      |

#### Notes:

1. Non-condensing.

### IV. Electrical Characteristics (T<sub>OP</sub> = -5 to 85°C, V<sub>CC</sub> = 3.15 to 3.45 Volts)

| Parameter                                    | Symbol                                                         | Min                                     | Typ                   | Max  | Unit             | Ref. |
|----------------------------------------------|----------------------------------------------------------------|-----------------------------------------|-----------------------|------|------------------|------|
| Supply Voltage                               | V <sub>cc1</sub> ,<br>V <sub>ccTx</sub> ,<br>V <sub>ccRx</sub> | 3.15                                    |                       | 3.45 | V                |      |
| Supply Current                               | I <sub>cc</sub>                                                |                                         |                       | 350  | mA               |      |
| <b>Link turn-on time</b>                     |                                                                |                                         |                       |      |                  |      |
| Transmit turn-on time                        |                                                                |                                         |                       | 2000 | ms               | 2    |
| <b>Transmitter (per Lane)</b>                |                                                                |                                         |                       |      |                  |      |
| Single ended input voltage tolerance         | V <sub>inT</sub>                                               | -0.3                                    |                       | 4.0  | V                |      |
| Differential data input swing                | V <sub>in,pp</sub>                                             | 180                                     |                       | 1200 | mV <sub>pp</sub> | 3    |
| Differential input threshold                 |                                                                |                                         | 50                    |      | mV               |      |
| AC common mode input voltage tolerance (RMS) |                                                                | 15                                      |                       |      | mV               |      |
| Differential input return loss               |                                                                | Per IEEE P802.3ba,<br>Section 86A.4.1.1 |                       |      | dB               | 4    |
| J2 Jitter Tolerance                          | J <sub>t2</sub>                                                | 0.17                                    |                       |      | UI               |      |
| J9 Jitter Tolerance                          | J <sub>t9</sub>                                                | 0.29                                    |                       |      | UI               |      |
| Data Dependent Pulse Width Shrinkage         | DDPWS                                                          | 0.07                                    |                       |      | UI               |      |
| Eye mask coordinates {X1, X2<br>Y1, Y2}      |                                                                |                                         | 0.11, 0.31<br>95, 350 |      | UI<br>mV         | 5    |
| <b>Receiver (per Lane)</b>                   |                                                                |                                         |                       |      |                  |      |
| Single-ended output voltage                  |                                                                | -0.3                                    |                       | 4.0  | V                |      |
| Differential data output swing               | V <sub>out,pp</sub>                                            | 0                                       |                       | 800  | mV <sub>pp</sub> | 7,8  |
| AC common mode output voltage (RMS)          |                                                                |                                         |                       | 7.5  | mV               |      |
| Termination mismatch at 1 MHz                |                                                                |                                         |                       | 5    | %                |      |
| Differential output return loss              |                                                                | Per IEEE P802.3ba,<br>Section 86A.4.2.1 |                       |      | dB               | 4    |
| Common mode output return loss               |                                                                | Per IEEE P802.3ba,<br>Section 86A.4.2.2 |                       |      | dB               | 4    |
| Output transition time, 20% to 80%           |                                                                | 28                                      |                       |      | ps               |      |
| J2 Jitter output                             | J <sub>o2</sub>                                                |                                         |                       | 0.42 | UI               |      |
| J9 Jitter output                             | J <sub>o9</sub>                                                |                                         |                       | 0.65 | UI               |      |
| Eye mask coordinates #1 {X1, X2<br>Y1, Y2}   |                                                                |                                         | 0.29, 0.5<br>150, 425 |      | UI<br>mV         | 6    |
| Eye mask coordinates #2 {X1, X2<br>Y1, Y2}   |                                                                |                                         | 0.29, 0.5<br>125, 500 |      | UI<br>mV         | 5    |
| Power Supply Ripple Tolerance                | PSR                                                            | 50                                      |                       |      | mV <sub>pp</sub> |      |

Notes:

1. Maximum total power value is specified across the full temperature and voltage range.
2. From power-on and end of any fault conditions.
3. After internal AC coupling. Self-biasing 100Ω differential input.
4. 10 MHz to 11.1 GHz range
5. Hit ratio =  $5 \times 10^{-5}$ . Valid for all settings in Figure 2.
6. Hit ratio =  $5 \times 10^{-5}$ . Valid only for the shaded settings in Figure 2.
7. AC coupled with 100Ω differential output impedance.
8. Settable in 4 discrete steps via the I2C interface. See Figure 2 for Vout settings.

| Power (mW) |     | Pre-Emphasis into 100ohms (mV) |      |      |      |
|------------|-----|--------------------------------|------|------|------|
|            |     | 0                              | 125  | 175  | 325  |
| Vout (mV)  | 0   | 599                            |      |      |      |
|            | 317 | 751                            | 935  | 971  | 1075 |
|            | 422 | 787                            | 971  | 1007 | 1111 |
|            | 739 | 883                            | 1055 | 1103 | 1190 |

Figure 2 – Power Dissipation (mW, maximum) vs. Rx Output Conditions

**V. Optical Characteristics ( $T_{OP} = -5$  to  $85^{\circ}\text{C}$ ,  $V_{CC} = 3.15$  to  $3.45$  Volts)**

| Parameter                                                | Symbol           | Min                               | Typ  | Max  | Unit  | Ref. |
|----------------------------------------------------------|------------------|-----------------------------------|------|------|-------|------|
| <b>Transmitter (per Lane)</b>                            |                  |                                   |      |      |       |      |
| Signaling Speed per Lane                                 |                  |                                   | 10.5 |      | GBd   | 1    |
| Center wavelength                                        |                  | 840                               |      | 860  | nm    |      |
| RMS Spectral Width                                       | SW               |                                   |      | 0.65 | nm    |      |
| Average Launch Power per Lane                            | TXP <sub>x</sub> | -7.6                              |      | 0.0  | dBm   |      |
| Transmit OMA per Lane                                    | TxOMA            | -5.6                              |      | 3.0  | dBm   | 2    |
| Difference in Power between any two lanes [OMA]          | DP <sub>x</sub>  |                                   |      | 4.0  | dB    |      |
| Peak Power per Lane                                      | PP <sub>x</sub>  |                                   |      | 4.0  | dBm   |      |
| Launch Power [OMA] minus TDP per Lane                    | P-TDP            | -6.5                              |      |      | dBm   |      |
| TDP per Lane                                             | TDP              |                                   |      | 3.5  | dBm   |      |
| Optical Extinction Ratio                                 | ER               | 3.0                               |      |      | dB    |      |
| Optical Return Loss Tolerance                            | ORL              |                                   |      | 12   | dB    |      |
| Encircled Flux                                           | FLX              | > 86% at 19 um<br>< 30% at 4.5 um |      |      | dBm   |      |
| Average launch power of OFF transmitter, per lane        |                  |                                   |      | -30  | dBm   |      |
| Relative Intensity Noise                                 | RIN              |                                   |      | -128 | dB/Hz |      |
| Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3} |                  | 0.23, 0.34, 0.43, 0.27, 0.35, 0.4 |      |      |       |      |

| Parameter                                               | Symbol           | Min      | Typ  | Max  | Unit    | Ref. |
|---------------------------------------------------------|------------------|----------|------|------|---------|------|
| <b>Receiver (per Lane)</b>                              |                  |          |      |      |         |      |
| Signaling Speed per Lane                                |                  |          | 10.5 |      | GBd     | 3    |
| Center wavelength                                       |                  | 840      |      | 860  | nm      |      |
| Damage Threshold                                        | DT               | 3.4      |      |      | dBm     |      |
| Average Receive Power per Lane                          | RXP <sub>x</sub> | -9.5     |      | 2.4  | dBm     |      |
| Receive Power (OMA) per Lane                            | RxOMA            |          |      | 3.0  | dBm     |      |
| Stressed Receiver Sensitivity (OMA) per Lane            | SRS              |          |      | -5.4 | dBm     |      |
| Peak Power, per lane                                    | PP <sub>x</sub>  |          |      | 4    | dBm     |      |
| Receiver Reflectance                                    | Rfl              |          |      | -12  | dB      |      |
| Vertical eye closure penalty, per lane                  |                  |          |      | 1.9  | dB      |      |
| Stressed eye J2 jitter, per Lane                        |                  |          |      | 0.3  | UI      |      |
| Stressed eye J9 jitter, per Lane                        |                  |          |      | 0.47 | UI      |      |
| OMA of each aggressor lane                              |                  |          |      | -0.4 | dBm     |      |
| Rx jitter tolerance: Jitter frequency and p-p amplitude |                  | (75, 5)  |      |      | kHz, UI |      |
|                                                         |                  | (375, 1) |      |      | kHz, UI |      |
| LOS De-Assert                                           | LOS <sub>D</sub> |          |      | -12  | dBm     |      |
| LOS Assert                                              | LOS <sub>A</sub> | -30      |      |      | dBm     |      |
| LOS Hysteresis                                          |                  | 0.5      |      |      | dBm     |      |

**Notes:**

1. Transmitter consists of 4 lasers operating at a maximum rate of 10.5Gb/s each.
2. Even if TDP is <0.9dB, the OMA min must exceed this value.
3. Receiver consists of 4 photodetectors operating at a maximum rate of 10.5Gb/s each.

**VI. Memory Map and Control Registers**

Compatible with SFF-8436<sup>1</sup> and SFF-8636.<sup>2</sup> Please see Finisar Application Note AN-2079<sup>6</sup> for implementation details.

**VII. Environmental Specifications**

Finisar FTL410QE2N transceivers have an operating temperature range from -5°C to +85°C case temperature.

| Environmental Specifications | Symbol           | Min | Typ | Max | Units | Ref. |
|------------------------------|------------------|-----|-----|-----|-------|------|
| Case Operating Temperature   | T <sub>op</sub>  | -5  |     | 85  | °C    |      |
| Storage Temperature          | T <sub>sto</sub> | -40 |     | 85  | °C    |      |

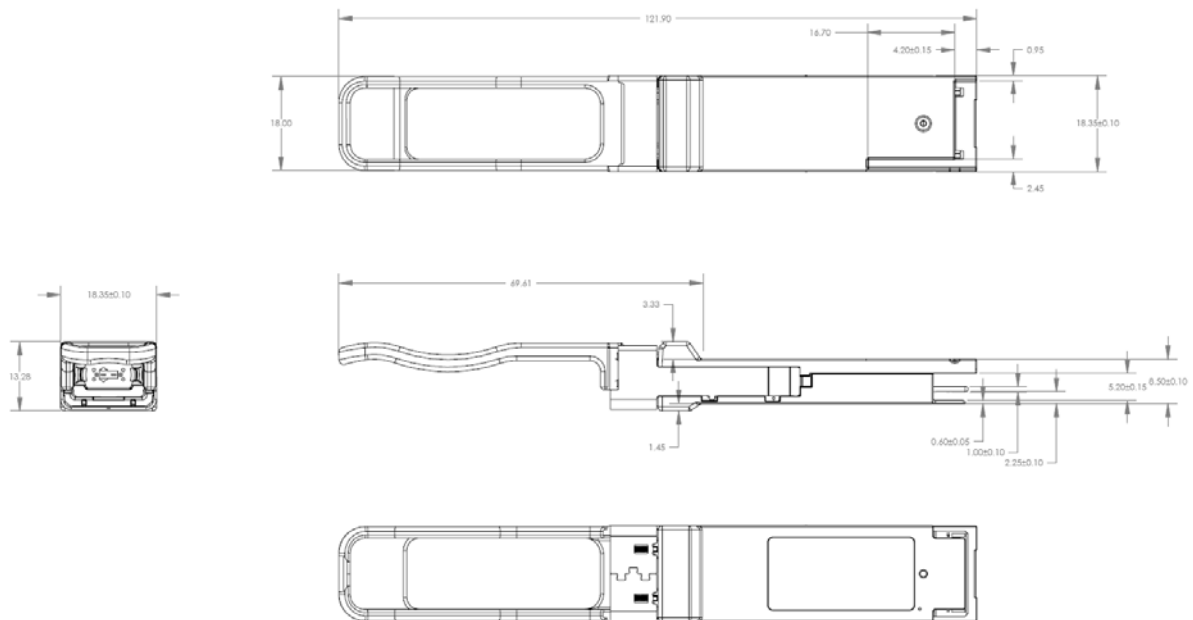
## VIII. Regulatory Compliance

Finisar FTL410QE2N transceivers are RoHS-6 Compliant. Copies of certificates are available at Finisar Corporation upon request.

FTL410QE2N transceiver modules are Class 1 laser eye safety compliant per IEC 60825-1.

## IX. Mechanical Specifications

The FTL410QE2N mechanical specifications are compliant to the QSFP+ MSA transceiver module specifications.



**Figure 3 – FTL410QE2N mechanical drawing**



Figure 4 – FTL410QE2N product label

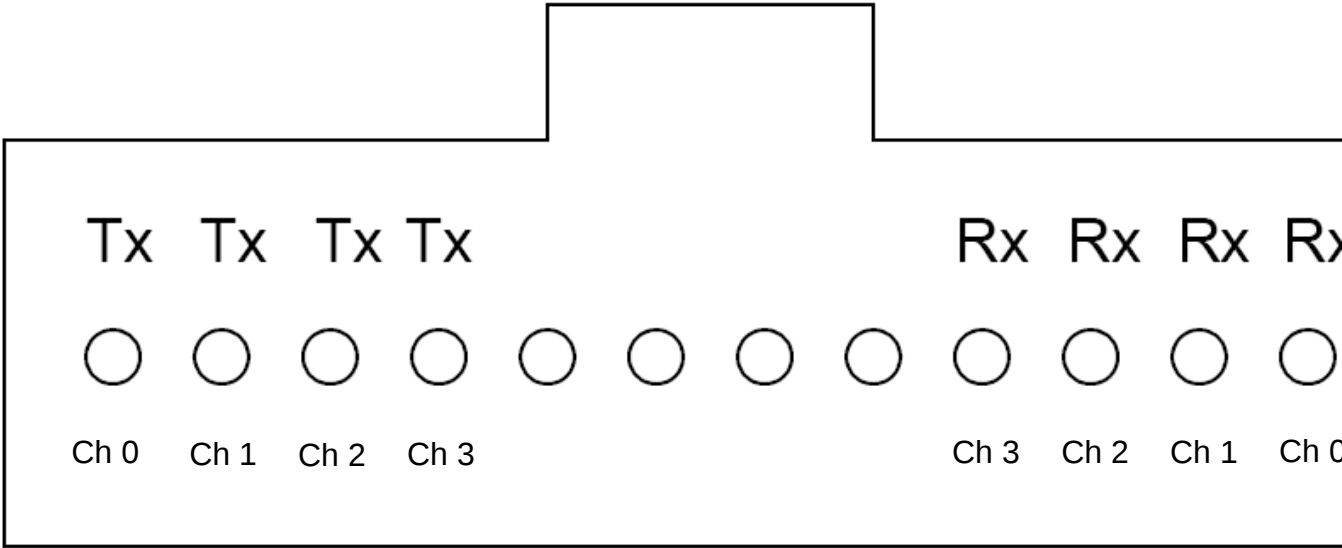


Figure 5 – FTL410QE2N optical lane assignment  
(front view of MPO receptacle)

**X. References**

1. SFF-8436 – Specification for QSFP+ Copper and Optical Transceiver, Rev 4.8, October 2013.
2. SFF-8636 – Specification for Common Management Interface, Rev 1.7, January 2014.
3. IEEE 802.3ba – PMD Type 40GBASE-SR4.
4. Directive 2011/65/EU of the European Council Parliament and of the Council, “on the restriction of the use of certain hazardous substances in electrical and electronic equipment”. Certain products may use one or more exemptions as allowed by the Directive.
5. “Application Note AN-2038: Finisar Implementation of RoHS Compliant Transceivers”.
6. “Application Note AN-2079: QSFP Module EEPROM Mapping”, Rev. G, Finisar Corporation, May, 2013.

**XI. For More Information**

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