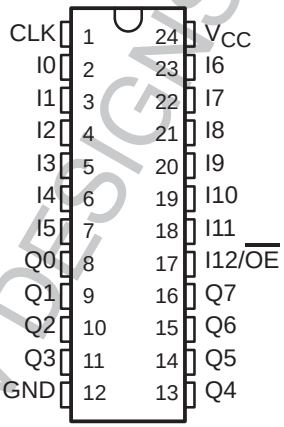
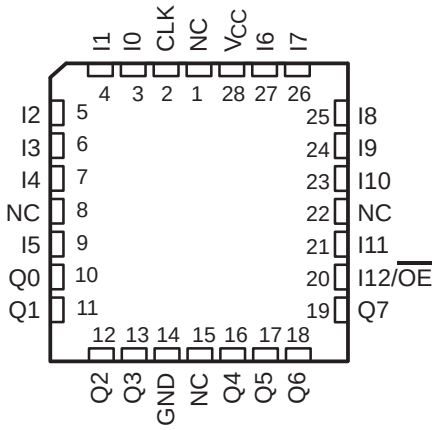
- **58-MHz Max Clock Rate**
- **Ideal for Waveform Generation and High-Performance State Machine Applications**
- **6-Bit Internal Binary Counter**
- **8-Bit Internal State Register**
- **Programmable Clock Polarity**
- **Outputs Programmable for Registered or Combinational Operation**
- **6-Bit Counter Simplifies Logic Equation Development in State Machine Designs**
- **Programmable Output Enable**

JT OR NT PACKAGE
(TOP VIEW)



FK OR FN PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TIBPSG507AC is a 13 × 80 × 8 Programmable Sequence Generator (PSG) that offers the system designer unprecedented flexibility in a high-performance field-programmable logic device. Applications such as waveform generators, state machines, dividers, timers, and simple logic reduction are all possible with the PSG. By utilizing the built-in binary counter, the PSG is capable of generating complex timing controllers. The binary counter also simplifies logic equation development in state machine and waveform generator applications.

The TIBPSG507AC contains 80 product (AND) terms, a 6-bit binary counter with control logic, eight S/R state holding registers, and eight outputs. The eight outputs can be individually programmed for either registered or combinational operation. The clock input is fuse programmable for either positive- or negative-edge operation.

The 6-bit binary counter is controlled by a synchronous-clear and a count/hold function. Each control function has a nonregistered and registered option. When either SCLR0 or SCLR1 is taken high, the counter resets to zero on the next active clock edge. When either $\overline{\text{CNT}}$/HLD0 or $\overline{\text{CNT}}$/HLD1 is taken high, the counter is held at the present count and is not allowed to advance on the active clock edge. The SCLR function overrides the $\overline{\text{CNT}}$/HLD feature when both lines are simultaneously high.

Clock polarity is programmable through the clock polarity fuse. Leaving this fuse intact selects positive-edge triggering. Negative-edge triggering is selected by blowing this fuse. Pin 17 functions as an input and/or an output enable. When the output enable fuse is intact, all outputs are always enabled allowing pin 17 to be used strictly as an input. Blowing the output enable fuse lets pin 17 function as an output enable and an input. In this mode, the outputs are enabled when pin 17 is low and are in a high-impedance state when pin 17 is high.

NOT RECOMMENDED FOR NEW DESIGNS

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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description (continued)

The eight outputs can be individually programmed for combinational operation by blowing the output multiplexer fuse. After power up, the device must be initialized to the desired state. When the output multiplexer fuse is left intact, registered operation is selected.

The TIBPSG507AC is characterized for operation from 0°C to 75°C.

6-BIT COUNTER CONTROL FUNCTION TABLE (see Note 1)

$\overline{CNT}$/HLD1	$\overline{CNT}$/HLD0	SCLR1	SCLR0	OPERATION
L	L	L	L	counter active
X	X	X	H	synchronous clear
X	X	H	X	synchronous clear
X	H	L	L	hold counter
H	X	L	L	hold counter

NOTE 1: When all fuses are blown on a product line (AND), its output will be high. When all fuses are blown on a sum line (OR), its output will be low. All product and sum terms are low on devices with fuses intact.

S/R FUNCTION TABLE (see Note 2)

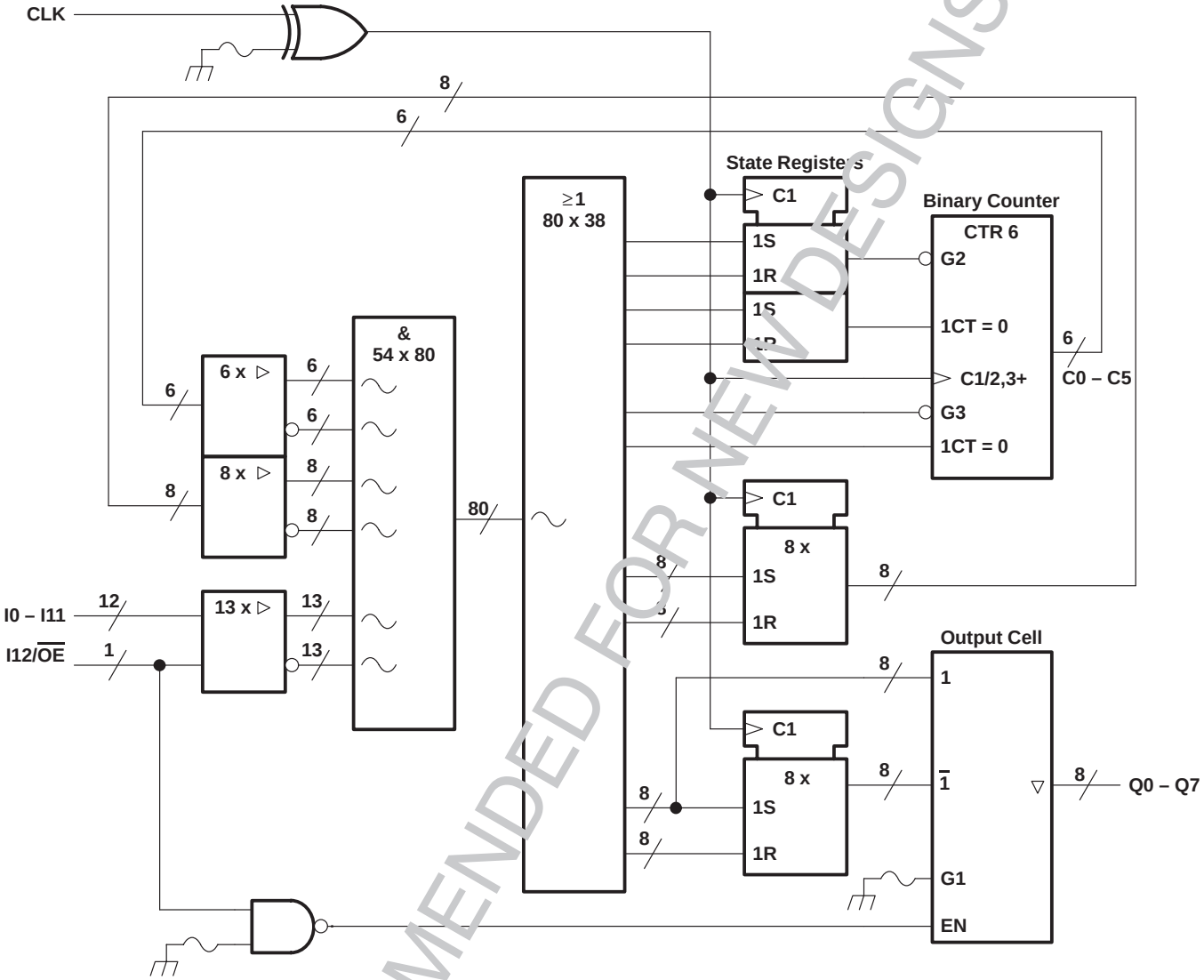
CLK POLARITY FUSE	CLK	S	R	STATE REGISTER
INTACT	↑	L	L	Q_0
INTACT	↑	L	H	L
INTACT	↑	H	L	H
INTACT	↑	H	H	INDET†
BLOWN	↓	L	L	Q_0
BLOWN	↓	L	H	L
BLOWN	↓	H	L	H
BLOWN	↓	H	H	INDET†

† Output state is indeterminate

NOTE 2: After power up, the device must be initialized to its desired state. Q_0 is the state of the S/R register before the active clock edge.

NOT RECOMMENDED FOR NEW DESIGNS

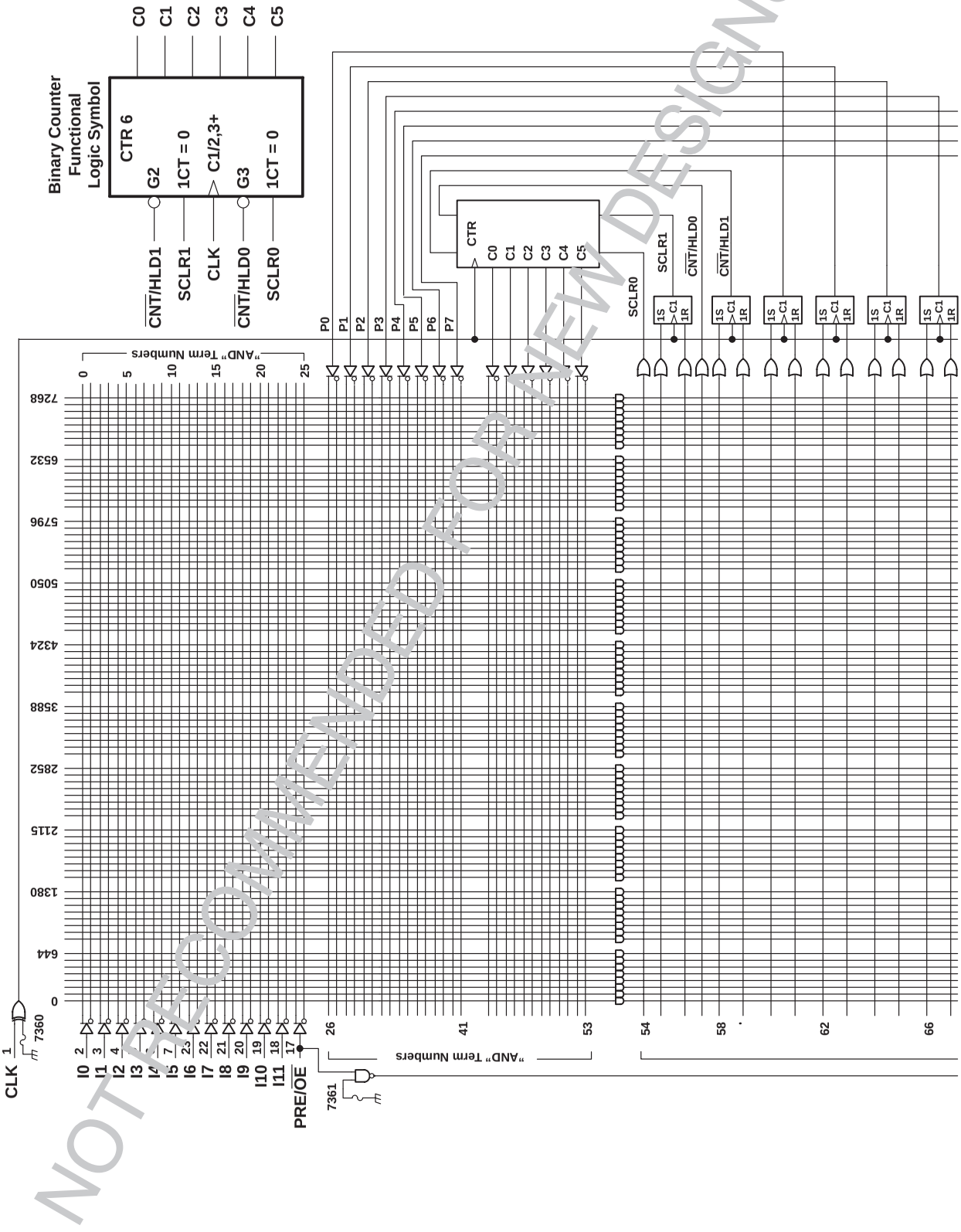
functional block diagram (positive logic)



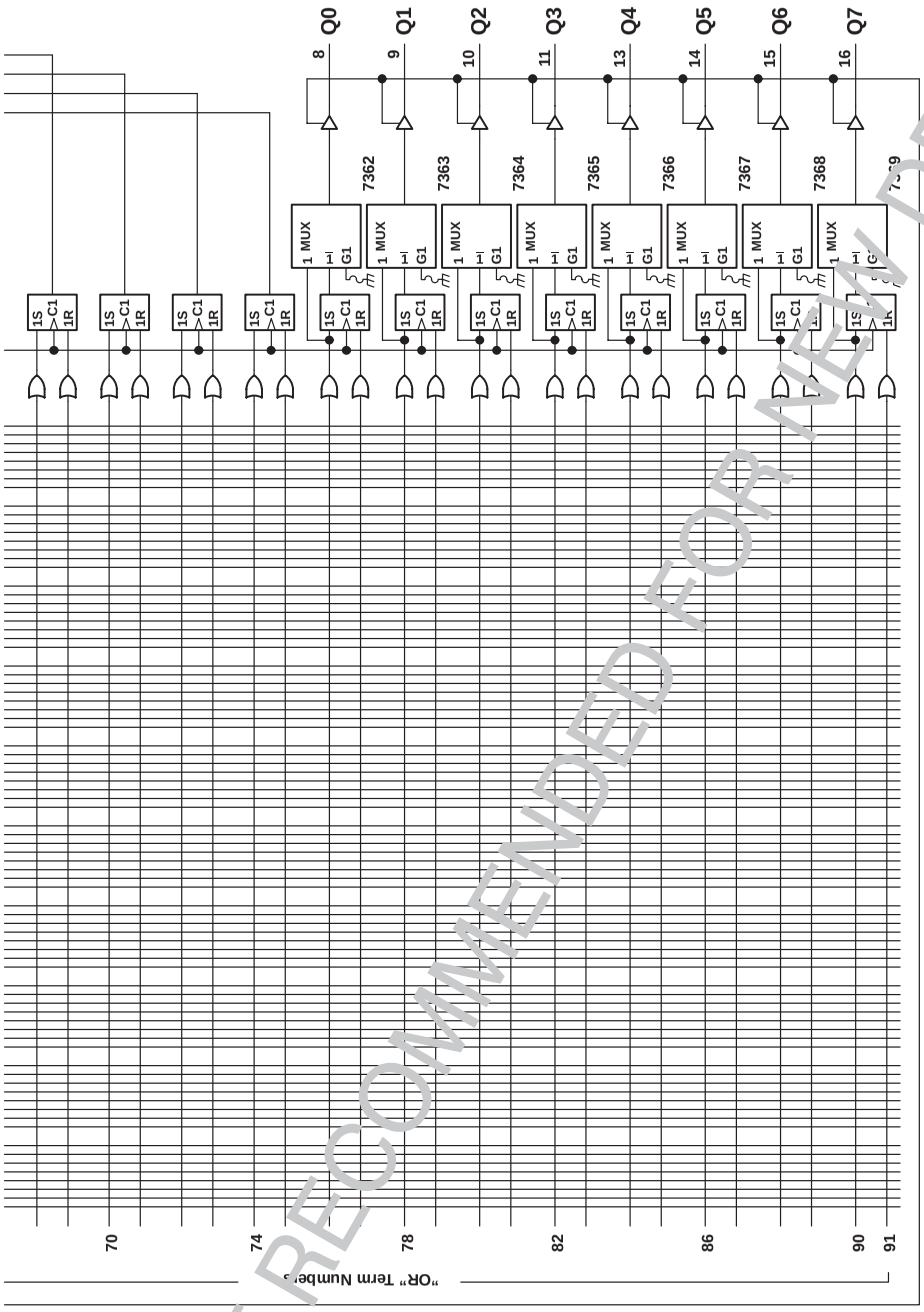
denotes fused inputs

NOT RECOMMENDED FOR NEW DESIGNS

logic diagram (positive logic)



NOT RECOMMENDED FOR NEW DESIGNS



All inputs to AND gates, exclusive-OR gates, and multiplexers with a blown link assume the logic-1 state.
All OR gate inputs with a blown link assume the logic-0 state.

NOT RECOMMENDED FOR NEW DESIGNS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 3) . . . . . 7 V
Input voltage (see Note 3) . . . . . 5.5 V
Voltage applied to disabled output (see Note 3) . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 75°C
Storage temperature range . . . . . –65°C to 150°C

NOTE 3: These ratings apply except for programming pins during a programming cycle or during the diagnostic mode.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				–3.2	mA
I_{OL}	Low-level output current				16	mA
t_w	Pulse duration	Clock high	6			ns
		Clock low	6			
t_{su}	Setup time before CLK active transition†	Input or feedback to S/R↑ inputs	12			ns
		Input or feedback to S/R↓ inputs‡	19			
		Input or feedback to SCLR0	20			
		Input or feedback to $\overline{\text{CNT}}$/HLD0	25			
t_h	Hold time after CLK active transition†	Input or feedback at S/R inputs	0			ns
		Input or feedback at SCLR0	0			
		Input or feedback at $\overline{\text{CNT}}$/HLD0	0			
T_A	Operating free-air temperature		0	25	75	°C

† Internal setup and hold times, t_{su} feedback to SCLR1, feedback to $\overline{\text{CNT}}$/HLD1; t_h feedback at SCLR1 and feedback at $\overline{\text{CNT}}$/HLD1, are guaranteed by f_{max} specifications. The active transition of CLK is determined by the programmed state of the CLK polarity fuse.
‡ See the OR term loading section and Figure 3.

NOT RECOMMENDED FOR NEW DESIGNS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.75 V,	I_I = –18 mA				–1.2	V
V_{OH}	V_{CC} = 4.75 V,	I_{OH} = –3.2 mA		2.4	3.2		V
V_{OL}	V_{CC} = 4.75 V,	I_{OL} = 16 mA			0.25	0.5	V
I_{OZH}	V_{CC} = 5.25 V,	V_O = 2.7 V				20	µA
I_{OZL}	V_{CC} = 5.25 V,	V_O = 0.4 V				–20	µA
I_I	V_{CC} = 5.25 V,	V_I = 5.5 V				0.1	mA
I_{IH}	V_{CC} = 5.25 V,	V_I = 2.7 V				20	µA
I_{IL}	V_{CC} = 5.25 V,	V_I = 0.4 V				–0.25	mA
I_O‡	V_{CC} = 5.25 V,	V_O = 0.5 V		–30		–130	mA
I_{CC}	V_{CC} = 5.25 V,	See Note 4,	Outputs open		156	210	mA
C_i	f = 1 MHz,	V_I = 2 V			7		pF
C_o	f = 1 MHz,	V_O = 2 V			11		pF
C_{clk}	f = 1 MHz,	V_{CLK} = 2 V			14		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	TYP†	MAX	UNIT
f_{max}§	6-Bit counter with SCLR1 or $\overline{CNT}$/HLD1		R1 = 300 Ω, R2 = 390 Ω, See Figure 6	58	65		MHz
	6-Bit counter with SCLR0			40	55		
	6-Bit counter with $\overline{CNT}$/HLD0			33	50		
	With external feedback (see Figure 1)			45	60		
t_{pd}¶	CLK	Q (nonregistered)#		6		25	ns
		Q (registered)		3		10	
	I or Feedback	Q (nonregistered)		6		20	ns
t_{en}	$\overline{OE}$↓	Q		1	6	10	ns
t_{dis}	$\overline{OE}$↑	Q		1	6	10	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ This parameter approximates I_{OS}. The condition V_O = 0.5 V takes tester noise into account. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
§ See the f_{max} calculations section.
¶ The active edge of CLK is determined by the programmed state of the CLK polarity fuse.
# t_{pd} CLK to Q (nonregistered) is the same for data clocked from the counter or state registered.
NOTE 4: When the clock is programmed for negitive edge, then V_I = 4.5 V. When the clock is programmed for positive edge, then V_I = 0.

NOT RECOMMENDED FOR NEW DESIGNS

f_{max} calculations

The following are the different speeds that can be achieved when using the TIBPSG507AC as a state machine. The way the 6-bit counter is controlled will largely determine the operating frequency of the state machine.

f_{max} for a 6-bit counter using SCLR1 or $\overline{CNT}$/HLD1 = $\frac{1}{t_{su} + t_{pd}\ \text{CLK to Q}}$ where setup time t_{su} for input or feedback to the S/R inputs = 12 ns and propagation delay time t_{pd} CLK to Q for the internal S/R registers = 5 ns (difference in t_{pd} from CLK and feedback, 25 to 20).

Thus: f_{max} for this condition = $\frac{1}{(12 + 5)\ \text{ns}} = \frac{1}{17\ \text{ns}} = 58\ \text{MHz}$

f_{max} for a 6-bit counter using SCLR0 for reset = $\frac{1}{t_{su} + t_{pd}\ \text{CLK to Q}}$ where setup time t_{su} for input or feedback to the SCLR0 inputs = 20 ns and propagation delay time t_{pd} CLK to Q for the internal S/R registers = 5 ns (difference in t_{pd} from CLK and feedback, 25 to 20)

Thus: f_{max} for this condition = $\frac{1}{(20 + 5)\ \text{ns}} = \frac{1}{25\ \text{ns}} = 40\ \text{MHz}$.

f_{max} for a 6-bit counter using $\overline{CNT}$/HLD0 for reset = $\frac{1}{t_{su} + t_{pd}\ \text{CLK to Q}}$ where setup time t_{su} for input or feedback to $\overline{CNT}$/HLD0 = 25 ns and propagation delay time t_{pd} CLK to Q for the internal S/R registers = 5 ns (difference in t_{pd} from CLK and feedback, 25 to 20).

Thus: f_{max} for this condition = $\frac{1}{(25 + 5)\ \text{ns}} = \frac{1}{30\ \text{ns}} = 33\ \text{MHz}$.

programming information

Texas Instruments programmable logic devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers that are capable of programming Texas Instruments programmable logic is also available, upon request, from the nearest TI sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

NOT RECOMMENDED FOR NEW DESIGNS

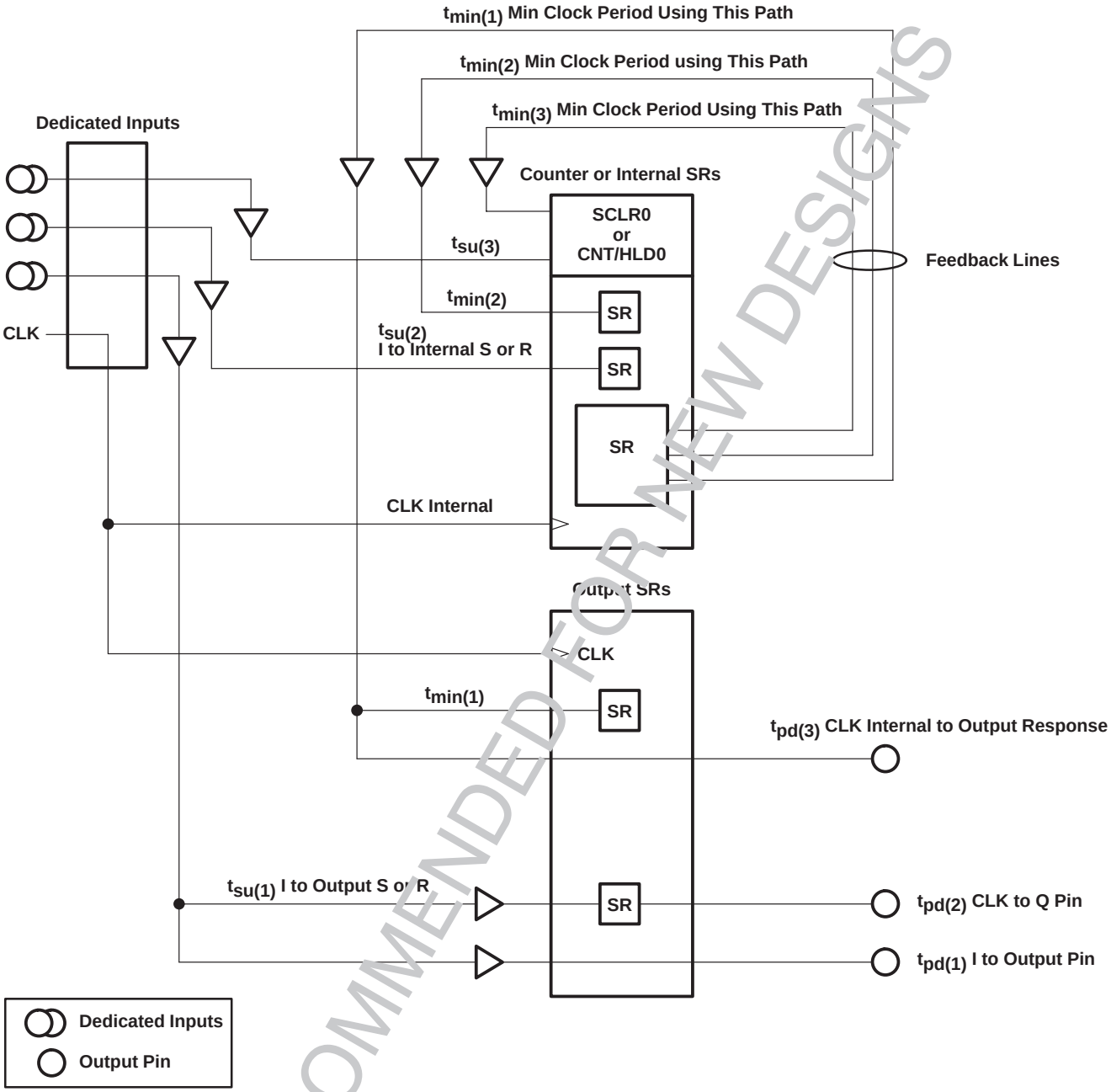


Figure 1. Timing Model

NOT RECOMMENDED FOR NEW DESIGNS

glossary — timing model

$tpd_{(1)}$ — Maximum time interval from the time a signal edge is received at any input pin to the time any logically affected combinational output pin delivers a response.

$t_{pd(2)}$ — Maximum time interval from a positive edge on the clock input pin to data delivery on the output pin corresponding to any output SR register.

$t_{pd(3)}$ — Maximum time interval from the positive edge on the clock input pin to the response on any logically affected combinational configured output (at the pin), where data origin is any internal SR register or counter bit.

$t_{su(1)}$ — Minimum time interval that must be allowed between the data edge on any dedicated input and the active clock edge on the clock input pin when data affects the S or R line of any output SR register.

$t_{su(2)}$ — Minimum time interval that must be allowed between the data edge on any dedicated input and the active clock edge on the clock input pin when data affects the S or R line of any internal SR register.

$t_{su(3)}$ — Minimum time interval that must be allowed between the data edge on any dedicated input and the active clock edge on the clock input pin only when entering data on the $\overline{CNT}$/HLD0 line.

$t_{su(4)}$ — Minimum time interval that must be allowed between the data edge on any dedicated input and the active clock edge on the clock input pin only when entering data on the SCLR0 line.

$t_{min(1)}$ — Minimum clock period (or 1/[maximum frequency]) that the device will accommodate when using feedback from any internal SR register or counter bit to feed the S or R line of any output SR register.

$t_{min(2)}$ — Minimum clock period (or 1/[maximum frequency]) that the device will accommodate when using feedback from any internal SR register to feed the S or R line of any internal SR register.

$t_{min(3)}$ — Minimum clock period (or 1/[maximum frequency]) that the device will accommodate when using feedback from any internal SR register or counter bit to feed SCLR0 or $\overline{CNT}$/HLD0.

PARAMETER VALUES FOR TIMING MODEL

$t_{pd(1)}$ = 20 ns	$t_{su(1)}$ = 12 ns†	$t_{min(1)}$ = 17 ns
$t_{pd(2)}$ = 10 ns	$t_{su(2)}$ = 12 ns†	$t_{min(2)}$ = 17 ns
$t_{pd(3)}$ = 25 ns	$t_{su(3)}$ = 25 ns	$t_{min(3)}$ = 25 ns
	$t_{su(4)}$ = 20 ns	

INTERNAL NODE NUMBERS

SCLR0	25	CNTHLD0	28	P0-P7	SET 31-38
SCLR1	SET 26	CNTHLD1	SET 29		RESET 39-46
	RESET 27		RESET 30	Q0-Q7	RESET 47-54
		C0-C5	55-60		

† Use t_{su} = 19 ns for applications where the setup time for S/R↓ inputs are required.

NOT RECOMMENDED FOR NEW DESIGNS

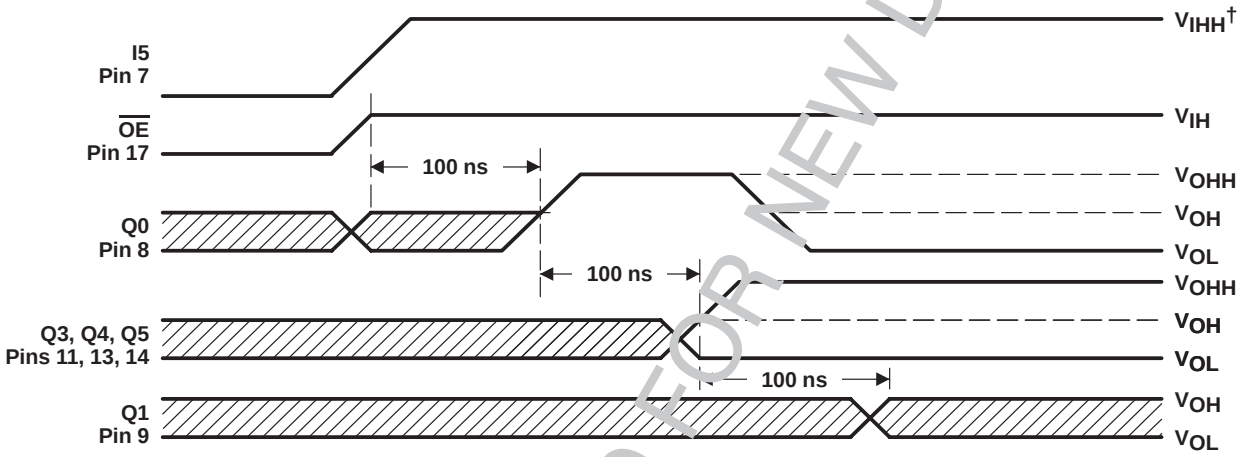
diagnostics

A diagnostic mode is provided that allows the user to inspect the contents of the state registers. The following are step-by-step procedures required for the diagnostics.

Step 1. Disable all outputs by taking pin 17 ($\overline{OE}$) high (see Note 5).
Step 2. Take pin 8 (Q0) to V_{IHH} to enable the diagnostics test sequence.
Step 3. Apply appropriate levels of voltage to pins 11 (Q3), 13 (Q4), and 14 (Q5) to select the desired state register (see Table 1).

The voltage level monitored on pin 9 will indicate the state of the selected state register.

NOTE 5: If pin 17 is being used as an input to the array, then pin 7 (I5) must be taken to V_{IHH} before pin 17 is taken high.



† V_{IHH} = 10.25 V min, 10.5 V nom, 10.75 V max

Figure 2. Diagnostics Waveforms

Table 1. Addressing State Registers During Diagnostics

REGISTER BINARY ADDRESS			BURIED REGISTER
PIN 11	PIN13	PIN 14	SELECTED
L	L	L	SCLR0
L	L	H	SCLR1
L	L	HH	$\overline{CNT}$/HLD0
L	H	L	$\overline{CNT}$/HLD1
L	H	H	P0
L	H	HH	P1
L	HH	L	P2
L	HH	H	P3
L	HH	HH	P4
H	L	L	P5
H	L	H	P6
H	L	HH	P7
H	H	L	C0
H	H	H	C1
H	H	HH	C2
H	HH	L	C3
H	HH	H	C4
H	HH	HH	C5

NOT RECOMMENDED FOR NEW DESIGNS

PRINCIPLES OF OPERATION

PSG design theory

Most state machine and waveform generator designs can be simplified with the PSG by referencing all or part of each sequence to a binary count. The internal state registers can then be used to keep track of which binary count sequence is in operation, to store input data and keep track of internally generated status bits, or as output registers when connected to a nonregistered output cell. State registers can also be used to expand the binary counter when a larger counter is needed.

Through the use of the binary counter, the number of product lines and state registers required for a design is usually reduced. In addition, the designer does not have to be concerned about generating wait states where the outputs are unaffected because these can be timed from the binary counter. For detailed information and examples using this design concept, see *A Designer's Guide to the TIBPSG507* applications report.

OR term loading

As shown in Figure 3 and by the f_{max} calculation, f_{max} is affected by the number of terms connected to each OR array line. Theoretically, f_{max} is calculated as:

$$f_{max} = \frac{1}{t_{su} + t_{pd}\ \text{CLK to Q}}$$

Since the setup time (input or feedback to S/R↓) varies with the number of terms connected to each OR array line, (due to capacitance loading) f_{max} will also vary. Figure 3 illustrates the relationship between the number of terms connected per OR line and the setup time.

Use Figure 3 to determine the worst-case setup time for a particular application. Identify the OR array line with the maximum number of terms connected. Count the number of terms and use the graph to determine the setup time.

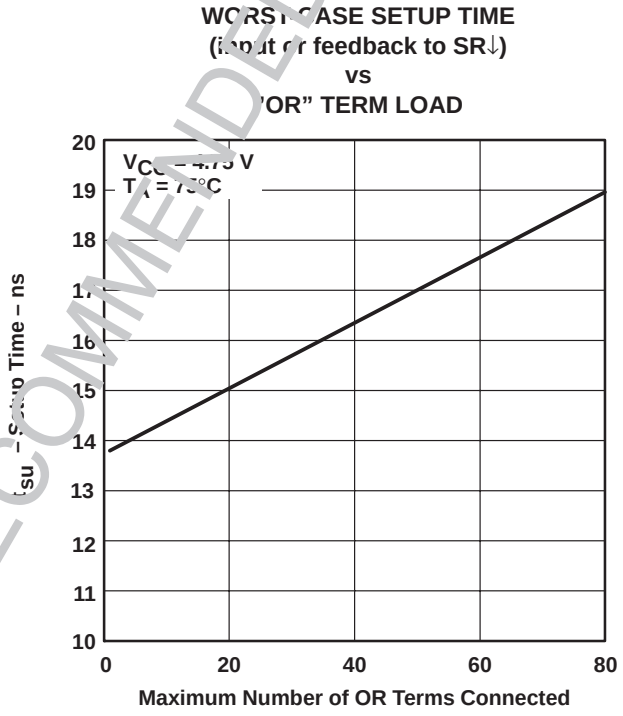


Figure 3

NOT RECOMMENDED FOR NEW DESIGNS

f_{max} with external feedback

The configuration shown is a typical state-machine design with feedback signals sent off-chip. This external feedback could go back to the device inputs or to a second device in a multi-chip state machine. The slowest path defining the clock period is the sum of the clock-to-output delay time and the setup time for the input or feedback signals (t_{su} + t_{pd} CLK to Q).

Thus: f_{max} with external feedback = $\dfrac{1}{t_{su} + t_{pd}\ \text{CLK to Q}}$

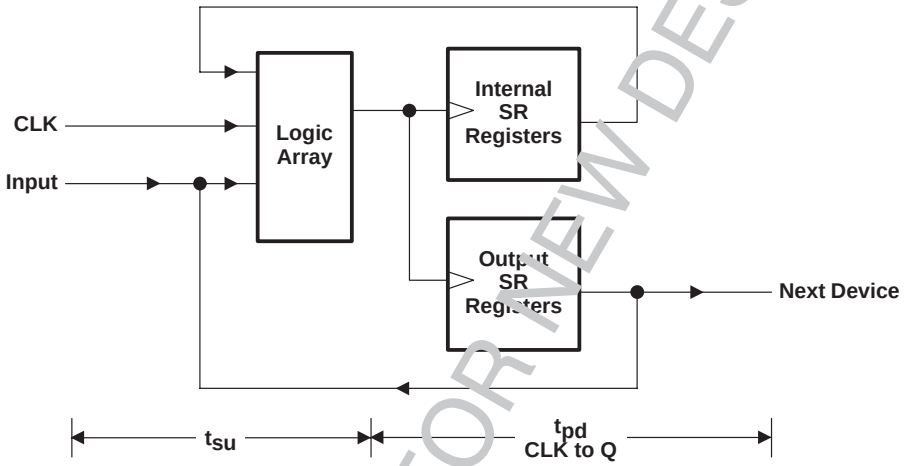
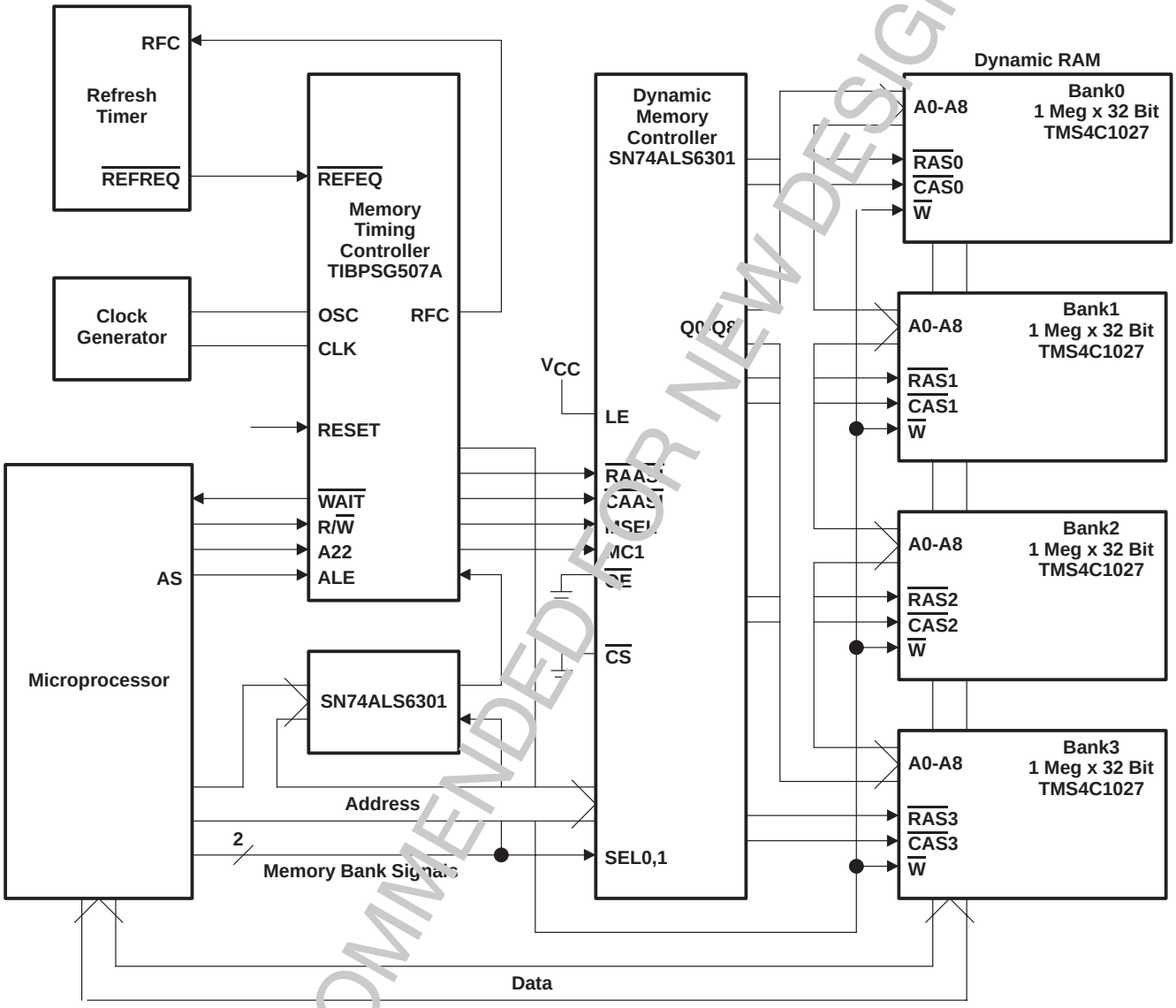


Figure 4

NOT RECOMMENDED FOR NEW DESIGNS

APPLICATION INFORMATION

The TIBPSG507AC is used in this application to generate the required memory timing control signals ($\overline{RAS}$, $\overline{CAS}$, etc.) for the memory timing controller.

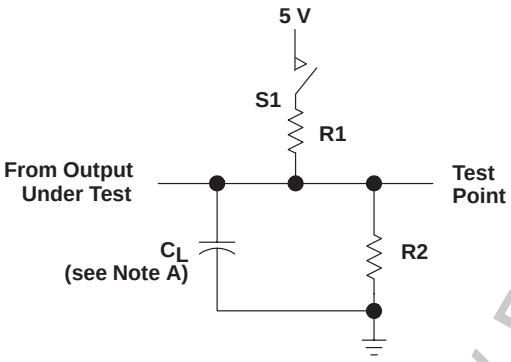


For detailed information, please see the *Systems Solution for Static Column Decode* Application Report.

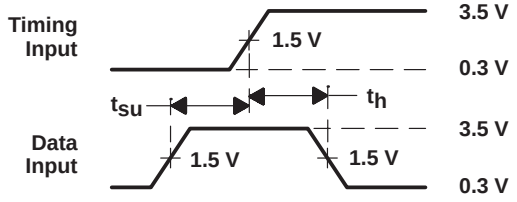
Figure 5

NOT RECOMMENDED FOR NEW DESIGNS

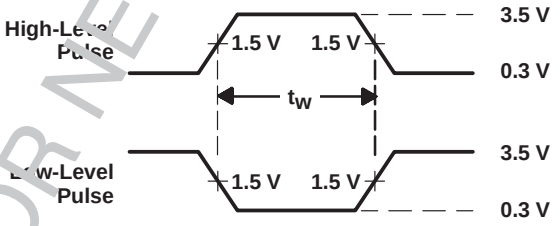
PARAMETER MEASUREMENT INFORMATION



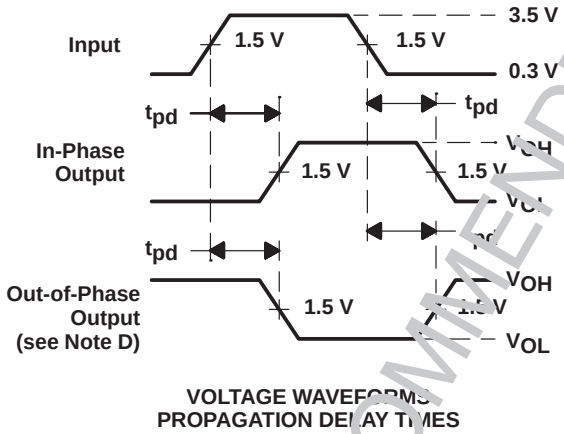
LOAD CIRCUIT FOR 3-STATE OUTPUTS



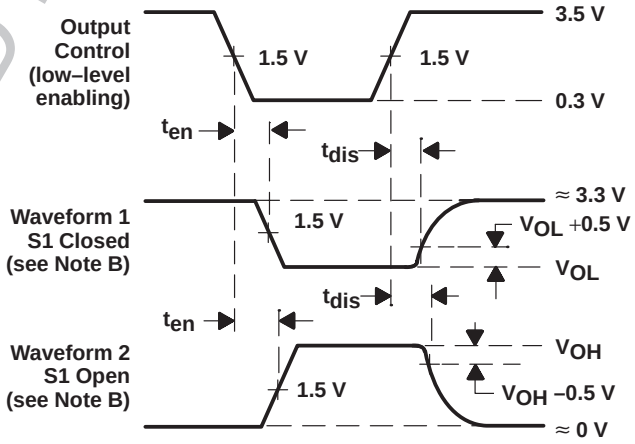
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATIONS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f \leq 2$ ns, duty cycle = 50%.
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.
E. Equivalent loads may be used for testing.

Figure 6. Load Circuit and Voltage Waveforms

NOT RECOMMENDED FOR NEW DESIGNS

TYPICAL CHARACTERISTICS

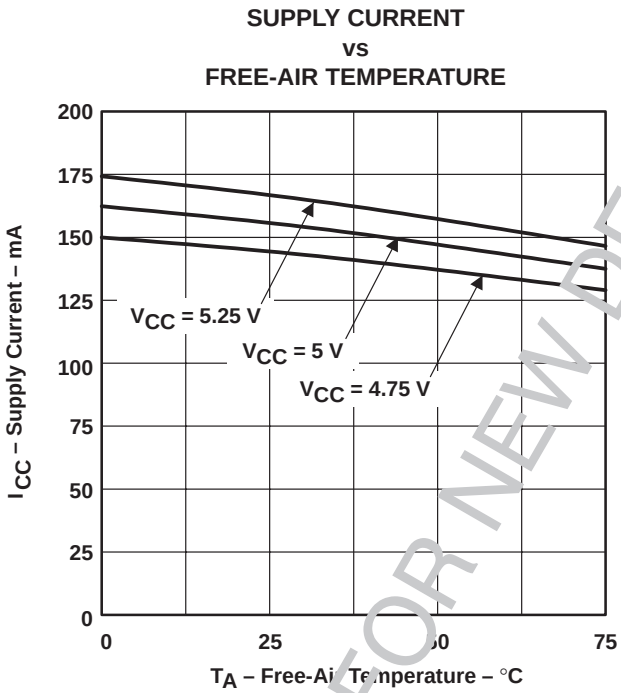


Figure 7

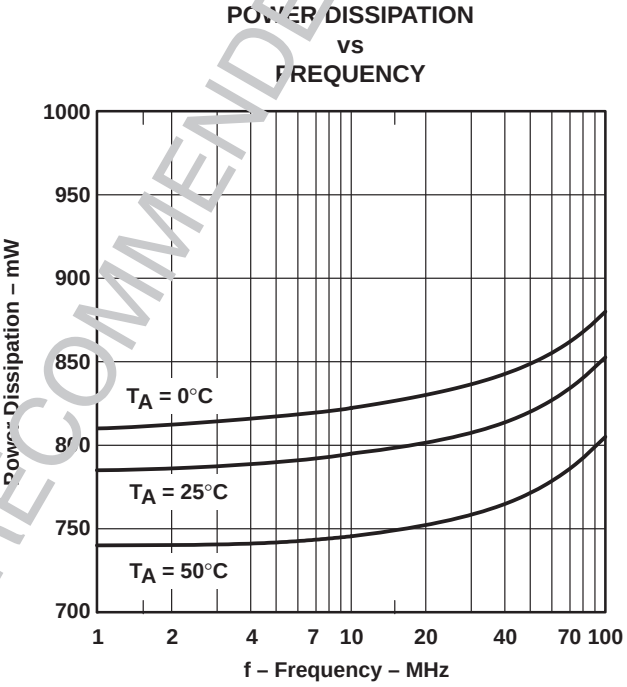


Figure 8

NOT RECOMMENDED FOR NEW DESIGNS

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME vs SUPPLY VOLTAGE

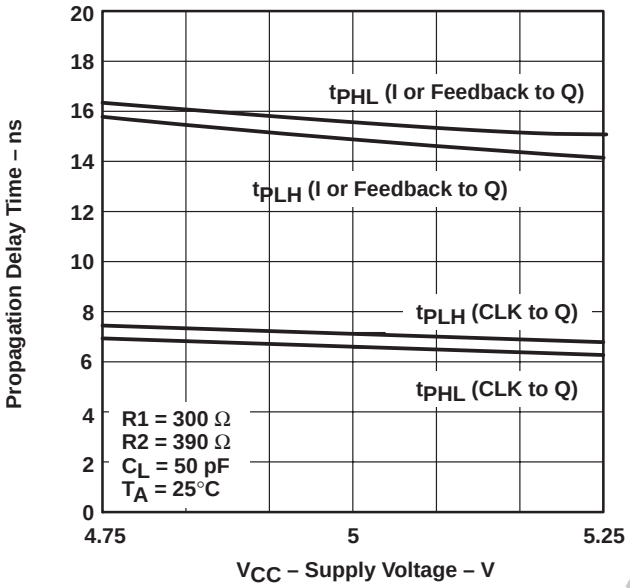


Figure 9

PROPAGATION DELAY TIME vs LOAD CAPACITANCE

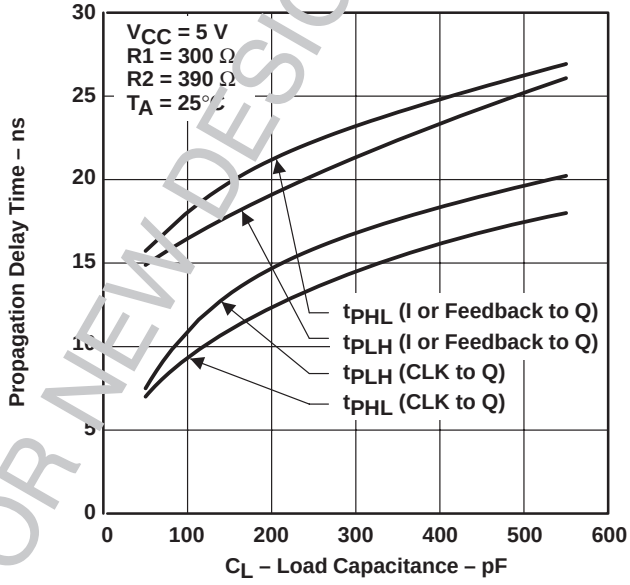


Figure 10

PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE

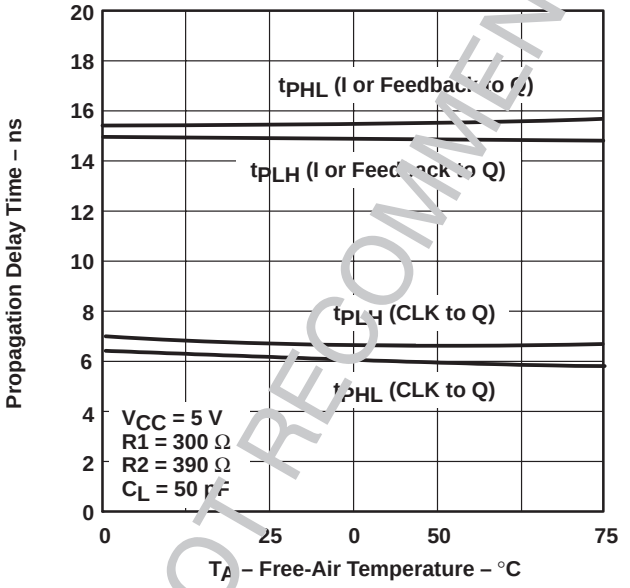


Figure 11

PROPAGATION DELAY TIME vs NUMBER OF OUTPUTS SWITCHING

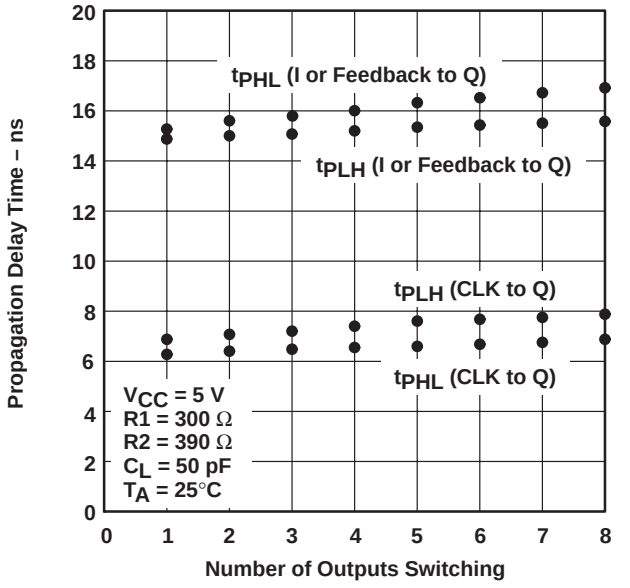


Figure 12

NOT RECOMMENDED FOR NEW DESIGNS

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