700 MHz to 2700 MHz Quadrature Modulator

Data Sheet

AD8349

FEATURES

Output frequency range: 700 MHz to 2700 MHz
Modulation bandwidth: dc to 160 MHz (large signal BW)
1 dB output compression: 5.6 dBm @ 2140 MHz
Output disable function: output below −50 dBm in < 50 ns
Noise floor: −156 dBm/Hz
Phase quadrature error: 0.3 degrees @ 2140 MHz
Amplitude balance: 0.1 dB
Single supply: 4.75 V to 5.5 V
Pin compatible with AD8345/AD8346s
16-lead, exposed-paddle TSSOP package

APPLICATIONS

Cellular/PCS communication systems infrastructure
WCDMA/CDMA2000/PCS/GSM/EDGE
Wireless LAN/wireless local loop
LMDS/broadband wireless access systems

FUNCTIONAL BLOCK DIAGRAM

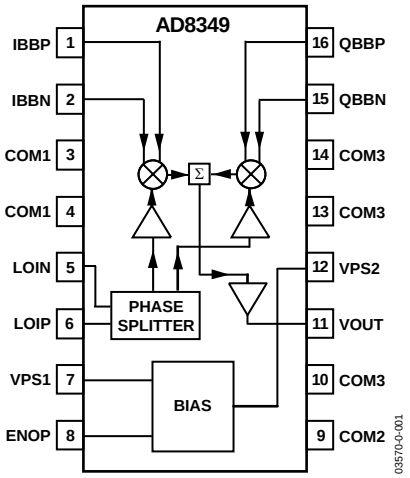


Figure 1.

PRODUCT DESCRIPTION

The AD8349 is a silicon, monolithic, RF quadrature modulator that is designed for use from 700 MHz to 2700 MHz. Its excellent phase accuracy and amplitude balance enable high performance direct RF modulation for communication systems.

The differential LO input signal is buffered, and then split into an in-phase (I) signal and a quadrature-phase (Q) signal using a polyphase phase splitter. These two LO signals are further buffered and then mixed with the corresponding I channel and Q channel baseband signals in two Gilbert cell mixers. The mixers' outputs are then summed together in the output amplifier. The output amplifier is designed to drive 50 Ω loads.

The RF output can be switched on and off within 50 ns by applying a control pulse to the ENOP pin.

The AD8349 can be used as a direct-to-RF modulator in digital communication systems such as GSM, CDMA, and WCDMA base stations, and QPSK or QAM broadband wireless access transmitters. Its high dynamic range and high modulation accuracy also make it a perfect IF modulator in local multipoint distribution systems (LMDS) using complex modulation formats.

The AD8349 is fabricated using Analog Devices' advanced complementary silicon bipolar process, and is available in a 16-lead, exposed-paddle TSSOP package. Its performance is specified over a −40°C to +85°C temperature range.

Rev. B
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TABLE OF CONTENTS

Features ... 1
Applications ... 1
Functional Block Diagram ... 1
Product Description ... 1
Revision History ... 2
Specifications ... 3
Absolute Maximum Ratings ... 5
ESD Caution ... 5
Pin Configuration and Function Descriptions ... 6
Equivalent Circuits ... 7
Typical Performance Characteristics ... 8
Circuit Description ... 14
Overview ... 14
LO Interface ... 14
V-to-I Converter ... 14
Mixers ... 14
D-to-S Amplifier ... 14
Bias Circuit ... 14
Output Enable ... 14
Basic Connections ... 15
Baseband I and Q Inputs ... 15
Single-Ended Baseband Drive ... 15
LO Input Drive Level ... 16
Frequency Range ... 16
LO Input Impedance Matching ... 16
Single-Ended LO Drive ... 17
RF Output ... 17
Output Enable ... 17
Baseband DAC Interface ... 18
AD9777 Interface ... 18
Biasing and Filtering ... 18
Reducing Undesired Sideband Leakage ... 19
Reduction of LO Feedthrough ... 19
Sideband Suppression and LO Feedthrough vs. Temperature ... 20
Single Sideband Performance vs. Baseband Drive Level ... 20
Improving Third Harmonic Distortion ... 20
Applications ... 21
3GPP WCDMA Single-Carrier Application ... 21
WCDMA MultiCarrier Application ... 21
GSM/EDGE Application ... 22
Soldering Information ... 23
LO Generation Using PLLs ... 23
Transmit DAC Options ... 23
Evaluation Board ... 24
Characterization Setups ... 26
SSB Setup ... 26
Outline Dimensions ... 27
Ordering Guide ... 27

REVISION HISTORY

2/12—Rev. A to Rev. B

Added EPAD Note ... 6
Changes to Ordering Guide ... 27

11/04—Data Sheet Changed from Rev. 0 to Rev. A

Changes to Figure 25 through Figure 30 ... 11
Changes to Figure 37 through Figure 39 ... 13
Change to WCDMA MultiCarrier Application section ... 21
Change to Figure 60 and Figure 61 ... 21

11/03—Revision 0: Initial Version

SPECIFICATIONS

V_S = 5 V; ambient temperature (T_A) = 25°C; LO = −6 dBm; I/Q inputs = 1.2 V p-p differential sine waves in quadrature on a 400 mV dc bias; baseband frequency = 1 MHz; LO source and RF output load impedances are 50 Ω, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
Operating Frequency		700		2700	MHz
LO = 900 MHz					
Output Power		1.5	4	6	dBm
Output P1 dB			7.6		dBm
Carrier Feedthrough			−45	−30	dBm
Sideband Suppression			−35	−31	dBc
Third Harmonic[1]	$P_{OUT} - (F_{LO} + (3 \times F_{BB}))$, P_{OUT} = 4 dBm		−39	−36	dBc
Output IP3	$F1_{BB}$ = 3 MHz, $F2_{BB}$ = 4 MHz, P_{OUT} = -4.2 dBm		21		dBm
Quadrature Error			1.9		degree
I/Q Amplitude Balance			0.1		dB
Noise Floor	20 MHz offset from LO, all BB inputs 400 mV dc bias only		−155		dBm/Hz
	20 MHz offset from LO, BB inputs = 1.2 V p-p differential on 400 mV dc		−150		dBm/Hz
GSM Sideband Noise	LO = 884.8 MHz, 6 MHz offset from LO, P_{OUT} = 2 dBm		−152		dBc/Hz
LO = 1900 MHz					
Output Power		0	3.8	6	dBm
Output P1dB			6.8		dBm
Carrier Feedthrough			−38		dBm
Sideband Suppression			−40	−36	dBc
Third Harmonic[1]	$P_{OUT} - (F_{LO} + (3 \times F_{BB}))$, P_{OUT} = 3.8 dBm		−37	−36	dBc
Output IP3	$F1_{BB}$ = 3 MHz, $F2_{BB}$ = 4 MHz, P_{OUT} = −4.5 dBm		22		dBm
Quadrature Error			0.7		degree
I/Q Amplitude Balance			0.1		dB
Noise Floor	20 MHz offset from LO, all BB inputs 400 mV dc bias only		−156		dBm/Hz
	20 MHz offset from LO, BB inputs = 1.2 V p-p differential on 400 mV dc		−150		dBm/Hz
GSM Sideband Noise	LO = 1960 MHz, 6 MHz offset from LO, P_{OUT} = 2 dBm		−151		dBc/Hz
LO = 2140 MHz					
Output Power		−2	2.4	5.1	dBm
Output P1dB			5.6		dBm
Carrier Feedthrough			−42	−30	dBm
Sideband Suppression			−43	−36	dBc
Third Harmonic[1]	$P_{OUT} - (F_{LO} + (3 \times F_{BB}))$, P_{OUT} = 2.4 dBm		−37	−36	dBc
Output IP3	$F1_{BB}$ = 3 MHz, $F2_{BB}$ = 4 MHz, P_{OUT} = −6.5 dBm		19		dBm
Quadrature Error			0.3		degree
I/Q Amplitude Balance			0.1		dB
Noise Floor	20 MHz offset from LO, all BB inputs 400 mV dc bias only		−156		dBm/Hz
	20 MHz offset from LO, BB inputs = 1.2 V p-p differential on 400 mV dc		−151		dBm/Hz
WCDMA Noise Floor	LO = 2140 MHz. 30 MHz offset from LO, P_{CHAN} = −17.3 dBm		−156		dBm/Hz
LO INPUTS	Pins LOIP and LOIN				
LO Drive Level	Characterization performed at typical level	−10	−6	0	dBm
Nominal Impedance			50		Ω
Input Return Loss	Drive via 1:1 balun, LO = 2140 MHz		−8.6		dB
BASEBAND INPUTS	Pins IBBP, IBBN, QBBP, QBBN				
I and Q Input Bias Level			400		mV
Input Bias Current			11		µA
Input Offset Current			1.8		µA
Bandwidth (0.1 dB)	LO = 1500 MHz, baseband input = 600 mV p-p sine wave on 400 mV dc		10		MHz
	LO = 1500 MHz, baseband input = 60 mV p-p sine wave on 400 mV dc		24		MHz

Parameter	Conditions	Min	Typ	Max	Unit
Bandwidth (3 dB)	LO = 1500 MHz, baseband input = 600 mV p-p sine wave on 400 mV dc		160		MHz
	LO = 1500 MHz, baseband input = 60 mV p-p sine wave on 400 mV dc		340		MHz
OUTPUT ENABLE	Pin ENOP				
Off Isolation	ENOP Low		−78	−50	dBm
Turn-On Settling Time	ENOP Low to High (90% of envelope)		20		ns
Turn-Off Settling Time	ENOP High to Low (10% of envelope)		50		ns
ENOP High Level (Logic 1)		2.0			V
ENOP Low Level (Logic 0)				0.8	V
POWER SUPPLIES	Pins VPS1 and VPS2				
Voltage		4.75		5.5	V
Supply Current	ENOP = High		135	150	mA
	ENOP = Low		130	145	mA

[1] The amplitude of the third harmonic relative to the single sideband power decreases with decreasing baseband drive level (see Figure 19, Figure 20, and Figure 21).

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage VPOS	5.5 V
IBBP, IBBN, QBBP, QBBN	0 V, 2.5 V
LOIP and LOIN	10 dBm
Internal Power Dissipation	800 mW
θ_{JA} (Exposed Paddle Soldered Down)	30°C/W
Maximum Junction Temperature	125°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

tresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

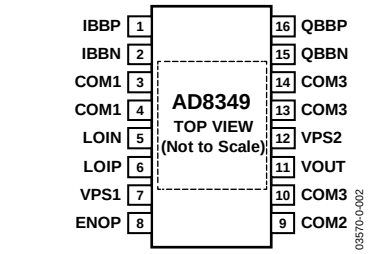


Figure 2.

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description	Equivalent Circuit
1, 2, 15, 16	IBBP, IBBN, QBBN, QBBP	Differential In-Phase and Quadrature Baseband Inputs. These high impedance inputs must be dc-biased to approximately 400 mV dc, and must be driven from a low impedance source. Nominal characterized ac signal swing is 600 mV p-p on each pin (100 mV to 700 mV). This results in a differential drive of 1.2 V p-p with a 400 mV dc bias. These inputs are not self-biased and must be externally biased.	Circuit A
3, 4	COM1	Common Pin for LO Phase Splitter and LO Buffers. COM1, COM2, and COM3 should all be connected to a ground plane via a low impedance path.	
5, 6	LOIN, LOIP	Differential Local Oscillator Inputs. Internally dc-biased to approximately 1.8 V when V_S = 5.0 V. Pins must be ac-coupled. Single-ended drive is possible with degradation in performance.	Circuit B
7	VPS1	Positive Supply Voltage (4.75 V to 5.5 V) for the LO Bias-Cell and Buffer. VPS1 and VPS2 should be connected to the same supply. To ensure adequate external bypassing, connect 0.1 µF and 100 pF capacitors between VPS1 and ground.	
8	ENOP	Output Enable. This pin can be used to enable or disable the RF output. Connect to high logic level for normal operation. Connect to low logic level to disable output.	Circuit C
9	COM2	Common Pin for the Output Amplifier. COM1, COM2, and COM3 should all be connected to a ground plane via a low impedance path.	
10, 13, 14	COM3	Common Pin for Input V-to-I Converters and Mixer Cores. COM1, COM2, and COM3 should all be connected to a ground plane via a low impedance path.	
11	VOUT	Device Output. Single-ended, 50 Ω internally biased RF output. Pin must be ac-coupled to the load.	Circuit D
12	VPS2	Positive Supply Voltage (4.75 V to 5.5 V) for the Baseband Input V-to-I Converters, Mixer Core, Band Gap Reference, and Output Amplifer. VPS1 and VPS2 should be connected to the same supply. To ensure adequate external bypassing, connect 0.1 µF and 100 pF capacitors between VPS2 and ground.	
	EP	Exposed Paddle. Connect to the ground plane via a low impedance path.	

EQUIVALENT CIRCUITS

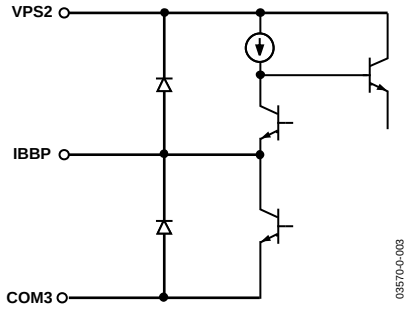


Figure 3. Circuit A

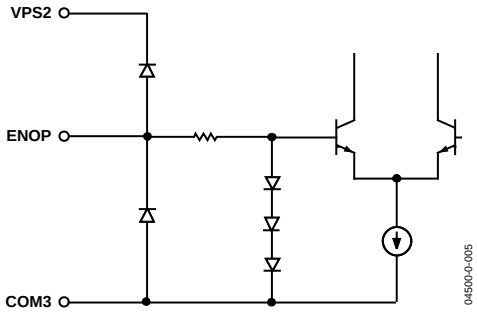


Figure 5. Circuit C

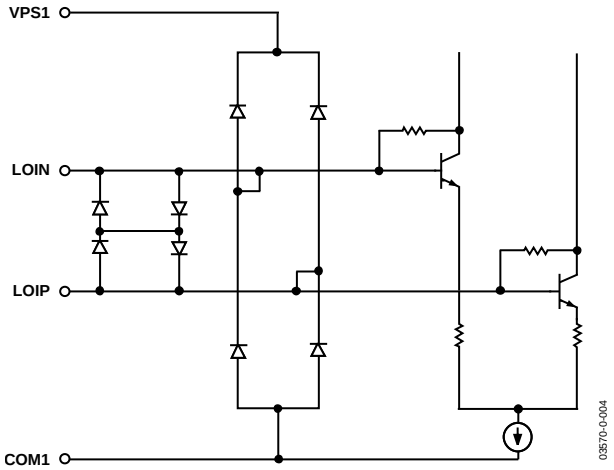


Figure 4. Circuit B

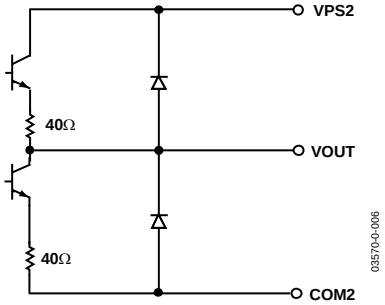


Figure 6. Circuit D

TYPICAL PERFORMANCE CHARACTERISTICS

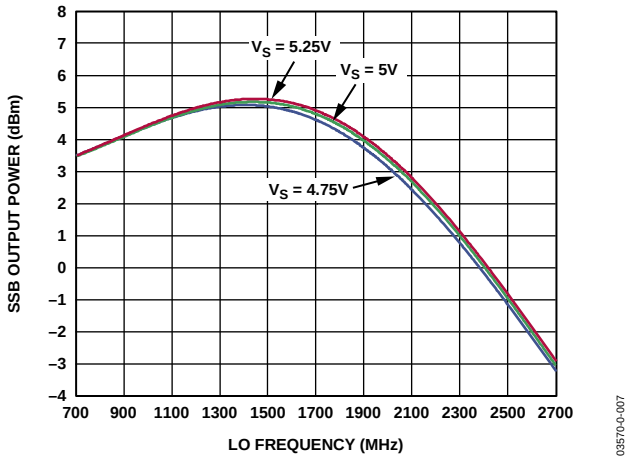


Figure 7. Single Sideband (SSB) Output Power (P_{OUT}) vs. LO Frequency (F_{LO}) (I and Q Inputs Driven in Quadrature at Baseband Frequency (F_{BB}) = 1 MHz, I and Q Inputs at 1.2 V p-p Differential, T_A = 25°C)

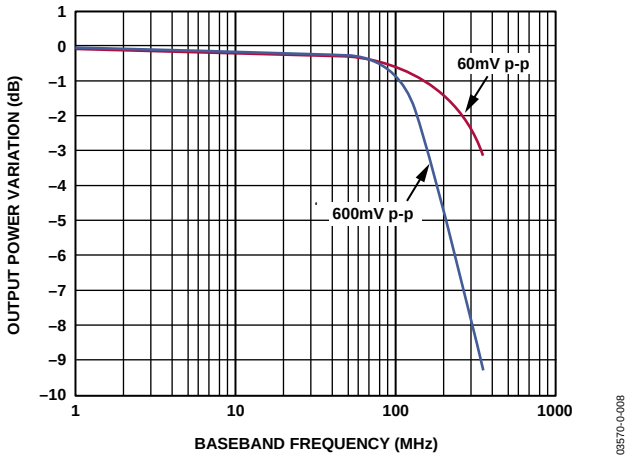


Figure 8. I and Q Input Bandwidth Normalized to Gain @ 1 MHz (F_{LO} = 1500 MHz, T_A = 25°C)

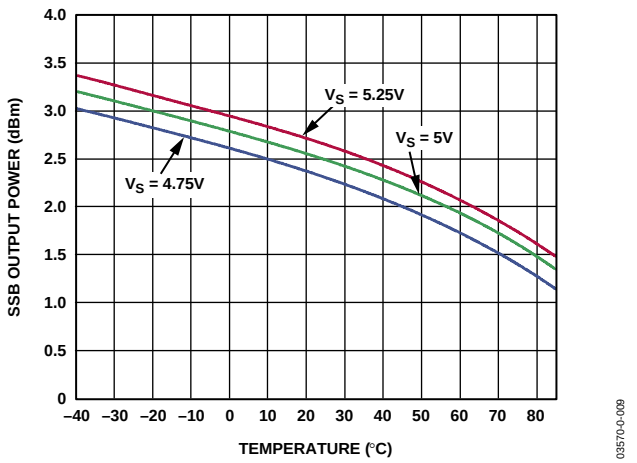


Figure 9. SSB P_{OUT} vs. Temperature (F_{LO} = 2140 MHz, F_{BB} = 1 MHz, I and Q Inputs Driven in Quadrature at 1.2 V p-p Differential)

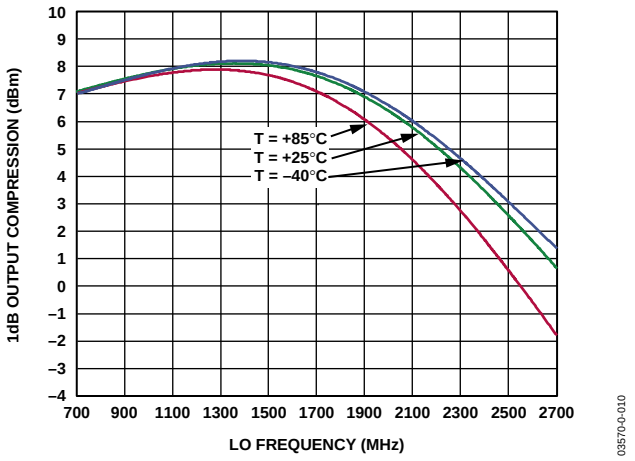


Figure 10. SSB Output 1 dB Compression Point (OP1dB) vs. F_{LO} (F_{BB} = 1 MHz, I and Q Inputs Driven in Quadrature , T_A = 25°C)

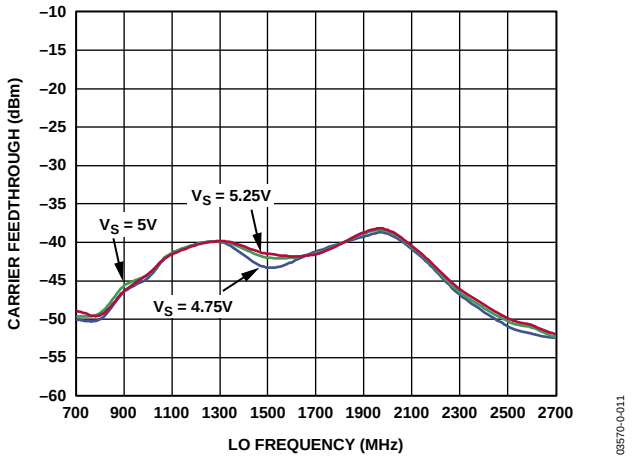


Figure 11. Carrier Feedthrough vs. F_{LO} (F_{BB} = 1 MHz, I and Q Inputs Driven in Quadrature at 1.2 V p-p Differential, T_A = 25°C)

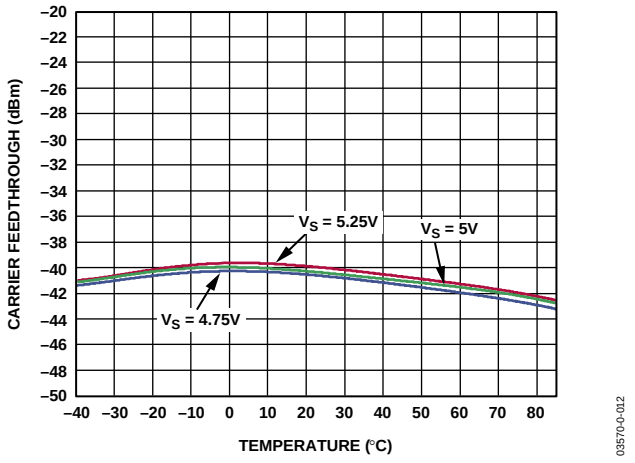


Figure 12. Carrier Feedthrough vs. Temperature (F_{LO} = 2140 MHz, F_{BB} = 1 MHz, I and Q Inputs Driven in Quadrature at 1.2 V p-p Differential, T_A = 25°C)

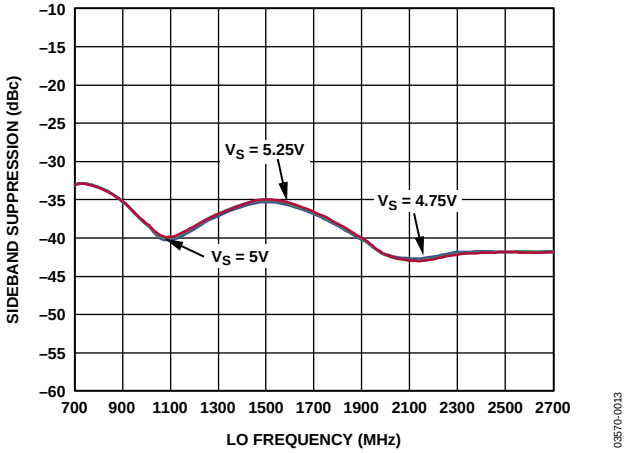


Figure 13. Sideband Suppression vs. F_{LO} (F_{BB} = 1 MHz, I and Q Inputs Driven in Quadrature at 1.2 V p-p Differential, T_A = 25°C)

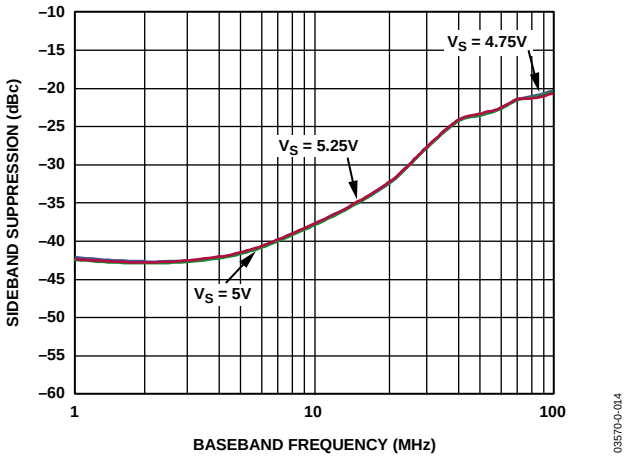


Figure 14. Sideband Suppression vs. F_{BB} (F_{LO} = 2140 MHz, I and Q Inputs Driven in Quadrature at 1.2 V p-p Differential, T_A = 25°C)

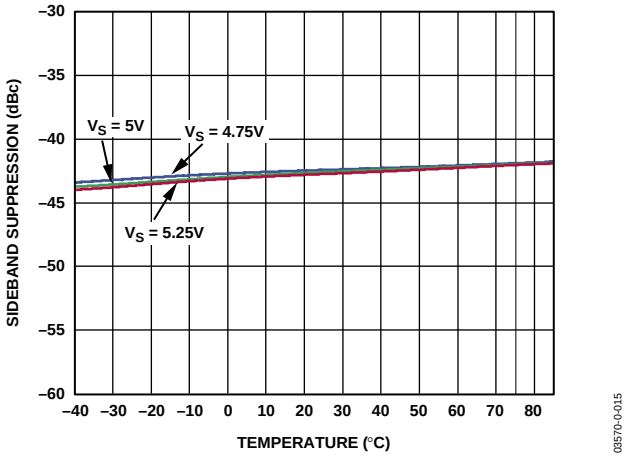


Figure 15. Sideband Suppression vs. Temperature (F_{LO} = 2140 MHz, F_{BB} = 1 MHz, I and Q Inputs Driven in Quadrature at 1.2 V p-p Differential)

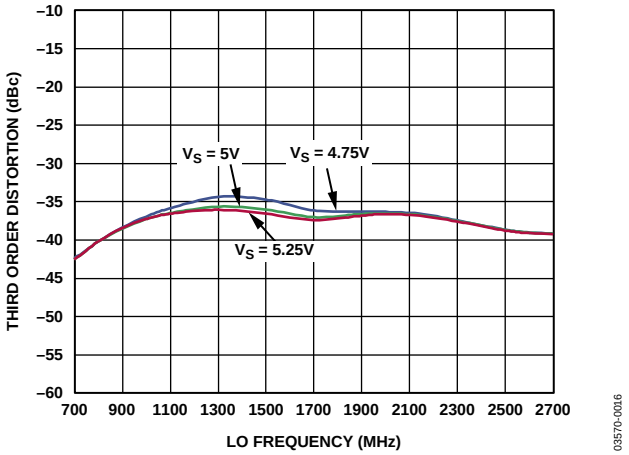


Figure 16. Third Order Distortion vs. F_{LO} (F_{BB} = 1 MHz, I and Q Inputs Driven in Quadrature at 1.2 V p-p Differential, T_A = 25°C)

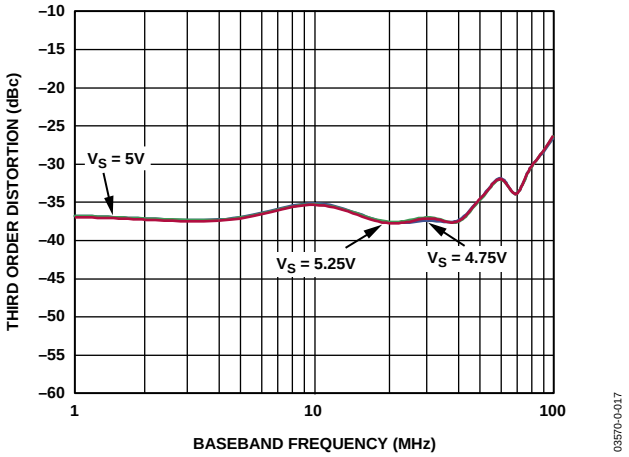


Figure 17. Third Order Distortion vs. F_{BB} (F_{LO} = 2140 MHz, I and Q Inputs Driven in Quadrature at 1.2 V p-p Differential, T_A = 25°C)

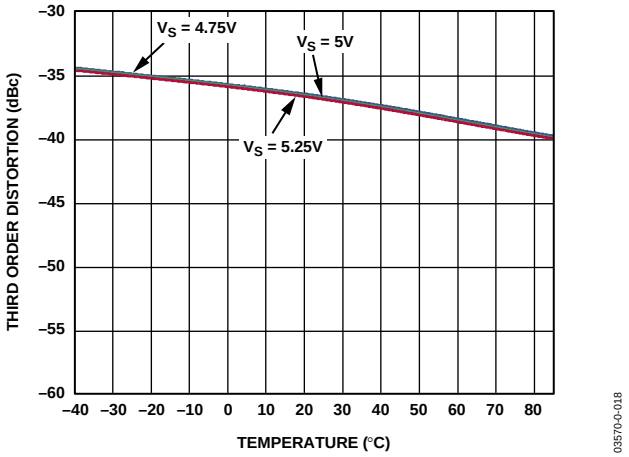


Figure 18. Third Order Distortion vs. Temperature (F_{LO} = 2140 MHz, F_{BB} = 1 MHz, I and Q Inputs Driven in Quadrature at 1.2 V p-p Differential)

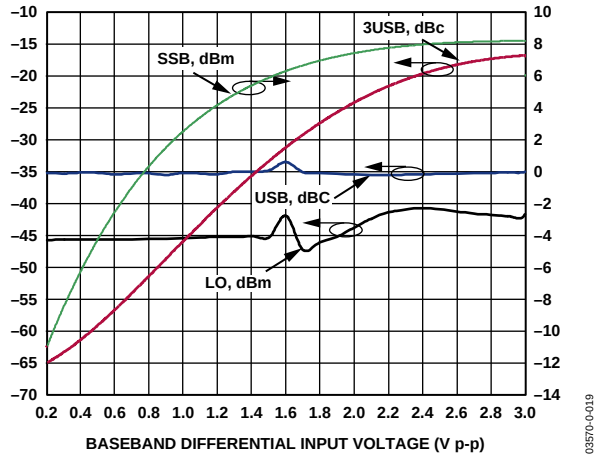


Figure 19. Third Order Distortion (3USB), Carrier Feedthrough, Sideband Suppression, and SSB P_{OUT} vs. Baseband Differential Input Level (F_{LO} = 900 MHz, F_{BB} = 1 MHz, I and Q Inputs Driven in Quadrature, T_A = 25°C)

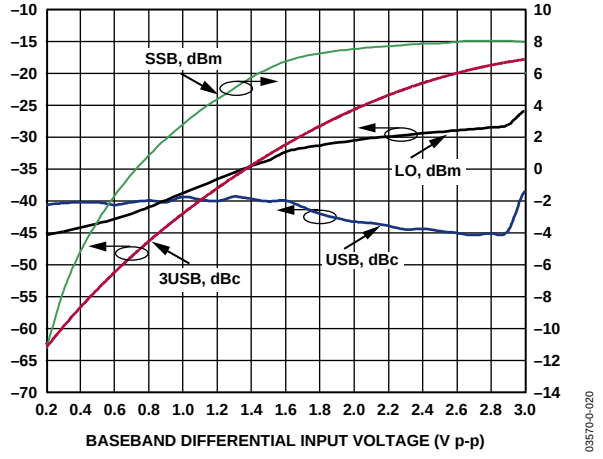


Figure 20. Third Order Distortion (3USB), Carrier Feedthrough, Sideband Suppression, and SSB P_{OUT} vs. Baseband Differential Input Level (F_{LO} = 1900 MHz, F_{BB} = 1 MHz, I and Q Inputs Driven in Quadrature, T_A = 25°C)

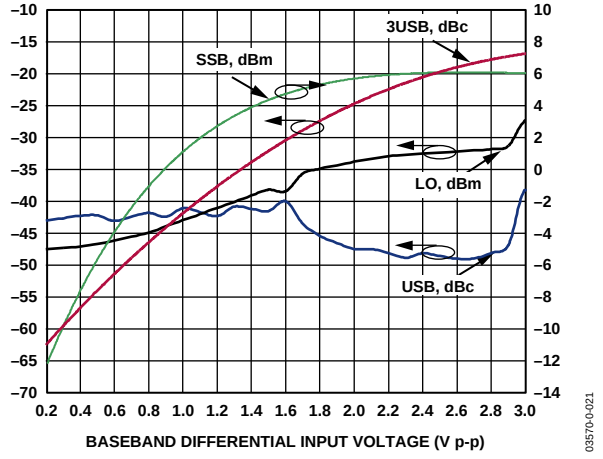


Figure 21. Third Order Distortion (3USB), Carrier Feedthrough, Sideband Suppression, and SSB P_{OUT} vs. Baseband Differential Input Level (F_{LO} = 2140 MHz, F_{BB} = 1 MHz, I and Q Inputs Driven in Quadrature, T_A = 25°C)

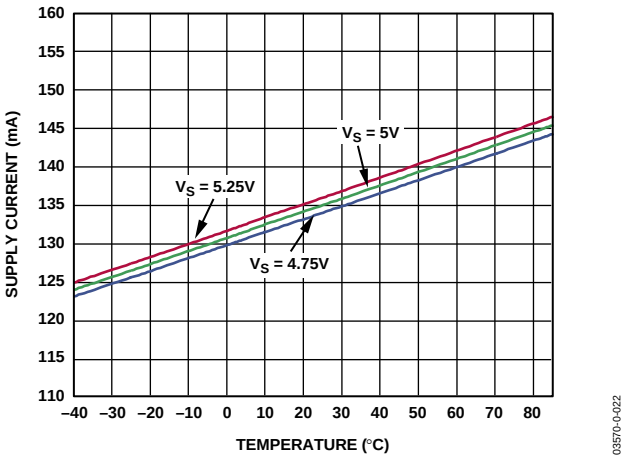


Figure 22. Power Supply Current vs. Temperature

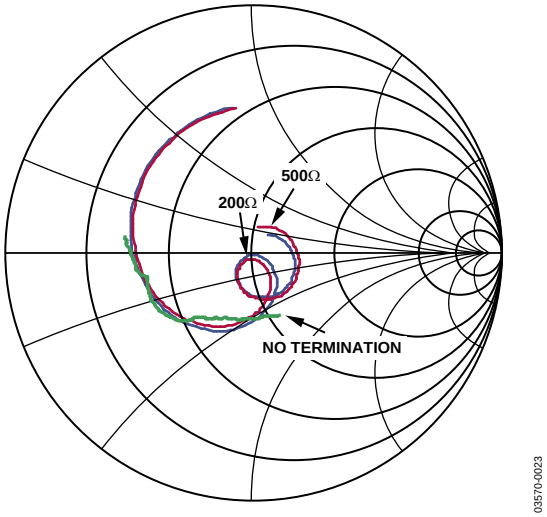


Figure 23. Smith Chart of LOIP Port S_{11} (LOIN Pin AC-Coupled to Ground). Curves with Balun and External Termination Resistors Also Shown (T_A = 25°C)

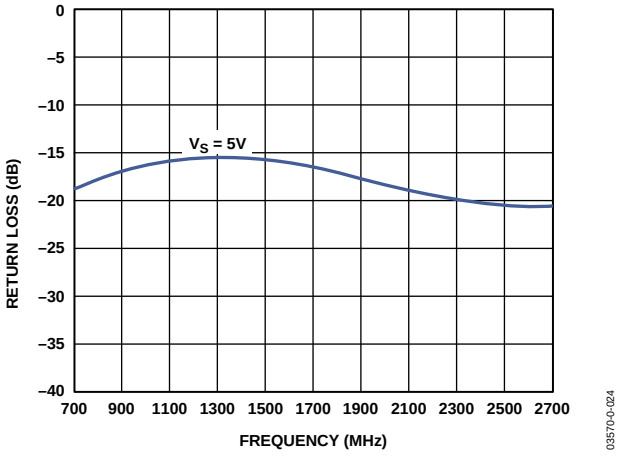


Figure 24. Return Loss $|S_{22}|$ of V_{OUT} Output (T_A = 25°C)

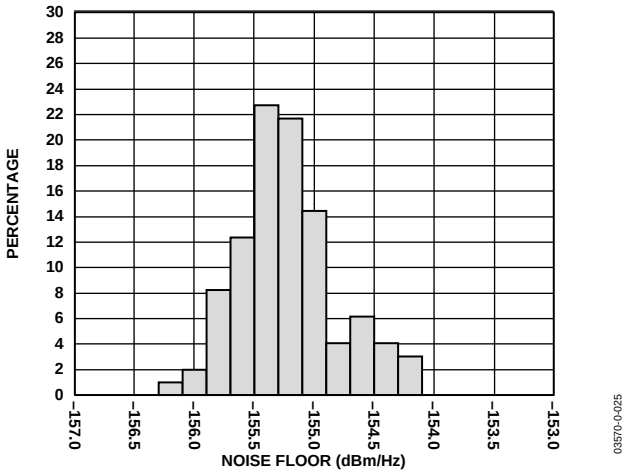


Figure 25. 20 MHz Offset Noise Floor Distribution at F_{LO} = 900 MHz (BB Inputs at a Bias of 400 mV with no AC signal, T_A = 25°C)

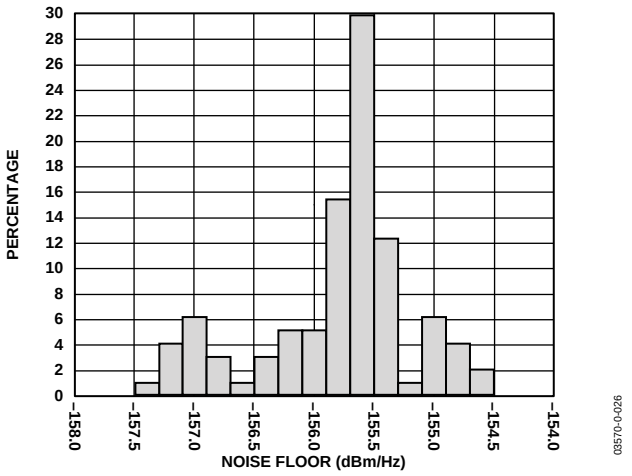


Figure 26. 20 MHz Offset Noise Floor Distribution at F_{LO} = 1900 MHz (BB Inputs at a Bias of 400 mV with no AC signal, T_A = 25°C)

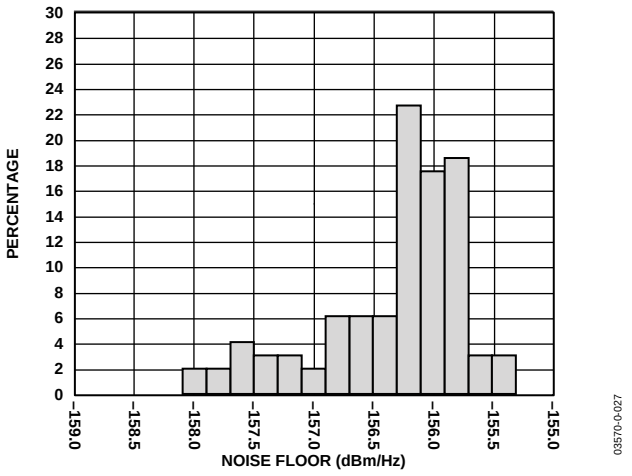


Figure 27. 20 MHz Offset Noise Floor Distribution at F_{LO} = 2140 MHz (BB Inputs at a Bias of 400 mV with no AC signal, T_A = 25°C)

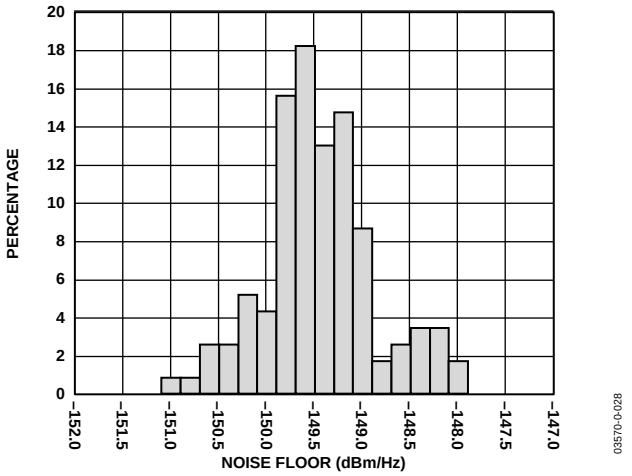


Figure 28. 20 MHz Offset Noise Floor Distribution at F_{LO} = 940 MHz (F_{BB} = 1 MHz, I and Q Inputs Driven in Quadrature at 1.2 V p-p, T_A = 25°C)

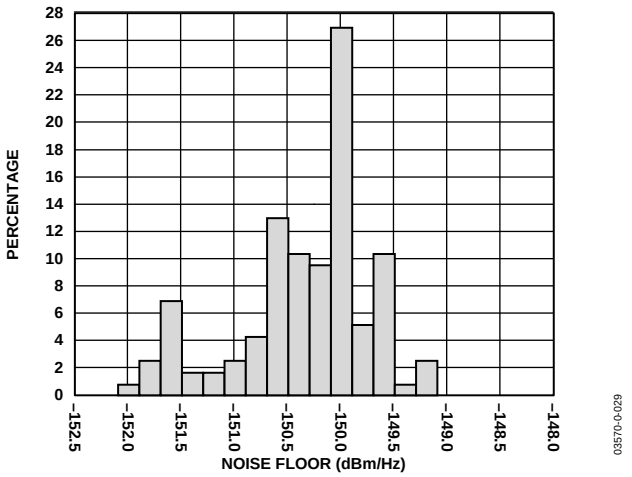


Figure 29. 20 MHz Offset Noise Floor Distribution at F_{LO} = 1960 MHz (F_{BB} = 1 MHz, I and Q Inputs Driven in Quadrature at 1.2 V p-p, T_A = 25°C)

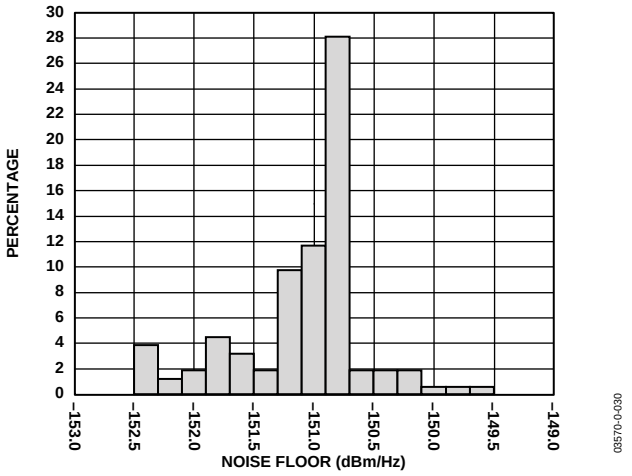


Figure 30. 20 MHz Offset Noise Floor Distribution at F_{LO} = 2140 MHz (F_{BB} = 1 MHz, I and Q Inputs Driven in Quadrature at 1.2 V p-p, T_A = 25°C)

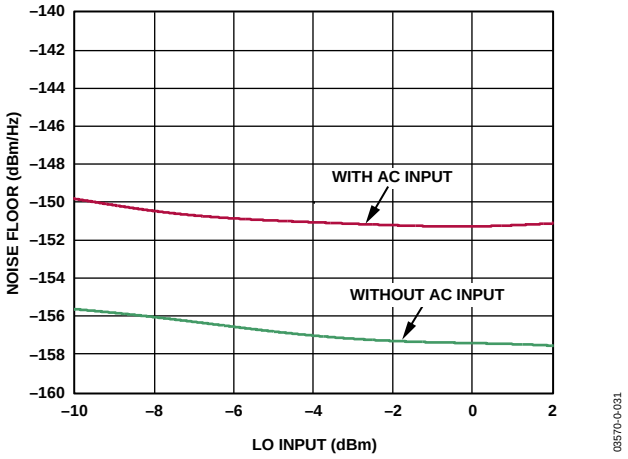


Figure 31. 20 MHz Offset Noise Floor vs. LO Input Power (F_{LO} = 2140 MHz, T_A = 25°C)

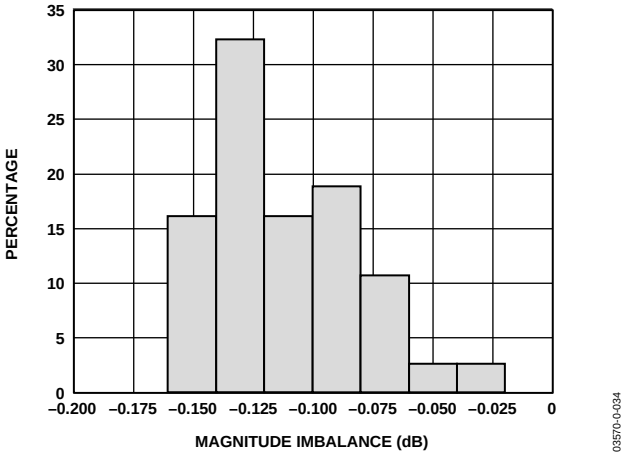


Figure 34. I and Q Inputs Quadrature Phase Imbalance Distribution (F_{LO} = 2140 MHz, F_{BB} = 1 MHz, I and Q Inputs Driven in Quadrature at 1.2 V p-p Differential, T_A = 25°C)

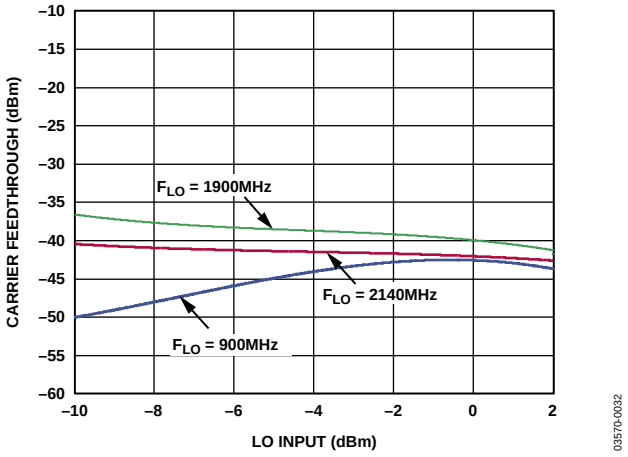


Figure 32. Carrier Feedthrough vs. LO Input Power (F_{BB} = 1 MHz, I and Q Inputs Driven in Quadrature at 1.2 V p-p Differential, T_A = 25°C)

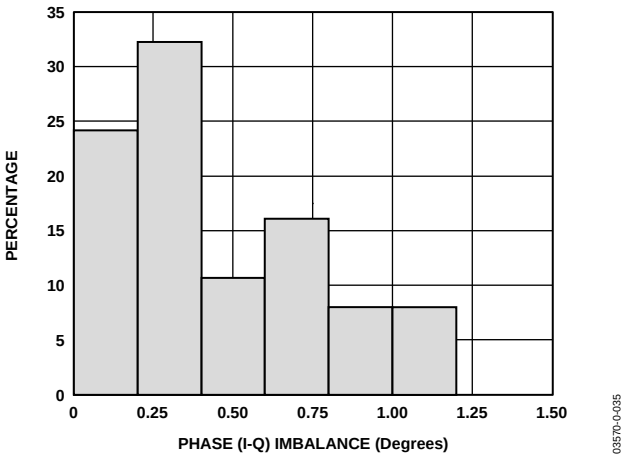


Figure 35. I and Q Inputs Amplitude Imbalance Distribution (F_{LO} = 2140 MHz, F_{BB} = 1 MHz, I and Q Inputs Driven in Quadrature at 1.2 V p-p Differential, T_A = 25°C)

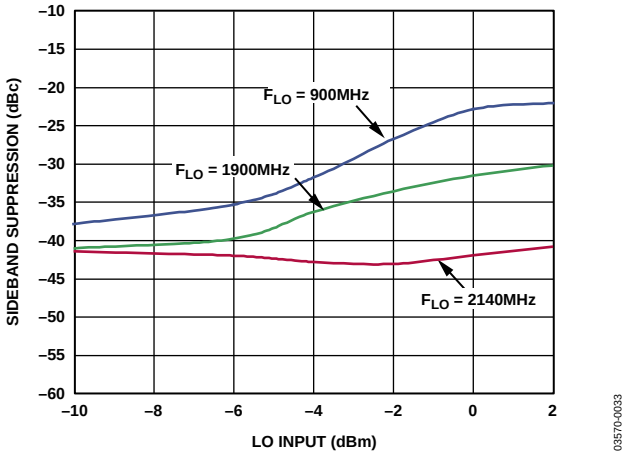


Figure 33. Sideband Suppression vs. LO Input Power (F_{BB} = 1 MHz, I and Q Inputs Driven in Quadrature at 1.2 V p-p Differential, T_A = 25°C)

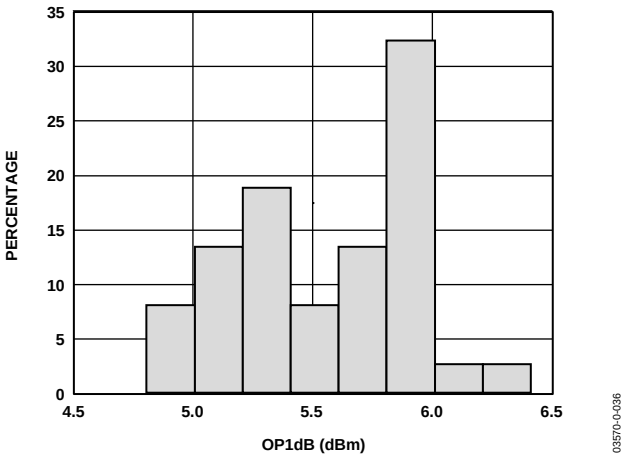


Figure 36. OP1dB Distribution. (F_{LO} = 2140 MHz, F_{BB} = 1 MHz, I and Q Inputs Driven in Quadrature, T_A = 25°C)

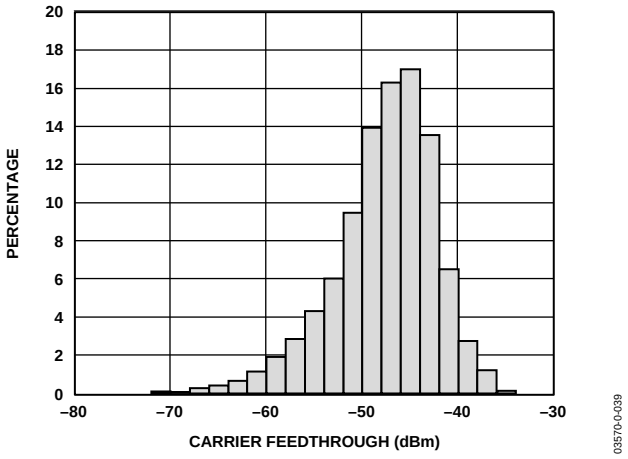


Figure 37. Carrier Feedthrough Distribution at F_{LO} = 900 MHZ (F_{BB} = 1 MHz, I and Q Inputs Driven in Quadrature at 1.2 V p-p, T_A = 25°C)

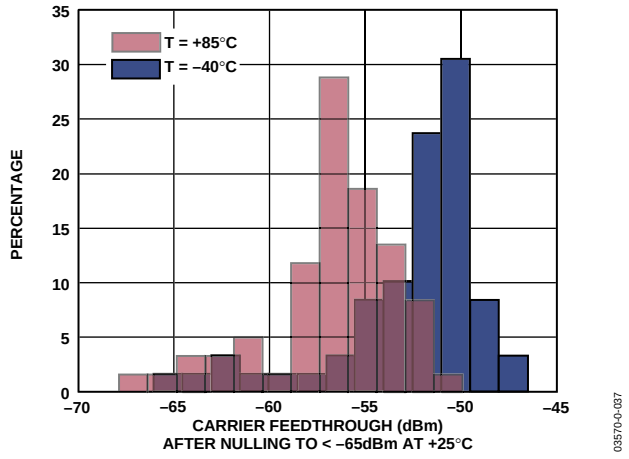


Figure 40. Carrier Feedthrough Distribution at Temperature Extremes, After Carrier Feedthrough Nulled to < - 65 dBm at T_A = 25°C. (F_{LO} = 2140 MHz, I and Q Inputs at a bias of 400 mV)

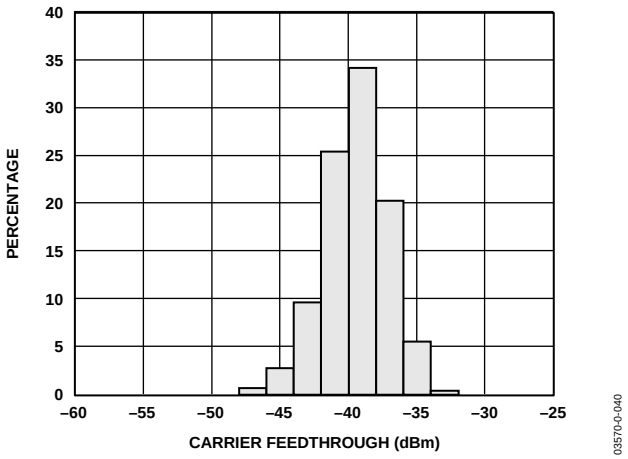


Figure 38. Carrier Feedthrough Distribution at F_{LO} = 1900 MHz (F_{BB} = 1 MHz, I and Q Inputs Driven in Quadrature at 1.2 Vp-p, T_A = 25°C)

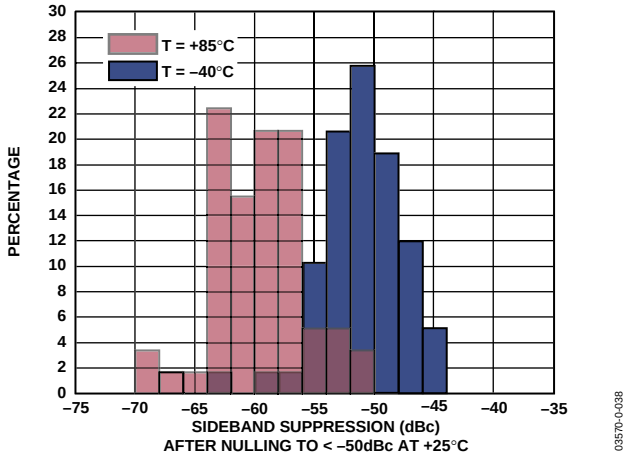


Figure 41. Sideband Suppression Distribution at Temperature Extremes, After Sideband Suppression Nulled to < -50 dBc at T_A = 25°C. (F_{LO} = 2140 MHz, F_{BB} = 1 MHz, I and Q Inputs biased at 0.4 V)

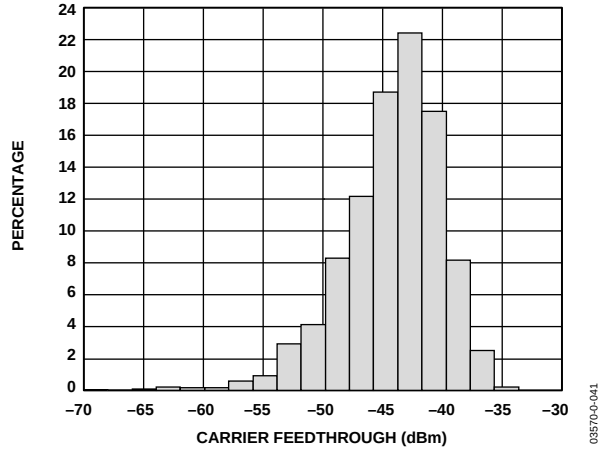


Figure 39. Carrier Feedthrough Distribution at F_{LO} = 2140 MHz (F_{BB} = 1 MHz, I and Q Inputs Driven in Quadrature at 1.2 V p-p, T_A = 25°C)

CIRCUIT DESCRIPTION

OVERVIEW

The AD8349 can be divided into five sections: the local oscillator (LO) interface, the baseband voltage-to-current (V-to-I) converter, the mixers, the differential-to-single-ended (D-to-S) amplifier, and the bias circuit. A detailed block diagram of the device is shown in Figure 42.

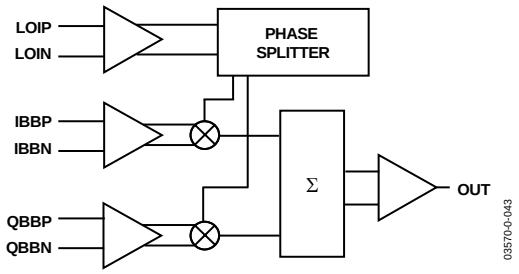


Figure 42. Block Diagram

The LO interface generates two LO signals at 90 degrees of phase difference to drive two mixers in quadrature. Baseband signals are converted into currents by the V-to-I converters, which feed into the two mixers. The outputs of the mixers combine to feed the differential-to-single-ended amplifier, which provides a 50 Ω output interface. Reference currents to each section are generated by the bias circuit. Additionally, the RF output is controlled by an output enable pin (ENOP), which is capable of switching the output on and off within 50 ns. A detailed description of each section follows.

LO INTERFACE

The LO interface consists of interleaved stages of buffer amplifiers and polyphase phase splitters. An input buffer provides a 50 Ω termination to the LO signal source driving LOIP and LOIN. The buffer also increases the LO signal amplitude to drive the phase splitter. The phase splitter is formed by an R-C polyphase network that splits the buffered LO signal into two parts in precise quadrature phase relation with each other. Each LO signal then passes through a buffer amplifier to compensate for the signal loss through the phase splitter. The two signals pass through another polyphase network to enhance the quadrature accuracy over the full operating frequency range. The outputs of the second phase splitter are fed into the driver amplifiers for the mixers' LO inputs.

V-TO-I CONVERTER

The differential baseband input voltages that are applied to the baseband input pins are fed to two op amps that perform a differential voltage-to-current conversion. The differential output currents of these op amps then feed each of their respective mixers.

MIXERS

The AD8349 has two double-balanced mixers, one for the in-phase channel (I channel) and one for the quadrature channel (Q channel). Both mixers are based on the Gilbert cell design of four cross-connected transistors. The output currents from the two mixers sum together in a pair of resistor-inductor (R-L) loads. The signals developed across the R-L loads are sent to the D-to-S amplifier.

D-TO-S AMPLIFIER

The output D-to-S amplifier consists of two emitter followers driving a totem pole output stage. Output impedance is established by the emitter resistors in the output transistors. The output of this stage connects to the output (VOUT) pin.

BIAS CIRCUIT

A band gap reference circuit generates the proportional-to-absolute-temperature (PTAT) reference currents used by different sections. The band gap reference circuit also generates a temperature stable current in the V-to-I converters to produce a temperature independent slew rate.

OUTPUT ENABLE

During normal operation (ENOP = high), the output current from the V-to-I converters feeds into the mixers, where they mix with the two phases of LO signals. When ENOP is pulled low, the V-to-I output currents are steered away from the mixers, thus turning off the RF output. Power to the final stage of LO drivers is also removed to minimize LO feedthrough. Even when the output is disabled, the differential-to-single-ended stage is still powered up to maintain constant output impedance.

BASIC CONNECTIONS

The basic connections for operating the AD8349 are shown in Figure 43. A single power supply of between 4.75 V and 5.5 V is applied to pins VPS1 and VPS2. A pair of ESD protection diodes connect internally between VPS1 and VPS2, so these must be tied to the same potential. Both pins should be individually decoupled using 100 pF and 0.1 μF capacitors to ground. These capacitors should be located as close as possible to the device. For normal operation, the output enable pin, ENOP, must be pulled high. The turn-on threshold for ENOP is 2 V. Pins COM1, COM2, and COM3 should all be tied to the same ground plane through low impedance paths.

BASEBAND I AND Q INPUTS

The I and Q inputs should be driven differentially. The typical differential drive level (as used for characterization measurements) for the I and Q baseband signals is 1.2 V p-p, which is equivalent to 600 mV p-p on each baseband input. The baseband inputs have to be externally biased to a level between 400 mV and 500 mV. The optimum level for the best performance is 400 mV. The recommended drive level of 1.2 V p-p does not indicate a maximum drive level. If operation closer to compression is desired, the 1.2 V p-p differential limit can be exceeded.

For baseband signals with a high peak-to-average ratio (e.g., CDDA or WCDMA), the peak signal level will have to be below the AD8349's compression level in order to prevent clipping of the signal peaks. Clipping of signal peaks increases distortion. In the case of CDMA and WCDMA inputs, clipping results in an increase of signal leakage into adjacent channels. In general, the baseband drive should be at a level where the peak signal power of the output signal is at least a crest factor below the AD8349's output compression point. Refer to the Applications section for drive-level considerations in WCDMA and GSM/EDGE systems.

Reducing the baseband drive level also has the benefit of increasing the bandwidth of the baseband input. This would allow the AD8349 to be used in applications requiring a high modulation bandwidth, e.g., as the IF modulator in high data-rate microwave radios.

SINGLE-ENDED BASEBAND DRIVE

Where only single-ended I and Q signals are available, a differential amplifier, such as the AD8132 or AD8138, can be used to generate the required differential drive signal for the AD8349.

Figure 44 shows an example of a circuit that converts a ground-referenced, single-ended signal to a differential signal, and adds the required 400 mV bias voltage.

The baseband inputs can also be driven with a single-ended signal biased to 400 mV, with the unused inputs biased to 400 mV dc. This mode of operation is not recommended, however, because any dc level difference between the bias level of the drive signal and the dc level on the unused input (including the effect of temperature drift), can result in increased LO feedthrough. Additionally, the maximum low distortion output power will be reduced by 6 dB.

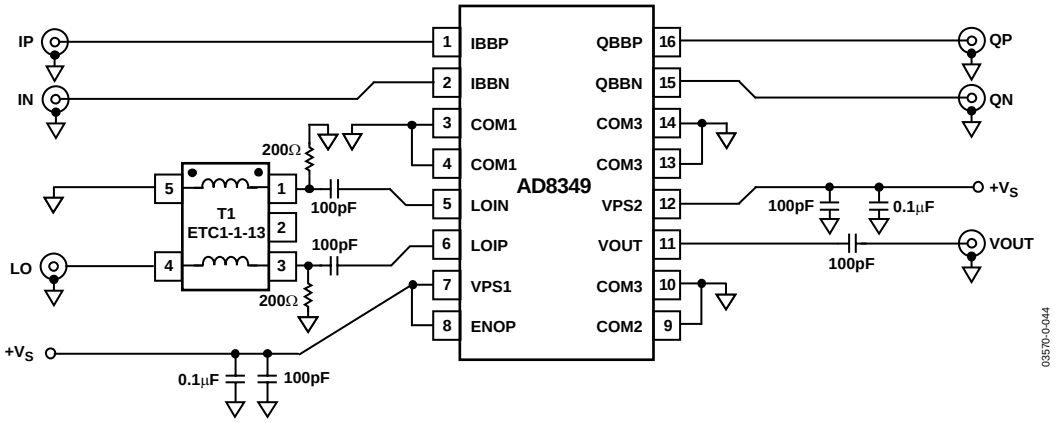


Figure 43. Basic Connections

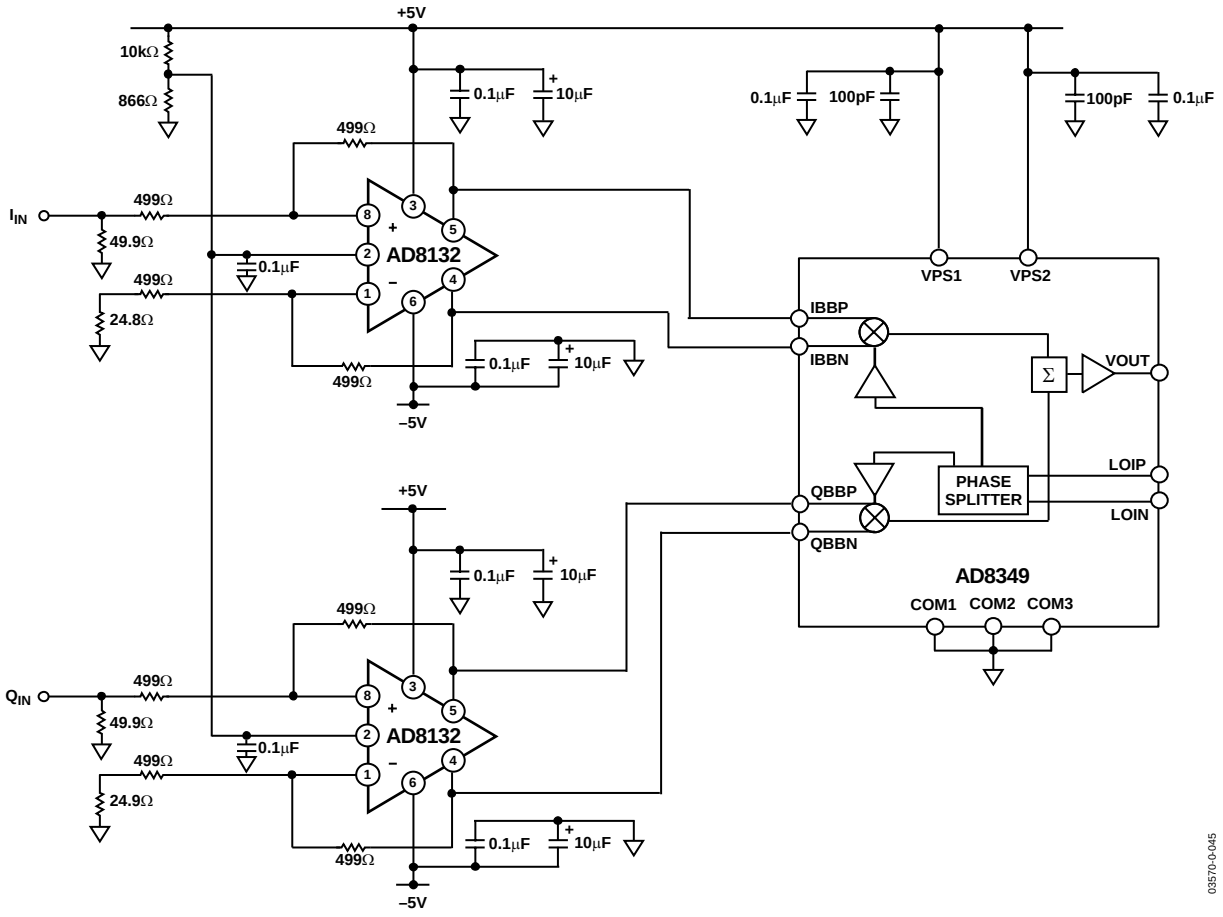


Figure 44. Single-Ended IQ Drive Circuit

LO INPUT DRIVE LEVEL

The local oscillator inputs are designed to be driven differentially. The device is specified with an LO drive level of –6 dBm. This level was chosen to provide the best noise performance. Increasing the LO drive level degrades sideband suppression and increases carrier feedthrough, while improving noise performance. Reducing the LO drive level creates the opposite effect: improved sideband suppression and reduced carrier feedthrough.

FREQUENCY RANGE

The LO frequency range is from 700 MHz to 2700 MHz. These limits are defined by the nature of the LO phase splitter circuitry. The phase splitter generates LO drive signals for the internal mixers, which are 90 degrees out of phase from each other. Outside of the specified frequency range (700 MHz to 2700 MHz), this quadrature accuracy degrades, resulting in poor sideband rejection performance. Figure 45 and Figure 46 show the sideband suppression of a typical device operating outside the specified LO frequency range. The level of sideband suppression and degradation is also influenced by manufacturing process variations.

LO INPUT IMPEDANCE MATCHING

Single-ended LO sources are transformed into a differential signal via a 1:1 balun (ETC1-1-13). A 200 Ω shunt resistor to GND on each LO input on the device side of the balun reduces the return loss for the LO input port. Because the LO input pins are internally dc-biased, ac coupling capacitors must be used on each LO input pin.

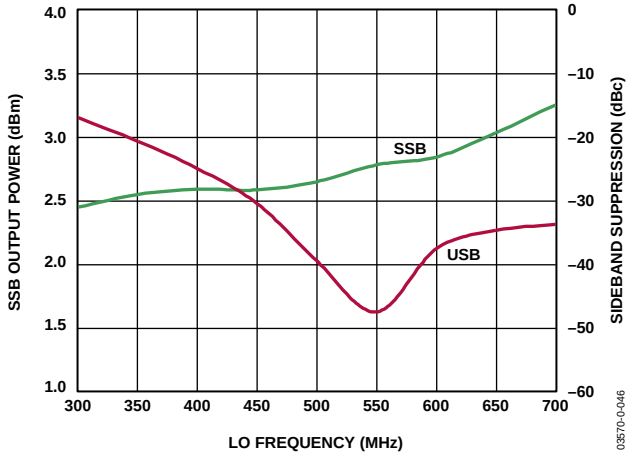


Figure 45. Sideband Suppression below 700 MHz

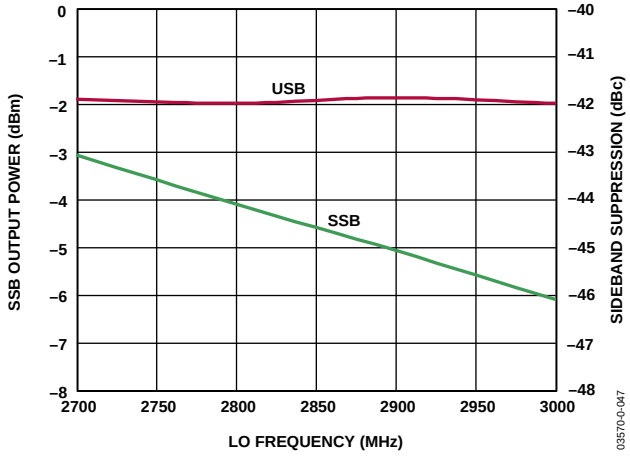


Figure 46. Sideband Suppression above 2700 MHz

SINGLE-ENDED LO DRIVE

The LO input can be driven single-ended at the expense of higher LO feedthrough at most frequencies (see Figure 48). LOIN is ac-coupled to ground, and LOIP is driven through a coupling capacitor from a single-ended 50 Ω source (see Figure 47).

A 400 Ω shunt resistor on the signal-source side of the ac coupling capacitor was used for the measurement.

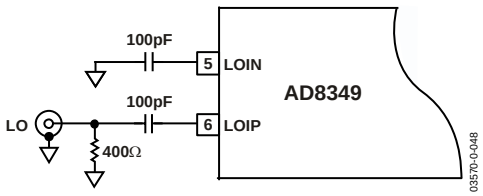


Figure 47. Schematic for Single-Ended LO Drive

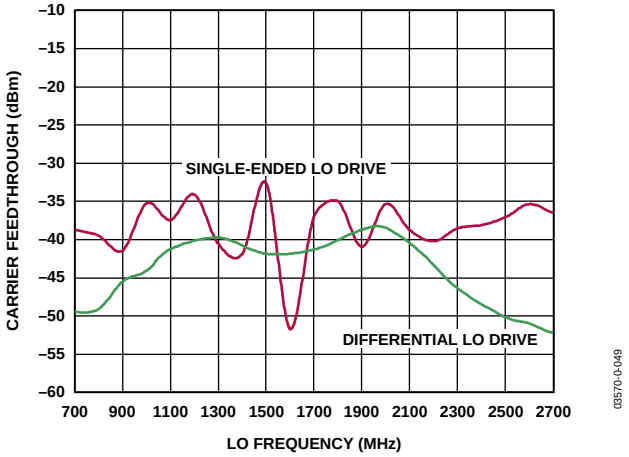


Figure 48. LO Feedthrough vs. Frequency, Single-Ended vs. Differential LO Drive (Single-Sideband Modulation)

RF OUTPUT

The RF output is designed to drive a 50 Ω load, but should be ac-coupled, as shown in Figure 43, because of internal dc biasing. The RF output impedance is close to 50 Ω and provides fairly good return loss over the specified operating frequency range (see Figure 24). As a result, no additional matching circuitry is required if the output is driving a 50 Ω load. The output power of the AD8349 under nominal conditions (1.2 V p-p differential baseband drive, 400 mV dc baseband bias, and a 5 V supply) is shown in Figure 7.

OUTPUT ENABLE

The ENOP pin can be used to turn the RF output on and off. This pin should be held high (greater than 2 V) for normal operation. Taking ENOP low (less than 800 mV) disables the output power and provides an off-isolation level of < –50 dBm at the output.

Figure 49 and Figure 50 show the enable and disable time domain responses of the ENOP function at 900 MHz. Typical enable and disable times are approximately 20 ns and 50 ns, respectively.

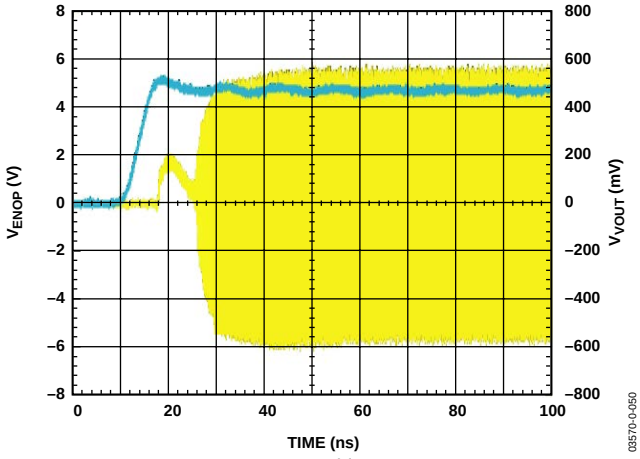


Figure 49. ENOP Enable Time, 900 MHz

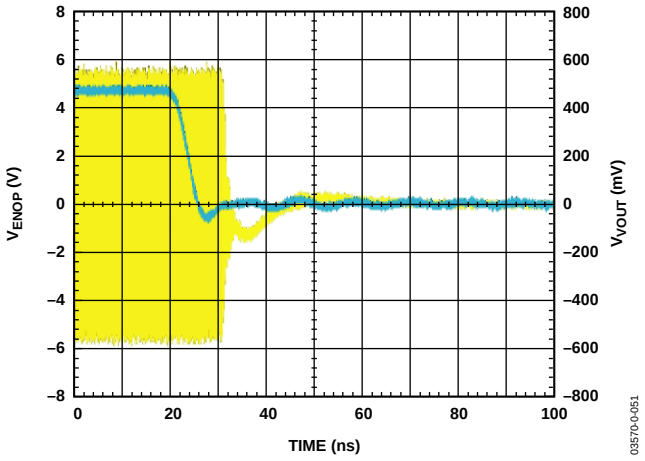


Figure 50. ENOP Disable Time, 900 MHz

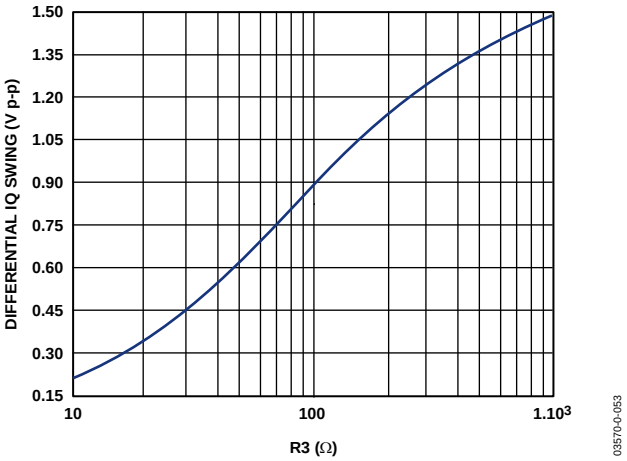


Figure 52. Relationship Between R3 in Figure 51 and Peak Baseband Input Voltage

BASEBAND DAC INTERFACE

The recommended baseband input swing and bias levels of the AD8349's differential baseband inputs allow for direct connection to most baseband DACs without the need for any external active components. Typically these DACs have a differential full-scale output current from 0 mA to 20 mA on each differential output. These currents can be easily converted to voltages using ground-referenced shunt resistors. Most baseband DACs for transmit chains are designed with two DACs in a single package.

AD9777 INTERFACE

The AD977x family of dual DACs is well suited to driving the baseband inputs of the AD8349. The AD9777 is a dual 16-bit DAC that can generate either a baseband output or a complex IF using the device's complex modulator.

The basic interface between the AD9777's I_{OUT} outputs and the AD8349's differential baseband inputs is shown in Figure 51. The Resistors R1 and R2 set the dc bias level, and R3 sets the amplitude of the baseband input voltage swing.

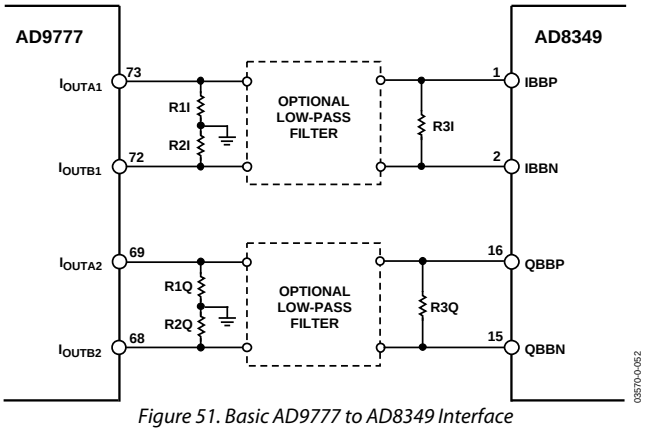


Figure 51. Basic AD9777 to AD8349 Interface

BIASING AND FILTERING

A value of 40 Ω on R1 and R2 in Figure 51 will generate the required 400 mV dc bias. Note that this is independent of the value of R3. Figure 52 shows the relationship between the value of R3 and the peak baseband input voltage with the 40 Ω resistors in place. From Figure 52, it can be seen that a value of 240 Ω will provide a peak-to-peak swing of approximately 1.2 V p-p differential into the AD8349's baseband inputs.

The closest available resistor values are 40.2 Ω and 240 Ω, and these values were used in the characterization of the AD8349 when the DAC was used as a signal source.

When using a DAC, low-pass image reject filters are typically used to eliminate images that are produced by the DAC. They provide the added benefit of eliminating broadband noise that might feed into the modulator from the DAC.

Figure 53 shows a single sideband spectrum at 2140 MHz. The baseband sine and cosine signals come from the digital output of a Rohde & Schwarz AMIQ arbitrary waveform generator. These signals drive the AD9777 dual DAC, which in turn drives the AD8349's baseband inputs. Note that the AD9777's complex modulator is not being used.

Due to offset voltages, internal device mismatch, and imperfect quadrature over the AD8349's operating range, the SSB spectrum has a number of undesirable components such as LO feedthrough and undesired sideband leakage. When the AD8349 is driven by a modulated baseband signal, (e.g. 8-PSK, GMSK, QPSK, or QAM), these nonidealities will manifest themselves as degraded error vector magnitude (EVM) and degraded spectral purity.

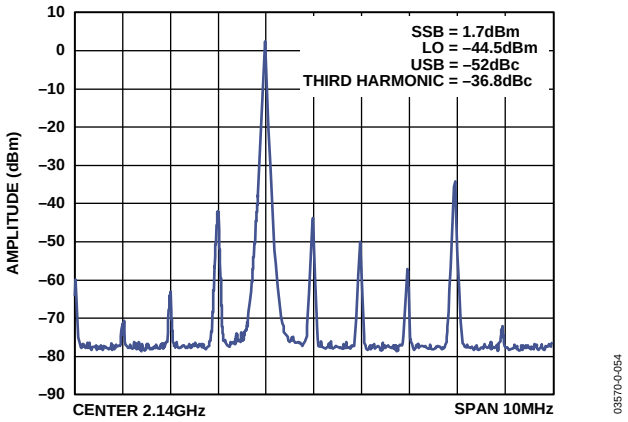


Figure 53. AD8349 Single Sideband Spectrum at 2140 MHz

REDUCING UNDESIRED SIDEBAND LEAKAGE

Undesired sideband leakage is the result of phase and amplitude imbalances between the I and Q channel baseband signals. Therefore, to reduce the undesired sideband leakage, the amplitude and phase of the baseband signals have to be matched at the mixer cores. Because of mismatches in the baseband input paths leading to the mixers, perfectly matched baseband signals at the pins of the device may not be perfectly matched when they reach the mixers. Therefore, slight adjustments have to be made to the phase and amplitudes of the baseband signals to compensate for these mismatches.

Begin by making one of the inputs, say the I channel, the reference signal. Then adjust the amplitude and phase of the Q channel's signal until the unwanted sideband power reaches a trough. The AD9777 has built-in gain adjust registers that allow this to be performed easily. If an iterative adjustment is performed between the amplitude and the phase, the undesired sideband leakage can be minimized significantly.

Note that the compensated sideband rejection performance degrades as the operating baseband frequency is moved away from the frequency at which the compensation was performed. As a result, the frequency of the I and Q sine waves should be approximately half the baseband bandwidth of the modulated carrier. For example, if the modulator is being used to transmit a single WCDMA carrier whose baseband spectrum spans from dc to 3.84/2 MHz, the calibration could be effectively performed with 1 MHz I and Q sine waves.

REDUCTION OF LO FEEDTHROUGH

Because the I and Q signals are being multiplied with the LO, any internal offset voltages on these inputs will result in leakage of the LO to the output. Additionally, any imbalance in the LO to RF in the mixers will also cause the LO signal to leak through the mixer to the RF output. The LO feedthrough is clearly visible in the single sideband spectrum. The nominal LO feedthrough of –42 dBm can be reduced further by applying offset compensation voltages on the I and Q inputs. Note that the LO feedthrough is reduced by varying the differential offset voltages on the I and Q inputs (xBBP – xBBN), not by varying the nominal bias level of 400 mV. This is easily accomplished by programming and then storing the appropriate DAC offset code required to minimize the LO feedthrough. This, however, requires a dc-coupled path from the DAC to the I and Q inputs.

The procedure for reducing the LO feedthrough is simple. A differential offset voltage is applied from the I DAC until the LO feedthrough reaches a trough. With this offset level held, a differential offset voltage is applied to the Q DAC until a lower trough is reached (This is an iterative process).

Figure 54 shows a plot of LO feedthrough vs. I channel offset (in mV) after the Q channel offset has been nulled. This suggests that the compensating offset voltage should have a resolution of at least 100 µV to reduce the LO feedthrough to be less than –65 dBm. Figure 55 shows the single sideband spectrum at 2140 MHz after the nulling of the LO. The reduced LO feedthrough can clearly be seen when compared with the performance shown in Figure 53.

Compensated LO feedthrough degrades somewhat as the LO frequency is moved away from the frequency at which the compensation was performed. This variation is very small across a 30 MHz or 60 MHz cellular band, however. This small variation is due to the effects of LO-to-RF output leakage around the package and on the board.

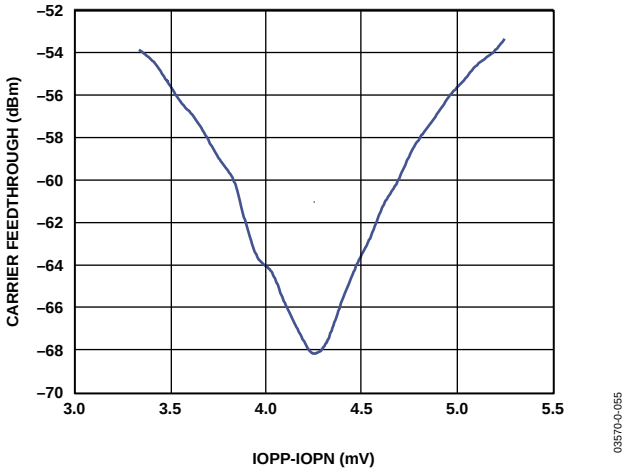


Figure 54. Plot of LO Feedthrough vs. I Channel Baseband Offset (Q Channel Offset Nulled)

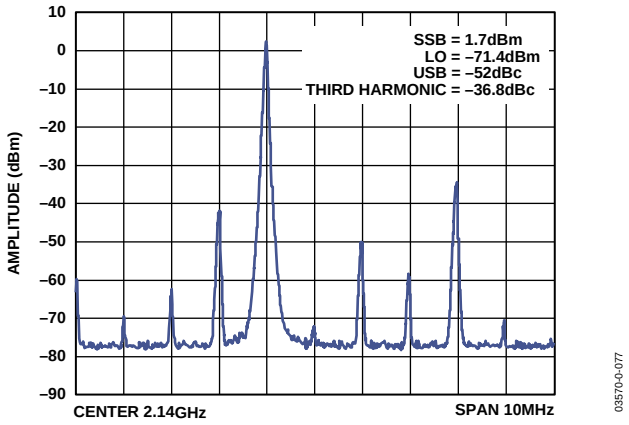


Figure 55. AD8349 Single Sideband Spectrum at 2140 MHz after LO Nulling

SIDEBAND SUPPRESSION AND LO FEEDTHROUGH VS. TEMPERATURE

In practical applications, reduction of LO feedthrough and undesired sideband suppression can be performed as a one time calibration, with the required correction factors being stored in nonvolatile RAM. These compensation schemes hold up well over temperature. Figure 40 and Figure 41 show the variation in LO feedthrough and sideband suppression over temperature after compensation is performed at 25°C.

SINGLE SIDEBAND PERFORMANCE VS. BASEBAND DRIVE LEVEL

Figure 56 shows the SSB output power and noise floor in dBc/100 kHz versus baseband drive level at LO frequencies of 940 MHz, 1960 MHz, and 2140 MHz.

IMPROVING THIRD HARMONIC DISTORTION

While sideband suppression can be improved by adjusting the relative baseband amplitudes and phase, the only means available to reduce the third harmonic is to reduce the output power. (See Figure 19, Figure 20, and Figure 21). It is worth noting, however, that as the output power is reduced, the noise floor, in dBc, stays fairly constant at the higher end of the power curve (Figure 56). This indicates that the output power can be reduced to a level that yields an acceptable third harmonic without incurring a signal-to-noise ratio penalty. The constant SNR vs. output power relationship also indicates that baseband voltage variations can be effectively used to control system output power and/or regulate signal chain gain.

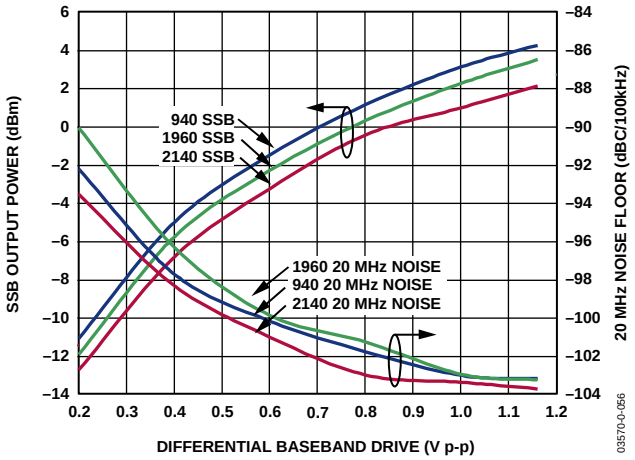


Figure 56. SSB P_{OUT} and 20 MHz Noise Floor vs. Baseband Drive Level (F_{LO} = 940 MHz, 1960 MHz, and 2140 MHz)

APPLICATIONS

3GPP WCDMA SINGLE-CARRIER APPLICATION

The interpolation filter used for the measurement of WCDMA performance is shown in Figure 57. This third order Bessel filter has a 3 dB bandwidth of 12 MHz. While the 3GPP single channel bandwidth is only 3.84 MHz, this wide 3 dB bandwidth of 12 MHz was driven by the need for a flat group delay out to at least half the bandwidth of the baseband signal. Figure 58 shows a plot of a WCDMA spectrum at 2140 MHz using the 3 GPP Test Model 1 (64 channels active). At an output power of –17.3 dBm, an adjacent channel power ratio (ACPR) just shy of –69 dBc was measured.

Figure 59 shows the variation in ACPR with output power at 1960 MHz and 2140 MHz. It also shows the noise floor measured at an offset of 30 MHz from the center of the modulated WCDMA signal. From the graphs, it can be seen that there is an optimal output power at which to operate that delivers the best ACPR. If the output power is increased beyond that point, the ACPR degrades as the result of increased distortion. Below that optimum, the ACPR degrades due to a reduction in the signal-to-noise ratio of the signal.

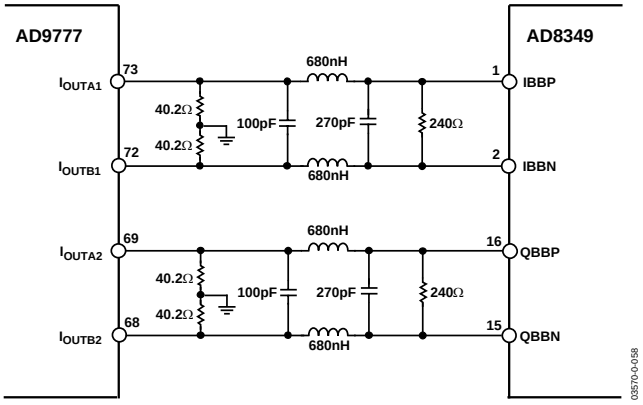


Figure 57. Single-Carrier WCDMA Application Circuit (DAC-Modulator Interconnect)

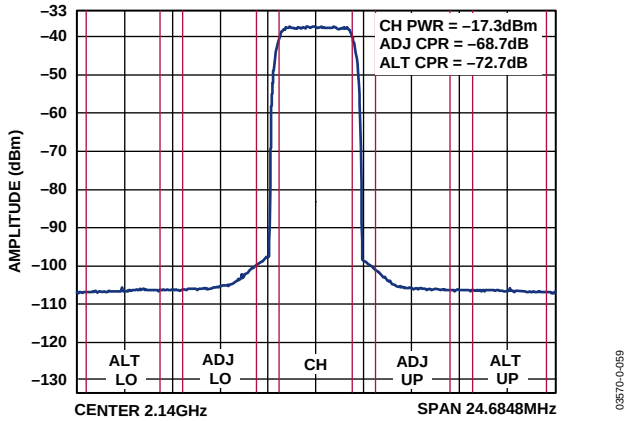


Figure 58. Single-Carrier WCDMA Spectral Plot at 2140 MHz, including Adjacent and Alternate Channel Power Ratio

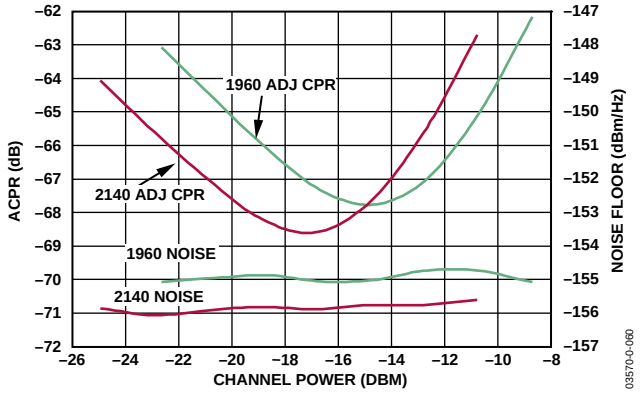


Figure 59. Single-Carrier WCDMA ACPR and Noise Floor (dBm/Hz) at 30 MHz Carrier Offset vs. Channel Power at 1960 MHz and 2140 MHz (Test Model 1 with 64 Active Channels)

WCDMA MULTICARRIER APPLICATION

The high dynamic range of the AD8349 also permits use in multicarrier WCDMA applications. Figure 60 shows a 4-carrier WCDMA spectrum at 1960 MHz. At a per-carrier power of –24.2 dBm, an ACPR of –60.4dB is achieved. Figure 61 shows the variation in ACP and noise floor (dBc/Hz) with output power.

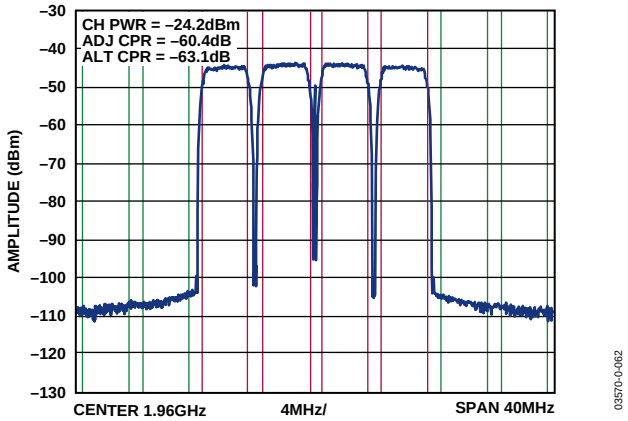


Figure 60. 4-Carrier WCDMA Spectral Plot at 1960 MHz, Including Adjacent and Alternate Channel Power Ratio

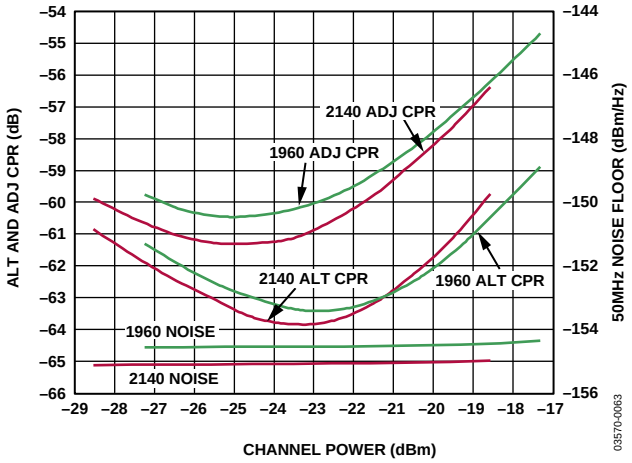


Figure 61. 4-Carrier WCDMA Adjacent and Alternate Channel Power Ratio and 50 MHz Noise Floor (dBm/Hz) vs. Per-Channel Power at 1960 MHz and 2140 MHz

GSM/EDGE APPLICATION

Figure 62 and Figure 64 show plots of GMSK error vector magnitude (EVM), spectral performance, and noise floor (dBc/100 kHz at 6 MHz carrier offset) at 885 MHz and 1960 MHz. Based on spectral performance, a maximum output power level of around 2 dBm is appropriate. Note, however, that as the output power decreases below this level, there is only a very slight increase in the dBc noise floor. This indicates that baseband drive variation can be used to control or correct the gain of the signal chain over a range of at least 5 dB, with little or no SNR penalty.

Figure 63 and Figure 65 show plots of 8-PSK EVM, spectral performance, and noise floor at 885 MHz and 1960 MHz.

An LO drive level of approximately −6 dBm is recommended for GMSK and 8-PSK. A higher LO drive power will improve the noise floor slightly; however, it also tends to degrade EVM.

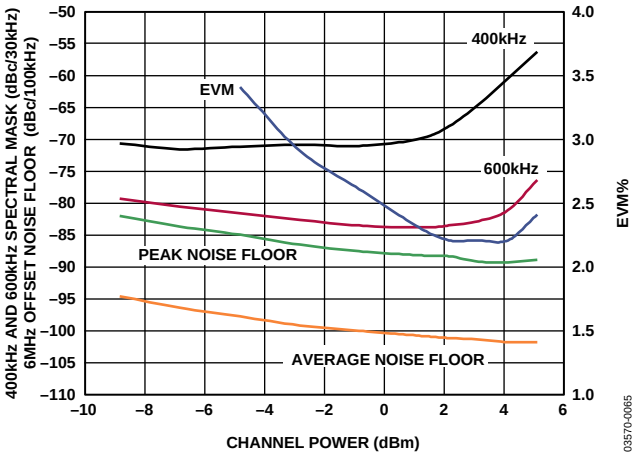


Figure 62.GMSK EVM, Spectral Performance, and Noise Floor vs. Channel Power (Frequency = 885 MHz)

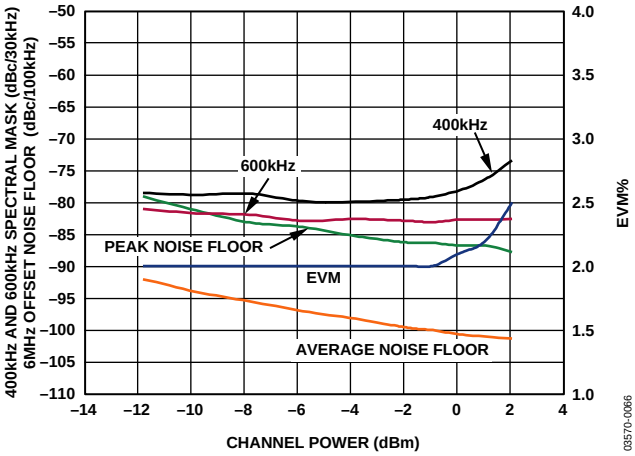


Figure 63. 8-PSK EVM, Spectral Performance, and Noise Floor vs. Channel Power (Frequency = 885 MHz)

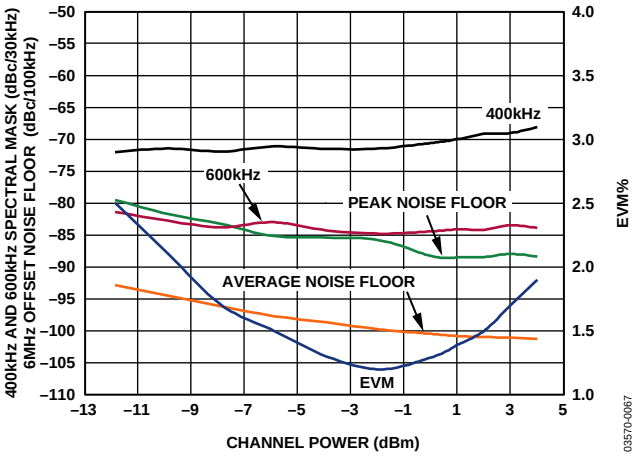


Figure 64. GMSK EVM, Spectral Performance, and Noise Floor vs. Channel Power (Frequency = 1960 MHz)

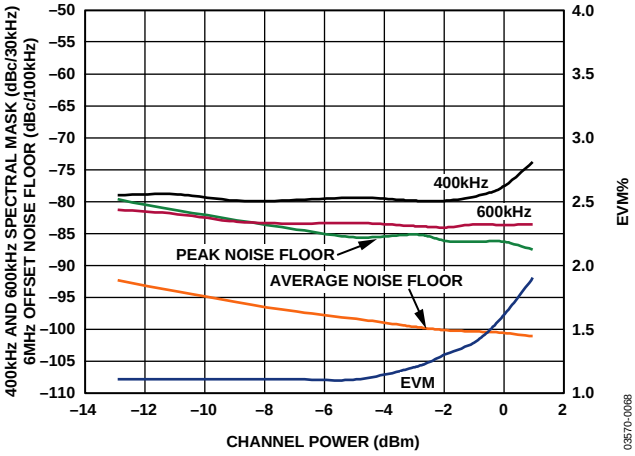


Figure 65. 8-PSK EVM, Spectral Performance, and Noise Floor vs. Channel Power (Frequency = 1960 MHz)

SOLDERING INFORMATION

The AD8349 is available in a 16-lead TSSOP package with an exposed paddle. The exposed paddle must be soldered to the exposed metal of a ground plane for a lowered thermal impedance and reduced inductance to ground. This results in a junction-to-air thermal impedance (θ_{JA}) of 30°C/W. If multiple ground planes are present, the area under the exposed paddle should be stitched together with vias.

LO GENERATION USING PLLS

Analog Devices has a line of PLLs that can be used for generating the LO signal. Table 4 lists the PLLs together with their maximum frequency and phase noise performance.

Table 4. ADI PLL Selection Table

ADI Model	Frequency F_{IN} (MHz)	At 1 kHz Phase Noise dBc/Hz, 200 kHz PFD
ADF4111BRU	1200	–78
ADF4111BCP	1200	–78
ADF4112BRU	3000	–86
ADF4112BCP	3000	–86
ADF4117BRU	1200	–87
ADF4118BRU	3000	–90

Analog Devices also offers the ADF4360 fully integrated synthesizer and VCO on a single chip that offers differential outputs for driving the local oscillator input of the AD8349. This means that the user can eliminate the use of the balun necessary for the single-ended-to-differential conversion. The ADF4360 comes as a family of chips with six operating frequency ranges. One can be chosen depending on the local oscillator frequency required. The user should be aware that while the use of the integrated synthesizer might come at the expense of slightly degraded noise performance from the AD8349, it can be a much cheaper alternative to a separate PLL and VCO solution. Figure 61 shows the options available.

Table 5. ADF4360 Family Operating Frequencies

ADI Model	Output Frequency Range (MHz)
ADF4360-1	2150/2450
ADF4360-2	1800/2150
ADF4360-3	1550/1950
ADF4360-4	1400/1800
ADF4360-5	1150/1400
ADF4360-6	1000/1250
ADF4360-7	Lower frequencies set by external L

TRANSMIT DAC OPTIONS

The AD9777 recommended in the previous sections of this data sheet is by no means the only DAC that can be used to drive the AD8349. There are other DACs that are appropriate, depending on the level of performance required. Table 6 lists the dual Tx-DACs that ADI offers.

Table 6. ADI Dual Tx – DAC Selection Table

Part	Resolution (Bits)	Update Rate (MSPS Min)
AD9709	8	125
AD9761	10	40
AD9763	10	125
AD9765	12	125
AD9767	14	125
AD9773	12	160
AD9775	14	160
AD9777	16	160

EVALUATION BOARD

A populated AD8349 evaluation board is available.

The AD8349 has an exposed paddle underneath the package, which is soldered to the board. The evaluation board is designed without any components on the underside of the board so that heat may be applied under the AD8349 for easy removal and replacement of the DUT.

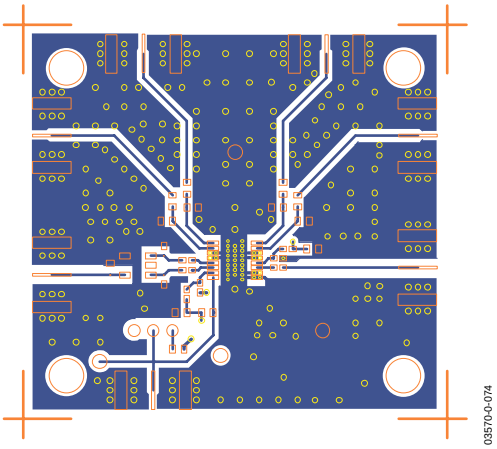


Figure 66. Layout of Evaluation Board, Top Layer

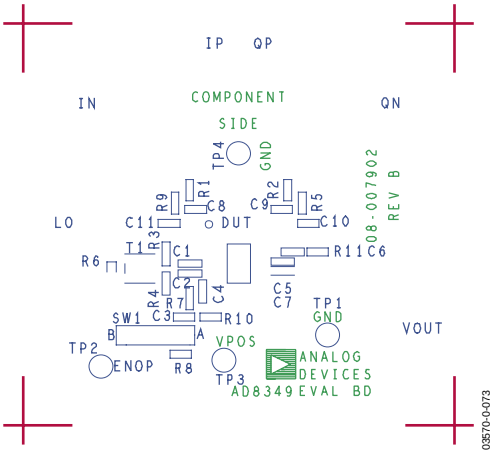


Figure 67. Evaluation Board Silkscreen

Table 7. Evaluation Board Configuration Options

Component	Function	Default Condition
TP1, TP4, TP3	Power Supply and Ground Vector Pins.	Not applicable
SW1, ENOP, TP2	Output Enable: Place in the A position to connect the ENOP pin to $+V_S$ via pull-up resistor R10. Place in the B position to disable the device by grounding the pin ENOP through a 49.9 Ω pull-down resistor. The device may be enabled via an external voltage applied to the SMA connector ENOP or TP2.	SW1 = A
R1, R2, R5, R9, C8–C11	Baseband Input Filters: These components can be used to implement a low-pass filter for the baseband signals.	R1, R2, R5, R9 = 0 Ω, C8 – C11 = OPEN

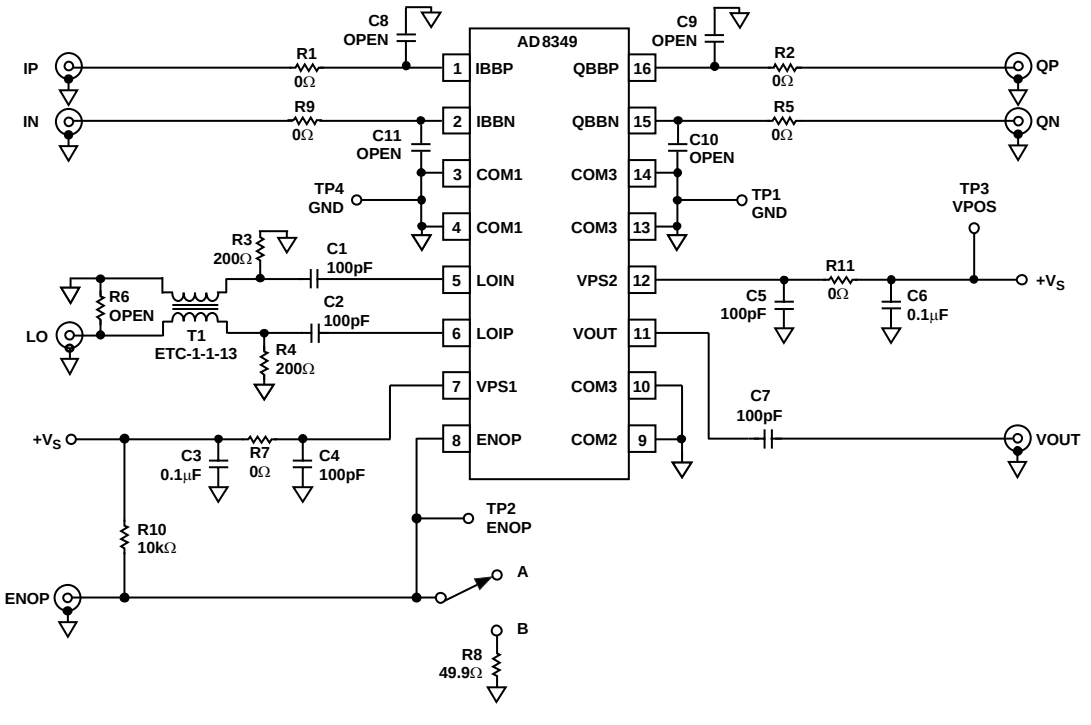


Figure 68. Evaluation Board Schematic

CHARACTERIZATION SETUPS

SSB SETUP

The primary setup used to characterize the AD8349 is shown in Figure 69. This setup was used to evaluate the product as a single-sideband modulator. The interface board has circuitry that converts the single-ended I and Q inputs from the arbitrary function generator to differential inputs with a dc bias of 400 mV. Additionally, the interface board provides connections for power supply routing. The HP34970A and its associated plug-in 34901 were used to monitor power supply currents and voltages being supplied to the AD8349 characterization board.

Two HP34907 plug-ins were used to provide additional miscellaneous dc and control signals to the interface board. The LO input was driven directly by an RF signal generator and the output was measured directly with a spectrum analyzer. With the I channel driven by a sine wave and the Q channel by a cosine wave, the lower sideband is the single sideband (SSB) output. The typical SSB output spectrum is shown in Figure 53.

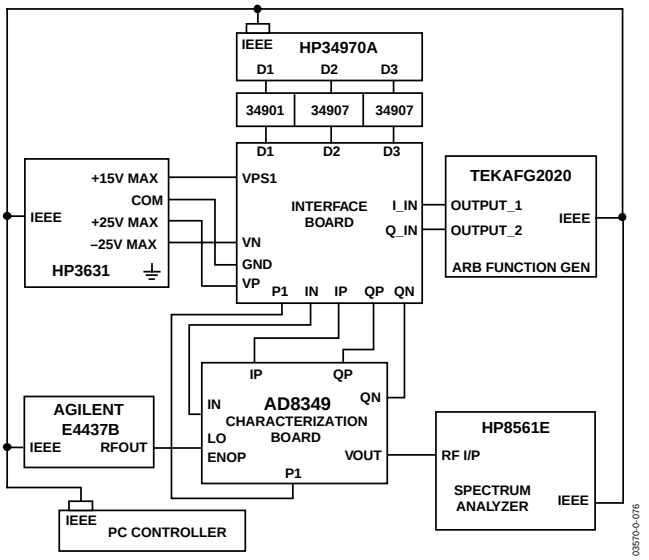


Figure 69. Characterization Board SSB Test Setup

OUTLINE DIMENSIONS

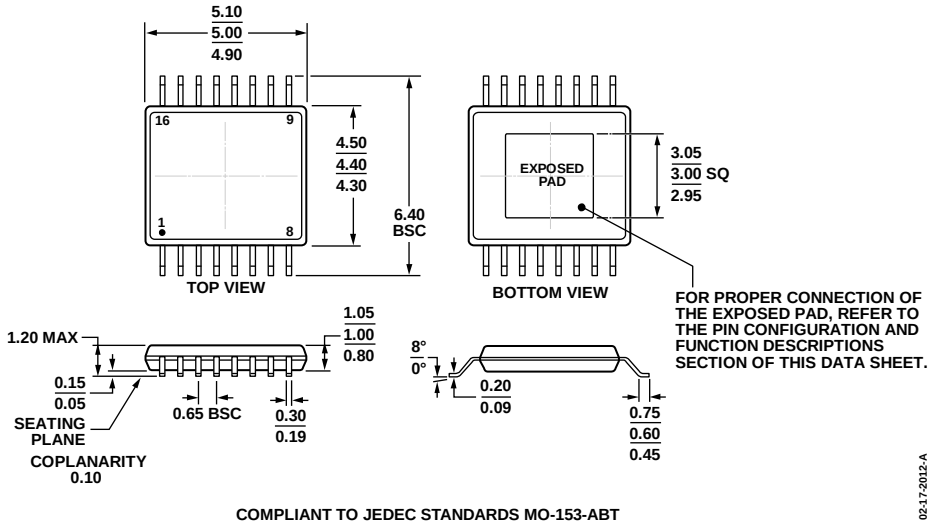


Figure 70. 16-Lead Thin Shrink Small Outline with Exposed Pad [TSSOP_EP]
(RE-16-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range (°C)	Package Description	Package Option
AD8349ARE-REEL7	–40 to +85	16-Lead TSSOP_EP, 7" Tape and Reel	RE-16-2
AD8349AREZ	–40 to +85	16-Lead TSSOP_EP, Tube	RE-16-2
AD8349AREZ-RL7	–40 to +85	16-Lead TSSOP_EP, 7" Tape and Reel	RE-16-2
AD8349-EVALZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

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D03570-0-2/12(B)

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