Dual Low Noise, Picoampere Bias Current, JFET Input Op Amp

FEATURES

- **Input Bias Current, Warmed Up: 20pA Max**
- **100% Tested Low Voltage Noise: 8nV/√Hz Max**
- S8 and N8 Package Standard Pinout
- Very Low Input Capacitance: 1.5pF
- Voltage Gain: 1.2 Million Min
- Offset Voltage: 2mV Max
- Input Resistance: $10^{13}\Omega$
- Gain-Bandwidth Product: 5.3MHz Typ
- Guaranteed Specifications with ±5V Supplies
- Guaranteed Matching Specifications

APPLICATIONS

- Photocurrent Amplifiers
- Hydrophone Amplifiers
- High Sensitivity Piezoelectric Accelerometers
- Low Voltage and Current Noise Instrumentation Amplifier Front Ends
- Two and Three Op Amp Instrumentation Amplifiers
- Active Filters

DESCRIPTION

The LT1169 achieves a new standard of excellence in noise performance for a dual JFET op amp. For the first time low voltage noise (6nV/√Hz) is simultaneously offered with extremely low current noise (1fA/√Hz), providing the lowest total noise for high impedance transducer applications. Unlike most JFET op amps, the very low input bias current (5pA Typ) is maintained over the entire common mode range which results in an extremely high input resistance ($10^{13}\Omega$). When combined with a very low input capacitance (1.5pF) an extremely high input impedance results, making the LT1169 the first choice for amplifying low level signals from high impedance transducers. The low input capacitance also assures high gain linearity when buffering AC signals from high impedance transducers.

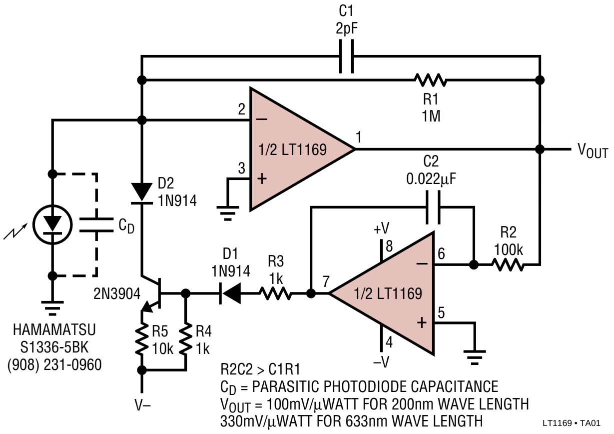
The LT1169 is unconditionally stable for gains of 1 or more, even with 1000pF capacitive loads. Other key features are 0.6mV V_{OS} and a voltage gain over 4 million. Each individual amplifier is 100% tested for voltage noise, slew rate (4.2V/µs), and gain-bandwidth product (5.3MHz).

The LT1169 is offered in the S8 and N8 packages.

A full set of matching specifications are provided for precision instrumentation amplifier front ends. Specifications at ±5V supply operation are also provided. For an even lower voltage noise please see the LT1113 data sheet.

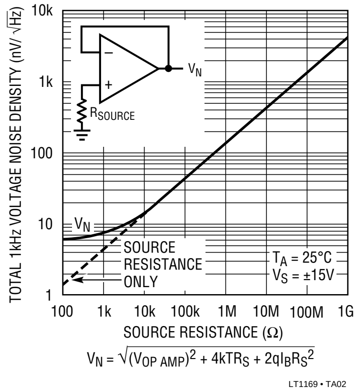
TYPICAL APPLICATION

Low Noise Light Sensor with DC Servo



R2C2 > C1R1
C_D = PARASITIC PHOTODIODE CAPACITANCE
V_{OUT} = 100mV/µWATT FOR 200nm WAVE LENGTH
330mV/µWATT FOR 633nm WAVE LENGTH

1kHz Output Voltage Noise Density vs Source Resistance

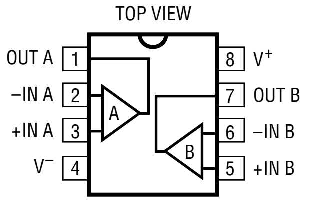


$V_N = \sqrt{(V_{OP\,AMP})^2 + 4kTR_S + 2qI_BR_S^2}$

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
−55°C to 105°C	±20V
105°C to 125°C	±16V
Differential Input Voltage	±40V
Input Voltage (Equal to Supply Voltage)	±20V
Output Short-Circuit Duration	Indefinite
Operating Temperature Range	−40°C to 85°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PDIP

S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 80°C/W (N8)
T_{JMAX} = 160°C, θ_{JA} = 190°C/W (S8)

ORDER PART NUMBER
LT1169CN8 LT1169CS8
S8 PART MARKING
1169

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS **V_S = ±15V, V_{CM} = 0V, T_A = 25°C, unless otherwise noted.**

SYMBOL	PARAMETER	CONDITIONS (Note 1)	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage			0.60	2.0	mV
		V_S = ±5V		0.65	2.2	mV
I_{OS}	Input Offset Current	Warmed Up (Note 2)		2.5	15	pA
		T_J = 25°C (Note 5)		0.7	4	pA
I_B	Input Bias Current	Warmed Up (Note 2)		4.0	20	pA
		T_J = 25°C (Note 5)		1.5	5	pA
e_n	Input Noise Voltage	0.1Hz to 10Hz		2.4		μV_{P-P}
	Input Noise Voltage Density	f_O = 10Hz		17		$nV/\sqrt{Hz}$
		f_O = 1000Hz		6	8	$nV/\sqrt{Hz}$
i_n	Input Noise Current Density	f_O = 10Hz, f_O = 1kHz (Note 3)		1		$fA/\sqrt{Hz}$
R_{IN}	Input Resistance					
	Differential Mode			10^{14}		Ω
	Common Mode	V_{CM} = −10V to 13V		10^{13}		Ω
C_{IN}	Input Capacitance			1.5		pF
		V_S = ±5V		2.0		pF
V_{CM}	Input Voltage Range (Note 4)		13.0	13.5		V
			−10.5	−11.0		V
CMRR	Common Mode Rejection Ratio	V_{CM} = −10V to 13V	82	95		dB
PSRR	Power Supply Rejection Ratio	V_S = ±4.5V to ± 20V	83	98		dB
A_{VOL}	Large-Signal Voltage Gain	V_O = ±12V, R_L = 10k	1000	4500		V/mV
		V_O = ±10V, R_L = 1k	500	3000		V/mV
V_{OUT}	Output Voltage Swing	R_L = 10k	±13.0	±13.8		V
		R_L = 1k	±12.0	±13.0		V
SR	Slew Rate	$R_L \geq 2k$ (Note 6)	2.4	4.2		V/µs
GBW	Gain-Bandwidth Product	f_O = 100kHz	3.3	5.3		MHz
	Channel Separation	f_O = 10Hz, V_O = ±10V, R_L = 1k		126		dB
I_S	Supply Current per Amplifier			5.3	6.50	mA
		V_S = ±5V		5.3	6.45	mA
ΔV_{OS}	Offset Voltage Match			0.8	3.5	mV
ΔI_B^+	Noninverting Bias Current Match	Warmed Up (Note 2)		3	20	pA
ΔCMRR	Common Mode Rejection Match	(Note 8)	78	94		dB
ΔPSRR	Power Supply Rejection Match	(Note 8)	80	95		dB

ELECTRICAL CHARACTERISTICS

V_S = ±15V, V_{CM} = 0V, 0°C ≤ T_A ≤ 70°C, (Note 9), unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 1)		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		●		0.7	3.2	mV
		V_S = ±5V	●		0.8	3.4	mV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Voltage Drift	(Note 5)	●		20	50	µV/°C
I_{OS}	Input Offset Current		●		10	50	pA
I_B	Input Bias Current		●		180	400	pA
V_{CM}	Input Voltage Range		●	12.9	13.4		V
			●	−10.0	−10.8		V
CMRR	Common Mode Rejection Ratio	V_{CM} = −10V to 12.9V	●	79	94		dB
PSRR	Power Supply Rejection Ratio	V_S = ±4.5V to ±20V	●	81	97		dB
A_{VOL}	Large-Signal Voltage Gain	V_O = ±12V, R_L = 10k	●	800	3400		V/mV
		V_O = ±10V, R_L = 1k	●	400	2400		V/mV
V_{OUT}	Output Voltage Swing	R_L = 10k	●	±12.5	±13.5		V
		R_L = 1k	●	±11.5	±12.7		V
SR	Slew Rate	R_L ≥ 2k (Note 6)	●	1.9	4		V/µs
GBW	Gain-Bandwidth Product	f_O = 100kHz	●	3	4.2		MHz
I_S	Supply Current per Amplifier		●		5.3	6.55	mA
		V_S = ±5V	●		5.3	6.50	mA
ΔV_{OS}	Offset Voltage Match		●		1.5	5	mV
ΔI_B^+	Noninverting Bias Current Match		●		5.5	50	pA
ΔCMRR	Common Mode Rejection Match	(Note 8)	●	74	93		dB
ΔPSRR	Power Supply Rejection Match	(Note 8)	●	77	93		dB

V_S = ±15V, V_{CM} = 0V, −40°C ≤ T_A ≤ 85°C, (Note 7), unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 1)		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		●		0.8	3.8	mV
		V_S = ±5V	●		0.9	4.0	mV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Voltage Drift		●		20	50	µV/°C
I_{OS}	Input Offset Current		●		30	200	pA
I_B	Input Bias Current		●		320	1200	pA
V_{CM}	Input Voltage Range		●	12.6	13.0		V
			●	−10.0	−10.5		V
CMRR	Common Mode Rejection Ratio	V_{CM} = −10V to 12.6V	●	78	93		dB
PSRR	Power Supply Rejection Ratio	V_S = ±4.5V to ±20V	●	79	96		dB
A_{VOL}	Large-Signal Voltage Gain	V_O = ±12V, R_L = 10k	●	750	3000		V/mV
		V_O = ±10V, R_L = 1k	●	300	2000		V/mV
V_{OUT}	Output Voltage Swing	R_L = 10k	●	±12.5	±12.5		V
		R_L = 1k	●	±11.3	±12.0		V
SR	Slew Rate	R_L ≥ 2k	●	1.8	3.8		V/µs
GBW	Gain-Bandwidth Product	f_O = 100kHz	●	2.7	4		MHz
I_S	Supply Current per Amplifier		●		5.30	6.55	mA
		V_S = ±5V	●		5.25	6.50	mA

ELECTRICAL CHARACTERISTICS $V_S = \pm15V$, $V_{CM} = 0V$, $-40°C \le T_A \le 85°C$, (Note 7), unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 1)		MIN	TYP	MAX	UNITS
ΔV_{OS}	Offset Voltage Match		●		1.8	6	mV
ΔI_B^+	Noninverting Bias Current Match		●		10	180	pA
ΔCMRR	Common Mode Rejection Match	(Note 8)	●	73	93		dB
ΔPSRR	Power Supply Rejection Match	(Note 8)	●	75	92		dB

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Typical parameters are defined as the 60% yield of parameter distributions of individual amplifiers, i.e., out of 100 LT1169s (200 op amps) typically 120 op amps will be better than the indicated specification.

Note 2: I_B and I_{OS} readings are extrapolated to a warmed-up temperature from 25°C measurements and 45°C characterization data.

Note 3: Current noise is calculated from the formula:

$$i_n = (2qI_B)^{1/2}$$

where $q = 1.6 \times 10^{-19}$ coulomb. The noise of source resistors up to 200M swamps the contribution of current noise.

Note 4: Input voltage range functionality is assured by testing offset voltage at the input voltage range limits to a maximum of 2.8mV.

Note 5: This parameter is not 100% tested.

Note 6: Slew rate is measured in $A_V = -1$; input signal is ±7.5V, output measured at ±2.5V.

Note 7: The LT1169 is designed, characterized and expected to meet these extended temperature limits, but is not tested at –40°C and 85°C. Guaranteed I grade parts are available; consult factory.

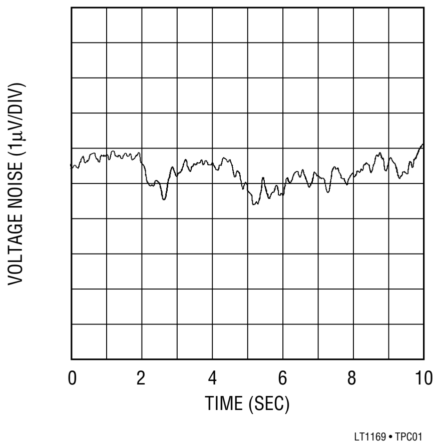
Note 8: ΔCMRR and ΔPSRR are defined as follows:

1. CMRR and PSRR are measured in µV/V on the individual amplifiers.
2. The difference is calculated between the matching sides in µV/V.
3. The result is converted to dB.

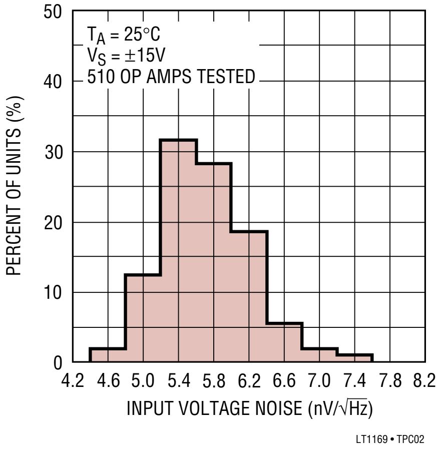
Note 9: The LT1169 is measured in an automated tester in less than one second after application of power. Depending on the package used, power dissipation, heat sinking, and air flow conditions, the fully warmed-up chip temperature can be 10°C to 50°C higher than the ambient temperature.

TYPICAL PERFORMANCE CHARACTERISTICS

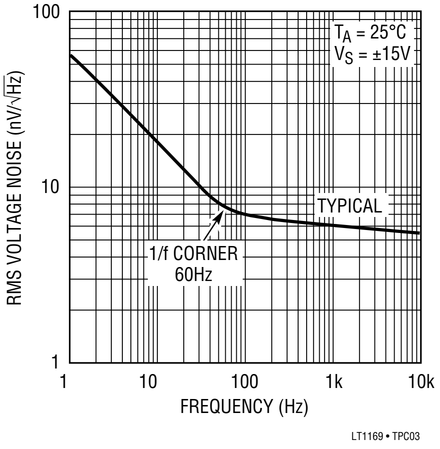
0.1Hz to 10Hz Voltage Noise



1kHz Input Noise Voltage Distribution

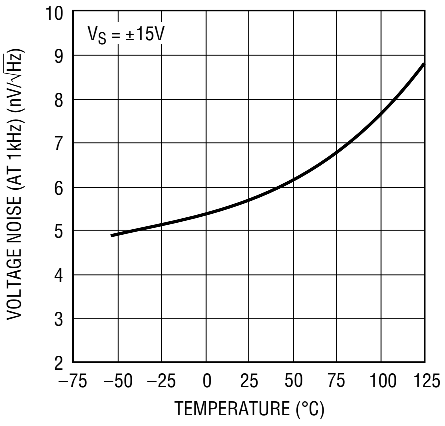


Voltage Noise vs Frequency



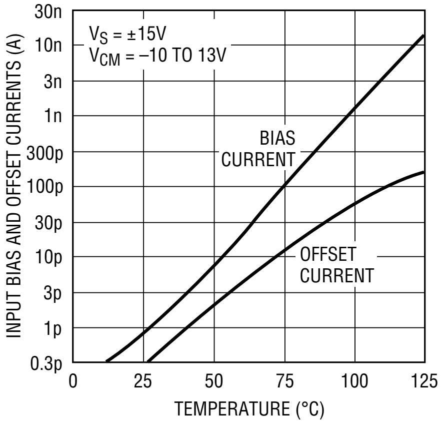
TYPICAL PERFORMANCE CHARACTERISTICS

Voltage Noise vs Chip Temperature



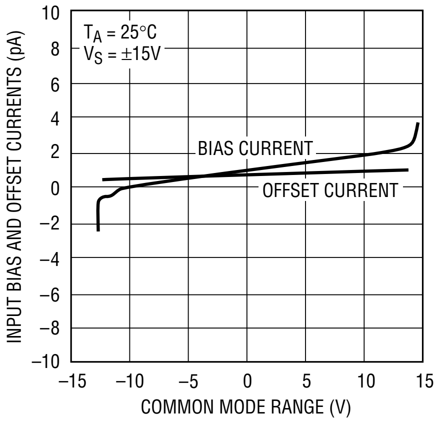
LT1169 • TPC04

Input Bias and Offset Currents vs Chip Temperature



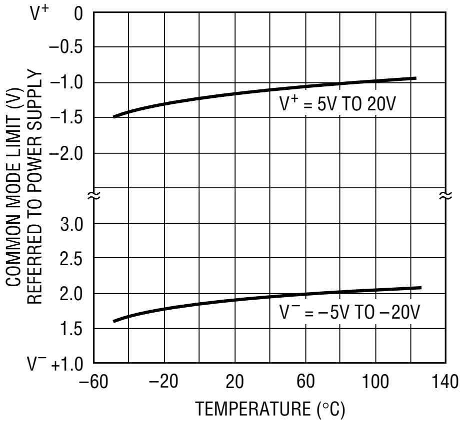
LT1169 • TPC05*

Input Bias and Offset Currents Over the Common Mode Range



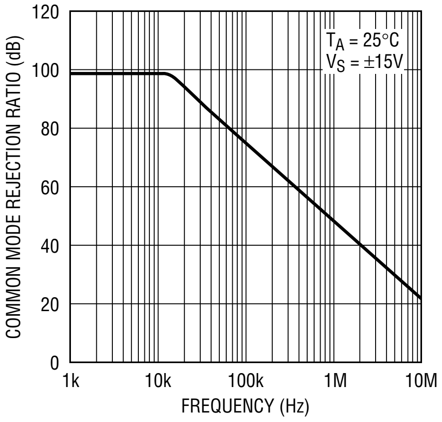
LT1169 • TPC06

Common Mode Limit vs Temperature



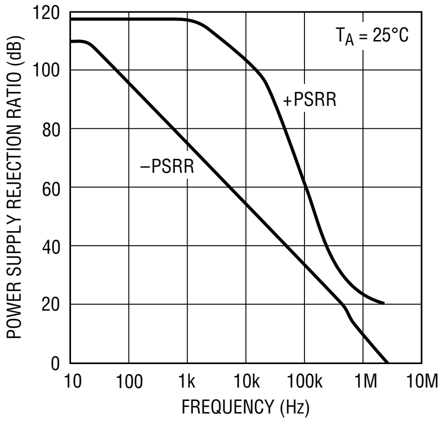
LT1169 • TPC07

Common Mode Rejection Ratio vs Frequency



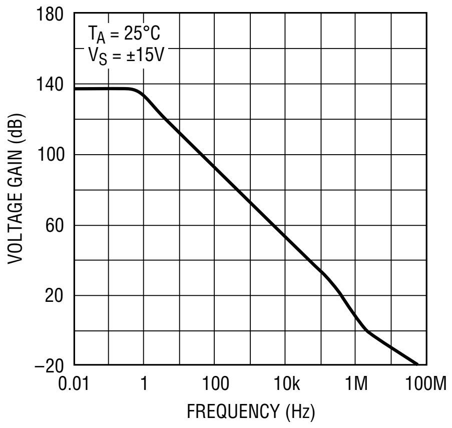
LT1169 • TPC08

Power Supply Rejection Ratio vs Frequency



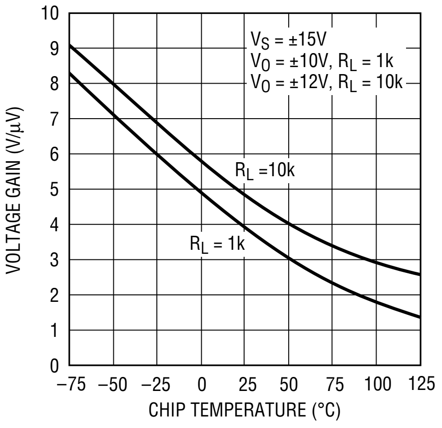
LT1169 • TPC09

Voltage Gain vs Frequency



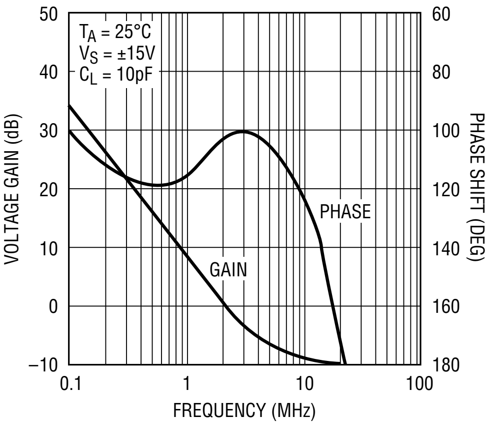
LT1169 • TPC10

Voltage Gain vs Chip Temperature



LT1169 • TPC11

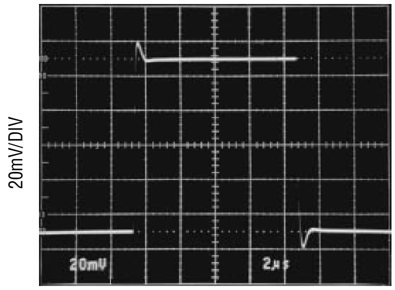
Gain and Phase Shift vs Frequency



LT1169 • TPC12

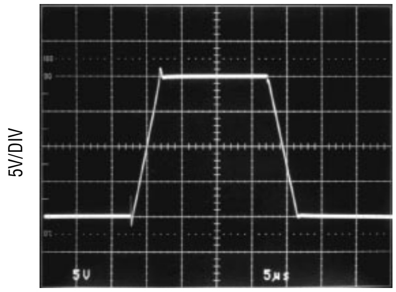
TYPICAL PERFORMANCE CHARACTERISTICS

Small-Signal Transient Response



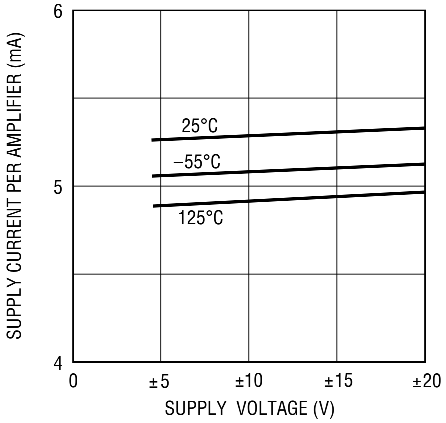
$A_V = 1$ 2μs/DIV LT1169 • TPC13
$C_L = 10pF$
$V_S = \pm15V, \pm5V$

Large-Signal Transient Response



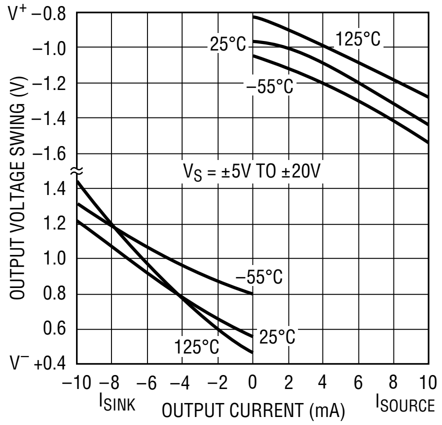
$A_V = 1$ 5μs/DIV LT1169 • TPC14
$C_L = 10pF$
$V_S = \pm15V$

Supply Current vs Supply Voltage



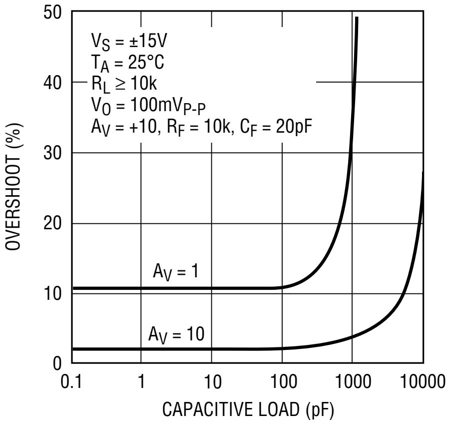
LT1169 • TPC15

Output Voltage Swing vs Load Current



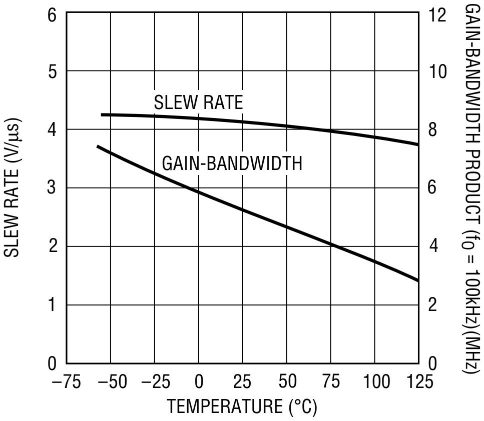
LT1169 • TPC16

Capacitive Load Handling



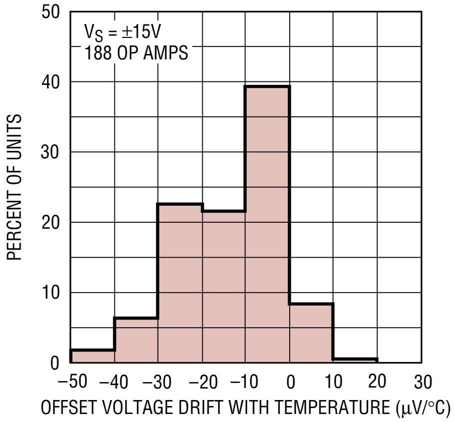
LT1169 • TPC17

Slew Rate and Gain-Bandwidth Product vs Temperature



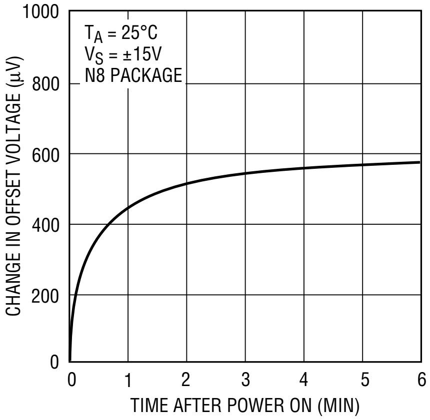
LT1169 • TPC18

Distribution of Offset Voltage Drift with Temperature



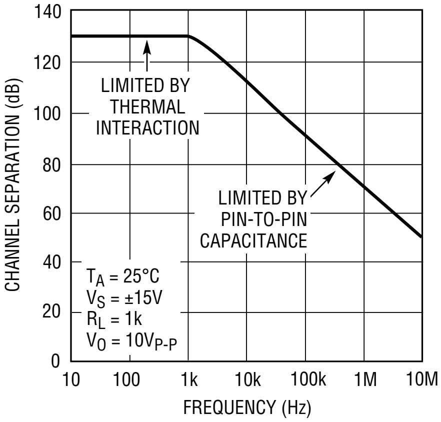
LT1169 • TPC19

Warm-Up Drift



LT1169 • TPC20

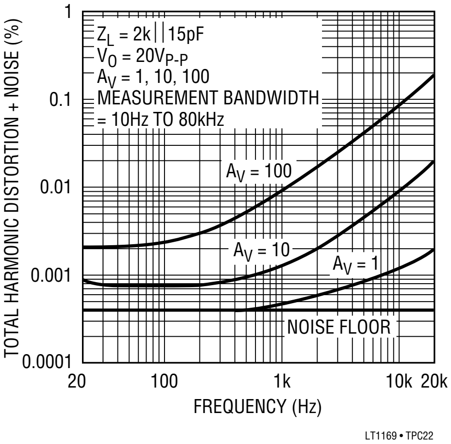
Channel Separation vs Frequency



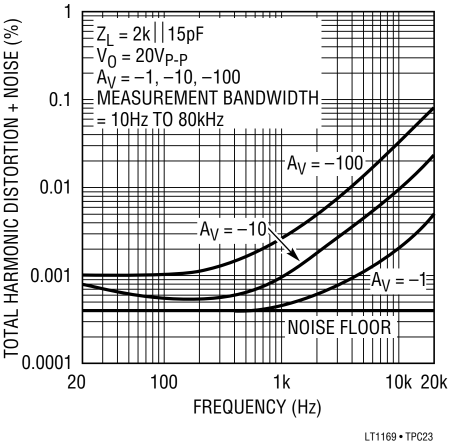
LT1169 • TPC21

TYPICAL PERFORMANCE CHARACTERISTICS

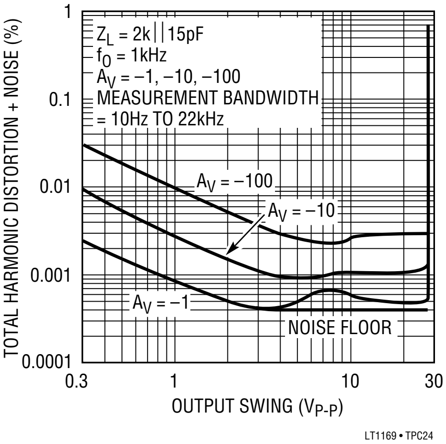
THD and Noise vs Frequency for Noninverting Gain



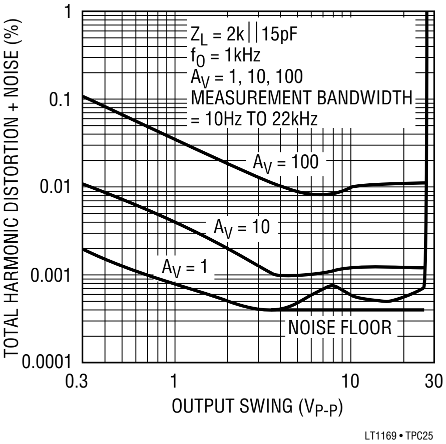
THD and Noise vs Frequency for Inverting Gain



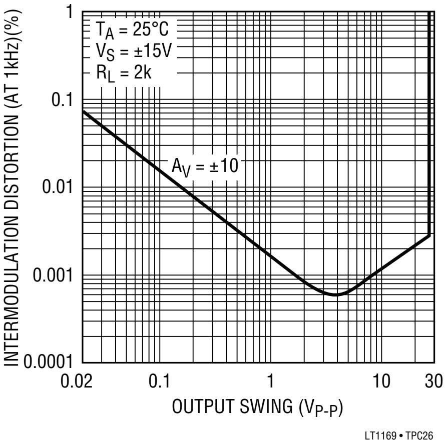
THD and Noise vs Output Amplitude for Inverting Gain



THD and Noise vs Output Amplitude for Noninverting Gain



CCIF IMD Test (Equal Amplitude Tones at 13kHz, 14kHz)*



* SEE LT1115 DATA SHEET FOR DEFINITION OF CCIF TESTING

APPLICATIONS INFORMATION

LT1169 vs the Competition

With improved noise performance, the LT1169 dual in the plastic DIP directly replaces such JFET op amps as the OPA2111, OPA2604, OP215, and the AD822. The combination of low current and voltage noise of the LT1169 allows it to surpass most dual and single JFET op amps. The LT1169 can replace many of the lowest noise bipolar amps that are used in amplifying low level signals from high impedance transducers. The best bipolar op amps will eventually lose out to the LT1169 when transducer impedance increases due to higher current noise.

The extremely high input impedance ($10^{13}\Omega$) assures that the input bias current is almost constant over the entire common mode range. Figure 1 shows how the LT1169 stands up to the competition. Unlike the competition, as the input voltage is swept across the entire common mode range the input bias current of the LT1169 hardly changes. As a result the current noise does not degrade. This makes the LT1169 the best choice in applications where an amplifier has to buffer signals from a high impedance transducer.

APPLICATIONS INFORMATION

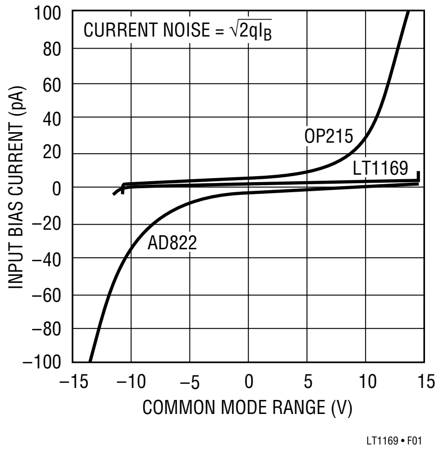
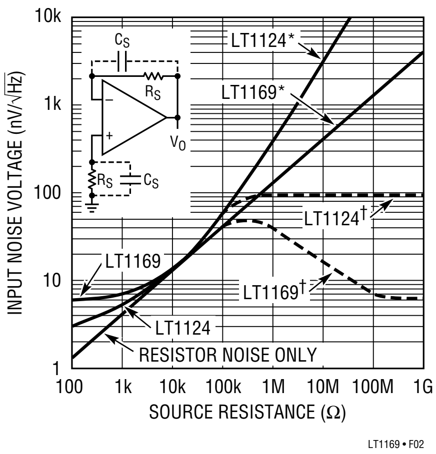


Figure 1. Comparison of LT1169, OP215, and AD822 Input Bias Current vs Common Mode Range

Amplifying Signals from High Impedance Transducers

The low voltage and current noise offered by the LT1169 makes it useful in a wide range of applications, especially where high impedance, capacitive transducers are used such as hydrophones, precision accelerometers, and photodiodes. The total output noise in such a system is the gain times the RMS sum of the op amp's input referred voltage noise, the thermal noise of the transducer, and the op amp's input bias current noise times the transducer impedance. Figure 2 shows total input voltage noise versus source resistance. In a low source resistance (<5k) application the op amp voltage noise will dominate the total noise. This means the LT1169 is superior to most dual JFET op amps. Only the lowest noise bipolar op amps have the advantage at low source resistances. As the source resistance increases from 5k to 50k, the LT1169 will match the best bipolar op amps for noise performance, since the thermal noise of the transducer (4kTR) begins to dominate the total noise. A further increase in source resistance, above 50k, is where the op amp's current noise component ($2qI_BR^2$) will eventually dominate the total noise. At these high source resistances, the LT1169 will out perform the lowest noise bipolar op amps due to the inherently low current noise of FET input op amps. Clearly, the LT1169 will extend the range of high impedance transducers that can be used for high signal-to-noise ratios. This makes the LT1169 the best choice for high impedance, capacitive transducers.



SOURCE RESISTANCE = $2R_S = R$
* PLUS RESISTOR
† PLUS RESISTOR || 1000pF CAPACITOR

$V_n = A_V\sqrt{V_{n(OP\ AMP)}^2 + 4kTR + 2qI_BR^2}$

Figure 2. Comparison of LT1169 and LT1124 Total Output 1kHz Voltage Noise vs Source Resistance

Optimization Techniques for Charge Amplifiers

The high input impedance JFET front end makes the LT1169 suitable in applications where very high charge sensitivity is required. Figure 3 illustrates the LT1169 in its inverting and noninverting modes of operation. A charge amplifier is shown in the inverting mode example; the gain depends on the principal of charge conservation at the input of the LT1169. The charge across the transducer capacitance C_S is transferred to the feedback capacitor C_F resulting in a change in voltage dV, which is equal to dQ/C_F. The gain therefore is $1 + C_F/C_S$. For unity-gain, the C_F should equal the transducer capacitance plus the input capacitance of the LT1169 and R_F should equal R_S.

In the noninverting mode example, the transducer current is converted to a change in voltage by the transducer capacitance, C_S. This voltage is then buffered by the LT1169 with a gain of 1 + R1/R2. A DC path is provided by R_S, which is either the transducer impedance or an external resistor. Since R_S is usually several orders of magnitude greater than the parallel combination of R1 and R2, R_B is added to balance the DC offset caused by the noninverting input bias current and R_S. The input bias currents, although small at room temperature, can create significant errors over increasing temperature, especially with transducer resistances of up to 1000MΩ or more. The optimum value for R_B is determined by equating the thermal noise ($4kTR_S$) to the current noise ($2qI_B$) times R_S^2. Solving for R_S results in $R_B = R_S = 2V_T/I_B$. A parallel

APPLICATIONS INFORMATION

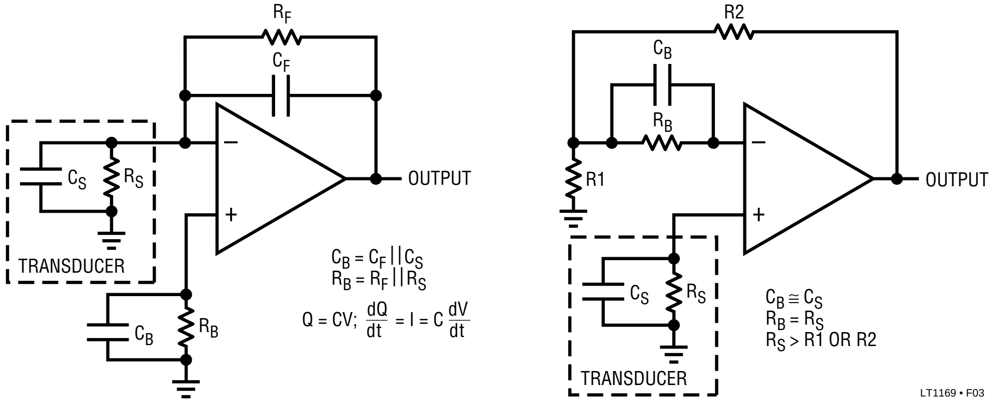
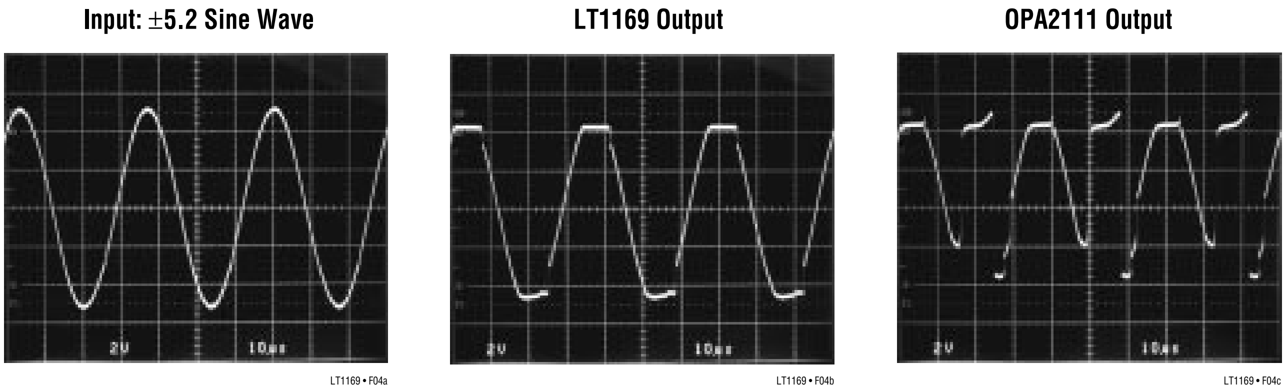


Figure 3. Inverting and Noninverting Gain Configurations



Input: ±5.2 Sine Wave

LT1169 Output

OPA2111 Output

Figure 4. Voltage Follower with Input Exceeding the Common Mode Range ($V_S = \pm5V$)

capacitor C_B, is used to cancel the phase shift caused by the op amp input capacitance and R_B.

Reduced Power Supply Operation

To take full advantage of a wide input common-mode range, the LT1169 was designed to eliminate phase reversal. Referring to the photographs in Figure 4, the LT1169 is shown operating in the follower mode ($A_V = 1$) at ±5V supplies with the input swinging ±5.2V. The output of the LT1169 clips cleanly and recovers with no phase reversal, unlike the competition as shown by the last photograph. This has the benefit of preventing lockup in servo systems and minimizing distortion components. The effect of input and output overdrive on one amplifier has no effect on the other, as each amplifier is biased independently.

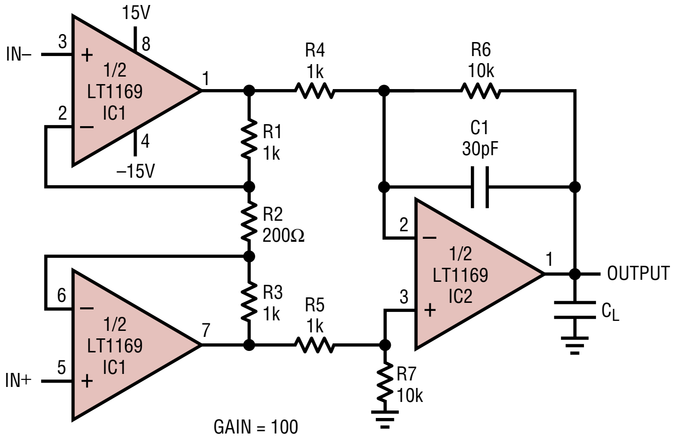
Advantages of Matched Dual Op Amps

In many applications the performance of a system depends on the matching between two operational amplifiers rather than the individual characteristics of the two op amps. Two or three op amp instrumentation amplifiers, tracking voltage references and low drift active filters are some of the circuits requiring matching between two op amps.

The well-known triple op amp configuration in Figure 5 illustrates these concepts. Output offset is a function of the difference between the two halves of the LT1169. This error cancellation principle holds for a considerable number of input referred parameters in addition to offset voltage and bias current. Input bias current will be the average of the two noninverting input currents (I_B^+). The difference between these two currents (ΔI_B^+) is the offset current of the instrumentation amplifier. Common-mode and power supply rejections will be dependent only on the match between the two amplifiers (assuming perfect resistor matching).

The concepts of common mode and power supply rejection ratio match (ΔCMRR and ΔPSRR) are best demonstrated with a numerical example:

APPLICATIONS INFORMATION



GAIN = 100
BANDWIDTH = 330kHz
INPUT REFERRED NOISE = 8.7nV/√Hz AT 1kHz
WIDEBAND NOISE DC TO 330kHz = $5.3\mu V_{RMS}$
$C_L \le 0.01\mu F$

Figure 5. Three Op Amp Instrumentation Amplifier

Assume $CMRR_A = 50\mu V/V$ or 86dB,
and $CMRR_B = 39\mu V/V$ or 88dB,
then $\Delta CMRR = 11\mu V/V$ or 99dB;
if $CMRR_B = -39\mu V/V$ which is still 88dB,
then $\Delta CMRR = 89\mu V/V$ or 81dB

By specifying and guaranteeing all of these matching parameters, the LT1169 can significantly improve the performance of matching-dependent circuits.

Typical performance of the instrumentation amplifier:

Input offset voltage = 0.8mV
Input bias current = 4pA
Input offset current = 3pA
Input resistance = $10^{13}\Omega$
Input noise = $3.4\mu V_{P-P}$

High Speed Operation

The low noise performance of the LT1169 was achieved by enlarging the input JFET differential pair to maximize the first stage gain. Enlarging the JFET geometry also increases the parasitic gate capacitance, which if left unchecked, can result in increased overshoot and ringing. When the feedback around the op amp is resistive (R_F), a pole will be created with R_F, the source resistance and capacitance (R_S,C_S), and the amplifier input capacitance (C_{IN} = 1.5pF). In closed-loop gain configurations with R_S and R_F in the MΩ range (Figure 6), this pole can create excess phase shift and even oscillation. A small capacitor (C_F) in parallel with R_F eliminates this problem. With $R_S(C_S + C_{IN}) = R_FC_F$, the effect of the feedback pole is completely removed.

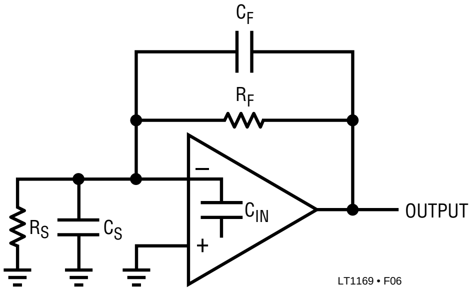
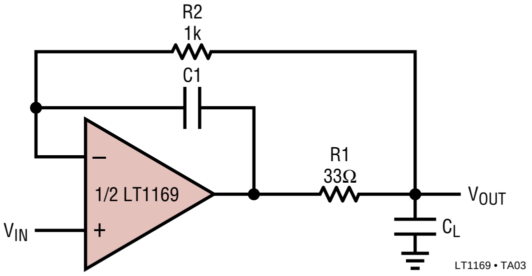


Figure 6

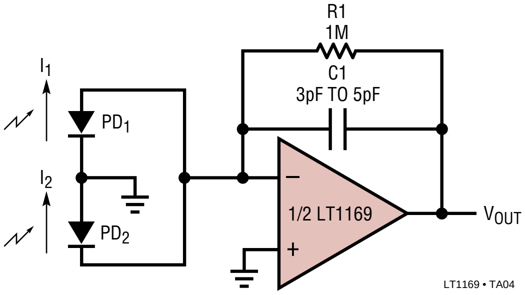
TYPICAL APPLICATIONS

Unity-Gain Buffer with Extended Load Capacitance Drive Capability



$C1 = C_L \le 0.1\mu F$
OUTPUT SHORT CIRCUIT CURRENT (~ 30mA) WILL LIMIT THE RATE
AT WHICH THE VOLTAGE CAN CHANGE ACROSS LARGE CAPACITORS
$(I = C\frac{dV}{dt})$

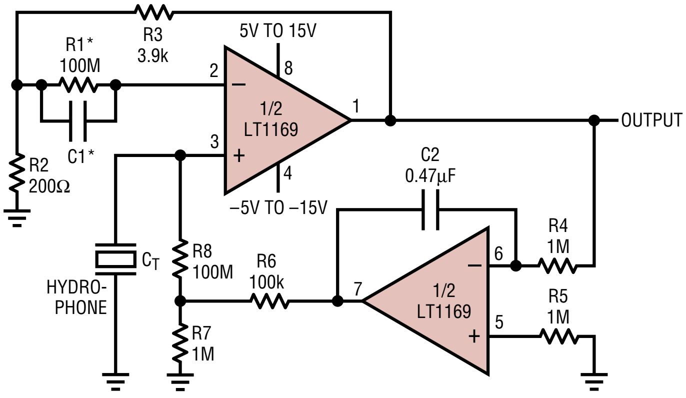
Light Balance Detection Circuit



$V_{OUT} = 1M \times (I_1 - I_2)$
PD_1, PD_2 = HAMAMATSU S1336-5BK
WHEN EQUAL LIGHT ENTERS PHOTODIODES, V_{OUT} < 3mV.

TYPICAL APPLICATIONS

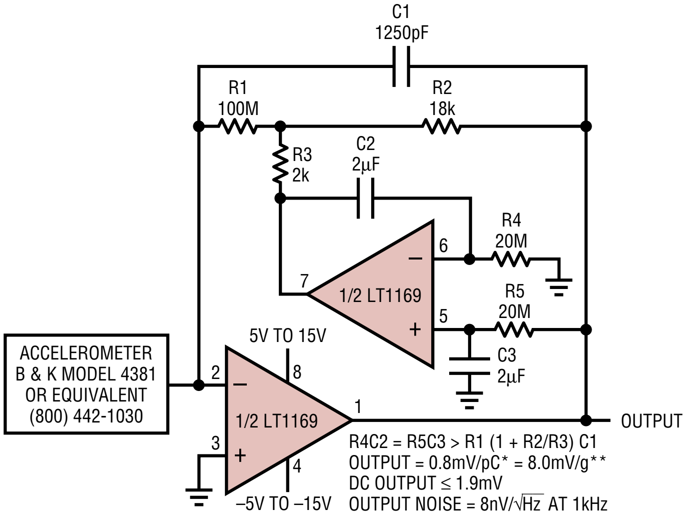
Low Noise Hydrophone Amplifier with DC Servo



DC OUTPUT ≤ 2.5mV FOR $T_A < 70°C$
OUTPUT VOLTAGE NOISE = $128nV/\sqrt{Hz}$ AT 1kHz (GAIN = 20)
C1 ≈ C_T ≈ 100pF TO 5000pF; R4C2 > $R8C_T$; *OPTIONAL

LT1169 • TA05

Accelerometer Amplifier with DC Servo



R4C2 = R5C3 > R1 (1 + R2/R3) C1
OUTPUT = 0.8mV/pC* = 8.0mV/g**
DC OUTPUT ≤ 1.9mV
OUTPUT NOISE = $8nV/\sqrt{Hz}$ AT 1kHz

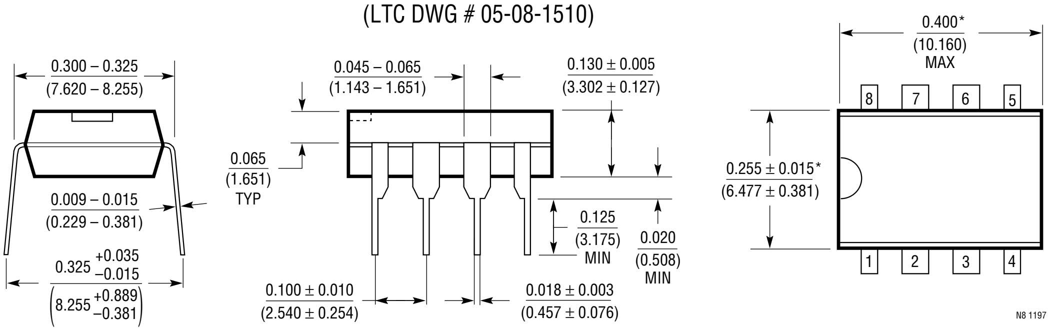
*PICOCOULOMBS
**g = EARTH'S GRAVITATIONAL CONSTANT

LT1169 • TA07

PACKAGE DESCRIPTION

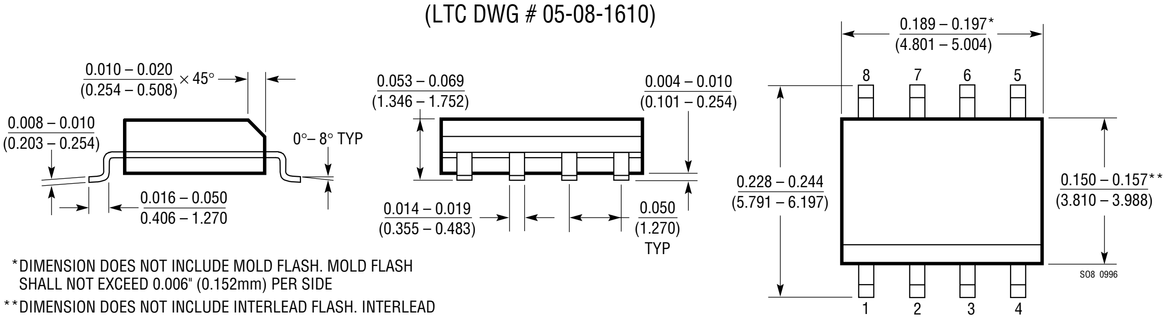
Dimensions in inches (millimeters) unless otherwise noted.

N8 Package
8-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

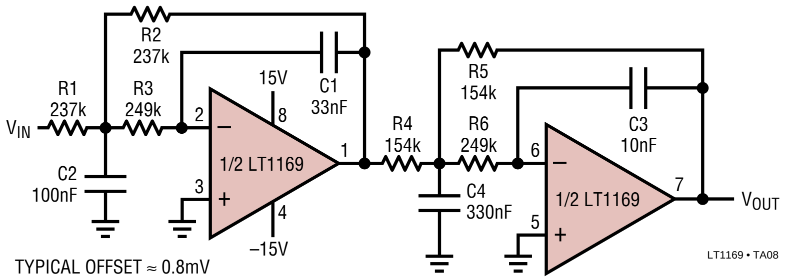
S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH
SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE
**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD
FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

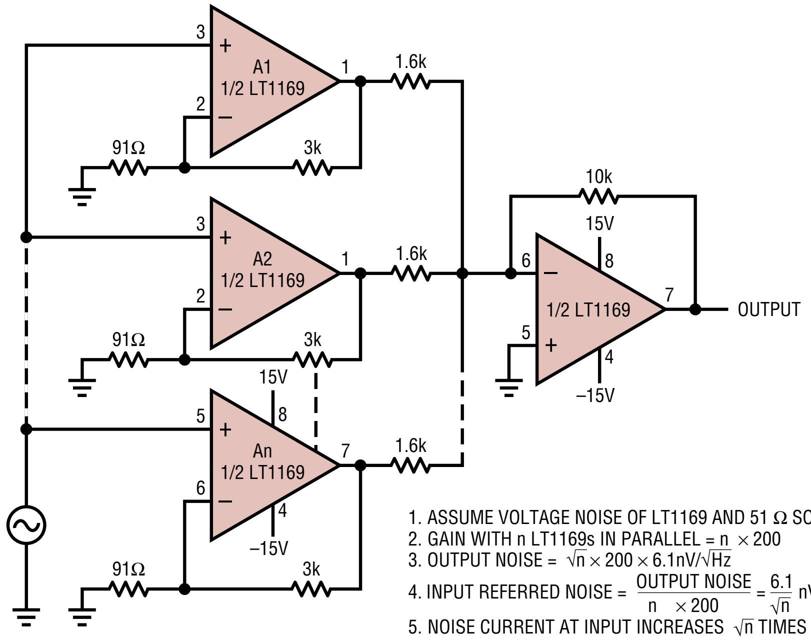
TYPICAL APPLICATIONS

10Hz Fourth Order Chebyshev Lowpass Filter (0.01dB Ripple)



TYPICAL OFFSET ≈ 0.8mV
1% TOLERANCES
FOR $V_{IN} = 10V_{P\text{-}P}$, $V_{OUT} = -121\text{dB AT } f > 330\text{Hz}$
$= -6\text{dB AT } f = 16.3\text{Hz}$
LOWER RESISTOR VALUES WILL RESULT IN LOWER THERMAL NOISE AND LARGER CAPACITORS

Paralleling Amplifiers to Reduce Voltage Noise



1. ASSUME VOLTAGE NOISE OF LT1169 AND 51 Ω SOURCE RESISTOR = $6.1\text{nV}/\sqrt{\text{Hz}}$
2. GAIN WITH n LT1169s IN PARALLEL = $n \times 200$
3. OUTPUT NOISE = $\sqrt{n} \times 200 \times 6.1\text{nV}/\sqrt{\text{Hz}}$
4. INPUT REFERRED NOISE = $\dfrac{\text{OUTPUT NOISE}}{n \times 200} = \dfrac{6.1}{\sqrt{n}}\ \text{nV}/\sqrt{\text{Hz}}$
5. NOISE CURRENT AT INPUT INCREASES $\sqrt{n}$ TIMES
6. IF n = 5, GAIN = 1000, BANDWIDTH = 110kHz, RMS NOISE, DC TO 1MHz = $\dfrac{2.1\mu V}{\sqrt{5}} = 1.0\mu V$

LT1169 • TA06

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1113	Lowest Noise Dual JFET Op Amp	$4.5\text{nV}/\sqrt{\text{Hz}}$ Voltage Noise
LT1462	Micro Power Dual JFET Op Amp	3.0pA I_B, 45μA I_{SUPPLY}
LT1464	Low Power Dual JFET Op Amp	3.0pA (Max) Input Bias Current

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417 • (408) 432-1900
FAX: (408) 434-0507 • TELEX: 499-3977 • www.linear-tech.com

Стандарт
Электрон
Связь

Мы молодая и активно развивающаяся компания в области поставок электронных компонентов. Мы поставляем электронные компоненты отечественного и импортного производства напрямую от производителей и с крупнейших складов мира.

Благодаря сотрудничеству с мировыми поставщиками мы осуществляем комплексные и плановые поставки широчайшего спектра электронных компонентов.

Собственная эффективная логистика и склад в обеспечивает надежную поставку продукции в точно указанные сроки по всей России.

Мы осуществляем техническую поддержку нашим клиентам и предпродажную проверку качества продукции. На все поставляемые продукты мы предоставляем гарантию .

Осуществляем поставки продукции под контролем ВП МО РФ на предприятия военно-промышленного комплекса России , а также работаем в рамках 275 ФЗ с открытием отдельных счетов в уполномоченном банке. Система менеджмента качества компании соответствует требованиям ГОСТ ISO 9001.

Минимальные сроки поставки, гибкие цены, неограниченный ассортимент и индивидуальный подход к клиентам являются основой для выстраивания долгосрочного и эффективного сотрудничества с предприятиями радиоэлектронной промышленности, предприятиями ВПК и научно-исследовательскими институтами России.

С нами вы становитесь еще успешнее!

Наши контакты:

Телефон: +7 812 627 14 35

Электронная почта: sales@st-electron.ru

Адрес: 198099, Санкт-Петербург,
Промышленная ул, дом № 19, литера Н,
помещение 100-Н Офис 331