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February 1997 Revised August 2004

NC7ST86

TinyLogic® HST 2-Input Exclusive-OR Gate

General Description

The NC7ST86 is a single 2-Input high performance CMOS Exclusive-OR Gate, with TTL-compatible inputs. Advanced Silicon Gate CMOS fabrication assures high speed and low power circuit operation. ESD protection diodes inherently guard both inputs and outputs with respect to the $\rm V_{CC}$ and GND rails. High gain circuitry offers high noise immunity and reduced sensitivity to input edge rate. The TTL-compatible inputs facilitate TTL to NMOS/CMOS interfacing. Device performance is similar to MM74HCT but with ½ the output current drive of HC/HCT.

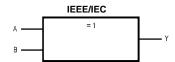
Features

- Space saving SOT23 or SC70 5-lead package
- Ultra small MicroPak™ leadless package
- High Speed; t_{PD} <8 ns typ, V_{CC} = 5V, C_L = 15 pF
- \blacksquare Low Quiescent Power; I_{CC} <1 μA typ, V_{CC} = 5.5V
- Balanced Output Drive; 2 mA I_{OL}, -2 mA I_{OH}
- TTL-compatible inputs

Ordering Code:

Order Number	Package Number	Product Code Top Mark	Package Description	Supplied As	
NC7ST86M5X	MA05B	8S86	5-Lead SOT23, JEDEC MO-178, 1.6mm	3k Units on Tape and Reel	
NC7ST86P5X	MAA05A	T86	5-Lead SC70, EIAJ SC-88a, 1.25mm Wide	3k Units on Tape and Reel	
NC7ST86L6X	MAC06A	D6	6-Lead MicroPak, 1.0mm Wide	5k Units on Tape and Reel	

Logic Symbol



Pin Descriptions

Pin Names	Descriptions
A, B	Input
Y	Output
NC	No Connect

Function Table

$$\mathbf{Y} = \mathbf{A} \oplus \mathbf{B}$$

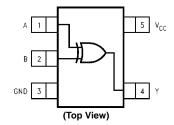
Inp	Output				
Α	A B				
L	L	L			
L	Н	Н			
Н	L	Н			
Н	Н	L			

H = HIGH Logic Level L = LOW Logic Level

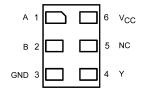
 $\label{eq:total_cond} \mbox{TinyLogio} \mbox{\mathbb{B} is a registered trademark of Fairchild Semiconductor Corporation.} \\ \mbox{MicroPak}^{\mbox{\mathbb{M}}} \mbox{\mathbb{M} is a trademark of Fairchild Semiconductor Corporation.} \\$

Connection Diagrams

Pin Assignments for SOT23 and SC70



Pad Assignments for MicroPak



(Top Thru View)

Absolute Maximum Ratings(Note 1)

-0.5V to +7.0V Supply Voltage (V_{CC}) DC Input Diode Current (I_{IK})

 $V_{IN} < -0.5V$ -20 mA $V_{IN} \ge V_{CC} + 0.5V$ +20 mA

DC Input Voltage (V_{IN}) -0.5V to V_{CC} +0.5V

DC Output Diode Current (I_{OK})

 $V_{OUT} < -0.5V$ -20 mA $V_{OUT} > V_{CC} + 0.5V$ +20 mA

Output Voltage (V_{OUT}) -0.5V to V_{CC} +0.5V

DC Output Source or Sink

Current (I_{OUT}) ±12.5 mA

DC V_{CC} or Ground Current per

Supply Pin (I $_{\rm CC}$ or I $_{\rm GND}$) ±25 mA

-65°C to +150°C Storage Temperature (T_{STG})

Junction Temperature (T_J) 150°C

Lead Temperature (T_L);

(Soldering, 10 seconds) 260°C

Power Dissipation (PD) @+85°C

SOT23-5 200 mW

SC70-5 150 mW

Recommended Operating Conditions (Note 2)

Supply Voltage 4.5V to 5.5V Input Voltage (V_{IN}) 0V to V_{CC} Output Voltage (V_{OUT}) 0V to V_{CC}

Operating Temperature (T_A) -40°C to +85°C

Input Rise and Fall Time (t_r, t_f)

 $V_{CC} = 5.0V$ 0 to 500 ns

Thermal Resistance (θ_{JA})

SOT23-5 300°C/W

SC70-5 425°C/W

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of circuits outside the databook specifica-

Note 2: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

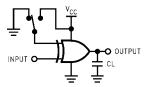
Symbol	Parameter	V _{CC}	**		$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$		Units	Conditions	
Cyllibol	i didilicici	(V)			Max	Min Max		Oille	Conditions
V _{IH}	HIGH Level Input Voltage	4.5–5.5	2.0			2.0		V	
V _{IL} LOW Level Input Voltage		4.5-5.5			8.0		0.8	V	
V _{OH}	HIGH Level Output Voltage	4.5	4.4	4.5		4.4		V	$I_{OH} = -20 \mu A$, $V_{IN} = V_{IL}$,
		4.5	4.18	4.35		4.13		V	$V_{IH} I_{OH} = -2 \text{ mA}$
V _{OL}	LOW Level Output Voltage	4.5		0	0.1		0.1	V	$I_{OL}=20~\mu\text{A},~V_{IN}=V_{IL},$
		4.5		0.10	0.26		0.33	V	$V_{IH} I_{OL} = 2 \text{ mA}$
I _{IN}	Input Leakage Current	5.5			±0.1		±1.0	μΑ	$0 \le V_{IN} \le 5.5V$
I _{CC}	Quiescent Supply Current	5.5			1.0		10.0	μΑ	$V_{IN} = V_{CC}$ or GND
I _{CCT} I _{CC} per Input		5.5			2.0		2.9	mA	One Input $V_{IN} = 0.5V$ or 2.4V,
									Other Input V _{CC} or GND

AC Electrical Characteristics

Symbol	Parameter	v _{cc}	$T_A = +25$ °C		$T_A = -40^{\circ}C$ to $+85^{\circ}C$		Units	Conditions	Figure	
Cynnbon		(V)	Min	Тур	Max	Min	Max	Units	Conditions	Number
t _{PLH} ,	Propagation Delay	5.0		4.4	14			ns	C _L = 15 pF	Figures 1, 3
t _{PHL}		5.0		7.4	19					
		4.5		6.6	18		22	ns	C _L = 50 pF	
				13.1	29		33			
		5.5		5.6	16		20			
				12.5	28		32			
t _{TLH} ,	Output Transition Time	5.0		4	10			ns	C _L = 15 pF	
t_{THL}		4.5		11	25		31	ns	C ₁ = 50 pF	Figures 1, 3
		5.5		10	21		26	113	OL = 30 pi	, -
C _{IN}	Input Capacitance	Open		2	10			pF		
C _{PD}	Power Dissipation Capacitance	5.0		8				pF	(Note 3)	Figure 2

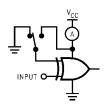
Note 3: C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption I_{CCD}) at no output loading and operating at 50% duty cycle. (See Figure 2.) C_{PD} is related to I_{CCD} dynamic operating current by expression: $I_{CCD} = (C_{PD}) (V_{CC}) (f_{|N}) + (I_{CC} \text{ static}).$

AC Loading and Waveforms



 C_L includes load and stray capacitance Input PRR = 1.0 MHz, t_W = 500 ns

FIGURE 1. AC Test Circuit



Input = AC Waveforms; PRR = Variable; Duty Cycle = 50%

FIGURE 2. I_{CCD} Test Circuit

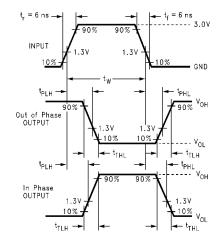
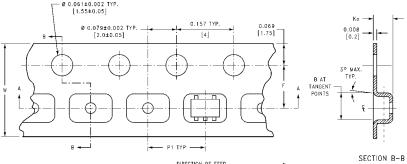


FIGURE 3. AC Waveforms

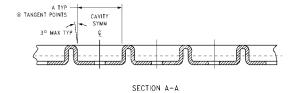
Tape and Reel Specification TAPE FORMAT for SOT23 and SC70

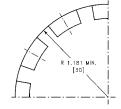
	50 120 and 507 0				
Package	Таре	Number	Cavity	Cover Tape	
Designator	Section	Cavities	Status	Status	
	Leader (Start End)	125 (typ)	Empty	Sealed	
M5X, P5X	Carrier	3000	Filled	Sealed	
	Trailer (Hub End)	75 (typ)	Empty	Sealed	

TAPE DIMENSIONS inches (millimeters)



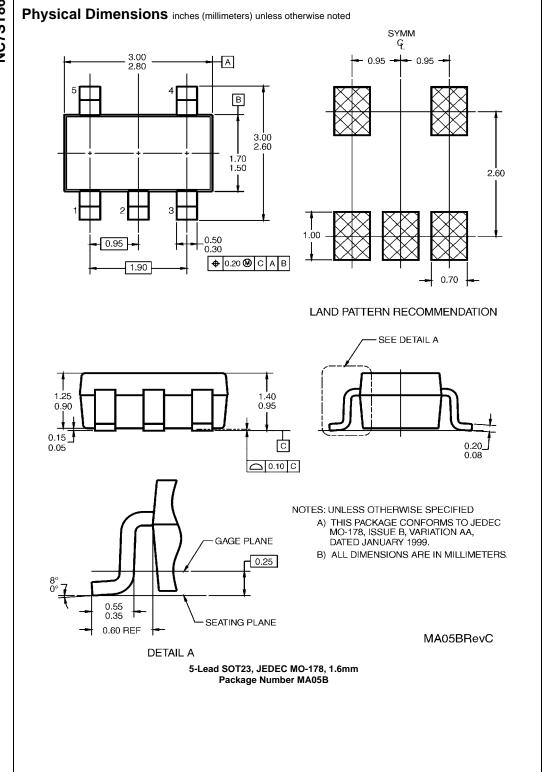
DIRECTION OF FEED

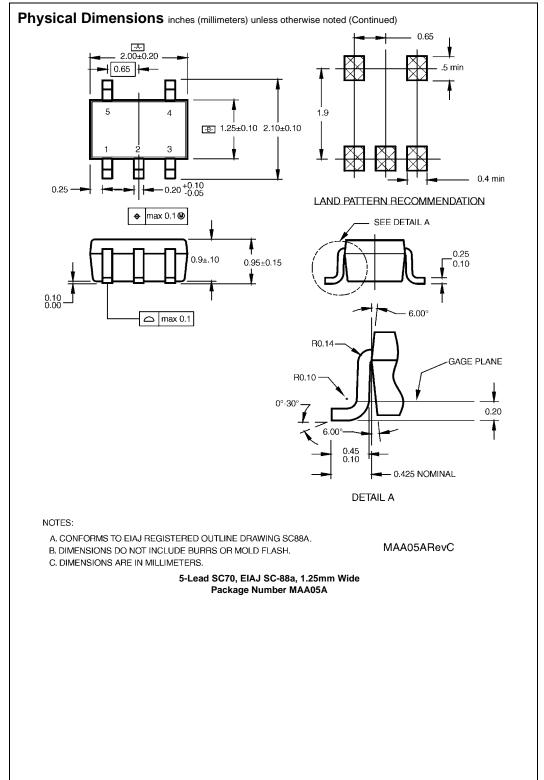




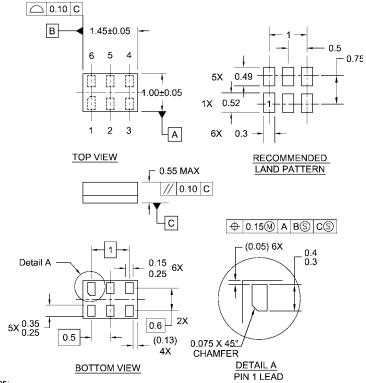
				BEND RADIUS NOT TO SCALE					
Package	Tape Size	DIM A	DIM B	DIM F	DIM K _o	DIM P1	DIM W		
SC70-5	8 mm	0.093	0.096	0.138 ± 0.004	0.053 ± 0.004	0.157	0.315 ± 0.004		
		(2.35)	(2.45)	(3.5 ± 0.10)	(1.35 ± 0.10)	(4)	(8 ± 0.1)		
SOT23-5	8 mm	0.130	0.130	0.138 ± 0.002	0.055 ± 0.004	0.157	0.315 ± 0.012		
		(3.3)	(3.3)	(3.5 ± 0.05)	(1.4 + 0.11)	(4)	(8 + 0.3)		

Tape and Reel Specification (Continued) TAPE FORMAT for MicroPak Package Tape Number Cavity Cover Tape Designator Section Cavities Status Status Leader (Start End) 125 (typ) Empty Sealed L6X Carrier 5000 Filled Sealed Trailer (Hub End) 75 (typ) **Empty** Sealed 2.00-1.75±0.10 В 8.00 ^{+0.30} -0.10 3.50±0.05 1.15±0.05 **-** → В◄ -ø 0.50 ±0.05 SECTION B-B DIRECTION OF FEED SCALE:10X 0.254±0.020 Г 0.70±0.05 SECTION A-A SCALE:10X **REEL DIMENSIONS** inches (millimeters) TAPE SLOT DETAIL X DETAIL X SCALE: 3X W1 W2 W3 Tape В С D Ν Α Size 0.331 + 0.059/-0.000 0.567 W1 + 0.078/-0.039 7.0 0.059 0.512 0.795 2.165 8 mm (177.8)(1.50)(13.00)(20.20)(55.00)(8.40 + 1.50 / -0.00)(W1 + 2.00/-1.00)(14.40)





Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Notes:

- 1. JEDEC PACKAGE REGISTRATION IS ANTICIPATED 2. DIMENSIONS ARE IN MILLIMETERS
- 3. DRAWING CONFORMS TO ASME Y14.5M-1994

MAC06ARevB

6-Lead MicroPak, 1.0mm Wide Package Number MAC06A

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