74LV393-Q100

Dual 4-bit binary ripple counter

Rev. 2 — 17 September 2014 **Product data sheet**

1. General description

The 74LV393-Q100 is a low–voltage Si-gate CMOS device and is pin and function compatible with 74HC393-Q100 and 74HCT393-Q100.

The 74LV393-Q100 is a dual 4-stage binary ripple counter. Each counter features a clock input ($n\overline{CP}$), an overriding asynchronous master reset input (nMR) and 4 buffered parallel outputs (nQ0 to nQ3). The counter advances on the HIGH-to-LOW transition of $n\overline{CP}$. A HIGH on nMR clears the counter stages and forces the outputs LOW, independent of the state of $n\overline{CP}$.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from –40 °C to +85 °C and from –40 °C to +125 °C
- Optimized for low voltage applications: 1.0 V to 3.6 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Typical V_{OLP} (output ground bounce) 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25 °C
- Typical V_{OHV} (output V_{OH} undershoot) 2 V at V_{CC} = 3.3 V, T_{amb} = 25 °C
- Two 4-bit binary counters with individual clocks
- Divide-by any binary module up to 28 in one package
- Two master resets to clear each 4-bit counter individually
- Complies with JEDEC standard no. 7A
- ESD protection:
  - MIL-STD-883, method 3015 exceeds 2000 V
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V (C = 200 pF, R = 0 Ω)

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	**Name**	**Description**	**Version**
74LV393D-Q100	–40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74LV393PW-Q100	–40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1

4. Functional diagram

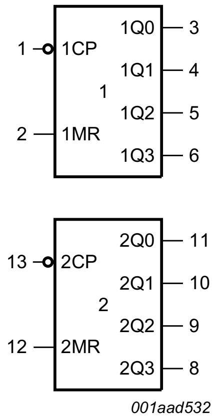


Fig 1. Logic symbol

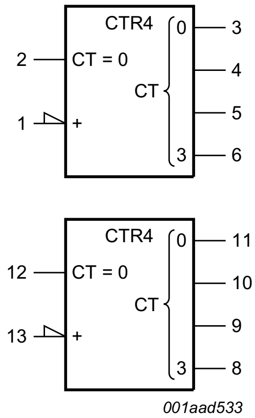


Fig 2. IEC logic symbol

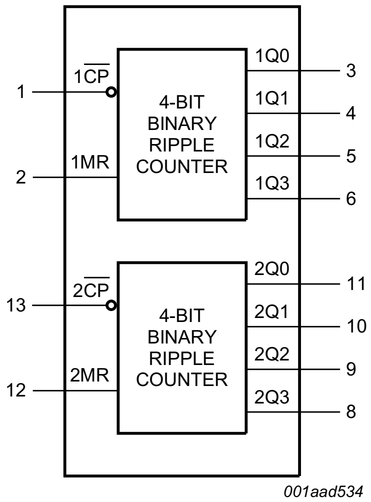


Fig 3. Functional diagram

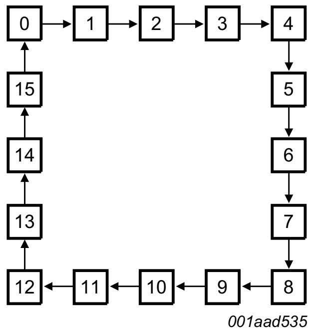


Fig 4. State diagram

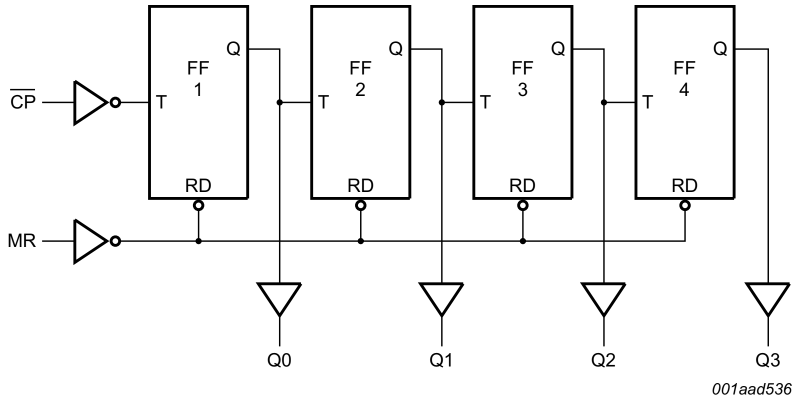


Fig 5. Logic diagram (one counter)

5. Pinning information

5.1 Pinning

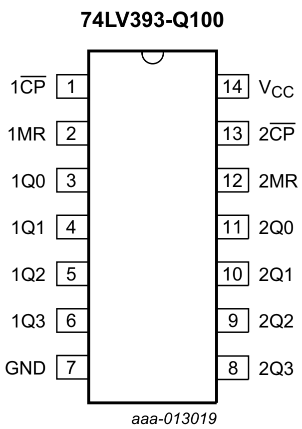


Fig 6. Pin configuration SO14

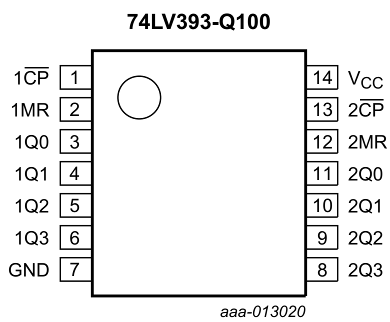


Fig 7. Pin configuration TSSOP14

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1$\overline{CP}$	1	clock input (HIGH-to-LOW, edge-triggered)
1MR	2	asynchronous master reset input (active HIGH)
1Q0	3	flip-flop output
1Q1	4	flip-flop output
1Q2	5	flip-flop output
1Q3	6	flip-flop output
GND	7	ground (0 V)
2Q3	8	flip-flop output
2Q2	9	flip-flop output
2Q1	10	flip-flop output
2Q0	11	flip-flop output
2MR	12	asynchronous master reset input (active HIGH)
2$\overline{CP}$	13	clock input (HIGH-to-LOW, edge-triggered)
V_{CC}	14	supply voltage

6. Functional description

Table 3. Count sequence for one counter [1]

Count	Output			
	nQ0	nQ1	nQ2	nQ3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

[1] H = HIGH voltage level; L = LOW voltage level.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		–0.5	+4.6	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	-	±50	mA
I_O	output current	$V_O = -0.5$ V to $V_{CC} + 0.5$ V	-	±25	mA
I_{CC}	supply current		-	+50	mA
I_{GND}	ground current		–50	-	mA
T_{stg}	storage temperature		–65	+150	°C
P_{tot}	total power dissipation	SO14 package [1]	-	500	mW
		TSSOP14 packages [2]	-	400	mW

[1] For SO14 package: P_{tot} derates linearly with 8 mW/K above 70 °C.

[2] For TSSOP14 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.0	3.3	3.6	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		–40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 1.0 V to 2.0 V	-	-	500	ns/V
		V_{CC} = 2.0 V to 2.7 V	-	-	200	ns/V
		V_{CC} = 2.7 V to 3.6 V	-	-	100	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 1.2 V	0.9	-	-	0.9	-	V
		V_{CC} = 2.0 V	1.4	-	-	1.4	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.2 V	-	-	0.3	-	0.3	V
		V_{CC} = 2.0 V	-	-	0.6	-	0.6	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}						
		I_O = –100 μA; V_{CC} = 1.2 V	-	1.2	-	-	-	V
		I_O = –100 μA; V_{CC} = 2.0 V	1.8	2.0	-	1.8	-	V
		I_O = –100 μA; V_{CC} = 2.7 V	2.5	2.7	-	2.5	-	V
		I_O = –100 μA; V_{CC} = 3.0 V	2.80	3.0	-	2.8	-	V
		I_O = –6 mA; V_{CC} = 3.0 V	2.40	2.82	-	2.20	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}						
		I_O = 100 μA; V_{CC} = 1.2 V	-	0	-	-	-	V
		I_O = 100 μA; V_{CC} = 2.0 V	-	0	0.2	-	0.2	V
		I_O = 100 μA; V_{CC} = 2.7 V	-	0	0.2	-	0.2	V
		I_O = 100 μA; V_{CC} = 3.0 V	-	0	0.2	-	0.2	V
		I_O = 6 mA; V_{CC} = 3.0 V	-	0.25	0.40	-	0.50	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 3.6 V	-	-	1.0	-	1.0	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 3.6 V	-	-	20.0	-	160	μA
ΔI_{CC}	additional supply current	quiescent per input $V_I = V_{CC} - 0.6$ V; V_{CC} = 2.7 V to 3.6 V	-	-	500	-	850	μA
C_I	input capacitance		-	3.5	-	-	-	pF

[1] All typical values are measured at T_{amb} = 25 °C.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit, see Figure 10.

Symbol	Parameter	Conditions		–40 °C to +85 °C			–40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	
t_{pd}	propagation delay	$n\overline{CP}$ to nQ0; see Figure 8	[3]						
		V_{CC} = 1.2 V		-	75	-	-	-	ns
		V_{CC} = 2.0 V		-	26	49	-	60	ns
		V_{CC} = 2.7 V		-	19	36	-	44	ns
		V_{CC} = 3.3 V, C_L = 15 pF		-	12	-	-	-	ns
		V_{CC} = 3.0 V to 3.6 V		-	14	29	-	35	ns
		nQ to nQn+1; see Figure 8	[3]						
		V_{CC} = 1.2 V		-	25	-	-	-	ns
		V_{CC} = 2.0 V		-	9	17	-	20	ns
		V_{CC} = 2.7 V		-	6	13	-	15	ns
		V_{CC} = 3.3 V, C_L = 15 pF		-	4	-	-	-	ns
		V_{CC} = 3.0 V to 3.6 V		-	5[2]	10	-	12	ns
t_{PHL}	HIGH to LOW propagation delay	nMR to nQx; see Figure 9							
		V_{CC} = 1.2 V		-	70	-	-	-	ns
		V_{CC} = 2.0 V		-	24	44	-	54	ns
		V_{CC} = 2.7 V		-	18	33	-	40	ns
		V_{CC} = 3.3 V, C_L = 15 pF		-	11	-	-	-	ns
		V_{CC} = 3.0 V to 3.6 V		-	13[2]	26	-	32	ns
t_t	transition time	nQx; see Figure 8	[4]						
		V_{CC} = 2.0 V		-	-	-	-	-	ns
		V_{CC} = 2.7 V		-	-	-	-	-	ns
		V_{CC} = 3.0 V to 3.6 V		-	-	-	-	-	ns
t_W	pulse width	$n\overline{CP}$ HIGH or LOW; see Figure 8							
		V_{CC} = 2.0 V		34	10	-	41	-	ns
		V_{CC} = 2.7 V		25	8	-	30	-	ns
		V_{CC} = 3.0 V to 3.6 V		20	6[2]	-	24	-	ns
		nMR HIGH; see Figure 9							
		V_{CC} = 2.0 V		34	12	-	41	-	ns
		V_{CC} = 2.7 V		25	9	-	30	-	ns
		V_{CC} = 3.0 V to 3.6 V		20	7[2]	-	24	-	ns
t_{rec}	recovery time	nMR to $n\overline{CP}$; see Figure 9							
		V_{CC} = 1.2 V		-	5	-	-	-	ns
		V_{CC} = 2.0 V		5	2	-	5	-	ns
		V_{CC} = 2.7 V		5	2	-	5	-	ns
		V_{CC} = 3.0 V to 3.6 V		5	1[2]	-	5	-	ns

Table 7. Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit, see Figure 10.

Symbol	Parameter	Conditions		−40 °C to +85 °C			−40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	
f_{max}	maximum frequency	see Figure 8							
		V_{CC} = 2.0 V		14	53	-	12	-	MHz
		V_{CC} = 2.7 V		19	72	-	16	-	MHz
		V_{CC} = 3.3 V, C_L = 15 pF		-	99	-	-	-	MHz
		V_{CC} = 3.0 V to 3.6 V		24	90[2]	-	20	-	MHz
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC}	[5]	-	23[2]	-	-	-	pF

[1] All typical values are measured at T_{amb} = 25 °C.

[2] Typical values are measured at V_{CC} = 3.3 V.

[3] t_{pd} is the same as t_{PLH} and t_{PHL}.

[4] t_t is the same as t_{THL} and t_{TLH}.

[5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

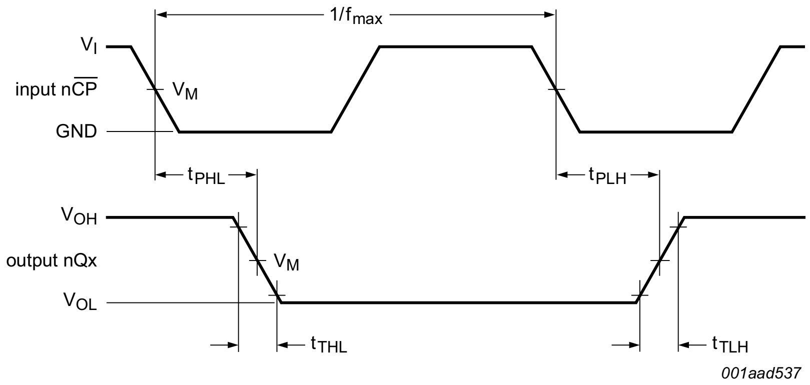
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

10.1 Waveforms



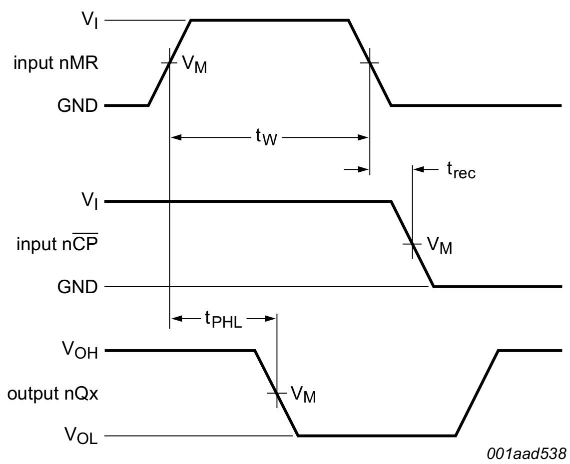
t_{TLH} = 10 % and t_{THL} = 90 %,

Measurement points are given in Table 8.

Fig 8. Propagation delays clock (nCP) to output (nQx), output transition times and maximum clock frequency

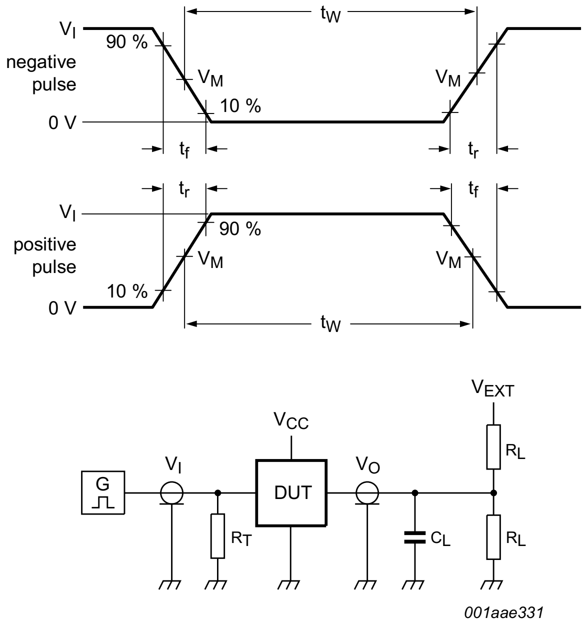
Table 8. Measurement points

Supply voltage V_{CC}	Input	Output		
	V_M	V_M	V_X	V_Y
< 2.7 V	$0.5V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.1V_{CC}$	$V_{OH} - 0.1V_{CC}$
2.7 V to 3.6 V	$1.5V_{CC}$	$1.5V_{CC}$	$V_{OL} + 0.3V_{CC}$	$V_{OH} - 0.3V_{CC}$



Measurement points are given in Table 8.

Fig 9. Propagation delays clock (nCP) to output (nQx), pulse width master reset (nMR), and recovery time master reset (nMR) to clock (nCP)



Test data is given in Table 9.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

S1 = Test selection switch.

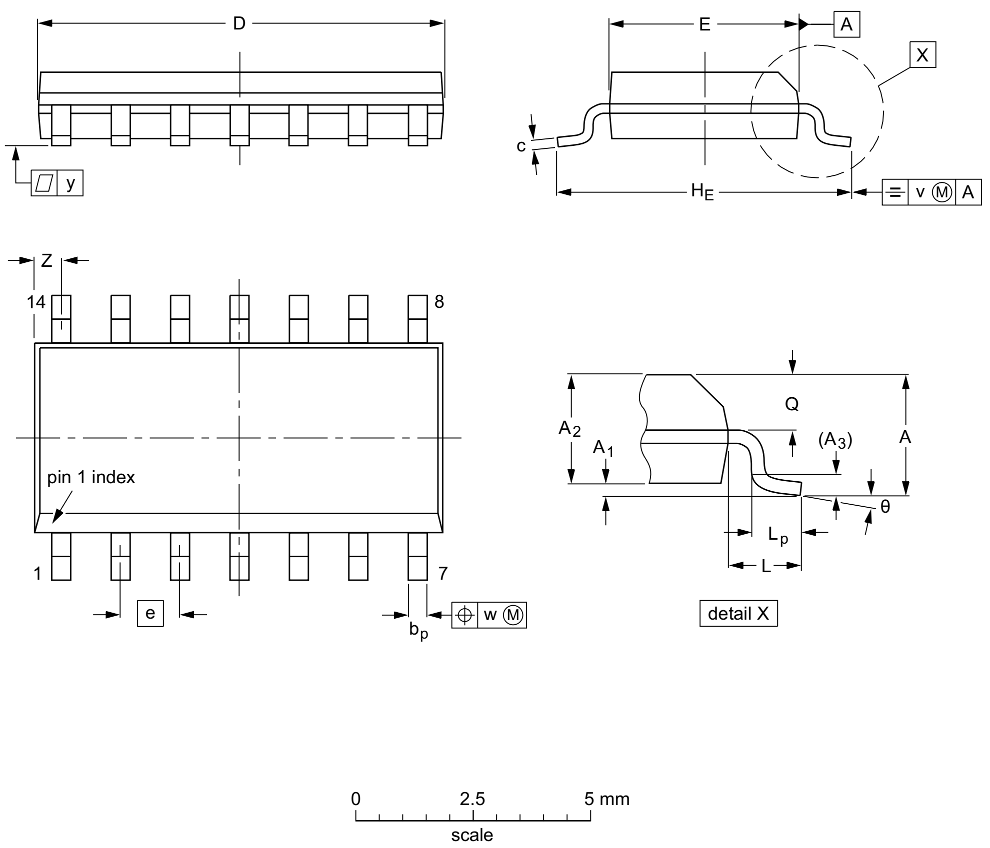
Fig 10. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V_{EXT}
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}
< 2.7 V	V_{CC}	≤ 2.5 ns	50 pF	1 kΩ	open
2.7 V to 3.6 V	2.7 V	≤ 2.5 ns	15 pF, 50 pF	1 kΩ	open

11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

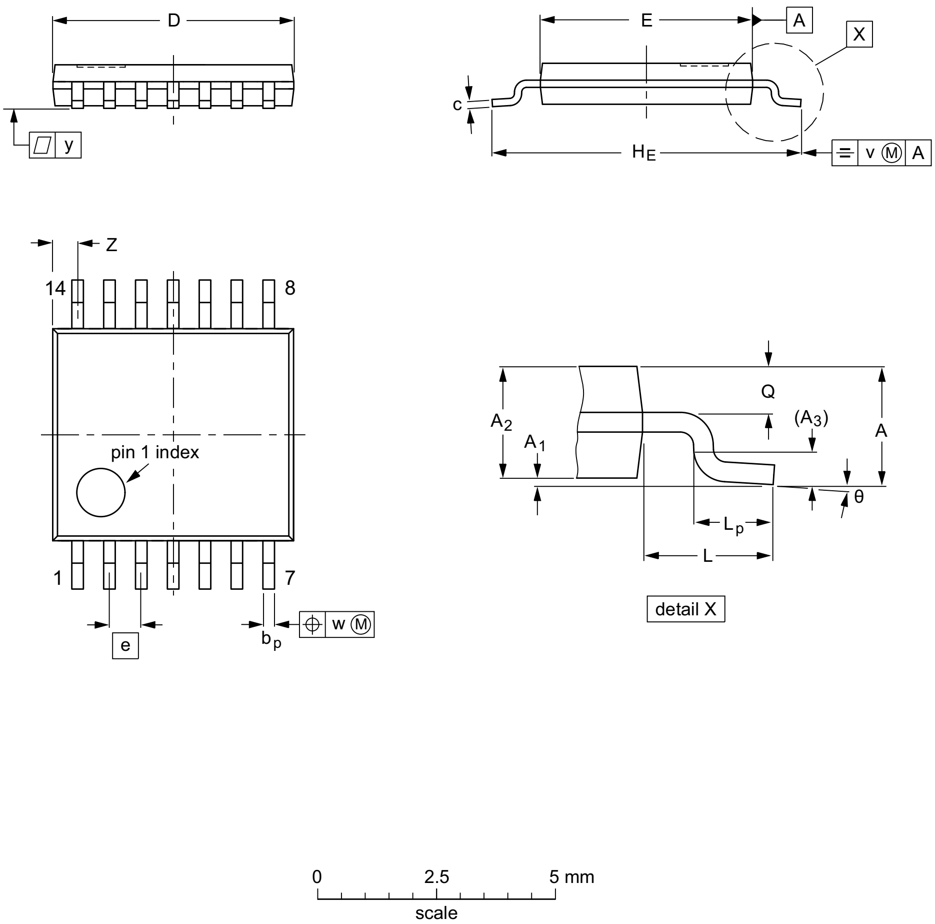
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

Fig 11. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

Fig 12. Package outline SOT402-1 (TSSOP14)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MIL	Military
MM	Machine Model

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LV393_Q100 v.2	20140917	Product data sheet	-	74LV393_Q100 v.1
Modifications:	• Figure 10 and Table 9 updated because of a missing load resistance in the test circuit.			
74LV393_Q100 v.1	20140526	Product data sheet	-	-

14. Legal information

14.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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16. Contents

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Стандарт
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