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June 2014 FDMC7672

N-Channel Power Trench[®] MOSFET 30 V, 16.9 A, 5.7 m Ω

Features

- Max $r_{DS(on)} = 5.7 \text{ m}\Omega$ at $V_{GS} = 10 \text{ V}$, $I_D = 16.9 \text{ A}$
- Max $r_{DS(on)} = 7.0 \text{ m}\Omega$ at $V_{GS} = 4.5 \text{ V}$, $I_D = 15.0 \text{ A}$
- High performance technology for extremely low r_{DS(on)}
- Termination is Lead-free and RoHS Compliant

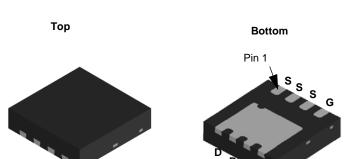


General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced Power Trench® process that has been especially tailored to minimize the on-state resistance. This device is well suited for Power Management and load switching applications common in Notebook Computers and Portable Battery Packs.

Application

- DC DC Buck Converters
- Notebook battery power management
- Load switch in Notebook





MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Paramo		Ratings	Units	
V_{DS}	Drain to Source Voltage			30	V
V_{GS}	Gate to Source Voltage			±20	V
	Drain Current -Continuous	T _C = 25 °C		20	
I_D	-Continuous	T _A = 25 °C	(Note 1a)	16.9	Α
	-Pulsed			50	
E _{AS}	Single Pulse Avalanche Energy		(Note 3)	144	mJ
Б	Power Dissipation	T _C = 25 °C		33	W
P_{D}	Power Dissipation	T _A = 25 °C	(Note 1a)	2.3	VV
T _J , T _{STG}	Operating and Storage Junction Tempera	ature Range		-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case		3.7	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	53	C/VV

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC7672	FDMC7672	MLP 3.3x3.3	13 "	12 mm	3000 units

Electrical Characteristics $T_J = 25$ °C unless otherwise noted

Parameter

Off Char	acteristics					
BV _{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μ A, referenced to 25 °C		13		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24 \text{ V}, V_{GS} = 0 \text{ V}$ $T_{J} = 125 \text{ °C}$			1 250	μΑ
I _{GSS}	Gate to Source Leakage Current	V _{GS} = 20 V, V _{DS} = 0 V			100	nA

Test Conditions

Min

Тур

Max

Units

On Characteristics

Symbol

V _{GS(th)}	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu A$	1.2	1.9	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25 °C		-6		mV/°C
r _{DS(on)} Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 16.9 \text{ A}$		4.3	5.7		
	Static Drain to Source On Resistance	$V_{GS} = 4.5 \text{ V}, I_D = 15.0 \text{ A}$		5.4	7.0	mΩ
	$V_{GS} = 10 \text{ V}, I_D = 16.9 \text{ A}$ $T_J = 125 ^{\circ}\text{C}$		5.5	6.9	11152	
g _{FS}	Forward Transconductance	V _{DD} = 5 V, I _D = 16.9 A		82		S

Dynamic Characteristics

C _{iss}	Input Capacitance	V 45.V.V 0.V	2925	3890	pF
C _{oss}	Output Capacitance	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V},$ $f = 1 \text{ MHz}$	1050	1400	pF
C _{rss}	Reverse Transfer Capacitance	1 - 1 1/11/12	80	120	pF
R_g	Gate Resistance		0.9	2.7	Ω

Switching Characteristics

t _{d(on)}	Turn-On Delay Time		13	24	ns
t _r	Rise Time	V _{DD} = 15 V, I _D = 16.9 A,	6	12	ns
t _{d(off)}	Turn-Off Delay Time	$V_{GS} = 10 \text{ V}, R_{GEN} = 6 \Omega$	31	49	ns
t _f	Fall Time		5	10	ns
0	Total Gate Charge	V _{GS} = 0 V to 10 V	40	57	nC
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0 \text{ V to } 4.5 \text{ V}$ $V_{DD} = 15 \text{ V}$	18	24	nC
Q_{gs}	Total Gate Charge	I _D = 16.9 A	9		nC
Q_{gd}	Gate to Drain "Miller" Charge		4		nC

Drain-Source Diode Characteristics

Vob Source to Drain Dioge Forward voltage	Source to Drain Diode, Forward Voltage	$V_{GS} = 0 \text{ V}, I_{S} = 16.9 \text{ A}$ (Note 2)	0.83	1.2	V
	$V_{GS} = 0 \text{ V}, I_{S} = 1.9 \text{ A}$ (Note 2)	0.72	1.2	v	
t _{rr}	Reverse Recovery Time	I _E = 16.9 A, di/dt = 100 A/μs	39	62	ns
Q _{rr}	Reverse Recovery Charge	1 F = 10.9 A, α//αt = 100 A/μs	18	32	nC

^{1.} $R_{\theta JA}$ is determined with the device mounted on a 1 in 2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 53 °C/W when mounted on a 1 in² pad of 2 oz copper



b.125 °C/W when mounted on a minimum pad of 2 oz copper

^{2:} Pulse Test: Pulse Width < 300 μ s, Duty cycle < 2.0 %. 3. E_{AS} of 144 mJ is based on starting T_J = 25 $^{\circ}$ C, L = 1 mH, I_{AS} = 17 A, V_{DD} = 27 V, V_{GS} = 10 V.

Typical Characteristics $T_J = 25$ °C unless otherwise noted

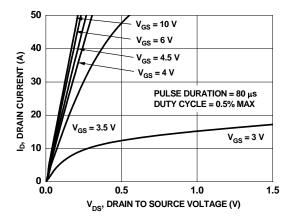


Figure 1. On-Region Characteristics

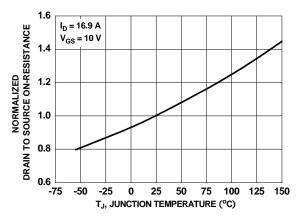


Figure 3. Normalized On-Resistance vs. Junction Temperature

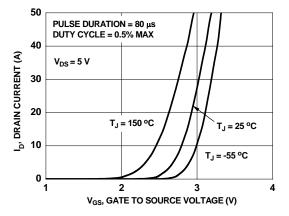


Figure 5. Transfer Characteristics

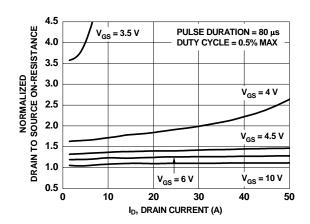


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

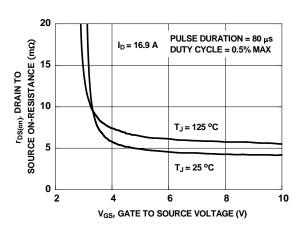


Figure 4. On-Resistance vs. Gate to Source Voltage

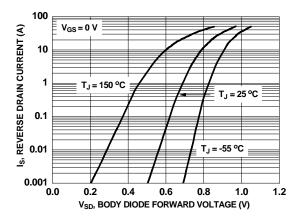


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

Typical Characteristics $T_J = 25$ °C unless otherwise noted

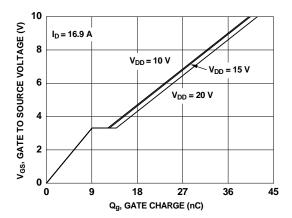


Figure 7. Gate Charge Characteristics

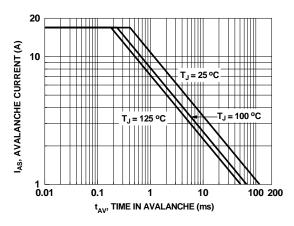


Figure 9. Unclamped Inductive Switching Capability

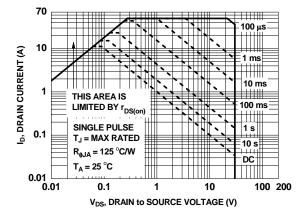


Figure 11. Forward Bias Safe Operating Area

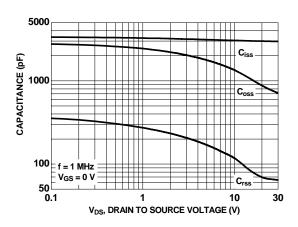


Figure 8. Capacitance vs. Drain to Source Voltage

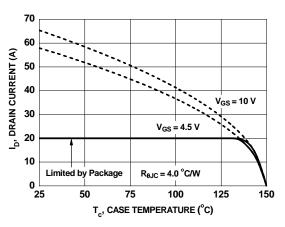


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

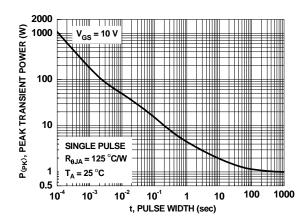


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25$ °C unless otherwise noted

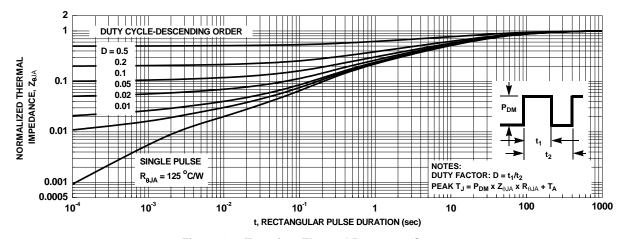
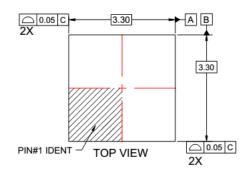
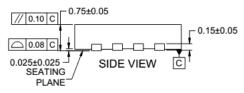
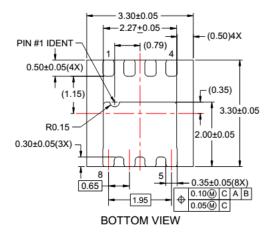


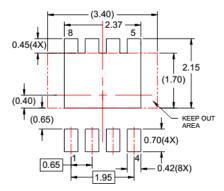
Figure 13. Transient Thermal Response Curve

Dimensional Outline and Pad Layout









RECOMMENDED LAND PATTERN

NOTES:

- A. DOES NOT CONFORM TO JEDEC REGISTRATION MO-229
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.
- E. DRAWING FILENAME: MKT-MLP08Srev3.



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