Product data sheet

1. General description

N-channel enhancement mode Field-Effect Transistor (FET) in a leadless medium power DFN2020MD-6 (SOT1220) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- · Low threshold voltage
- Trench MOSFET technology
- · Side wettable flanks for optical solder inspection
- ElectroStatic Discharge (ESD) protection > 1 kV HBM (class H1C)
- AEC-Q101 qualified

3. Applications

- · Relay driver
- High-speed line driver
- · Low-side load switch
- · Switching circuits

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit	
V_{DS}	drain-source voltage	T _j = 25 °C		-	-	20	V	
V_{GS}	gate-source voltage			-12	-	12	V	
I _D	drain current	V _{GS} = 4.5 V; T _{amb} = 25 °C	[1]	-	-	9	Α	
Static characte	Static characteristics							
R _{DSon}	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}; I_D = 9 \text{ A}; T_j = 25 \text{ °C}$		-	10	14	mΩ	

^[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm².



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5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	D	drain	15776	D
2	D	drain	7	
3	G	gate	2 5	G ← F ★ \
4	S	source	3 8 4	\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\
5	D	drain	Transparent top view	
6	D	drain	DFN2020MD-6 (SOT1220)	S
7	D	drain		017aaa255
8	S	source		

6. Ordering information

Table 3. Ordering information

Type number	Package					
	Name	Description	Version			
PMPB10XNEA	DFN2020MD-6	DFN2020MD-6: plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals	SOT1220			

7. Marking

Table 4. Marking codes

Type number	Marking code
PMPB10XNEA	4E

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8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	T _j = 25 °C		-	20	V
V _{GS}	gate-source voltage			-12	12	V
I _D	drain current	V _{GS} = 4.5 V; T _{amb} = 25 °C	[1]	-	9	Α
		V _{GS} = 4.5 V; T _{amb} = 100 °C	[1]	-	5.7	Α
I _{DM}	peak drain current	T_{amb} = 25 °C; single pulse; $t_p \le 10 \mu s$		-	36	Α
P _{tot}	total power dissipation	T _{amb} = 25 °C	[1]	-	1.7	W
		T _{sp} = 25 °C		-	12.5	W
T _j	junction temperature			-55	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C
Source-drain	diode					,
I _S	source current	T _{amb} = 25 °C	[1]	-	2	Α
ESD maximun	n rating			·		
V_{ESD}	electrostatic discharge voltage	НВМ	[2]	-	1000	V
Avalanche rug	gedness					,
E _{DS(AL)S}	non-repetitive drain- source avalanche energy	$T_{j(init)}$ = 25 °C; I_D = 2 A; DUT in avalanche (unclamped)		-	21	mJ

^[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm².

^[2] Measured between all pins.

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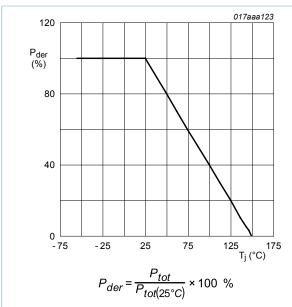


Fig. 1. Normalized total power dissipation as a function of junction temperature

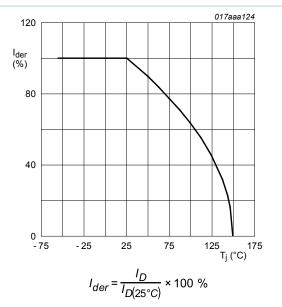
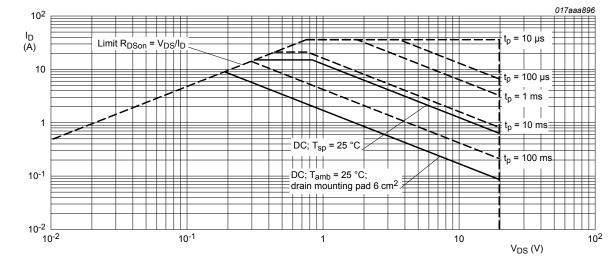


Fig. 2. Normalized continuous drain current as a function of junction temperature



I_{DM} = single pulse

Fig. 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

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9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
R _{th(j-a)}	thermal resistance from junction to ambient		[1]	-	235	270	K/W
			[2]	_	67	74	K/W
R _{th(j-sp)}	thermal resistance from junction to solder point			-	5	10	K/W

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm².

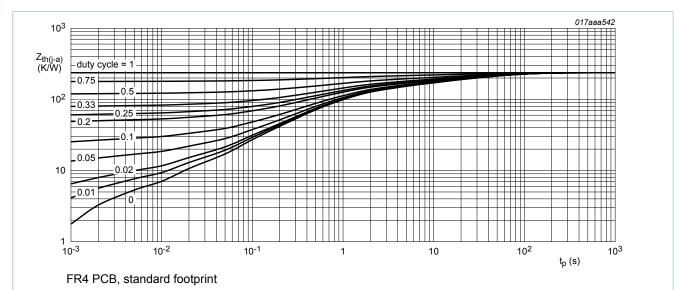


Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

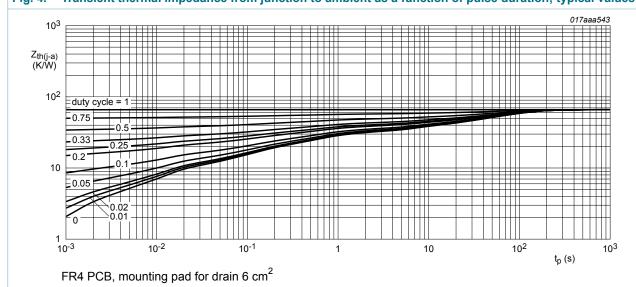


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

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10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	acteristics	1			,	
V _{(BR)DSS}	drain-source breakdown voltage	I_D = 250 μ A; V_{GS} = 0 V; T_j = 25 °C	20	-	-	V
V_{GSth}	gate-source threshold voltage	I_D = 250 μ A; V_{DS} = V_{GS} ; T_j = 25 °C	0.4	0.65	0.9	V
I _{DSS}	drain leakage current	V _{DS} = 20 V; V _{GS} = 0 V; T _j = 25 °C	-	-	1	μΑ
I _{GSS}	gate leakage current	V _{GS} = 8 V; V _{DS} = 0 V; T _j = 25 °C	-	-	10	μΑ
		$V_{GS} = -8 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-	-10	μΑ
R _{DSon}	drain-source on-state	V _{GS} = 4.5 V; I _D = 9 A; T _j = 25 °C	-	10	14	mΩ
	resistance	V _{GS} = 4.5 V; I _D = 9 A; T _j = 150 °C	-	15	21	mΩ
		V _{GS} = 2.5 V; I _D = 8 A; T _j = 25 °C	-	12	18	mΩ
		V _{GS} = 1.8 V; I _D = 3.7 A; T _j = 25 °C	-	16	25	mΩ
9 _{fs}	forward transconductance	$V_{DS} = 10 \text{ V}; I_D = 9 \text{ A}; T_j = 25 \text{ °C}$	-	60	-	S
R_G	gate resistance	f = 1 MHz	-	2	-	Ω
Dynamic ch	naracteristics				'	
Q _{G(tot)}	total gate charge	$V_{DS} = 10 \text{ V}; I_D = 6 \text{ A}; V_{GS} = 4.5 \text{ V};$	-	23	34	nC
Q_{GS}	gate-source charge	T _j = 25 °C	-	2.6	-	nC
Q _{GD}	gate-drain charge		-	4.5	-	nC
C _{iss}	input capacitance	V _{DS} = 10 V; f = 1 MHz; V _{GS} = 0 V;	-	2175	-	pF
C _{oss}	output capacitance	T _j = 25 °C	-	235	-	pF
C _{rss}	reverse transfer capacitance		-	205	-	pF
t _{d(on)}	turn-on delay time	$V_{DS} = 10 \text{ V}; I_D = 6 \text{ A}; V_{GS} = 4.5 \text{ V};$	-	13	-	ns
t _r	rise time	$R_{G(ext)} = 6 \Omega; T_j = 25 ^{\circ}C$	-	35	-	ns
t _{d(off)}	turn-off delay time	_	-	54	-	ns
t _f	fall time		-	50	-	ns
Source-dra	in diode		'			
V _{SD}	source-drain voltage	$I_S = 2 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 ^{\circ}\text{C}$	-	0.6	1.2	V
t _{rr}	reverse recovery time	$I_S = 2 \text{ A}; dI_S/dt = -100 \text{ A/}\mu\text{s}; V_{GS} = 0 \text{ V};$	-	13	-	ns
Q _r	recovered charge	$V_{DS} = 10 \text{ V}; T_j = 25 \text{ °C}$	_	5		nC

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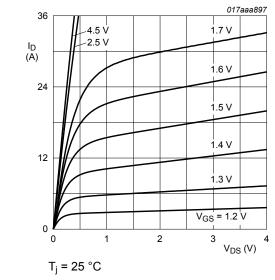


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

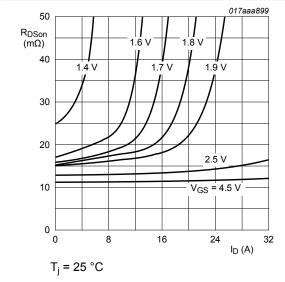


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

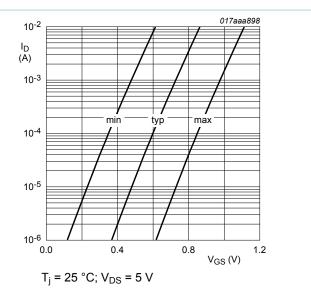


Fig. 7. Subthreshold drain current as a function of gate-source voltage

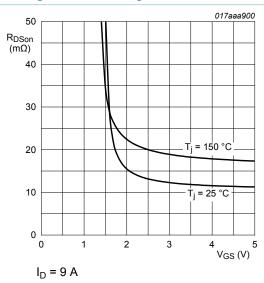


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

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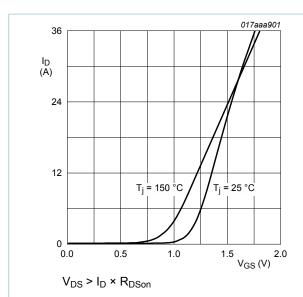


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

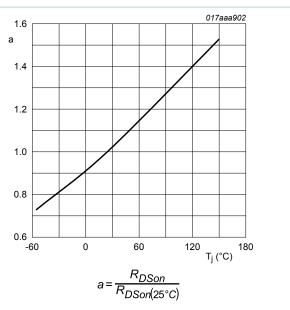


Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

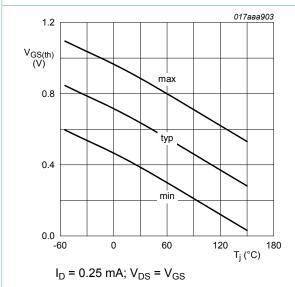


Fig. 12. Gate-source threshold voltage as a function of junction temperature

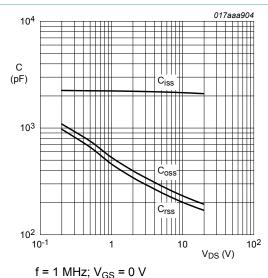


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

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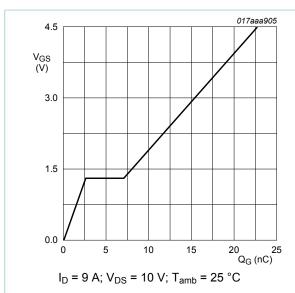


Fig. 14. Gate-source voltage as a function of gate charge; typical values

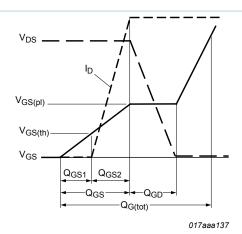


Fig. 15. MOSFET transistor: Gate charge waveform definitions

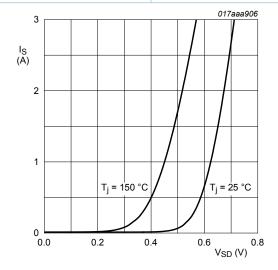
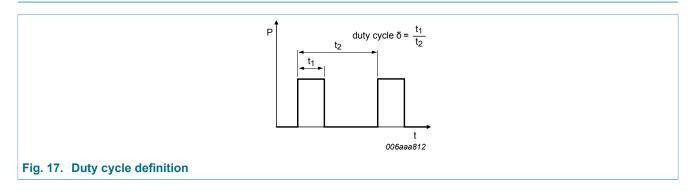


Fig. 16. Source current as a function of source-drain voltage; typical values

 $V_{GS} = 0 V$

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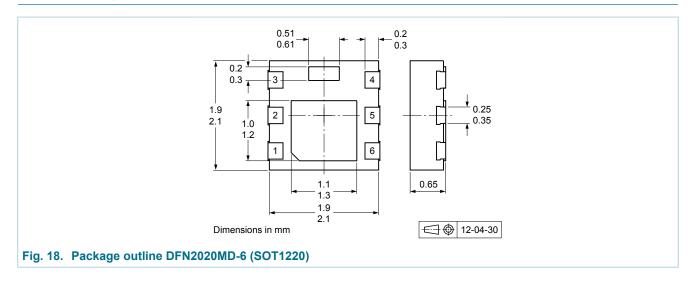
11. Test information



Quality information

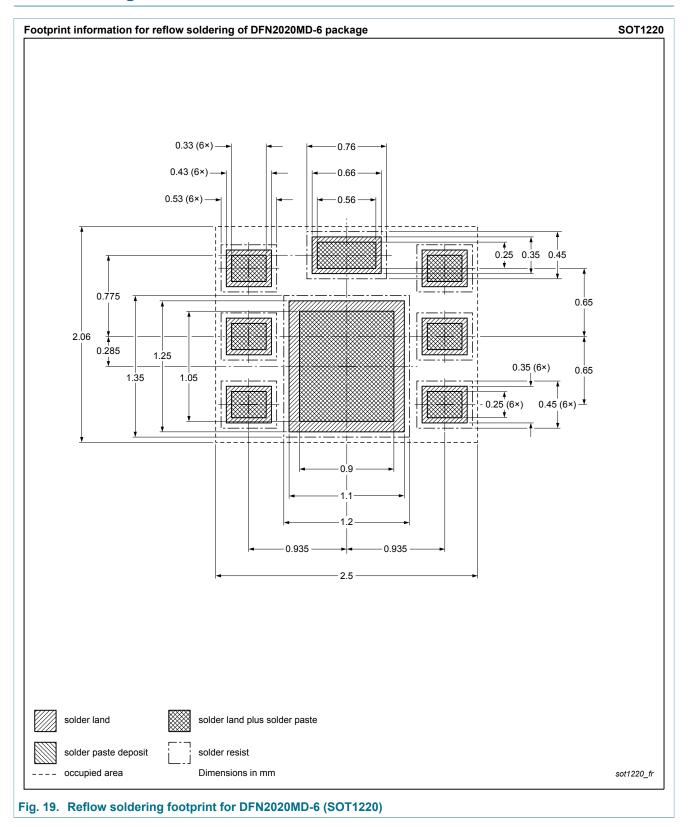
This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.

12. Package outline



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13. Soldering



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14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMPB10XNEA v.1	20180327	Product data sheet	-	-

20 V, N-channel Trench MOSFET

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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Промышленная ул, дом № 19, литера Н,

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