

Phase Control Thyristors (Hockey PUK Version), 350 A



TO-200AB (A-PUK)

FEATURES

- Center amplifying gate
- Metal case with ceramic insulator
- International standard case TO-200AB (A-PUK)
- Designed and qualified for industrial level
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT

TYPICAL APPLICATIONS

- DC motor controls
- Controlled DC power supplies
- AC controllers

PRODUCT SUMMARY

Package	TO-200AB (A-PUK)
Diode variation	Single SCR
$I_{T(AV)}$	350 A
V_{DRM}/V_{RRM}	400 V to 2000 V
V_{TM}	1.96 V
I_{GT}	150 mA
T_J	-40 °C to 125 °C

MAJOR RATINGS AND CHARACTERISTICS

PARAMETER	TEST CONDITIONS	VALUES	UNITS
$I_{T(AV)}$		350	A
	T_{hs}	55	°C
$I_{T(RMS)}$		660	A
	T_{hs}	25	°C
I_{TSM}	50 Hz	5000	A
	60 Hz	5230	
I^2t	50 Hz	125	kA ² s
	60 Hz	114	
V_{DRM}/V_{RRM}		400 to 2000	V
t_q	Typical	100	µs
T_J		-40 to 125	°C

ELECTRICAL SPECIFICATIONS

VOLTAGE RATINGS

TYPE NUMBER	VOLTAGE CODE	V_{DRM}/V_{RRM} , MAXIMUM REPETITIVE PEAK AND OFF-STATE VOLTAGE V	V_{RSM} , MAXIMUM NON-REPETITIVE PEAK VOLTAGE V	I_{DRM}/I_{RRM} MAXIMUM AT $T_J = T_J$ MAXIMUM mA
VS-ST180C..C	04	400	500	30
	08	800	900	
	12	1200	1300	
	16	1600	1700	
	18	1800	1900	
	20	2000	2100	



ABSOLUTE MAXIMUM RATINGS						
PARAMETER	SYMBOL	TEST CONDITIONS			VALUES	UNITS
Maximum average on-state current at heatsink temperature	I _{T(AV)}	180° conduction, half sine wave double side (single side) cooled			350 (140)	A
					55 (85)	°C
Maximum RMS on-state current	I _{T(RMS)}	DC at 25 °C heatsink temperature double side cooled			660	A
Maximum peak, one-cycle non-repetitive surge current	I _{TSM}	t = 10 ms	No voltage reapplied	Sinusoidal half wave, initial T _J = T _J maximum	5000	
		t = 8.3 ms			5230	
		t = 10 ms	100 % V _{RRM} reapplied		4200	
		t = 8.3 ms			4400	
Maximum I ² t for fusing	I ² t	t = 10 ms	No voltage reapplied		125	kA ² s
		t = 8.3 ms			114	
		t = 10 ms	100 % V _{RRM} reapplied		88	
		t = 8.3 ms			81	
Maximum I ² √t for fusing	I ² √t	t = 0.1 to 10 ms, no voltage reapplied			1250	kA ² √s
Low level value of threshold voltage	V _{T(TO)1}	(16.7 % × π × I _{T(AV)}) < I < π × I _{T(AV)} , T _J = T _J maximum			1.08	V
High level value of threshold voltage	V _{T(TO)2}	(I > π × I _{T(AV)}), T _J = T _J maximum			1.14	
Low level value of on-state slope resistance	r _{t1}	(16.7 % × π × I _{T(AV)}) < I < π × I _{T(AV)} , T _J = T _J maximum			1.18	mΩ
High level value of on-state slope resistance	r _{t2}	(I > π × I _{T(AV)}), T _J = T _J maximum			1.14	
Maximum on-state voltage	V _{TM}	I _{pk} = 750 A, T _J = T _J maximum, t _p = 10 ms sine pulse			1.96	V
Maximum holding current	I _H	T _J = 25 °C, anode supply 12 V resistive load			600	mA
Maximum (typical) latching current	I _L				1000 (300)	

SWITCHING				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum non-repetitive rate of rise of turned-on current	di/dt	Gate drive 20 V, 20 Ω, $t_r \leq 1$ μs $T_J = T_J$ maximum, anode voltage ≤ 80 % V_{DRM}	1000	A/μs
Typical delay time	t_d	Gate current 1 A, $di_g/dt = 1$ A/μs $V_d = 0.67$ % V_{DRM} , $T_J = 25$ °C	1.0	μs
Typical turn-off time	t_q	$I_{TM} = 300$ A, $T_J = T_J$ maximum, $di/dt = 20$ A/μs, $V_R = 50$ V, $dV/dt = 20$ V/μs, gate 0 V 100 Ω, $t_p = 500$ μs	100	

BLOCKING				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNIT S
Maximum critical rate of rise of off-state voltage	dV/dt	$T_J = T_J$ maximum linear to 80 % rated V_{DRM}	500	V/μs
Maximum peak reverse and off-state leakage current	I_{RRM}, I_{DRM}	$T_J = T_J$ maximum, rated V_{DRM}/V_{RRM} applied	30	mA



TRIGGERING					
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES		UNIT S
			typ.	max.	
Maximum peak gate power	P_{GM}	$T_J = T_J$ maximum, $t_p \leq 5$ ms	10		W
Maximum average gate power	$P_{G(AV)}$	$T_J = T_J$ maximum, $f = 50$ Hz, $d\% = 50$	2.0		
Maximum peak positive gate current	I_{GM}	$T_J = T_J$ maximum, $t_p \leq 5$ ms	3.0		A
Maximum peak positive gate voltage	$+V_{GM}$		20		V
Maximum peak negative gate voltage	$-V_{GM}$		5.0		
DC gate current required to trigger	I_{GT}	$T_J = -40$ °C	180	-	mA
		$T_J = 25$ °C	90	150	
		$T_J = 125$ °C	40	-	
DC gate voltage required to trigger	V_{GT}	$T_J = -40$ °C	2.9	-	V
		$T_J = 25$ °C	1.8	3.0	
		$T_J = 125$ °C	1.2	-	
DC gate current not to trigger	I_{GD}	$T_J = T_J$ maximum	10		mA
DC gate voltage not to trigger	V_{GD}		0.25		V

THERMAL AND MECHANICAL SPECIFICATIONS				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNIT S
Maximum operating junction temperature range	T_J		-40 to 125	°C
Maximum storage temperature range	T_{Stg}		-40 to 150	
Maximum thermal resistance, junction to heatsink	R_{thJ-hs}	DC operation single side cooled	0.17	K/W
		DC operation double side cooled	0.08	
Maximum thermal resistance, case to heatsink	R_{thC-hs}	DC operation single side cooled	0.033	
		DC operation double side cooled	0.017	
Mounting force, ± 10 %			4900 (500)	N (kg)
Approximate weight			50	g
Case style		See dimensions - link at the end of datasheet	TO-200AB (A-PUK)	

ΔR_{thJC} CONDUCTION					
CONDUCTION ANGLE	SINUSOIDAL CONDUCTION		RECTANGULAR CONDUCTION		TEST CONDITIONS
	SINGLE SIDE	DOUBLE SIDE	SINGLE SIDE	DOUBLE SIDE	
180°	0.015	0.015	0.011	0.011	$T_J = T_J$ maximum
120°	0.018	0.019	0.019	0.019	
90°	0.024	0.024	0.026	0.026	
60°	0.035	0.035	0.036	0.037	
30°	0.060	0.060	0.060	0.061	
					K/W

Note

- The table above shows the increment of thermal resistance R_{thJC} when devices operate at different conduction angles than DC

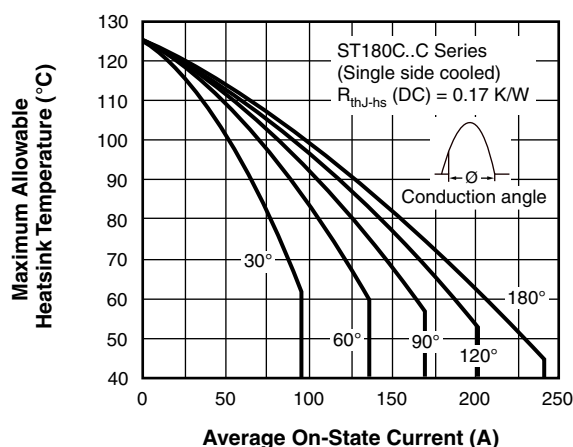


Fig. 1 - Current Ratings Characteristics

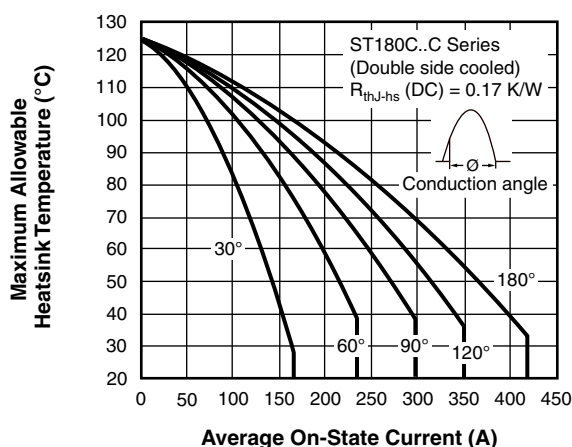


Fig. 3 - Current Ratings Characteristics

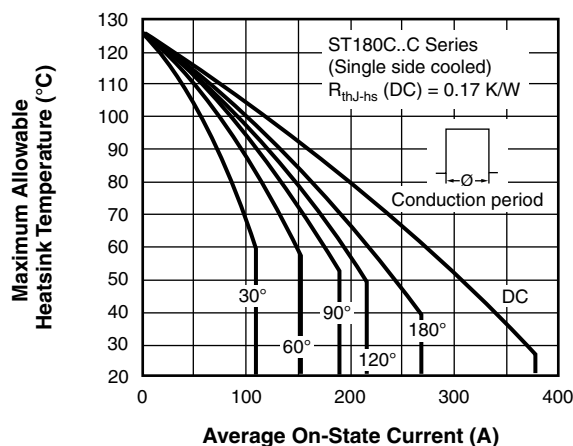


Fig. 2 - Current Ratings Characteristics

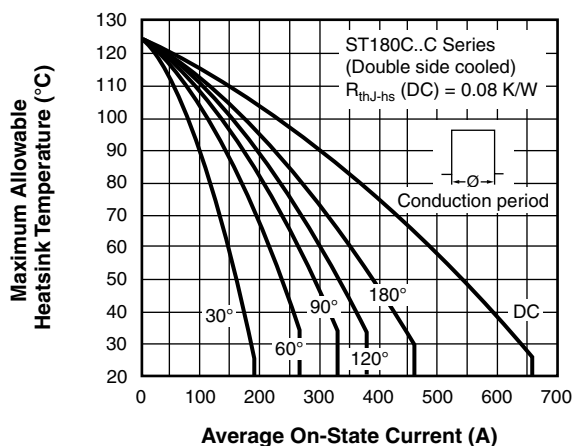


Fig. 4 - Current Ratings Characteristics

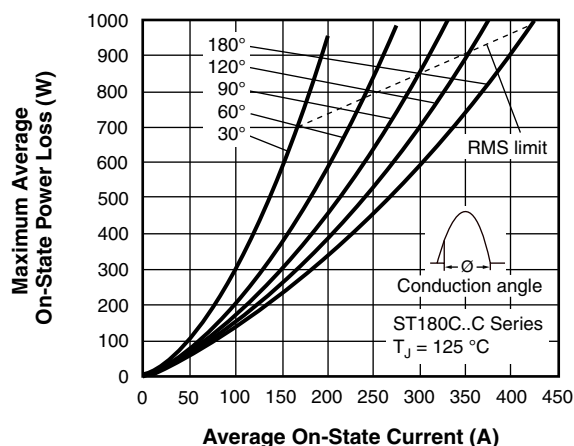


Fig. 5 - On-State Power Loss Characteristics

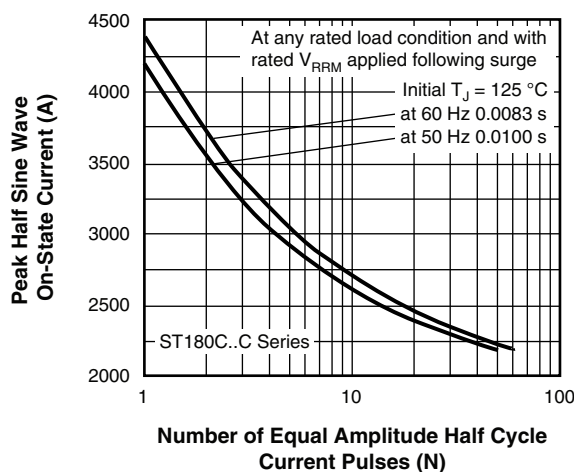


Fig. 7 - Maximum Non-Repetitive Surge Current Single and Double Side Cooled

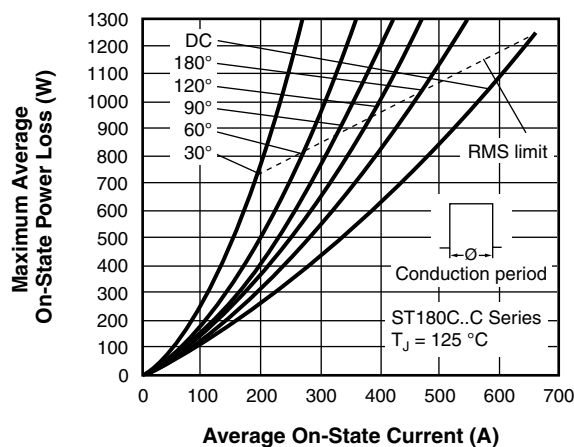


Fig. 6 - On-State Power Loss Characteristics

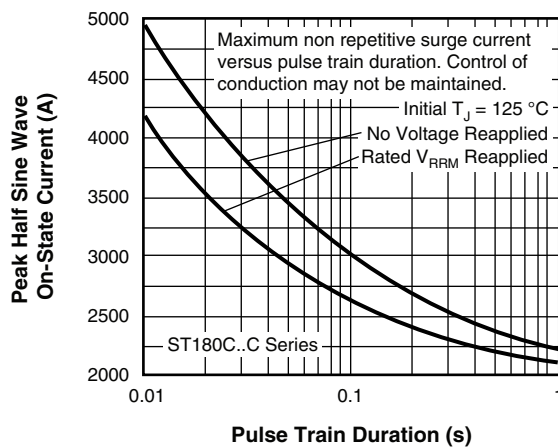


Fig. 8 - Maximum Non-Repetitive Surge Current Single and Double Side Cooled

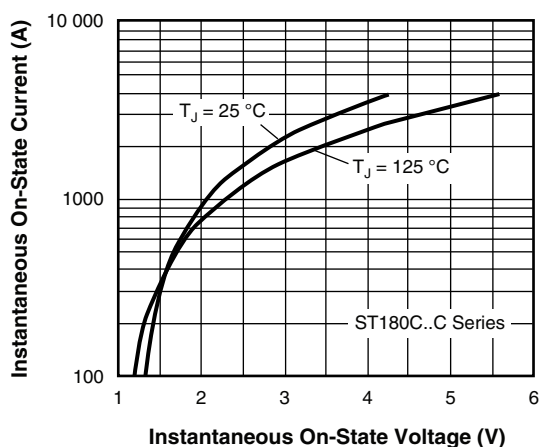


Fig. 9 - On-State Voltage Drop Characteristics

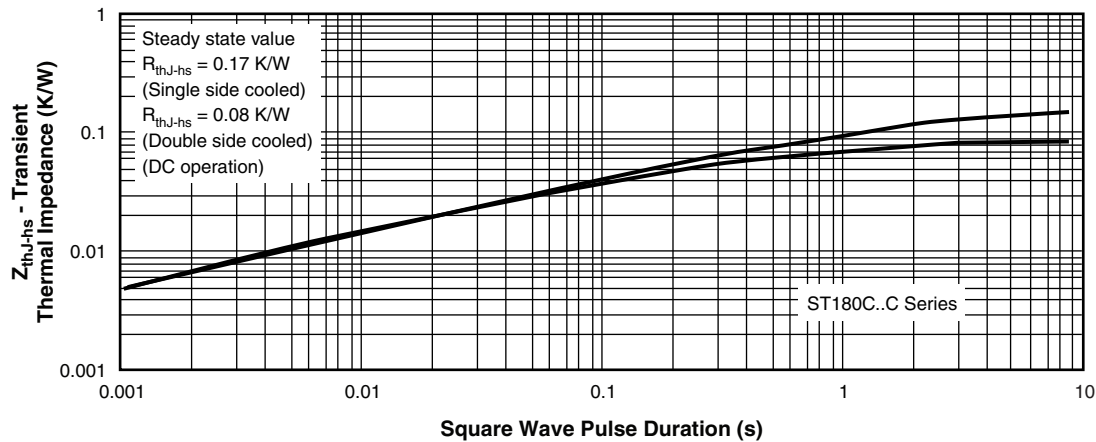
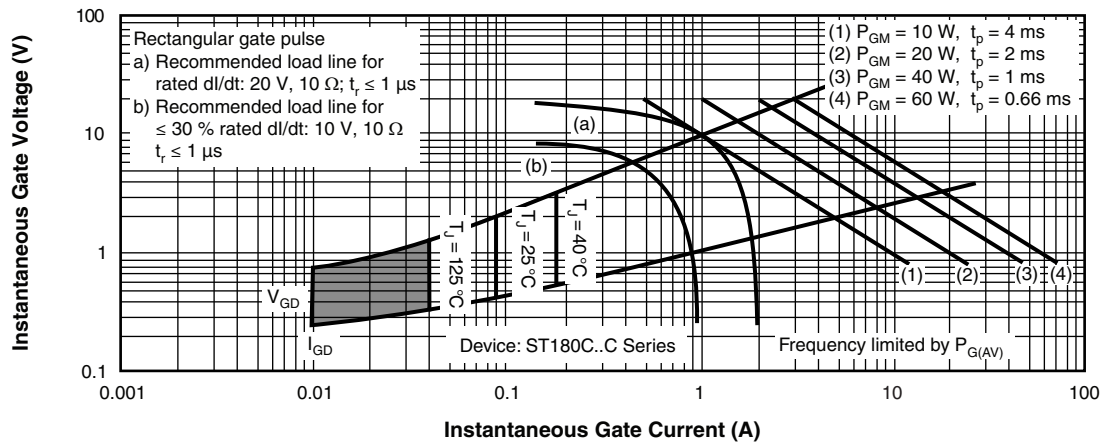

Fig. 10 - Thermal Impedance Z_{thJ-hs} Characteristics


Fig. 11 - Gate Characteristics



ORDERING INFORMATION TABLE

Device code	VS-	ST	18	0	C	20	C	1	-
	1	2	3	4	5	6	7	8	9

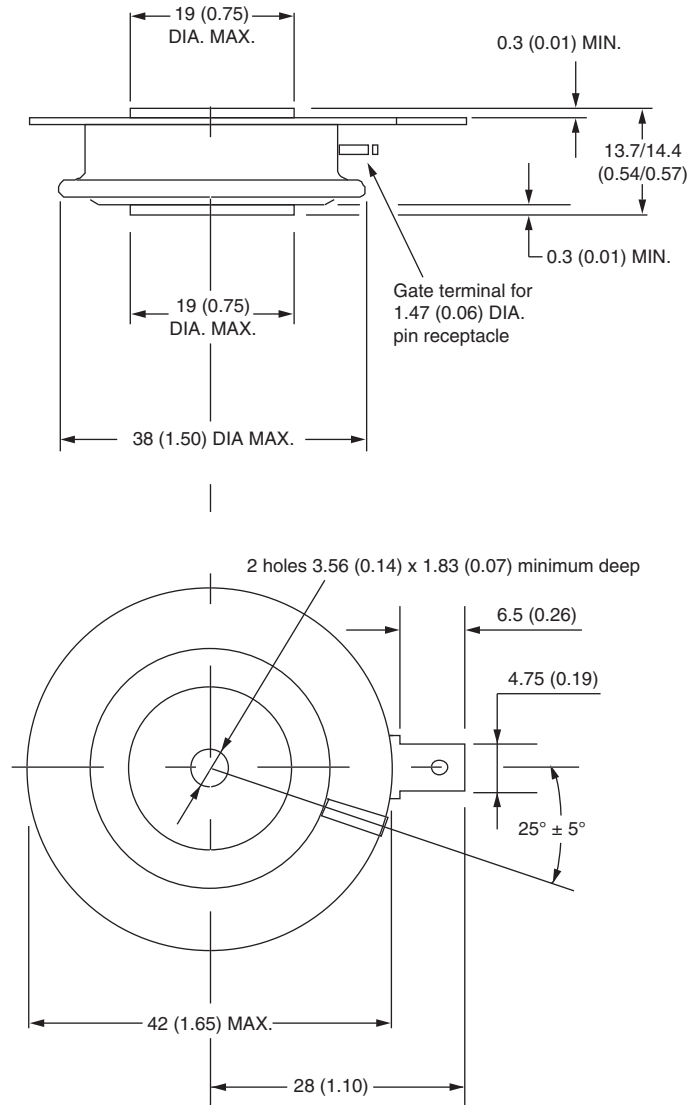
- | | | |
|----------|---|--|
| 1 | - | Vishay Semiconductors product |
| 2 | - | Thyristor |
| 3 | - | Essential part number |
| 4 | - | 0 = Converter grade |
| 5 | - | C = Ceramic PUK |
| 6 | - | Voltage code x 100 = V_{RRM} (see Voltage Ratings table) |
| 7 | - | C = PUK case TO-200AB (A-PUK) |
| 8 | - | 0 = Eyelet terminals (gate and auxiliary cathode unsoldered leads)
1 = Fast-on terminals (gate and auxiliary cathode unsoldered leads)
2 = Eyelet terminals (gate and auxiliary cathode soldered leads)
3 = Fast-on terminals (gate and auxiliary cathode soldered leads) |
| 9 | - | Critical dV/dt: • None = 500 V/ μ s (standard selection)
• L = 1000 V/ μ s (special selection) |

LINKS TO RELATED DOCUMENTS	
Dimensions	www.vishay.com/doc?95074

TO-200AB (A-PUK)

DIMENSIONS in millimeters (inches)

Anode to gate
Creepage distance: 7.62 (0.30) minimum
Strike distance: 7.12 (0.28) minimum



Quote between upper and lower pole pieces has to be considered after application of mounting force (see thermal and mechanical specification)



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