

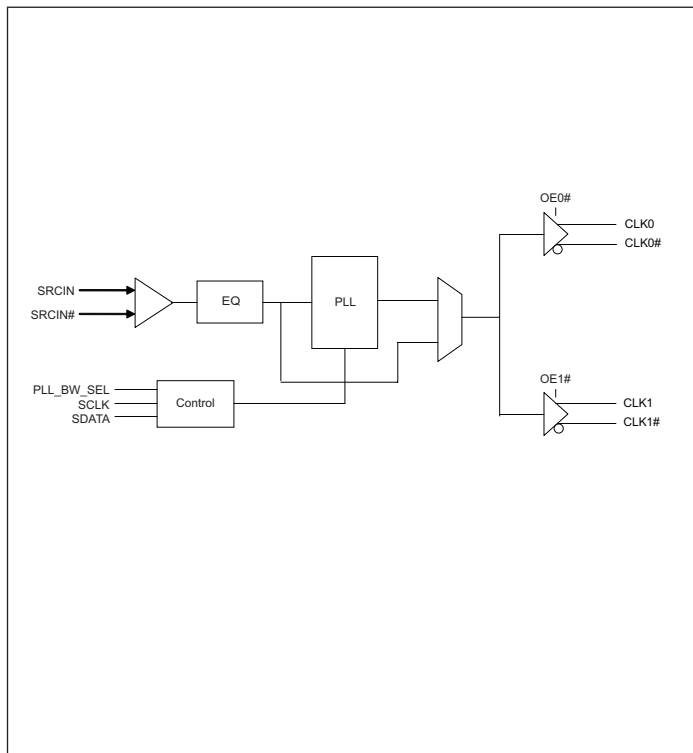
### Features

- PCIe Gen2/ Gen3\* compliant clock buffer/ZDB
- \* Gen3 performance only available in Commercial temp
- Internal equalization for better signal integrity
- 2 HCSL outputs
- Dual PLL bandwidth for SSC tracking
- Cycle-to-Cycle Jitter : 40ps (typ)
- Output-to-Output Skew <10ps
- 3.3V supply voltage
- TSSOP-20 packages

### Applications

- Servers
- Embedded computing systems
- Networking systems

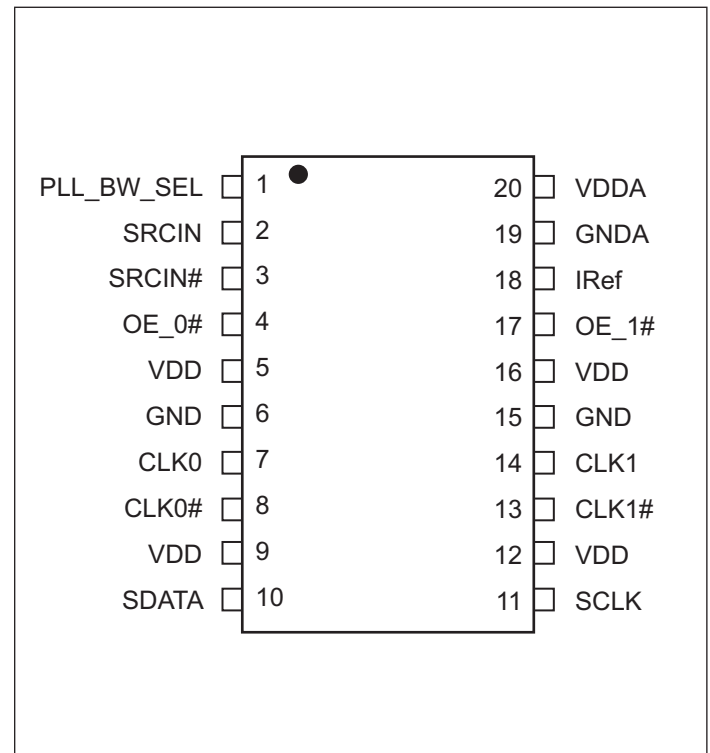
### Block Diagram



### Description

The PI6CEQ20200 is a high performance PCIe Gen2/ Gen3 zero delay buffer with two HCSL outputs. Pericom's proprietary equalization technique used in this device improves signal integrity and makes this device suitable for PCIe Gen2/ Gen3 applications even when the input from the main clock has to travel a long distance.

### Pin Configuration (20-Pin TSSOP & 20-Pin QSOP)



**Pin Description**

| Pin #        | Pin Name      | Type         | Description                                                                                |
|--------------|---------------|--------------|--------------------------------------------------------------------------------------------|
| 1            | PLL_BW_SEL    | Input        | CMOS input to select the PLL Bandwidth                                                     |
| 2, 3         | SRCIN, SRCIN# | Input        | HCSL inputs                                                                                |
| 4            | OE_0#         | Input        | Output enable for CLK0 and CLK0#. "0" is "enabled", "1" is "tri-stated. Internal pull-down |
| 5, 9, 12, 16 | VDD           | Power        | 3.3V Power Supply                                                                          |
| 6, 15        | GND           | Power        | Ground                                                                                     |
| 7, 8         | CLK0, CLK0#   | Input        | HCSL output                                                                                |
| 10           | SDATA         | Input/Output | SMBus data                                                                                 |
| 11           | SCLK          | Input        | SMBus clock input                                                                          |
| 13, 14       | CKL1#, CLK1   | Output       | HCSL output                                                                                |
| 17           | OE_1#         | Input        | Output enable for CLK1 and CLK1#. "0" is "enabled", "1" is "tri-stated. Internal pull-down |
| 18           | IRef          | Input        | External resistor connection for internal current reference                                |
| 19           | GNDA          | Power        | Analog and PLL Ground                                                                      |
| 20           | VDDA          | Power        | Analog and PLL power supply                                                                |

**Maximum Ratings** (Above which the useful life may be impaired. For user guidelines, not tested)

Storage temperature..... -65°C to +155°C  
 Ambient Temperature with Power Applied.....-40°C to +85°C  
 3.3V Analog Supply Voltage ..... -0.5 to +4.6V  
 ESD Protection(HBM) ..... 2000V

**Note:**

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Recommended Operating Conditions**

| Symbol                            | Description                                            | Test Conditions        | Min   | Type | Max   | Unit |
|-----------------------------------|--------------------------------------------------------|------------------------|-------|------|-------|------|
| V <sub>DD</sub>                   | Power supply                                           | -                      | 3.135 | -    | 3.465 | V    |
| I <sub>DD</sub>                   | Total Power Supply Current                             | -                      | -     | -    | 65    | mA   |
| I <sub>DD_Output tri-stated</sub> | Total power supply current with Outputs are tri-stated | Outputs are tri-stated | -     | -    | 30    | mA   |
| T <sub>A</sub>                    | Operating temperature                                  | Commercial temperature | 0     |      | +70   | °C   |
|                                   |                                                        | Industrial temperature | -40   |      | +85   |      |

**LVCMOS DC Electrical Characteristics** (Over Operating Conditions)

| Symbol          | Parameter                     | Conditions                        | Min. | Typ. | Max.                 | Unit |
|-----------------|-------------------------------|-----------------------------------|------|------|----------------------|------|
| V <sub>IH</sub> | Input High Voltage            | -                                 | 2    | -    | V <sub>DD</sub> +0.3 | V    |
| V <sub>IL</sub> | Input Low Voltage             | -                                 | -0.3 | -    | 0.8                  | V    |
| I <sub>IH</sub> | Input High Current            | V <sub>IN</sub> = V <sub>DD</sub> | -    | -    | 45                   | μA   |
| I <sub>IL</sub> | Input Low Current             | V <sub>IN</sub> = 0V              | -45  | -    | -                    | μA   |
| R <sub>PU</sub> | Internal pull up resistance   | -                                 | -    | 120  | -                    | kOhm |
| R <sub>DN</sub> | Internal pull down resistance | -                                 | -    | 120  | -                    | kOhm |

**Differential DC Input Characteristics** (Over Operating Conditions)

| Symbol          | Parameter               | Conditions                                | Min. | Typ. | Max. | Unit |
|-----------------|-------------------------|-------------------------------------------|------|------|------|------|
| I <sub>IH</sub> | Input High Current, IN- | V <sub>IN</sub> = V <sub>DD</sub> =3.465V | -    | -    | 5    | μA   |
|                 | Input High Current, IN+ |                                           |      |      | 45   | μA   |
| I <sub>IL</sub> | Input Low Current, IN-  | V <sub>IN</sub> = 0V                      | -45  | -    | -    | μA   |
|                 | Input Low Current, IN+  |                                           | -5   | -    | -    | μA   |
| V <sub>IH</sub> | Input High Voltage      | Single-ended swing                        | 660  | 700  | 850  | mV   |
| V <sub>IL</sub> | Input Low Voltage       |                                           | -150 | 0    |      | mV   |

**HCSL DC Electrical Characteristics** (Over Operating Conditions)

| Symbol              | Parameter                                                                                 | Conditions | Min. | Typ. | Max. | Unit |
|---------------------|-------------------------------------------------------------------------------------------|------------|------|------|------|------|
| V <sub>OH</sub>     | Output High Voltage                                                                       | -          | 660  | -    | 850  | mV   |
| V <sub>OL</sub>     | Output Low Voltage                                                                        | -          | -    | -    | 150  | mV   |
| V <sub>CROSS</sub>  | Absolute Crossing Point Voltages                                                          | -          | 250  | -    | 550  | mV   |
| ΔV <sub>CROSS</sub> | Total variation of V <sub>CROSS</sub> overall edges                                       | -          | -    | -    | 140  | mV   |
| I <sub>OH</sub>     | Output High Current w/475-Ohm resistor.<br>Connected between I <sub>REF</sub> pin and GND | -          | -    | 14   | -    | mA   |

**HCSL AC Switching Characteristics<sup>(\*1, \*2, \*3)</sup>** (Over Operating Conditions)

| Symbol                           | Parameter                                  | Conditions                                                                           | Min. | Typ. | Max. | Unit |
|----------------------------------|--------------------------------------------|--------------------------------------------------------------------------------------|------|------|------|------|
| F <sub>in</sub>                  | Input Frequency                            | -                                                                                    | 90   | 100  | 110  | MHz  |
| T <sub>r</sub> /T <sub>f</sub>   | Output Rise/Fall time                      | Between 0.175V and 0.525V <sup>*2</sup>                                              | 175  | -    | 700  | ps   |
| ΔT <sub>r</sub> /ΔT <sub>f</sub> | Rise and Fall Time Variation <sup>*2</sup> | -                                                                                    | -    | -    | 125  | ps   |
| T <sub>PD</sub>                  | Propagation delay in PLL mode              | PLL is enabled                                                                       |      |      | 650  | ps   |
| T <sub>PDBP</sub>                | Propagation delay in bypass mode           | PLL is bypassed                                                                      |      |      | 4.0  | ns   |
| T <sub>skew</sub>                | Output-to-Output Skew <sup>*3</sup>        | -                                                                                    | -    |      | 10   | ps   |
| T <sub>DC</sub>                  | Output Duty Cycle <sup>*3</sup>            | -                                                                                    | 47   | -    | 53   | %    |
| J <sub>C-C</sub>                 | Cycle to Cycle jitter                      | Differential waveform                                                                |      | 40   | 50   | ps   |
| J <sub>HF-RMS</sub>              | Phase jitter, high frequency               | RMS jitter applying PCIE Gen2 jitter mask <sup>*3</sup>                              | -    | -    | 3.1  | ps   |
|                                  |                                            | RMS jitter applying PCIE Gen3 jitter mask <sup>*3</sup>                              |      | 0.61 | 1.0  | ps   |
| J <sub>LF-RMS</sub>              | Phase jitter, low frequency                | RMS jitter applying PCIE Gen2 jitter mask <sup>*3</sup>                              | -    | -    | 3.0  | ps   |
|                                  |                                            | RMS jitter applying PCIE Gen3 jitter mask <sup>*3</sup> , commercial temp range only |      | -    | 3.0  | ps   |

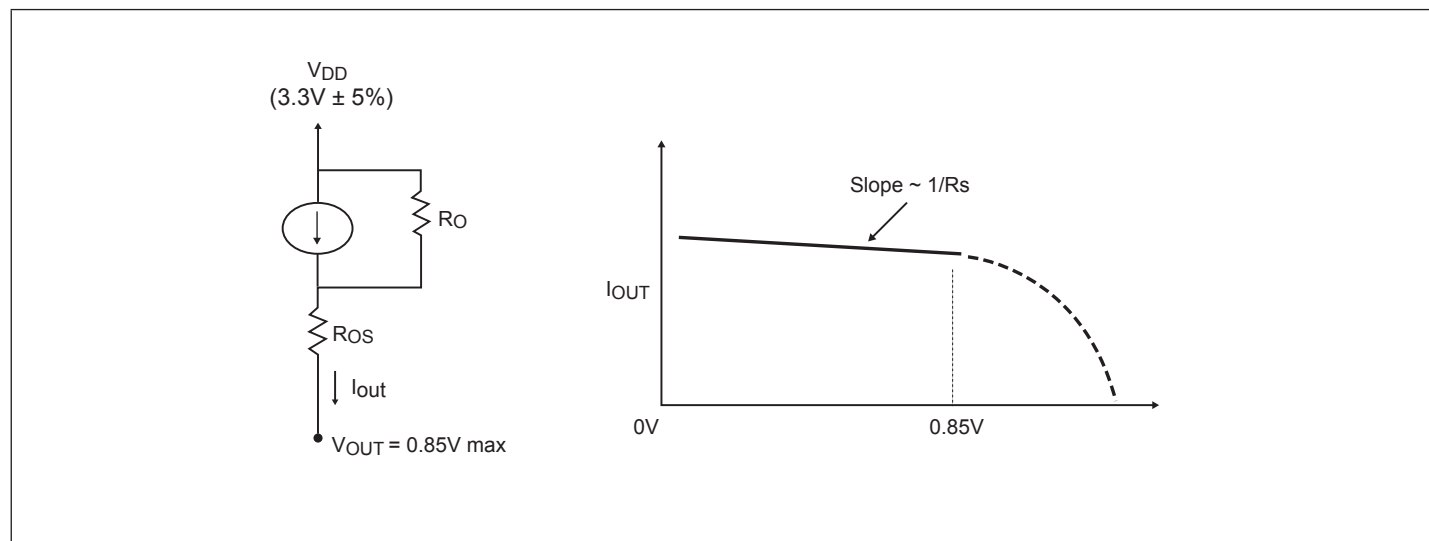
### HCSSL AC Switching Characteristics<sup>(\*1, \*2, \*3)</sup> (Over Operating Conditions) Continued..

| Symbol             | Parameter           | Conditions                                    | Min. | Typ. | Max. | Unit |
|--------------------|---------------------|-----------------------------------------------|------|------|------|------|
| PLL <sub>LBW</sub> | PLL Loop Bandwidth  | PLL_BW_SEL=1                                  | 1.3  |      | 3    | MHz  |
|                    |                     | PLL_BW_SEL=0                                  | 0.25 |      | 1    | MHz  |
| T <sub>OEN</sub>   | OE enable time      |                                               |      |      | 100  | ns   |
| T <sub>OEF</sub>   | OE disable time     |                                               |      |      | 100  | ns   |
| T <sub>SQD</sub>   | Squelch detect time | Input level is less than 150mV (single-ended) |      | 50   |      | ns   |

**Notes:**

1. Test configuration is R<sub>s</sub>=33Ω, R<sub>p</sub>=49.9Ω, and 2pF
2. Measurement is taken from Single Ended waveform.
3. Measurement is taken from Differential waveform.

### HCSSL Output Buffer Characteristics

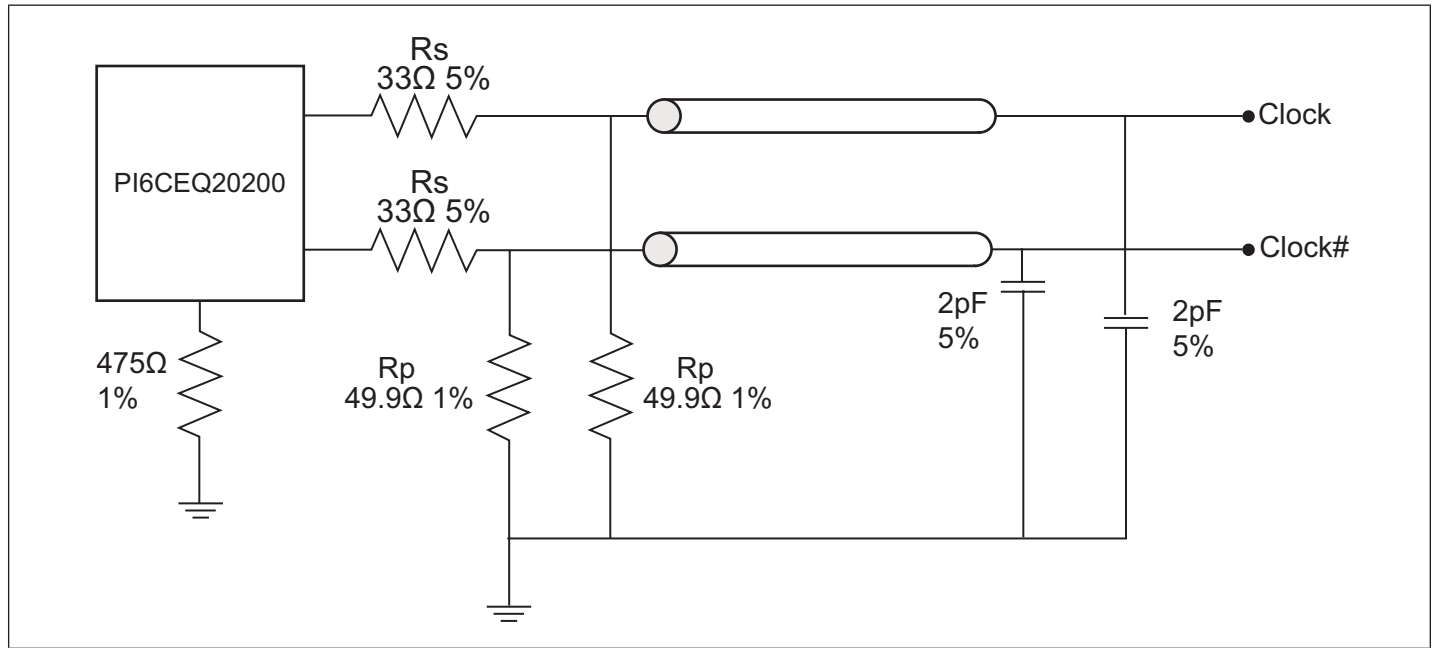


**Simplified diagram of current-mode output buffer**

### HCSSL Output Buffer Characteristics

| Symbol           | Minimum     | Maximum     |
|------------------|-------------|-------------|
| R <sub>O</sub>   | 3000Ω       | N/A         |
| R <sub>OS</sub>  | unspecified | unspecified |
| V <sub>OUT</sub> | N/A         | 850mV       |

### Configuration Test Load Board Termination for HCSL Output



### Serial Data Interface

This part is a slave only SMBus device that supports indexed block read and indexed block write protocol using a single 7-bit address and read/write bit as shown below.

### Address Assignment

| A6 | A5 | A4 | A3 | A2 | A1 | A0 | W/R |
|----|----|----|----|----|----|----|-----|
| 1  | 1  | 0  | 1  | 0  | 1  | 0  | 0/1 |

### Data Protocol

(Write)

| 1 bit     | 8 bits         | 1   | 8 bits          | 1   | 8 bits       | 1   | 8 bits      | 1   |     | 8 bits        | 1   | 1 bit    |
|-----------|----------------|-----|-----------------|-----|--------------|-----|-------------|-----|-----|---------------|-----|----------|
| Start bit | Slave Addr: D4 | Ack | Register offset | Ack | Byte Count=N | Ack | Data Byte 0 | Ack | ... | Data Byte N-1 | Ack | Stop bit |

(Read)

| 1 bit     | 8 bits         | 1   | 8 bits          | 1   | 1            | 8 bits         | 1   | 8 bits       | 1   | 8 bits      | 1   |     | 8 bits        | 1       | 1 bit    |
|-----------|----------------|-----|-----------------|-----|--------------|----------------|-----|--------------|-----|-------------|-----|-----|---------------|---------|----------|
| Start bit | Slave Addr: D4 | Ack | Register offset | Ack | Repeat start | Slave Addr: D5 | Ack | Byte Count=N | Ack | Data Byte 0 | Ack | ... | Data Byte N-1 | NOT Ack | Stop bit |

**Note:**

1. Register offset for indicating the starting register for indexed block write and indexed block read. Byte Count in write mode cannot be 0.

**Data Byte 0: Control Register**

| Bit | Name       | Control function       | Type | 0                             | 1                         | PWD |
|-----|------------|------------------------|------|-------------------------------|---------------------------|-----|
| 7   | SMB_EN     | SMBus enable           | RW   | Controlled by SMBus registers | Controlled by device pins | 1   |
| 6   | RESERVED   |                        | RW   |                               |                           | X   |
| 5   | RESERVED   |                        | RW   |                               |                           | X   |
| 4   | RESERVED   |                        | RW   |                               |                           | X   |
| 3   | RESERVED   |                        | RW   |                               |                           | X   |
| 2   | RESERVED   |                        | RW   |                               |                           | X   |
| 1   | PLL_BW_SEL | Select PLL Bandwidth   | RW   | Low BW                        | High BW                   | 1   |
| 0   | PLL Bypass | Select PLL bypass mode | RW   | PLL bypass                    | PLL enabled               | 1   |

**Data Byte 1: Control Register**

| Bit | Name     | Control function | Type | 0 | 1 | PWD |
|-----|----------|------------------|------|---|---|-----|
| 7   | RESERVED |                  | RW   |   |   | X   |
| 6   | RESERVED |                  | RW   |   |   | X   |
| 5   | RESERVED |                  | RW   |   |   | X   |
| 4   | RESERVED |                  | RW   |   |   | X   |
| 3   | RESERVED |                  | RW   |   |   | X   |
| 2   | RESERVED |                  | RW   |   |   | X   |
| 1   | RESERVED |                  | RW   |   |   | X   |
| 0   | RESERVED |                  | RW   |   |   | X   |

**Data Byte 2: Control Register**

| Bit | Name     | Control function | Type | 0 | 1 | PWD |
|-----|----------|------------------|------|---|---|-----|
| 7   | RESERVED |                  | RW   |   |   | X   |
| 6   | RESERVED |                  | RW   |   |   | X   |
| 5   | RESERVED |                  | RW   |   |   | X   |
| 4   | RESERVED |                  | RW   |   |   | X   |
| 3   | RESERVED |                  | RW   |   |   | X   |
| 2   | RESERVED |                  | RW   |   |   | X   |
| 1   | RESERVED |                  | RW   |   |   | X   |
| 0   | RESERVED |                  | RW   |   |   | X   |

**Data Byte 3: Control Register**

| Bit | Name   | Control function | Type | 0 | 1 | PWD |
|-----|--------|------------------|------|---|---|-----|
| 7   | RevID3 | Revision ID      | R    |   |   | 0   |
| 6   | RevID2 |                  | R    |   |   | 0   |
| 5   | RevID1 |                  | R    |   |   | 0   |
| 4   | RevID0 |                  | R    |   |   | 0   |
| 3   | VENID3 | Vendor ID        | R    |   |   | 0   |
| 2   | VENID2 |                  | R    |   |   | 0   |
| 1   | VENID1 |                  | R    |   |   | 0   |
| 0   | VENID0 |                  | R    |   |   | 0   |

**Data Byte 4: Control Register**

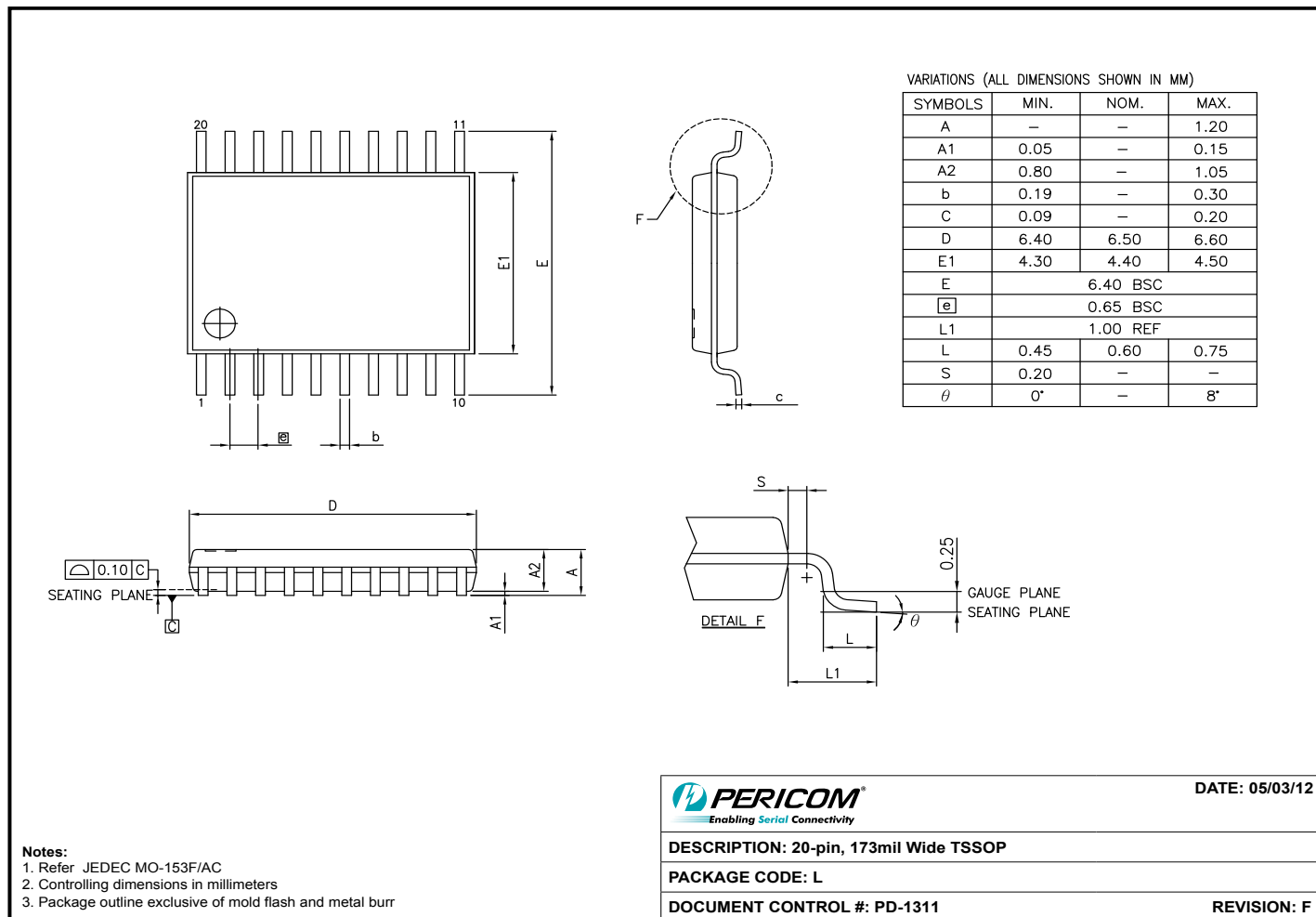
| Bit | Name      | Control function | Type | 0 | 1 | PWD |
|-----|-----------|------------------|------|---|---|-----|
| 7   | Device ID |                  | R    |   |   | 0   |
| 6   |           |                  | R    |   |   | 0   |
| 5   |           |                  | R    |   |   | 0   |
| 4   |           |                  | R    |   |   | 0   |
| 3   |           |                  | R    |   |   | 0   |
| 2   |           |                  | R    |   |   | 1   |
| 1   |           |                  | R    |   |   | 1   |
| 0   |           |                  | R    |   |   | 0   |

**Data Byte 5: Control Register**

| Bit | Name | Control function                                                                             | Type | 0 | 1 | PWD |
|-----|------|----------------------------------------------------------------------------------------------|------|---|---|-----|
| 7   | B57  | Write to this register will control how many bytes will be read back, default is 06=6 bytes. | RW   |   |   | 0   |
| 6   | B56  |                                                                                              | RW   |   |   | 0   |
| 5   | B55  |                                                                                              | RW   |   |   | 0   |
| 4   | B54  |                                                                                              | RW   |   |   | 0   |
| 3   | B53  |                                                                                              | RW   |   |   | 0   |
| 2   | B52  |                                                                                              | RW   |   |   | 1   |
| 1   | B51  |                                                                                              | RW   |   |   | 1   |
| 0   | B50  |                                                                                              | RW   |   |   | 0   |



## Packaging Mechanical: 20-Pin TSSOP (L)



12-0373

## Ordering Information

| Ordering Code    | Package Code | Package Type                                       | Operating Temperature |
|------------------|--------------|----------------------------------------------------|-----------------------|
| PI6CEQ20200LE    | L            | Pb-free & Green, 20-pin 173-mil TSSOP              | 0°C to 70°C           |
| PI6CEQ20200LEX   | L            | Pb-free & Green, 20-pin 173-mil TSSOP, Tape & Reel | 0°C to 70°C           |
| PI6CEQ20200LIE   | L            | Pb-free & Green, 20-pin 173-mil TSSOP              | -40°C to 85°C         |
| PI6CEQ20200LIEEX | L            | Pb-free & Green, 20-pin 173-mil TSSOP, Tape & Reel | -40°C to 85°C         |

Notes:

1. Thermal characteristics can be found on the company web site at [www.pericom.com/packaging/](http://www.pericom.com/packaging/)
2. E = Pb-free and Green
3. Adding an X suffix = Tape/Reel

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