

## Features

- Network support by hardware assisted Multiple PAN Address Filtering
- Advanced Hardware assisted Reduced Power Consumption
- High Performance, Low Power AVR<sup>®</sup> 8-Bit Microcontroller
- Advanced RISC Architecture
  - 135 Powerful Instructions – Most Single Clock Cycle Execution
  - 32x8 General Purpose Working Registers / On-Chip 2-cycle Multiplier
  - Up to 16 MIPS Throughput at 16 MHz and 1.8V – Fully Static Operation
- Non-volatile Program and Data Memories
  - 256K/128K/64K Bytes of In-System Self-Programmable Flash
    - Endurance: 10'000 Write/Erase Cycles @ 125°C (25'000 Cycles @ 85°C)
  - 8K/4K/2K Bytes EEPROM
    - Endurance: 20'000 Write/Erase Cycles @ 125°C (100'000 Cycles @ 25°C)
  - 32K/16K/8K Bytes Internal SRAM
- JTAG (IEEE std. 1149.1 compliant) Interface
  - Boundary-scan Capabilities According to the JTAG Standard
  - Extensive On-chip Debug Support
  - Programming of Flash EEPROM, Fuses and Lock Bits through the JTAG interface
- Peripheral Features
  - Multiple Timer/Counter & PWM channels
  - Real Time Counter with Separate Oscillator
  - 10-bit, 330 ks/s A/D Converter; Analog Comparator; On-chip Temperature Sensor
  - Master/Slave SPI Serial Interface
  - Two Programmable Serial USART
  - Byte Oriented 2-wire Serial Interface
- Advanced Interrupt Handler and Power Save Modes
- Watchdog Timer with Separate On-Chip Oscillator
- Power-on Reset and Low Current Brown-Out Detector
- Fully integrated Low Power Transceiver for 2.4 GHz ISM Band
  - High Power Amplifier support by TX spectrum side lobe suppression
  - Supported Data Rates: 250 kb/s and 500 kb/s, 1 Mb/s, 2 Mb/s
  - -100 dBm RX Sensitivity; TX Output Power up to 3.5 dBm
  - Hardware Assisted MAC (Auto-Acknowledge, Auto-Retry)
  - 32 Bit IEEE 802.15.4 Symbol Counter
  - SFD-Detection, Spreading; De-Spreading; Framing ; CRC-16 Computation
  - Antenna Diversity and TX/RX control / TX/RX 128 Byte Frame Buffer
- PLL synthesizer with 5 MHz and 500 kHz channel spacing for 2.4 GHz ISM Band
- Hardware Security (AES, True Random Generator)
- Integrated Crystal Oscillators (32.768 kHz & 16 MHz, external crystal needed)
- I/O and Package
  - 33 Programmable I/O Lines
  - 48-pad QFN (RoHS/Fully Green)
- Temperature Range: -40°C to 125°C Industrial
- Ultra Low Power consumption (1.8 to 3.6V) for AVR & Rx/Tx: 10.1mA/18.6 mA
  - CPU Active Mode (16MHz): 4.1 mA
  - 2.4GHz Transceiver: RX\_ON 6.0 mA / TX 14.5 mA (maximum TX output power)
  - Deep Sleep Mode: <700nA @ 25°C
- Speed Grade: 0 – 16 MHz @ 1.8 – 3.6V range with integrated voltage regulators

## Applications

- ZigBee<sup>®</sup> / IEEE 802.15.4-2011/2006/2003<sup>™</sup> – Full and Reduced Function Device
- General Purpose 2.4GHz ISM Band Transceiver with Microcontroller
- RF4CE, SP100, WirelessHART<sup>™</sup>, ISM Applications and IPv6 / 6LoWPAN



**8-bit AVR<sup>®</sup>**  
**Microcontroller**  
**with Low Power**  
**2.4GHz**  
**Transceiver for**  
**ZigBee and**  
**IEEE 802.15.4**

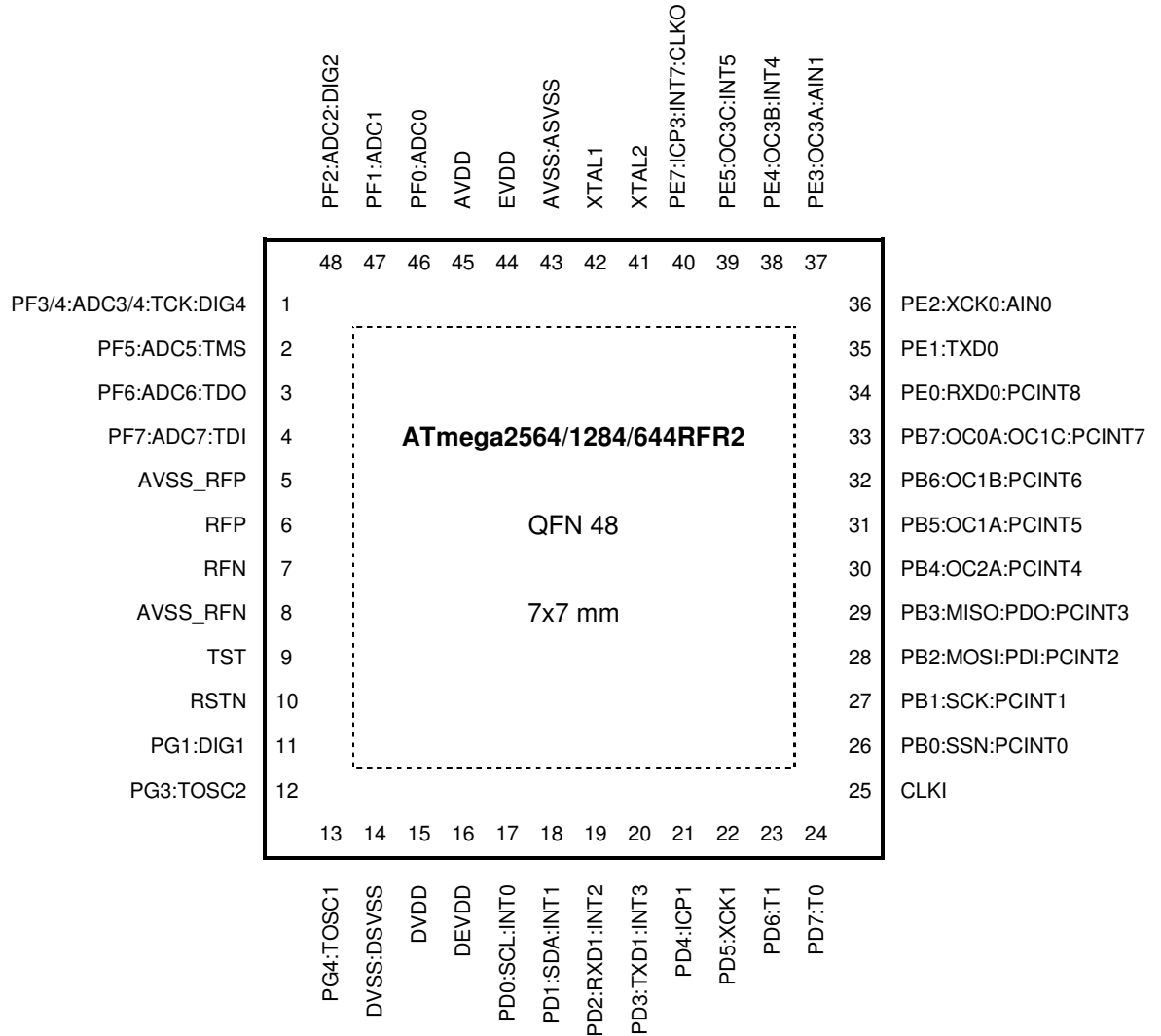
**ATmega2564RFR2**  
**ATmega1284RFR2**  
**ATmega644RFR2**

42073BS-MCU Wireless-09/14



# 1 Pin Configurations

Figure 1-1. Pinout ATmega2564/1284/644RFR2



Note: The large center pad underneath the QFN/MLF package is made of metal and internally connected to AVSS. It should be soldered or glued to the board to ensure good mechanical stability. If the center pad is left unconnected, the package might loosen from the board. It is not recommended to use the exposed paddle as a replacement of the regular AVSS pins.

## 2 Disclaimer

Typical values contained in this datasheet are based on simulation and characterization results of other AVR microcontrollers and radio transceivers manufactured in a similar process technology. Minimum and Maximum values will be available after the device is characterized.

## 3 Overview

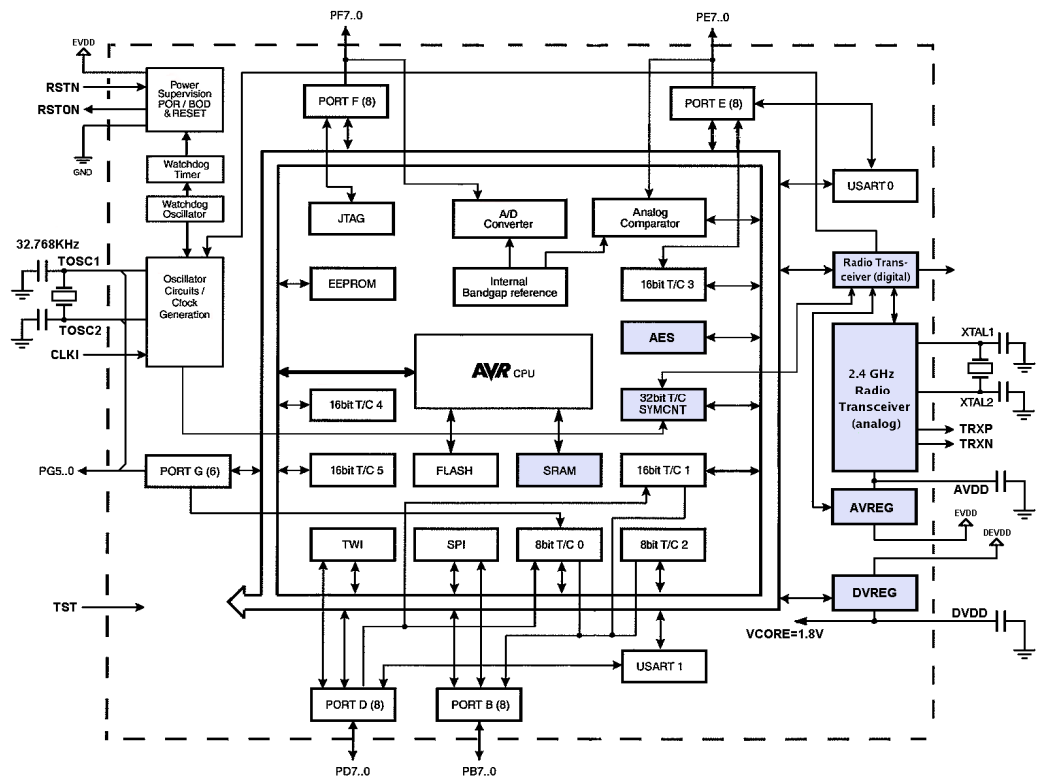
The ATmega2564/1284/644RFR2 is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture combined with a high data rate transceiver for the 2.4 GHz ISM band.

By executing powerful instructions in a single clock cycle, the device achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

The radio transceiver provides high data rates from 250 kb/s up to 2 Mb/s, frame handling, outstanding receiver sensitivity and high transmit output power enabling a very robust wireless communication.

### 3.1 Block Diagram

Figure 3-1 Block Diagram



The AVR core combines a rich instruction set with 32 general purpose working registers. All 32 registers are directly connected to the Arithmetic Logic Unit (ALU). Two independent registers can be accessed with one single instruction executed in one clock cycle. The resulting architecture is very code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers. The system includes internal voltage regulation and an advanced power management. Distinguished by the small leakage current it allows an extended operation time from battery.

The radio transceiver is a fully integrated ZigBee solution using a minimum number of external components. It combines excellent RF performance with low cost, small size and low current consumption. The radio transceiver includes a crystal stabilized fractional-N synthesizer, transmitter and receiver, and full Direct Sequence Spread

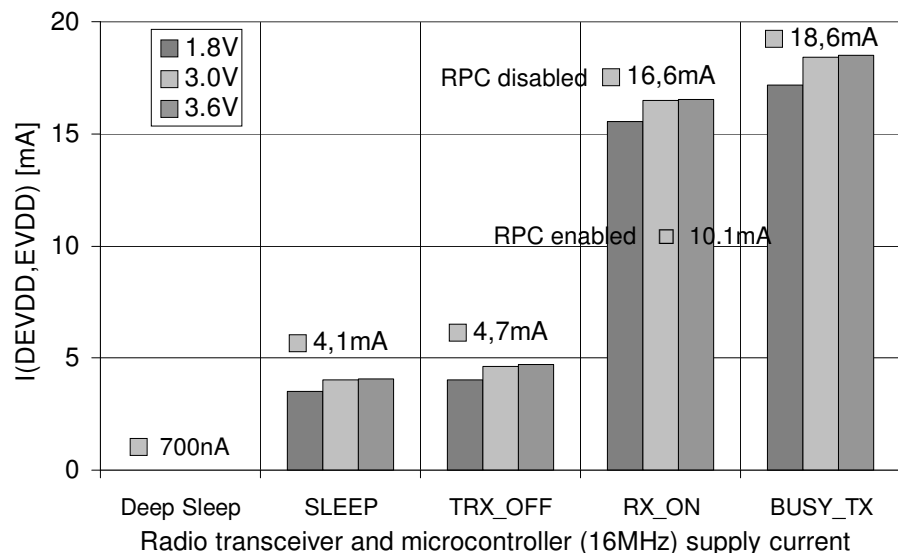
Spectrum Signal (DSSS) processing with spreading and despreading. The device is fully compatible with IEEE802.15.4-2011/2006/2003 and ZigBee standards.

The ATmega2564/1284/644RFR2 provides the following features: 256K/128K/64K Bytes of In-System Programmable (ISP) Flash with read-while-write capabilities, 8K/4K/2K Bytes EEPROM, 32K/16K/8K Bytes SRAM, up to 35 general purpose I/O lines, 32 general purpose working registers, Real Time Counter (RTC), 6 flexible Timer/Counters with compare modes and PWM, a 32 bit Timer/Counter, 2 USART, a byte oriented 2-wire Serial Interface, a 8 channel, 10 bit analog to digital converter (ADC) with an optional differential input stage with programmable gain, programmable Watchdog Timer with Internal Oscillator, a SPI serial port, IEEE std. 1149.1 compliant JTAG test interface, also used for accessing the On-chip Debug system and programming and 6 software selectable power saving modes.

The Idle mode stops the CPU while allowing the SRAM, Timer/Counters, SPI port, and interrupt system to continue functioning. The Power-down mode saves the register contents but freezes the Oscillator, disabling all other chip functions until the next interrupt or hardware reset. In Power-save mode, the asynchronous timer continues to run, allowing the user to maintain a timer base while the rest of the device is sleeping. The ADC Noise Reduction mode stops the CPU and all I/O modules except asynchronous timer and ADC, to minimize switching noise during ADC conversions. In Standby mode, the RC oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low power consumption. In Extended Standby mode, both the main RC oscillator and the asynchronous timer continue to run.

Typical supply current of the microcontroller with CPU clock set to 16MHz and the radio transceiver for the most important states is shown in the [Figure 3-2 below](#).

**Figure 3-2** Radio transceiver and microcontroller (16MHz) supply current



The transmit output power is set to maximum. If the radio transceiver is in SLEEP mode the current is dissipated by the AVR microcontroller only.

In Deep Sleep mode all major digital blocks with no data retention requirements are disconnected from main supply providing a very small leakage current. Watchdog timer, MAC symbol counter and 32.768kHz oscillator can be configured to continue to run.

The device is manufactured using Atmel's high-density nonvolatile memory technology. The On-chip ISP Flash allows the program memory to be reprogrammed in-system through an SPI serial interface, by a conventional nonvolatile memory programmer, or by on-chip boot program running on the AVR core. The boot program can use any interface to download the application program in the application Flash memory. Software in the boot Flash section will continue to run while the application Flash section is updated, providing true Read-While-Write operation. By combining an 8 bit RISC CPU with In-System Self-Programmable Flash on a monolithic chip, the Atmel ATmega2564/1284/644RFR2 is a powerful microcontroller that provides a highly flexible and cost effective solution to many embedded control applications.

The ATmega2564/1284/644RFR2 AVR is supported with a full suite of program and system development tools including: C compiler, macro assemblers, program debugger/simulators, in-circuit emulators, and evaluation kits.

## 3.2 Pin Descriptions

### 3.2.1 EVDD

External analog supply voltage.

### 3.2.2 DEVDD

External digital supply voltage.

### 3.2.3 AVDD

Regulated analog supply voltage (internally generated).

### 3.2.4 DVDD

Regulated digital supply voltage (internally generated).

### 3.2.5 DVSS

Digital ground.

### 3.2.6 AVSS

Analog ground.

### 3.2.7 Port B (PB7...PB0)

Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port B also provides functions of various special features of the ATmega2564/1284/644RFR2.

### 3.2.8 Port D (PD7...PD0)

Port D is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port D output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port D also provides functions of various special features of the ATmega2564/1284/644RFR2.

### 3.2.9 Port E (PE7,PE5...PE0)

Internally Port E is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port E output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port E pins that are externally pulled low will

source current if the pull-up resistors are activated. The Port E pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Due to the low pin count of the QFN48 package port E6 is not connected to a pin.

Port E also provides functions of various special features of the ATmega2564/1284/644RFR2.

### 3.2.10 Port F (PF7..PF5,PF4/3,PF2...PF0)

Internally Port F is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port F output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port F pins that are externally pulled low will source current if the pull-up resistors are activated. The Port F pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Due to the low pin count of the QFN48 package port F3 and F4 are connected to the same pin. The I/O configuration should be done carefully in order to avoid excessive power dissipation.

Port F also provides functions of various special features of the ATmega2564/1284/644RFR2.

### 3.2.11 Port G (PG4,PG3,PG1)

Internally Port G is a 6-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port G output buffers have symmetrical drive characteristics with both high sink and source capability. However the driver strength of PG3 and PG4 is reduced compared to the other port pins. The output voltage drop ( $V_{OH}$ ,  $V_{OL}$ ) is higher while the leakage current is smaller. As inputs, Port G pins that are externally pulled low will source current if the pull-up resistors are activated. The Port G pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Due to the low pin count of the QFN48 package port G0, G2 and G5 are not connected to a pin.

Port G also provides functions of various special features of the ATmega2564/1284/644RFR2.

### 3.2.12 AVSS\_RFP

AVSS\_RFP is a dedicated ground pin for the bi-directional, differential RF I/O port.

### 3.2.13 AVSS\_RFN

AVSS\_RFN is a dedicated ground pin for the bi-directional, differential RF I/O port.

### 3.2.14 RFP

RFP is the positive terminal for the bi-directional, differential RF I/O port.

### 3.2.15 RFN

RFN is the negative terminal for the bi-directional, differential RF I/O port.

### 3.2.16 RSTN

Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running. Shorter pulses are not guaranteed to generate a reset.

### 3.2.17 XTAL1

Input to the inverting 16MHz crystal oscillator amplifier. In general a crystal between XTAL1 and XTAL2 provides the 16MHz reference clock of the radio transceiver.

### 3.2.18 XTAL2

Output of the inverting 16MHz crystal oscillator amplifier.

## 3.2.19 TST

Programming and test mode enable pin. If pin TST is not used pull it to low.

## 3.2.20 CLKI

Input to the clock system. If selected, it provides the operating clock of the microcontroller.

## 3.3 Unused Pins

Floating pins can cause power dissipation in the digital input stage. They should be connected to an appropriate source. In normal operation modes the internal pull-up resistors can be enabled (in Reset all GPIO are configured as input and the pull-up resistors are still not enabled).

Bi-directional I/O pins shall not be connected to ground or power supply directly.

The digital input pins TST and CLKI must be connected. If unused pin TST can be connected to AVSS while CLKI should be connected to DVSS.

Output pins are driven by the device and do not float. Power supply pins respective ground supply pins are connected together internally.

XTAL1 and XTAL2 shall never be forced to supply voltage at the same time.

## 3.4 Compatibility and Feature Limitations of QFN-48 Package

### 3.4.1 AREF

The reference voltage output of the A/D converter is not connected to a pin in the ATmega2564/1284/644RFR2.

### 3.4.2 Port E6

The port E6 is not connected to a pin in the ATmega2564/1284/644RFR2. The alternate pin functions as clock input to timer 3 and external interrupt 6 are not available.

### 3.4.3 Port F3 and F4

The port F3 and F4 are connected to the same pin in the ATmega2564/1284/644RFR2. The output configuration should be done carefully in order to avoid excessive current consumption.

The alternate pin function of port F4 is used by the JTAG interface. If the JTAG interface is used the port F3 must be configured as input and the alternate pin function output DIG4 (RX/TX indicator) must be disabled. Otherwise the JTAG interface will not work. The SPIEN Fuse should be programmed in order to be able to erase a program that accidentally drive port F3.

There are just 7 single-ended input channel to the ADC available.

### 3.4.4 Port G0

The port G0 is not connected to a pin in the ATmega2564/1284/644RFR2. The alternate pin function DIG3 (inverted RX/TX indicator) is not available. If the JTAG interface is not used the DIG4 alternate pin function output of port F3 can still be used as RX/TX indicator.

### 3.4.5 Port G2

The port G2 is not connected to a pin in the ATmega2564/1284/644RFR2. The alternate pin function AMR (asynchronous automated meter reading input to timer 2) is not available.

### 3.4.6 Port G5

The port G5 is not connected to a pin in the ATmega2564/1284/644RFR2. The alternate pin function OC0B (output compare channel of 8-Bit timer 0) is not available.

### 3.4.7 RSTON

The RSTON reset output signaling the internal reset state is not connected to a pin in the ATmega2564/1284/644RFR2.

## 3.5 Configuration summary

According to the application requirements a variable memory size allows to optimize current consumption and leakage current.

**Table 3-1** Memory Configuration

Device	Flash	EEPROM	SRAM
ATmega2564RFR2	256KB	8KB	32KB
ATmega1284RFR2	128KB	4KB	16KB
ATmega644RFR2	64KB	2KB	8KB

Package and associated pin configuration are the same for all devices providing full functionality to the application.

**Table 3-2** System Configuration

Device	Package	GPIO	Serial IF	ADC channel
ATmega2564RFR2	QFN48	33	2 USART, SPI, TWI	7
ATmega1284RFR2	QFN48	33	2 USART, SPI, TWI	7
ATmega644RFR2	QFN48	33	2 USART, SPI, TWI	7

The devices are optimized for applications based on the ZigBee and the IEEE 802.15.4 specification. Having application stack, network layer, sensor interface and an excellent power control combined in a single chip many years of operation should be possible.

**Table 3-3** Application Profile

Device	Application
ATmega2564RFR2	Large Network Coordinator / Router for IEEE 802.15.4 / ZigBee Pro
ATmega1284RFR2	Network Coordinator / Router for IEEE 802.15.4
ATmega644RFR2	End node device / network processor

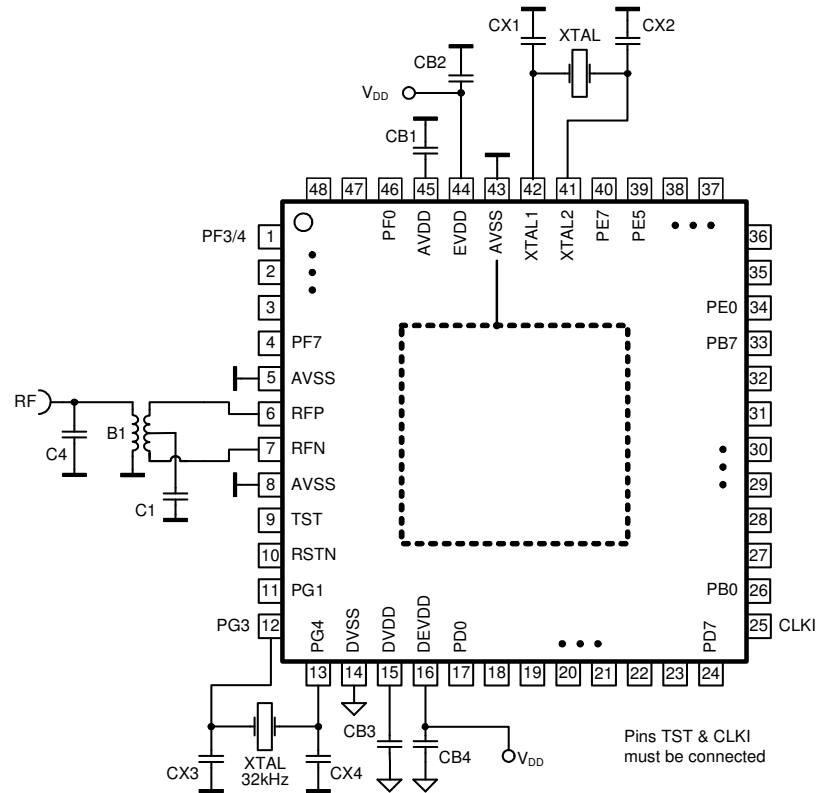


## 4 Application Circuits

### 4.1 Basic Application Schematic

A basic application schematic of the ATmega2564/1284/644RFR2 with a single-ended RF connector is shown in [Figure 4-1 below](#) and the associated Bill of Material in [Table 4-1 on page 10](#). The 50Ω single-ended RF input is transformed to the 100Ω differential RF port impedance using Balun B1. The capacitors C1 and C2 provide AC coupling of the RF input to the RF port, capacitor C4 improves matching.

**Figure 4-1.** Basic Application schematic (48-pin package)



The power supply bypass capacitors (CB2, CB4) are connected to the external analog supply pin (EVDD, pin 44) and external digital supply pin (DEVD, pin 16). The capacitor C1 provides the required AC coupling of RFN/RFP.

Floating pins can cause excessive power dissipation (e.g. during power on). They should be connected to an appropriate source. GPIO shall not be connected to ground or power supply directly.

The digital input pins TST and CLKI must be connected. If pin TST will never be used it can be connected to AVSS while an unused pin CLKI could be connected to DVSS (see chapter "Unused Pins" on page 7).

Capacitors CB1 and CB3 are bypass capacitors for the integrated analog and digital voltage regulators to ensure stable operation and to improve noise immunity. Capacitors should be placed as close as possible to the pins and should have a low-resistance and low-inductance connection to ground to achieve the best performance.

The crystal (XTAL), the two load capacitors (CX1, CX2), and the internal circuitry connected to pins XTAL1 and XTAL2 form the 16MHz crystal oscillator for the 2.4GHz transceiver. To achieve the best accuracy and stability of the reference frequency, large parasitic capacitances must be avoided. Crystal lines should be routed as short as possible and not in proximity of digital I/O signals. This is especially required for the High Data Rate Modes.

The 32.768 kHz crystal connected to the internal low power (sub 1 $\mu$ A) crystal oscillator provides a stable time reference for all low power modes including 32 Bit IEEE 802.15.4 Symbol Counter ("[MAC Symbol Counter](#)") and real time clock application using the asynchronous timer T/C2 ("[Timer/Counter2 with PWM and Asynchronous Operation](#)"). Total shunt capacitance including CX3, CX4 should not exceed 15pF across both pins. The very low supply current of the oscillator requires careful layout of the PCB and any leakage path must be avoided.

Crosstalk and radiation from switching digital signals to the crystal pins or the RF pins can degrade the system performance. The programming of minimum drive strength settings for the digital output signal is recommended (see "[DPDS0 - Port Driver Strength Register 0](#)").

**Table 4-1. Bill of Materials (BoM)**

Designator	Description	Value	Manufacturer	Part Number	Comment
B1	SMD balun SMD balun / filter	2.4 GHz	Wuerth Johanson Technology	748421245 2450FB15L0001	Filter included
CB1 CB3	LDO VREG bypass capacitor	1 $\mu$ F (100nF minimum)	AVX Murata	0603YD105KAT2A GRM188R61C105KA12D	X5R 10% 16V (0603)
CB2 CB4	Power supply bypass capacitor	1 $\mu$ F (100nF minimum)			
CX1, CX2	16MHz crystal load capacitor	12 pF	AVX Murata	06035A120JA GRP1886C1H120JA01	COG 5% 50V (0603)
CX3, CX4	32.768kHz crystal load capacitor	12 ... 25 pF			
C1, C2	RF coupling capacitor	22 pF	Epcos Epcos AVX	B37930 B37920 06035A220JAT2A	C0G 5% 50V (0402 or 0603)
C4 (optional)	RF matching	0.47 pF	Johnstech		
XTAL	Crystal	CX-4025 16 MHz SX-4025 16 MHz	ACAL Taitjen Siward	XWBBPL-F-1 A207-011	
XTAL 32kHz	Crystal				Rs=100 kOhm

## 5 Revision history

Please note that the referring page numbers in this section are referring to this document. The referring revision in this section are referring to the document revision

### Rev. 42073BS-MCU Wireless-09/14

1. Content unchanged - recreated for combined release with the datasheet.

### Rev. 8393AS-MCU Wireless-02/13

1. Initial release.



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