

Si823x Data Sheet

0.5 and 4.0 Amp ISOdrivers (2.5 and 5 kV_{RMS})

The Si823x isolated driver family combines two independent, isolated drivers into a single package. The Si8230/1/3/4 are high-side/low-side drivers, while the Si8232/5/7/8 are dual drivers. Versions with peak output currents of 0.5 A (Si8230/1/2/7) and 4.0 A (Si8233/4/5/8) are available. All drivers operate with a maximum supply voltage of 24 V.

The Si823x drivers utilize Silicon Labs' proprietary silicon isolation technology, which provides up to 5 kV_{RMS} withstand voltage per UL1577 and fast 45 ns propagation times. Driver outputs can be grounded to the same or separate grounds or connected to a positive or negative voltage. The TTL level compatible inputs with >400 mV hysteresis are available in individual control input (Si8230/2/3/5/7/8) or PWM input (Si8231/4) configurations. High integration, low propagation delay, small installed size, flexibility, and cost-effectiveness make the Si823x family ideal for a wide range of isolated MOSFET/IGBT gate drive applications.

Automotive Grade is available for certain part numbers. These products are built using automotive-specific flows at all steps in the manufacturing process to ensure the robustness and low defectivity required for automotive applications.

Industrial Applications

- Power delivery systems
- Motor control systems
- Isolated dc-dc power supplies
- Lighting control systems
- Plasma displays
- Solar and industrial inverters

Automotive Applications

- On-board chargers
- Battery management systems
- Charging stations
- Traction inverters
- Hybrid Electric Vehicles
- Battery Electric Vehicles

Safety Regulatory Approvals

- UL 1577 recognized
 - Up to 5000 V_{RMS} for 1 minute
- CSA component notice 5A approval
 - IEC 60950-1, 62368-1, 60601-1 (reinforced insulation)
- VDE certification conformity
 - VDE 0884-10
 - EN60950-1 (reinforced insulation)
- CQC certification approval
 - GB4943.1

KEY FEATURES

- Two completely isolated drivers in one package
 - Up to 5 kV_{RMS} input-to-output isolation
 - Up to 1500 V_{DC} peak driver-to-driver differential voltage
- HS/LS and dual driver versions
- Up to 8 MHz switching frequency
- 0.5 A peak output (Si8230/1/2/7)
- 4.0 A peak output (Si8233/4/5/8)
- High electromagnetic immunity
- RoHS-compliant packages:
 - SOIC-14/16 wide body
 - SOIC-16 narrow body
 - LGA-14
 - QFN-14 (pin to pin compatible with LGA-14 packages)
- AEC-Q100 qualification
- Automotive-grade OPNs available
 - AIAG compliant PPAP documentation support
 - IMDS and CAMDS listing support

1. Ordering Guide

Industrial and Automotive Grade OPNs

Industrial-grade devices (part numbers having an “-I” in their suffix) are built using well-controlled, high-quality manufacturing flows to ensure robustness and reliability. Qualifications are compliant with JEDEC, and defect reduction methodologies are used throughout definition, design, evaluation, qualification, and mass production steps.

Automotive-grade devices (part numbers having an “-A” in their suffix) are built using automotive-specific flows at all steps in the manufacturing process to ensure robustness and low defectivity. These devices are supported with AIAG-compliant Production Part Approval Process (PPAP) documentation, and feature International Material Data System (IMDS) and China Automotive Material Data System (CAMDS) listing. Qualifications are compliant with AEC-Q100, and a zero-defect methodology is maintained throughout definition, design, evaluation, qualification, and mass production steps.

Table 1.1. Si823x Ordering Guide ^{1, 2, 4}

Ordering Part Number (OPN)	Automotive OPN ^{5,6}	Inputs	Configuration	Peak Current	UVLO Voltage	Isolation Rating	Package Type		
Wide Body (WB) Package Options									
Si8230BB-D-IS	Si8230BB-AS	VIA, VIB	High Side/ Low Side	0.5 A	8 V	2.5 kVrms	SOIC-16 Wide Body		
Si8231BB-D-IS	Si8231BB-AS	PWM	High Side/ Low Side						
Si8232BB-D-IS	Si8232BB-AS	VIA,VIB	Dual Driver						
Si8234CB-D-IS	Si8234CB-AS	PWM	High Side/ Low Side	4.0 A	10 V			2.5 kVrms	SOIC-16 Wide Body
Si8233BB-D-IS	Si8233BB-AS	VIA,VIB	High Side/ Low Side		8 V				
Si8234BB-D-IS	Si8234BB-AS	PWM	High Side/ Low Side						
Si8235BB-D-IS	Si8235BB-AS	VIA,VIB	Dual Driver						
Si8230AB-D-IS	Si8230AB-AS	VIA, VIB	High Side/ Low Side	0.5 A	5 V	2.5 kVrms	SOIC-16 Wide Body		
Si8231AB-D-IS	Si8231AB-AS	PWM							
Si8232AB-D-IS	Si8232AB-AS	VIA,VIB	Dual Driver						
Si8233AB-D-IS	Si8233AB-AS	VIA,VIB	High Side/ Low Side	4.0 A	5 V			2.5 kVrms	SOIC-16 Wide Body
Si8234AB-D-IS	Si8234AB-AS	PWM							
Si8235AB-D-IS	Si8235AB-AS	VIA,VIB	Dual Driver						
Narrow Body (NB) Package Options									
Si8230BB-D-IS1	Si8230BB-AS1	VIA,VIB	High Side/ Low Side	0.5 A	8 V	2.5 kVrms	SOIC-16 Narrow Body		
Si8231BB-D-IS1	Si8231BB-AS1	PWM	High Side/ Low Side						
Si8232BB-D-IS1	Si8232BB-AS1	VIA,VIB	Dual Driver						

Ordering Part Number (OPN)	Automotive OPN ^{5,6}	Inputs	Configuration	Peak Current	UVLO Voltage	Isolation Rating	Package Type
Si8233BB-D-IS1	Si8233BB-AS1	VIA,VIB	High Side/ Low Side	4.0 A	8 V	2.5 kVrms	SOIC-16 Narrow Body
Si8234BB-D-IS1	Si8234BB-AS1	PWM	High Side/ Low Side				
Si8235BB-D-IS1	Si8235BB-AS1	VIA,VIB	Dual Driver			1.0 kVrms	
Si8235BA-D-IS1	Si8235BA-AS1	VIA,VIB	Dual Driver				
Si8230AB-D-IS1	Si8230AB-AS1	VIA,VIB	High Side/ Low Side	0.5 A	5 V	2.5 kVrms	SOIC-16 Narrow Body
Si8231AB-D-IS1	Si8231AB-AS1	PWM					
Si8232AB-D-IS1	Si8232AB-AS1	VIA,VIB	Dual Driver	4.0 A	5 V		
Si8233AB-D-IS1	Si8233AB-AS1	VIA,VIB	High Side/ Low Side				
Si8234AB-D-IS1	Si8234AB-AS1	PWM					
Si8235AB-D-IS1	Si8235AB-AS1	VIA,VIB	Dual Driver				
Si8230BC-D-IS1	Si8230BC-AS1	VIA,VIB	High Side/ Low Side	0.5 A	8 V	3.75 kVrms	SOIC-16 Narrow Body
Si8231BC-D-IS1	Si8231BC-AS1	PWM	High Side/ Low Side				
Si8232BC-D-IS1	Si8232BC-AS1	VIA,VIB	Dual Driver				
Si8233BC-D-IS1	Si8233BC-AS1	VIA,VIB	High Side/ Low Side	4.0 A	8 V	3.75 kVrms	SOIC-16 Narrow Body
Si8234BC-D-IS1	Si8234BC-AS1	PWM	High Side/ Low Side				
Si8235BC-D-IS1	Si8235BC-AS1	VIA,VIB	Dual Driver			1.0 kVrms	
Si8235BA-D-IS1	Si8235BA-AS1	VIA,VIB	Dual Driver				
Si8230AC-D-IS1	Si8230AC-AS1	VIA,VIB	High Side/ Low Side	0.5 A	5 V	3.75 kVrms	SOIC-16 Narrow Body
Si8231AC-D-IS1	Si8231AC-AS1	PWM					
Si8232AC-D-IS1	Si8232AC-AS1	VIA,VIB	Dual Driver				
Si8233AC-D-IS1	Si8233AC-AS1	VIA,VIB	High Side/ Low Side				
Si8234AC-D-IS1	Si8234AC-AS1	PWM					
Si8235AC-D-IS1	Si8235AC-AS1	VIA,VIB	Dual Driver				
LGA Package Options							
Si8233CB-D-IM	Si8233CB-AM	VIA,VIB	High Side/ Low Side	4.0 A	10 V	2.5 kVrms	LGA-14 5x5 mm
Si8233BB-D-IM	Si8233BB-AM				8 V		
Si8233AB-D-IM	Si8233AB-AM				5 V		
Si8234BB-D-IM	Si8234BB-AM	PWM			8 V		
Si8234AB-D-IM	Si8234AB-AM				5 V		
Si8235BB-D-IM	Si8235BB-AM	VIA,VIB	Dual Driver		8 V		
Si8235AB-D-IM	Si8235AB-AM				5 V		
QFN Package Options							

Ordering Part Number (OPN)	Automotive OPN ^{5,6}	Inputs	Configuration	Peak Current	UVLO Voltage	Isolation Rating	Package Type
Si8233AB-D-IM1	Si8233AB-AM1	VIA, VIB	High Side/ Low Side	4.0 A	5 V	2.5 kVrms	QFN-14
Si8233BB-D-IM1	Si8233BB-AM1				8 V		
Si8234AB-D-IM1	Si8234AB-AM1	PWM			5 V		
Si8234BB-D-IM1	Si8234BB-AM1				8 V		
Si8235AB-D-IM1	Si8235AB-AM1	VIA, VIB	Dual Driver		5 V		
Si8235BB-D-IM1	Si8235BB-AM1				8 V		
5 kV Ordering Options							
Si8230BD-D-IS	Si8230BD-AS	VIA, VIB	High Side/ Low Side	0.5 A	8 V	5.0 kVrms	SOIC-16 Wide Body
Si8231BD-D-IS	Si8231BD-AS	PWM	High Side/ Low Side				
Si8232BD-D-IS	Si8232BD-AS	VIA, VIB	Dual Driver				
Si8233BD-D-IS	Si8233BD-AS	VIA, VIB	High Side/ Low Side	4.0 A			
Si8234BD-D-IS	Si8234BD-AS	PWM	High Side/ Low Side				
Si8235BD-D-IS	Si8235BD-AS	VIA, VIB	Dual Driver				
Si8230AD-D-IS	Si8230AD-AS	VIA, VIB	High Side/ Low Side	0.5 A	5 V	5.0 kVrms	SOIC-16 Wide Body
Si8231AD-D-IS	Si8231AD-AS	PWM					
Si8232AD-D-IS	Si8232AD-AS	VIA, VIB	Dual Driver				
Si8233AD-D-IS	Si8233AD-AS	VIA, VIB	High Side/ Low Side	4.0 A	5 V		
Si8234AD-D-IS	Si8234AD-AS	PWM					
Si8235AD-D-IS	Si8235AD-AS	VIA, VIB	Dual Driver				
Si8230AD-D-IS3	Si8230AD-AS3	VIA, VIB	High Side/ Low Side	0.5 A	8 V		
Si8230BD-D-IS3	Si8230BD-AS3	VIA, VIB			5 V		
Si8233AD-D-IS3	Si8233AD-AS3	VIA, VIB		4.0 A	8 V		
Si8233BD-D-IS3	Si8233BD-AS3	VIA, VIB			5 V		
Si8235AD-D-IS3	Si8235AD-AS3	VIA, VIB	Dual Driver		8 V		
Si8235BD-D-IS3	Si8235BD-AS3	VIA, VIB	Dual Driver				
3 V VDDI Ordering Options							
Si8237AB-D-IS1	Si8237AB-AS1	VIA, VIB	Dual Driver	0.5 A	5 V	2.5 kVrms	SOIC-16 Narrow Body
Si8237BB-D-IS1	Si8237BB-AS1	VIA, VIB	Dual Driver		8 V		
Si8238AB-D-IS1	Si8238AB-AS1	VIA, VIB	Dual Driver	4.0 A	5 V		
Si8238BB-D-IS1	Si8238BB-AS1	VIA, VIB	Dual Driver		8 V		
Si8237AC-D-IS1	Si8237AC-AS1	VIA, VIB	Dual Driver	0.5 A	5 V	3.75 kVrms	SOIC-16 Narrow Body
Si8237BC-D-IS1	Si8237BC-AS1	VIA, VIB	Dual Driver		8 V		
Si8238AC-D-IS1	Si8238AC-AS1	VIA, VIB	Dual Driver	4.0 A	5 V		
Si8238BC-D-IS1	Si8238BC-AS1	VIA, VIB	Dual Driver		8 V		

Ordering Part Number (OPN)	Automotive OPN ^{5,6}	Inputs	Configuration	Peak Current	UVLO Voltage	Isolation Rating	Package Type
Si8237AD-D-IS	Si8237AD-AS	VIA, VIB	Dual Driver	0.5 A	5 V	5.0 kVrms	SOIC-16 Wide Body
Si8237BD-D-IS	Si8237BD-AS	VIA, VIB	Dual Driver		8 V		
Si8238AD-D-IS	Si8238AD-AS	VIA, VIB	Dual Driver	4.0 A	5 V		
Si8238BD-D-IS	Si8238BD-AS	VIA, VIB	Dual Driver		8 V		
Si8238AD-D-IS3	Si8238AD-AS3	VIA, VIB	Dual Driver		5 V		SOIC-14 Wide Body with increased creepage
Si8238BD-D-IS3	Si8238BD-AS3	VIA, VIB	Dual Driver		8 V		

1. All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.
2. "Si" and "SI" are used interchangeably.
3. An "R" at the end of the part number denotes tape and reel packaging option.
4. The temperature ranges is –40 to +125 °C.
5. Automotive-Grade devices (with an "–A" suffix) are identical in construction materials, topside marking, and electrical parameters to their Industrial-Grade (with an "–I" suffix) version counterparts. Automotive-Grade products are produced utilizing full automotive process flows and additional statistical process controls throughout the manufacturing flow. The Automotive-Grade part number is included on shipping labels.
6. In the top markings of each device, the Manufacturing Code represented by either "RTTTTT" or "TTTTTT" contains as its first character a letter in the range N through Z to indicate Automotive-Grade.

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2. System Overview

2.1 Top Level Block Diagrams



Figure 2.1. Si8230/3 Two-Input High-Side/Low-Side Isolated Drivers

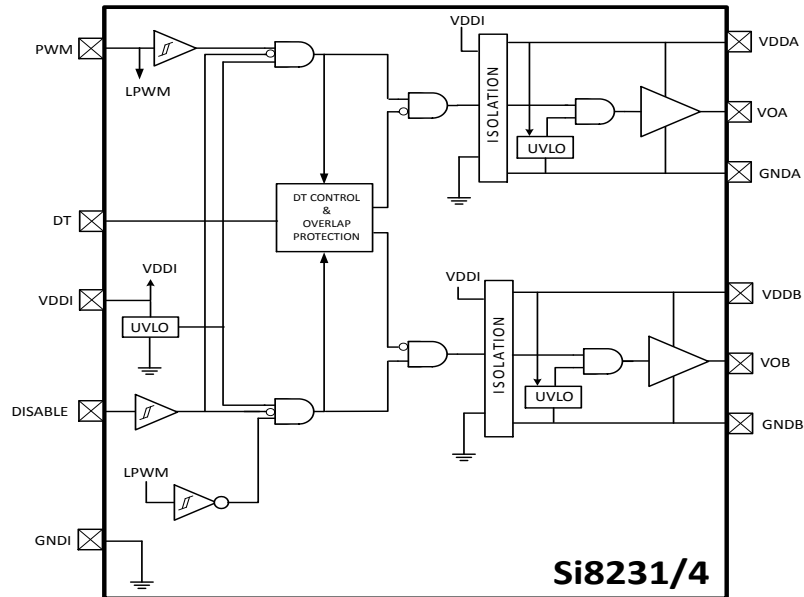


Figure 2.2. Si8231/4 Single-Input High-Side/Low-Side Isolated Drivers

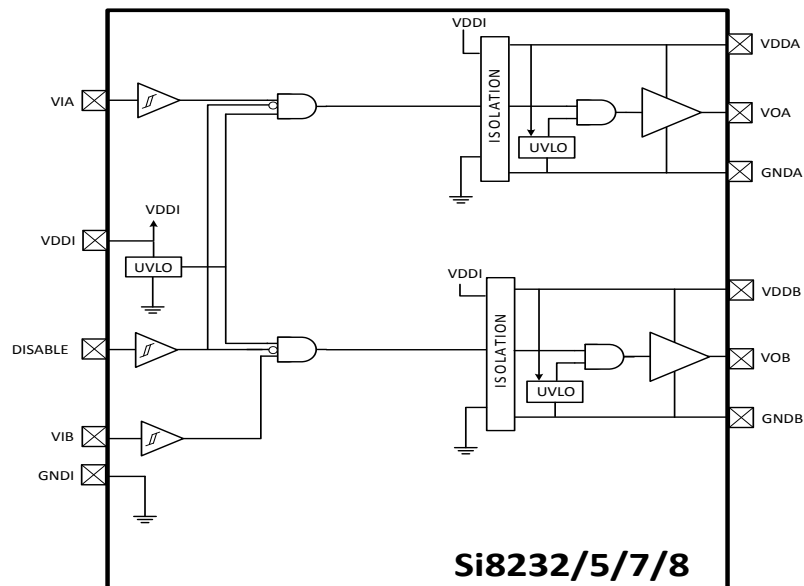


Figure 2.3. Si8232/5/7/8 Dual Isolated Drivers

2.2 Functional Description

The operation of an Si823x channel is analogous to that of an optocoupler and gate driver, except an RF carrier is modulated instead of light. This simple architecture provides a robust isolated data path and requires no special considerations or initialization at start-up. A simplified block diagram for a single Si823x channel is shown in the figure below.



Figure 2.4. Simplified Channel Diagram

A channel consists of an RF Transmitter and RF Receiver separated by a semiconductor-based isolation barrier. Referring to the Transmitter, input A modulates the carrier provided by an RF oscillator using on/off keying. The Receiver contains a demodulator that decodes the input state according to its RF energy content and applies the result to output B via the output driver. This RF on/off keying scheme is superior to pulse code schemes as it provides best-in-class noise immunity, low power consumption, and better immunity to magnetic fields. See the figure below for more details.



Figure 2.5. Modulation Scheme

2.3 Typical Operating Characteristics (0.5 Amp)

The typical performance characteristics depicted in [Figure 2.6 Rise/Fall Time vs. Supply Voltage](#) on page 11 through [Figure 2.15 Output Source Current vs. Temperature](#) on page 12 are for information purposes only. Refer to [Table 3.1 Electrical Characteristics](#)¹ on page 24 for actual specification limits.



Figure 2.6. Rise/Fall Time vs. Supply Voltage

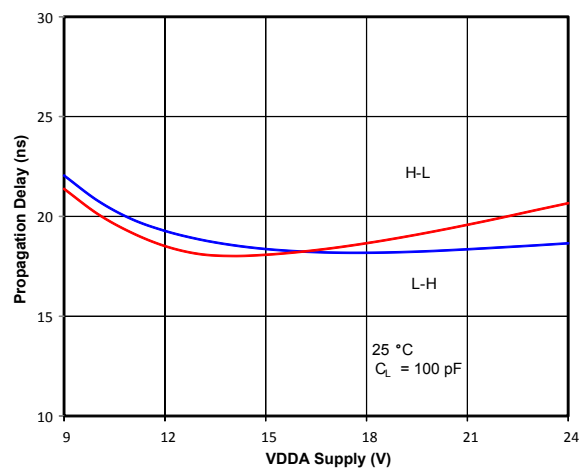


Figure 2.7. Propagation Delay vs. Supply Voltage



Figure 2.8. Rise/Fall Time vs. Load



Figure 2.9. Propagation Delay vs. Load



Figure 2.10. Propagation Delay vs. Temperature



Figure 2.11. Supply Current vs. Temperature



Figure 2.12. Supply Current vs. Supply Voltage

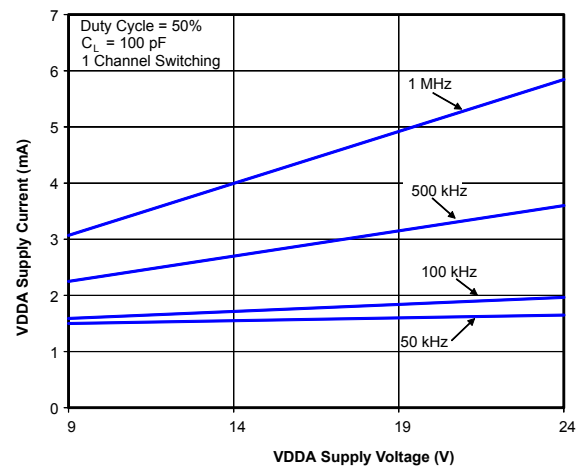


Figure 2.13. Supply Current vs. Supply Voltage



Figure 2.14. Output Source Current vs. Supply Voltage



Figure 2.15. Output Source Current vs. Temperature

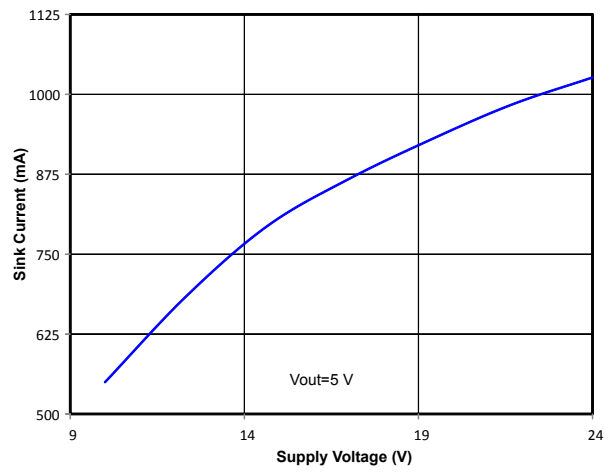


Figure 2.16. Output Sink Current vs. Supply Voltage

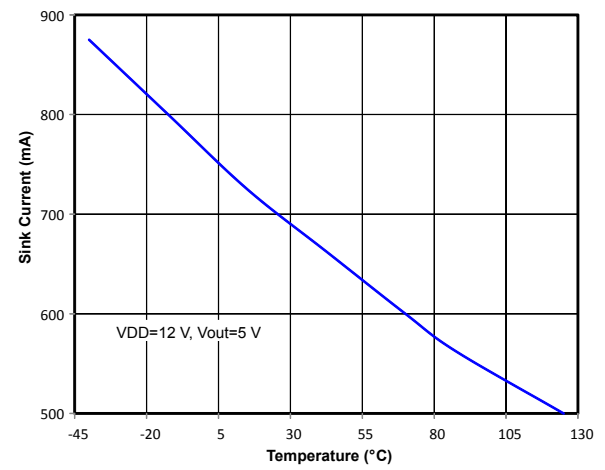


Figure 2.17. Output Sink Current vs. Temperature

2.4 Typical Operating Characteristics (4.0 Amp)

The typical performance characteristics depicted in [Figure 2.18 Rise/Fall Time vs. Supply Voltage](#) on page 14 through [Figure 2.27 Output Source Current vs. Temperature](#) on page 15 are for information purposes only. Refer to [Table 3.1 Electrical Characteristics¹](#) on page 24 for actual specification limits.



Figure 2.18. Rise/Fall Time vs. Supply Voltage



Figure 2.19. Propagation Delay vs. Supply Voltage



Figure 2.20. Rise/Fall Time vs. Load



Figure 2.21. Propagation Delay vs. Load



Figure 2.22. Propagation Delay vs. Temperature

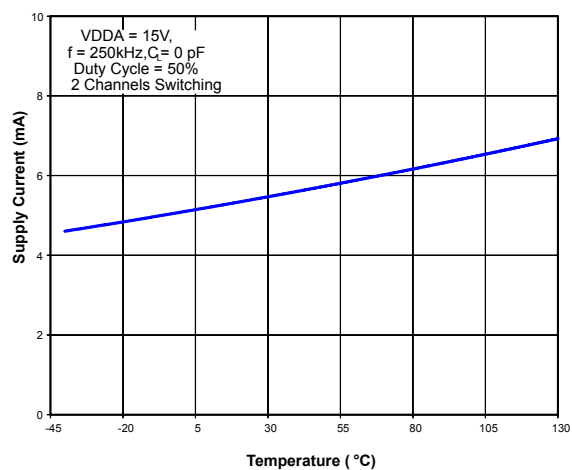


Figure 2.23. Supply Current vs. Temperature

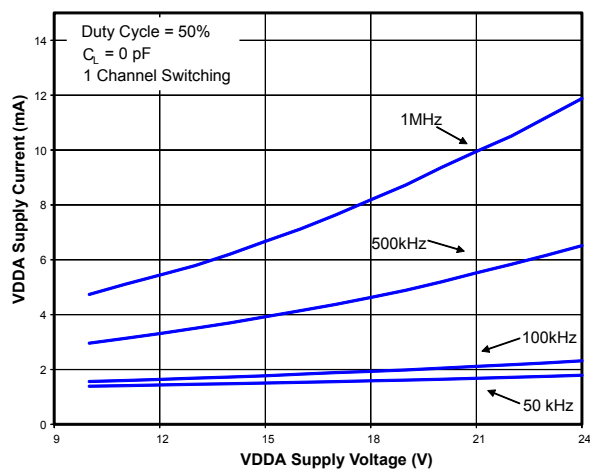


Figure 2.24. Supply Current vs. Supply Voltage

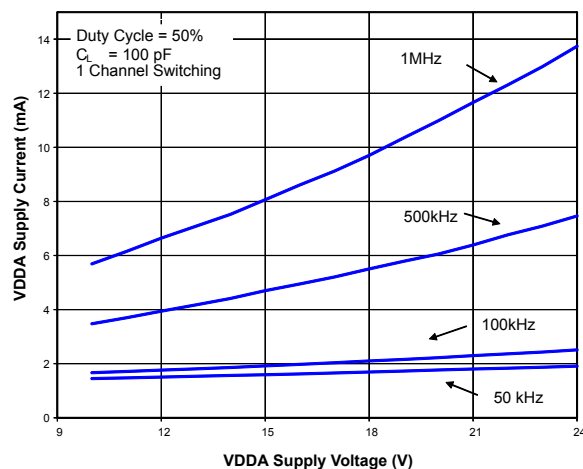


Figure 2.25. Supply Current vs. Supply Voltage



Figure 2.26. Output Source Current vs. Supply Voltage

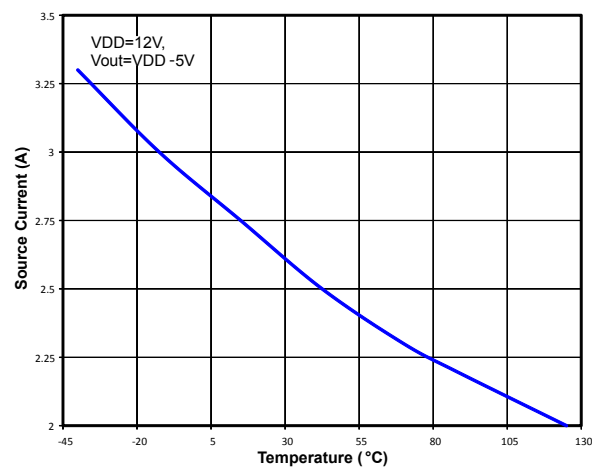


Figure 2.27. Output Source Current vs. Temperature



Figure 2.28. Output Sink Current vs. Supply Voltage



Figure 2.29. Output Sink Current vs. Temperature

2.5 Family Overview and Logic Operation During Startup

The Si823x family of isolated drivers consists of high-side, low-side, and dual driver configurations.

2.5.1 Products

The table below shows the configuration and functional overview for each product in this family.

Table 2.1. Si823x Family Overview

Part Number	Configuration	Overlap Protection	Programmable Dead Time	Inputs	Peak Output Current (A)
Si8230	High-Side/Low-Side	✓	✓	VIA, VIB	0.5
Si8231	High-Side/Low-Side	✓	✓	PWM	0.5
Si8232/7	Dual Driver	—	—	VIA, VIB	0.5
Si8233	High-Side/Low-Side	✓	✓	VIA, VIB	4.0
Si8234	High-Side/Low-Side	✓	✓	PWM	4.0
Si8235/8	Dual Driver	—	—	VIA, VIB	4.0

2.5.2 Device Behavior

The table below consists of truth tables for the Si8230/3, Si8231/4, and Si8232/5/7/8 families.

Table 2.2. Si823x Family Truth Table¹

Si8230/3 (High-Side/Low-Side) Truth Table						
Inputs		VDDI State	Disable	Output		Notes
VIA	VIB			VOA	VOB	
L	L	Powered	L	L	L	Output transition occurs after internal dead time expires.
L	H	Powered	L	L	H	Output transition occurs after internal dead time expires.
H	L	Powered	L	H	L	Output transition occurs after internal dead time expires.
H	H	Powered	L	L	L	Invalid state. Output transition occurs after internal dead time expires.
X ²	X ²	Unpowered	X	L	L	Output returns to input state within 7 μs of VDDI power restoration.
X	X	Powered	H	L	L	Device is disabled.
Si8231/4 (PWM Input High-Side/Low-Side) Truth Table						
PWM Input		VDDI State	Disable	Output		Notes
				VOA	VOB	
H		Powered	L	H	L	Output transition occurs after internal dead time expires.
L		Powered	L	L	H	Output transition occurs after internal dead time expires.
X ²		Unpowered	X	L	L	Output returns to input state within 7 μs of VDDI power restoration.
X		Powered	H	L	L	Device is disabled.
Si8232/5/7/8 (Dual Driver) Truth Table						
Inputs		VDDI State	Disable	Output		Notes
VIA	VIB			VOA	VOB	
L	L	Powered	L	L	L	Output transition occurs immediately (no internal dead time).
L	H	Powered	L	L	H	Output transition occurs immediately (no internal dead time).
H	L	Powered	L	H	L	Output transition occurs immediately (no internal dead time).
H	H	Powered	L	H	H	Output transition occurs immediately (no internal dead time).
X ²	X ²	Unpowered	X	L	L	Output returns to input state within 7 μs of VDDI power restoration.
X	X	Powered	H	L	L	Device is disabled.
Notes:						
1. This truth table assumes VDDA and VDDB are powered. If VDDA and VDDB are below UVLO, see 2.9 Undervoltage Lockout Operation for more information.						
2. Note that an input can power the input die through an internal diode if its source has adequate current.						

2.6 Power Supply Connections

Isolation requirements mandate individual supplies for VDDI, VDDA, and VDDDB. The decoupling caps for these supplies must be placed as close to the VDD and GND pins of the Si823x as possible. The optimum values for these capacitors depend on load current and the distance between the chip and the regulator that powers it. Low effective series resistance (ESR) capacitors, such as Tantalum, are recommended.

2.7 Power Dissipation Considerations

Proper system design must assure that the Si823x operates within safe thermal limits across the entire load range. The Si823x total power dissipation is the sum of the power dissipated by bias supply current, internal parasitic switching losses, and power dissipated by the series gate resistor and load. Equation 1 shows total Si823x power dissipation.

$$P_D = (V_{DDI})(I_{DDI}) + 2(I_{DD2})(V_{DD2}) + \left(f\left(Q_G\right)\left(V_{DD2}\right)\left[\frac{R_P}{R_P + R_G}\right] + \left(f\left(Q_G\right)\left(V_{DD2}\right)\left[\frac{R_N}{R_N + R_G}\right] + 2fC_{int}V_{DD2}^2\right)$$

where:

P_D is the total Si823x device power dissipation (W)

I_{DDI} is the input-side maximum bias current (3 mA)

I_{DD2} is the driver die maximum bias current (2.5 mA)

C_{int} is the internal parasitic capacitance (75 pF for the 0.5 A driver and 370 pF for the 4.0 A driver)

V_{DDI} is the input-side VDD supply voltage (2.7 to 5.5 V)

V_{DD2} is the driver-side supply voltage (10 to 24 V)

f is the switching frequency (Hz)

Q_G is the gate charge of the FET being driven

R_G is the external gate resistor

R_P is the $R_{DS(ON)}$ of the driver pull-up switch: ($R_P = 15 \Omega$ for the 0.5 A driver; $R_P = 2.7 \Omega$ for the 4.0 A driver)

R_N is the $R_{DS(ON)}$ of the driver pull-down switch: ($R_N = 5 \Omega$ for the 0.5 A driver and 1Ω for the 4.0 A driver)

Equation 1

Power dissipation example for 0.5 A driver using Equation 1 with the following givens:

$$V_{DD1} = 5.0 \text{ V}$$

$$V_{DD2} = 12 \text{ V}$$

$$f = 350 \text{ kHz}$$

$$R_G = 22 \Omega$$

$$Q_G = 25 \text{ nC}$$

$$P_d = 0.015 + 0.060 + (350 \times 10^3)(25 \times 10^{-9})\left(12\right)\left(\frac{5}{5 + 22}\right) + (350 \times 10^3)(25 \times 10^{-9})(12)\left(\frac{15}{15 + 22}\right) + 2[(350 \times 10^3)(75 \times 10^{-12})(144)] = 145 \text{ mW}$$

From which the driver junction temperature is calculated using Equation 2, where:

P_d is the total Si823x device power dissipation (W)

θ_{ja} is the thermal resistance from junction to air (105 °C/W in this example)

T_A is the ambient temperature

$$T_j = P_d \times \theta_{ja} \times T_A = (0.145)(105) + 20 = 35.2 \text{ } ^\circ\text{C}$$

The maximum power dissipation allowable for the Si823x is a function of the package thermal resistance, ambient temperature, and maximum allowable junction temperature, as shown in Equation 2:

$$P_{Dmax} \leq \frac{T_{jmax} - T_A}{\theta_{ja}}$$

where:

P_{Dmax} = Maximum Si823x power dissipation (W)

T_{jmax} = Si823x maximum junction temperature (150 °C)

T_A = Ambient temperature (20 °C)

θ_{ja} = Si823x junction-to-air thermal resistance (105 °C/W)

Equation 2

Substituting values for P_{Dmax} , T_{jmax} , T_A , and θ_{ja} into Equation 2 results in a maximum allowable total power dissipation of 1.29 W. Maximum allowable load is found by substituting this limit and the appropriate data sheet values from [Table 3.1 Electrical Characteristics¹](#) on page 24 into Equation 1 and simplifying. The result is Equation 3 (0.5 A driver) and Equation 4 (4.0 A driver), both of which assume $V_{DDI} = 5 \text{ V}$ and $V_{DDA} = V_{ddb} = 18 \text{ V}$.

$$Q_{G(MAX)} = \frac{0.164}{f} - 3.05 \times 10^{-9}$$

Equation 3

$$Q_{G(MAX)} = \frac{0.634}{f} - 5.81 \times 10^{-9}$$

Equation 4

Equation 3 and Equation 4 are graphed in the figure below, where the points along the load line represent the package dissipation-limited value of CL for the corresponding switching frequency.



2.8 Layout Considerations

It is most important to minimize ringing in the drive path and noise on the Si823x VDD lines. Care must be taken to minimize parasitic inductance in these paths by locating the Si823x as close to the device it is driving as possible. In addition, the VDD supply and ground trace paths must be kept short. For this reason, the use of power and ground planes is highly recommended. A split ground plane system having separate ground and VDD planes for power devices and small signal components provides the best overall noise performance.

2.9 Undervoltage Lockout Operation

Device behavior during start-up, normal operation and shutdown is shown in [Figure 2.30 Device Behavior during Normal Operation and Shutdown on page 21](#), where UVLO+ and UVLO- are the positive-going and negative-going thresholds respectively. Note that outputs VOA and VOB default low when input side power supply (VDDI) is not present.

2.9.1 Device Startup

Outputs VOA and VOB are held low during power-up until VDD is above the UVLO threshold for time period tSTART. Following this, the outputs follow the states of inputs VIA and VIB.

2.9.2 Undervoltage Lockout

Undervoltage Lockout (UVLO) is provided to prevent erroneous operation during device startup and shutdown or when VDD is below its specified operating circuits range. The input (control) side, Driver A and Driver B, each have their own undervoltage lockout monitors.

The Si823x input side enters UVLO when $VDDI \leq VDDI_{UV-}$, and exits UVLO when $VDDI > VDDI_{UV+}$. The driver outputs, VOA and VOB, remain low when the input side of the Si823x is in UVLO and their respective VDD supply (VDDA, VDDB) is within tolerance. Each driver output can enter or exit UVLO independently. For example, VOA unconditionally enters UVLO when VDDA falls below $VDDA_{UV-}$ and exits UVLO when VDDA rises above $VDDA_{UV+}$.

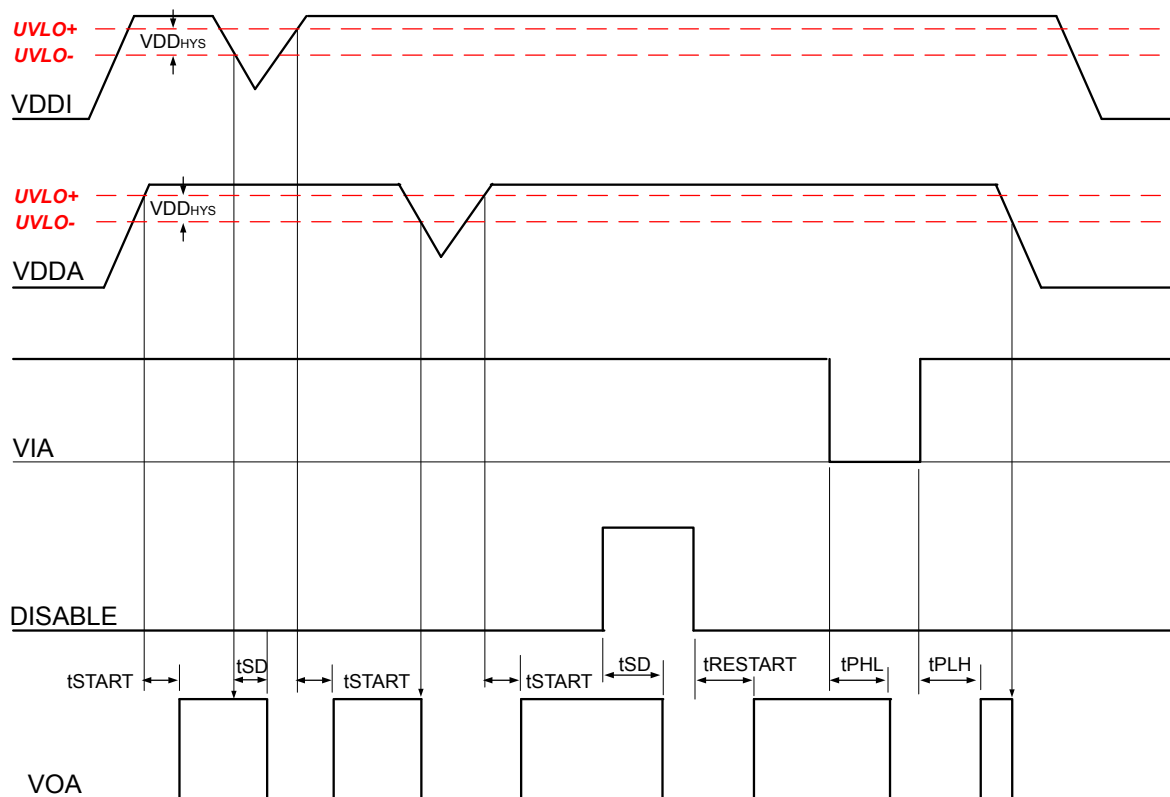


Figure 2.30. Device Behavior during Normal Operation and Shutdown

2.9.3 Undervoltage Lockout (UVLO)

The UVLO circuit unconditionally drives VO low when VDD is below the lockout threshold. Upon power up, the Si823x is maintained in UVLO until VDD rises above VDD_{UV+} . During power down, the Si823x enters UVLO when VDD falls below the UVLO threshold plus hysteresis (i.e., $VDD \leq VDD_{UV+} - VDD_{HYS}$).

2.9.4 Control Inputs

VIA, VIB, and PWM inputs are high-true, TTL level-compatible logic inputs. A logic high signal on VIA or VIB causes the corresponding output to go high. For PWM input versions (Si8231/4), VOA is high and VOB is low when the PWM input is high, and VOA is low and VOB is high when the PWM input is low.

2.9.5 Disable Input

When brought high, the DISABLE input unconditionally drives VOA and VOB low regardless of the states of VIA and VIB. Device operation terminates within t_{SD} after $DISABLE = V_{IH}$ and resumes within $t_{RESTART}$ after $DISABLE = V_{IL}$. The DISABLE input has no effect if VDDI is below its UVLO level (i.e., VOA, VOB remain low).

2.10 Programmable Dead Time and Overlap Protection

All high-side/low-side drivers (Si8230/1/3/4) include programmable overlap protection to prevent outputs VOA and VOB from being high at the same time. These devices also include programmable dead time, which adds a user-programmable delay between transitions of VOA and VOB. When enabled, dead time is present on all transitions, even after overlap recovery. The amount of dead time delay (DT) is programmed by a single resistor (RDT) connected from the DT input to ground per Equation 5. Note that the dead time pin can be tied to VDDI or left floating to provide a nominal dead time at approximately 400 ps.

$$DT \approx 10 \times RDT$$

where:

DT = dead time (ns) and

RDT = dead time programming resistor (k Ω)

Equation 5

The device driving VIA and VIB should provide a minimum dead time of TDD to avoid activating overlap protection. Input/output timing waveforms for the two-input drivers are shown in [Figure 2.31 Input / Output Waveforms for High-Side / Low-Side Two-Input Drivers on page 22](#), and dead time waveforms are shown in [Figure 2.32 Dead Time Waveforms for High-Side / Low-Side Two-input Drivers on page 23](#).



Figure 2.31. Input / Output Waveforms for High-Side / Low-Side Two-Input Drivers



Figure 2.32. Dead Time Waveforms for High-Side / Low-Side Two-input Drivers

3. Electrical Specifications

Table 3.1. Electrical Characteristics¹

2.7 V < VDDI < 5.5 V, VDDA = VDDB = 12 V or 15 V, TA = -40 to +125 °C, Typical specs at 25 °C, TJ = -40 to +150 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DC Specifications						
Input-side Power Supply Voltage	VDDI	Si8230/1/2/3/4/5	4.5	—	5.5	V
		Si8237/8	2.7	—	5.5	
Driver Supply Voltage	VDDA, VDDB	Voltage between VDDA and GNDA, and VDDB and GNDB (See 1. Ordering Guide)	6.5	—	24	V
Input Supply Quiescent Current	IDDI(Q)	Si8230/2/3/5/7/8	—	2	3	mA
		Si8231/4	—	3.5	5	mA
Output Supply Quiescent Current	IDDA(Q), IDDB(Q)	Current per channel	—	—	3.0	mA
Input Supply Active Current	IDDI	Input freq = 500 kHz, no load	—	3.5	—	mA
Output Supply Active Current	IDDA	Current per channel with Input freq = 500 kHz, no load	—	6	—	mA
	IDDB					
Input Pin Leakage Current	IVIA, IVIB, IPWM		-10	—	+10	µA dc
Input Pin Leakage Current (Si8230/1/2/3/4/5)	IDISABLE		-10	—	+10	µA dc
Input Pin Leakage Current (Si8237/8)			-1000	—	+1000	
Logic High Input Threshold	VIH		2.0	—	—	V
Logic Low Input Threshold	VIL		—	—	0.8	V
Input Hysteresis	VIHYST	Si8230/1/2/3/4/5/7/8	400	450	—	mV
Logic High Output Voltage	VOAH, VOBH	IOA, IOB = -1 mA	(VDDA / VDDB) — 0.04	—	—	V
Logic Low Output Voltage	VOAL, VOBL	IOA, IOB = 1 mA	—	—	0.04	V
Output Short-Circuit Pulsed Sink Current	IOA(SCL), IOB(SCL)	Si8230/1/2/7, Figure 3.1 IOL Sink Current Test Circuit on page 27	—	0.5	—	A
		Si8233/4/5/8, Figure 3.1 IOL Sink Current Test Circuit on page 27	—	4.0	—	A
Output Short-Circuit Pulsed Source Current	IOA(SCH), IOB(SCH)	Si8230/1/2/7, Figure 3.2 IOH Source Current Test Circuit on page 27	—	0.25	—	A
		Si8233/4/5/8, Figure 3.2 IOH Source Current Test Circuit on page 27	—	2.0	—	A

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Sink Resistance	$R_{ON(SINK)}$	Si8230/1/2/7	—	5.0	—	Ω
		Si8233/4/5/8	—	1.0	—	Ω
Output Source Resistance	$R_{ON(SOURCE)}$	Si8230/1/2/7	—	15	—	Ω
		Si8233/4/5/8	—	2.7	—	Ω
VDDI Undervoltage Threshold	$VDDI_{UV+}$	VDDI rising (Si8230/1/2/3/4/5)	3.60	4.0	4.45	V
VDDI Undervoltage Threshold	$VDDI_{UV-}$	VDDI falling (Si8230/1/2/3/4/5)	3.30	3.70	4.15	V
VDDI Lockout Hysteresis	$VDDI_{HYS}$	(Si8230/1/2/3/4/5)	—	250	—	mV
VDDI Undervoltage Threshold	$VDDI_{UV+}$	VDDI rising (Si8237/8)	2.15	2.3	2.5	V
VDDI Undervoltage Threshold	$VDDI_{UV-}$	VDDI falling (Si8237/8)	2.10	2.22	2.40	V
VDDI Lockout Hysteresis	$VDDI_{HYS}$	(Si8237/8)	—	75	—	mV
VDDA, VDDDB Undervoltage Threshold	$VDDA_{UV+}, VDDDB_{UV+}$	VDDA, VDDDB rising				
5 V Threshold			5.20	5.80	6.30	V
8 V Threshold			7.50	8.60	9.40	V
10 V Threshold			9.60	11.1	12.2	V
12.5 V Threshold			12.4	13.8	14.8	V
VDDA, VDDDB Undervoltage Threshold	$VDDA_{UV-}, VDDDB_{UV-}$	VDDA, VDDDB falling				
5 V Threshold			4.90	5.52	6.0	V
8 V Threshold			7.20	8.10	8.70	V
10 V Threshold			9.40	10.1	10.9	V
12.5 V Threshold			11.6	12.8	13.8	V
VDDA, VDDDB Lockout Hysteresis	$VDDA_{HYS}, VDDDB_{HYS}$	UVLO voltage = 5 V	—	280	—	mV
VDDA, VDDDB Lockout Hysteresis	$VDDA_{HYS}, VDDDB_{HYS}$	UVLO voltage = 8 V	—	600	—	mV
VDDA, VDDDB Lockout Hysteresis	$VDDA_{HYS}, VDDDB_{HYS}$	UVLO voltage = 10 V or 12.5 V	—	1000	—	mV
AC Specifications						
Minimum Pulse Width			—	10	—	ns
Propagation Delay	t_{PHL}, t_{PLH}	CL = 200 pF	—	30	45	ns
Pulse Width Distortion $t_{PLH} - t_{PHL}$	PWD		—	—	5.60	ns
Minimum Overlap Time ²	TDD	DT = VDDI, No-Connect	—	0.4	—	ns

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Programmed Dead Time ³	DT	Figure 2.32 Dead Time Waveforms for High-Side / Low-Side Two-input Drivers on page 23, RDT = 100 k	730	900	1170	ns
		Figure 2.32 Dead Time Waveforms for High-Side / Low-Side Two-input Drivers on page 23, RDT = 6 k	55	70	75	ns
Output Rise and Fall Time	t_R, t_F	$C_L = 200$ pF (Si8230/1/2/7)	—	—	20	ns
		$C_L = 200$ pF (Si8233/4/5/8)	—	—	12	ns
Shutdown Time from Disable True	t_{SD}		—	—	60	ns
Restart Time from Disable False	$t_{RESTART}$		—	—	60	ns
Device Start-up Time	t_{START}	Time from VDD_ = VDD_UV+ to VOA, VOB = VIA, VIB	—	—	40	μ s
Common Mode Transient Immunity	CMTI	VIA, VIB, PWM = VDDI or 0 V $V_{CM} = 1500$ V (see Figure 3.3 Common Mode Transient Immunity Test Circuit on page 28)	20	45	—	kV/ μ s

Notes:

1. VDDA = VDDDB = 12 V for 5, 8, and 10 V UVLO devices; VDDA = VDDDB = 15 V for 12.5 V UVLO devices.
2. TDD is the minimum overlap time without triggering overlap protection (Si8230/1/3/4 only).
3. The largest RDT resistor that can be used is 220 k Ω .

3.1 Test Circuits

Figures Figure 3.1 IOL Sink Current Test Circuit on page 27, Figure 3.2 IOH Source Current Test Circuit on page 27, and Figure 3.3 Common Mode Transient Immunity Test Circuit on page 28 depict sink current, source current, and common-mode transient immunity test circuits, respectively.

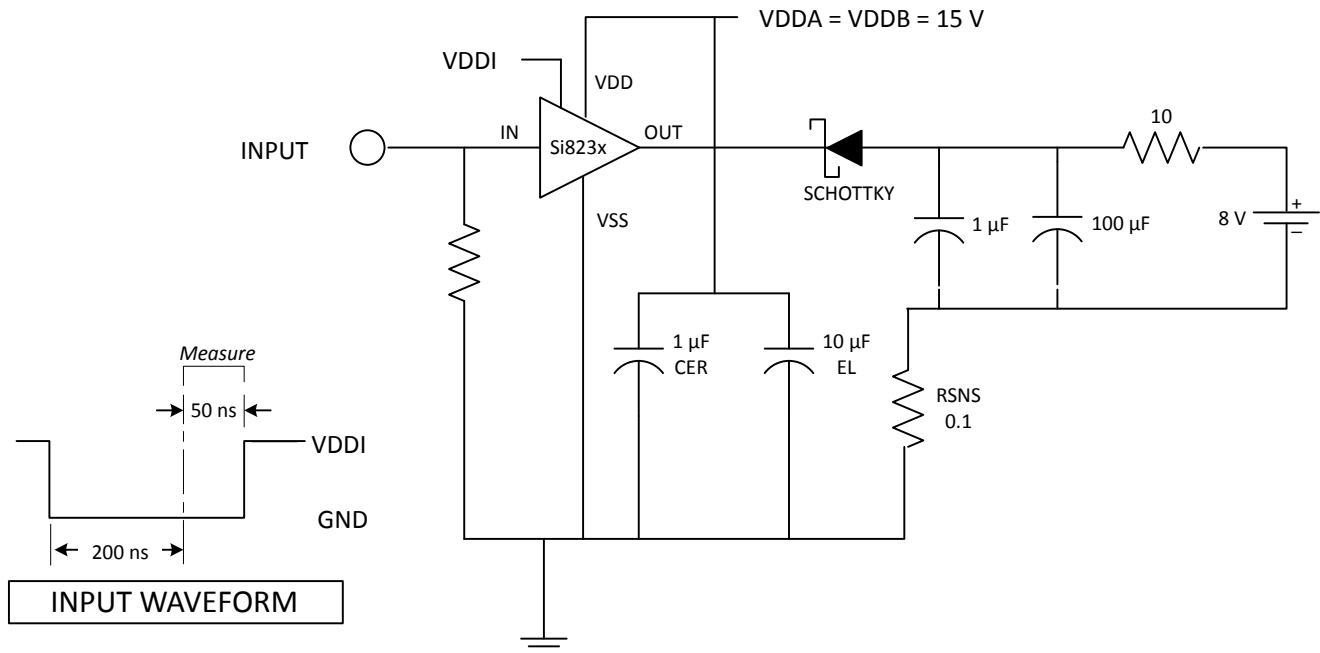


Figure 3.1. IOL Sink Current Test Circuit

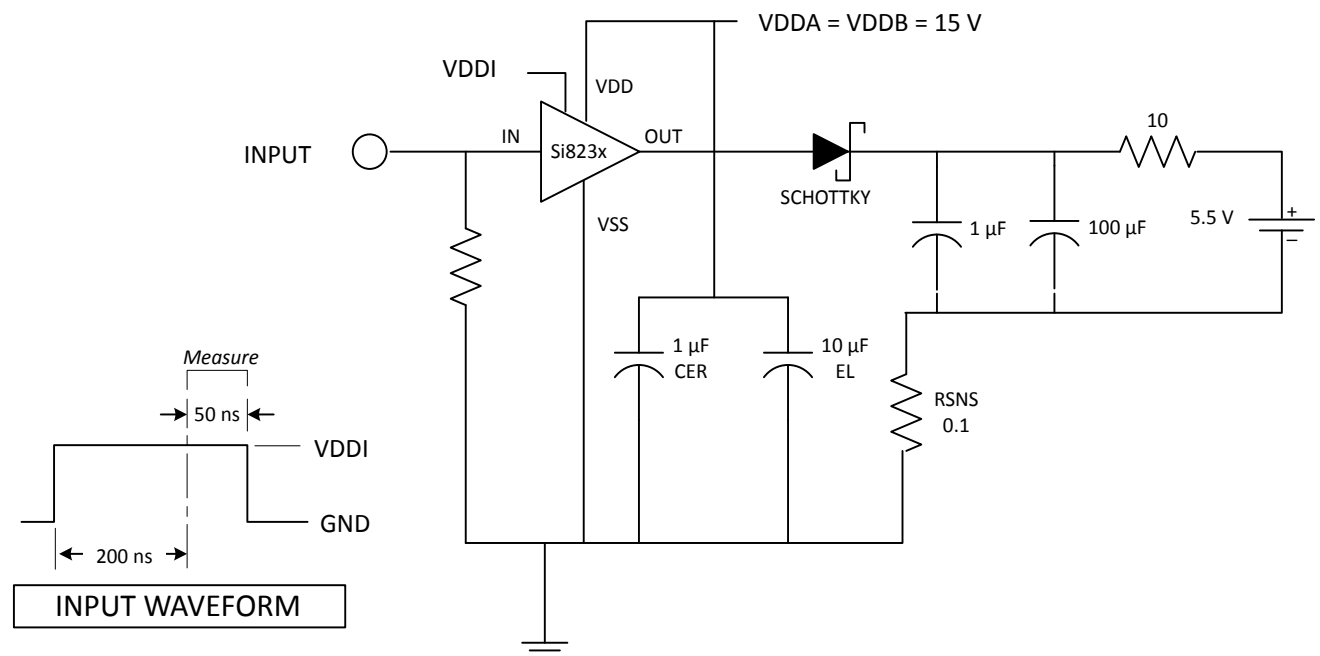


Figure 3.2. IOH Source Current Test Circuit



Figure 3.3. Common Mode Transient Immunity Test Circuit

Table 3.2. Regulatory Information¹

CSA
The Si823x is certified under CSA Component Acceptance Notice 5A. For more details, see Master Contract Number 232873.
60950-1, 62368-1: Up to 600 V _{RMS} reinforced insulation working voltage; up to 1000 V _{RMS} basic insulation working voltage.
60601-1: Up to 250 V _{RMS} working voltage and 2 MOPP (Means of Patient Protection).
VDE
The Si823x is certified according to VDE 0884-10 and EN 60950-1. For more details, see certificates 40018443, 40030763.
0884-10: Up to 891 V _{peak} for basic insulation working voltage.
60950-1: Up to 600 V _{RMS} reinforced insulation working voltage; up to 1000 V _{RMS} basic insulation working voltage.
UL
The Si823x is certified under UL1577 component recognition program. For more details, see File E257455.
Rated up to 5000 V _{RMS} isolation voltage for basic protection.
CQC
The Si823x is certified under GB4943.1-2011. For more details, see certificates CQC13001096106, CQC13001096108, and CQC17001178087.
Rated up to 600 V _{RMS} reinforced insulation working voltage; up to 1000 V _{RMS} basic insulation working voltage.

Note:

1. Regulatory Certifications apply to 2.5 kV_{RMS} rated devices which are production tested to 3.0 kV_{RMS} for 1 sec. Regulatory Certifications apply to 3.75 kV_{RMS} rated devices which are production tested to 4.5 kV_{RMS} for 1 sec. Regulatory Certifications apply to 5.0 kV_{RMS} rated devices which are production tested to 6.0 kV_{RMS} for 1 sec.
For more information, see [1. Ordering Guide](#).

Table 3.3. Insulation and Safety-Related Specifications

Parameter	Symbol	Test Condition	Value			Unit
			WBSOIC-14/16 5 kV _{RMS}	WBSOIC-14/16 NBSOIC-16 2.5 kV _{RMS} / 3.75 kV _{RMS}	14 LD LGA /QFN 2.5 kV _{RMS}	
Nominal External Air Gap (Clearance) ¹	CLR		8.0	8.0/4.01	3.5	mm
Nominal External Tracking (Creepage) ¹	CPG		8.0	8.0/4.01	3.5	mm
Minimum Internal Gap (Internal Clearance)	DTI		0.014	0.014	0.014	mm
Tracking Resistance	CTI or PTI	IEC60112	600	600	600	V
Erosion Depth	ED		0.019/0.122	0.019/0.122	0.021	mm
Resistance (Input-Output) ²	R _{IO}		10 ¹²	10 ¹²	10 ¹²	Ω
Capacitance (Input-Output) ²	C _{IO}	f = 1 MHz	1.4	1.4	1.4	pF
Input Capacitance ³	C _I		4.0	4.0	4.0	pF

Notes:

- The values in this table correspond to the nominal creepage and clearance values as detailed in [6.1 Package Outline: 16-Pin Wide Body SOIC](#), [6.2 Package Outline: 14-Pin Wide Body SOIC](#), [6.3 Package Outline: 16-Pin Narrow Body SOIC](#), [6.4 Package Outline: 14 LD LGA \(5 x 5 mm\)](#), [6.5 Package Outline: 14 LD QFN](#). VDE certifies the clearance and creepage limits as 4.7 mm minimum for the NB SOIC and 8.5 mm minimum for the WB SOIC package. UL does not impose a clearance and creepage minimum for component level certifications. CSA certifies the clearance and creepage of the WB SOIC package with designation "IS3" as 8 mm minimum. CSA certifies the clearance and creepage limits as 3.9 mm minimum for the NB SOIC and 7.6 mm minimum for the WB SOIC package with package designation "IS" as listed in the data sheet.
- To determine resistance and capacitance, the Si823x is converted into a 2-terminal device. Pins 1–8 (1–7, 14 LD LGA/QFN) are shorted together to form the first terminal and pins 9–16 (8–14, 14 LD LGA/QFN) are shorted together to form the second terminal. The parameters are then measured between these two terminals.
- Measured from input pin to ground.

Table 3.4. IEC 60664-1 Ratings

Parameter	Test Condition	Specification		
		WB SOIC-14/16	NB SOIC-16	14 LD LGA/QFN
Basic Isolation Group	Material Group	I	I	I
Installation Classification	Rated Mains Voltages < 150 V _{RMS}	I-IV	I-IV	I-IV
	Rated Mains Voltages < 300 V _{RMS}	I-IV	I-III	I-III
	Rated Mains Voltages < 400 V _{RMS}	I-III	I-II	I-II
	Rated Mains Voltages < 600 V _{RMS}	I-III	I-II	I-II

Table 3.5. VDE 0884-10 Insulation Characteristics¹

Parameter	Symbol	Test Condition	Characteristic		Unit
			WB SOIC-14/16	NB SOIC-16 14 LD LGA/QFN	
Maximum Working Insulation Voltage	V _{IORM}		891	560	V peak
Input to Output Test Voltage	V _{PR}	Method b1 (V _{IORM} × 1.875 = V _{PR} , 100% Production Test, t _m = 1 sec, Partial Discharge < 5 pC)	1671	1050	V peak
Transient Overvoltage	V _{IOTM}	t = 60 s	6000	4000	V peak
Surge Voltage	V _{IOSM}	Tested per IEC 60065 with surge voltage of 1.2 μs/50 μs Si823xxB/C/D tested with 4000 V	3077	3077	V peak
Pollution Degree (DIN VDE 0110, Table 1)			2	2	
Insulation Resistance at T _S , V _{IO} = 500 V	R _S		>10 ⁹	>10 ⁹	Ω
*Note: 1. Maintenance of the safety data is ensured by protective circuits. The Si823x provides a climate classification of 40/125/21.					

Table 3.6. VDE 0884-10 Safety Limiting Values¹

Parameter	Symbol	Test Condition	WB SOIC-14/16	NB SOIC-16	14 LD LGA/QFN	Unit
Case Temperature	T_S		150	150	150	°C
Safety Input Current	I_S	$\theta_{JA} = 100\text{ °C/W}$ (WB SO-IC-14/16), 105 °C/W (NB SOIC-16, 14 LD LGA/QFN) $V_{DDI} = 5.5\text{ V}$, $V_{DDA} = V_{DDB} = 24\text{ V}$, $T_J = 150\text{ °C}$, $T_A = 25\text{ °C}$	50	50	50	mA
Device Power Dissipation ²	P_D		1.2	1.2	1.2	W

Notes:

- Maximum value allowed in the event of a failure. Refer to the thermal derating curve in Figures [Figure 3.4 WB SOIC, NB SOIC, 14 LD LGA/QFN Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per VDE 0884-10 on page 31](#).
- The Si82xx is tested with $V_{DDI} = 5.5\text{ V}$, $V_{DDA} = V_{DDB} = 24\text{ V}$, $T_J = 150\text{ °C}$, $C_L = 100\text{ pF}$, input 2 MHz 50% duty cycle square wave.

Table 3.7. Thermal Characteristics

Parameter	Symbol	WB SOIC-14/16	NB SOIC-16	14 LD LGA/QFN	Unit
IC Junction-to-Air Thermal Resistance	θ_{JA}	100	105	105	°C/W



Figure 3.4. WB SOIC, NB SOIC, 14 LD LGA/QFN Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per VDE 0884-10

Table 3.8. Absolute Maximum Ratings¹

Parameter	Symbol	Min	Max	Unit
Storage Temperature ²	T _{STG}	–65	+150	°C
Ambient Temperature under Bias	T _A	–40	+125	°C
Junction Temperature	T _J	—	+150	°C
Input-side Supply Voltage	V _{DDI}	–0.6	6.0	V
Driver-side Supply Voltage	V _{DDA} , V _{ddb}	–0.6	30	V
Voltage on any Pin with respect to Ground	V _{IO}	–0.5	V _{DD} + 0.5	V
Output voltage to GND, repeat spike of –2 V for 200 ns, 200 kHz	VOA to GNDA, VOB to GNDB	–2	V _{DDA/B} + 0.5	V
Peak Output Current (t _{PW} = 10 μs, duty cycle = 0.2%) (0.5 Amp versions)	I _{OPK}	—	0.5	A
Peak Output Current (t _{PW} = 10 μs, duty cycle = 0.2%) (4.0 Amp versions)	I _{OPK}	—	4.0	A
Lead Solder Temperature (10 s)		—	260	°C
Maximum Isolation (Input to Output) (1 s) WB SOIC		—	6500	V _{RMS}
Maximum Isolation (Output to Output) (1 s) WB SOIC		—	2500	V _{RMS}
Maximum Isolation (Input to Output) (1 s) NB SOIC		—	4500	V _{RMS}
Maximum Isolation (Output to Output) (1 s) NB SOIC		—	2500	V _{RMS}
Maximum Isolation (Input to Output) (1 s) 14 LD LGA/QFN		—	3850	V _{RMS}
Maximum Isolation (Output to Output) (1 s) 14 LD LGA/QFN		—	650	V _{RMS}

Notes:

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. VDE certifies storage temperature from –40 to 150 °C.

4.2 Dual Driver

The figure below shows the Si823x configured as a dual driver. Note that the drain voltages of Q1 and Q2 can be referenced to a common ground or to different grounds with as much as 1500 V dc between them.



Figure 4.2. Si8232/5/7/8 in a Dual Driver Application

Because each output driver resides on its own die, the relative voltage polarities of VOA and VOB can reverse without damaging the driver. That is, the voltage at VOA can be higher or lower than that of VOB by VDD without damaging the driver. Therefore, a dual driver in a low-side high side/low side drive application can use either VOA or VOB as the high side driver. Similarly, a dual driver can operate as a dual low-side or dual high-side driver and is unaffected by static or dynamic voltage polarity changes.

5. Pin Descriptions



Table 5.1. Si8230/3 Two-Input HS/LS Isolated Driver (SOIC-16). WB SOIC-14 with IS3 package designation, has pins 12 & 13 missing

Pin	Name	Description
1	VIA	Non-inverting logic input terminal for Driver A.
2	VIB	Non-inverting logic input terminal for Driver B.
3	VDDI	Input-side power supply terminal; connect to a source of 4.5 to 5.5 V.
4	GNDI	Input-side ground terminal.
5	DISABLE	Device Disable. When high, this input unconditionally drives outputs VOA, VOB LOW. It is strongly recommended that this input be connected to external logic level to avoid erroneous operation due to capacitive noise coupling.
6	DT	Dead time programming input. The value of the resistor connected from DT to ground sets the dead time between output transitions of VOA and VOB. Defaults to 400 ps dead time when connected to VDDI or left open (see 2.10 Programmable Dead Time and Overlap Protection). If improved noise immunity is desired, a 10 nF capacitor may be added in parallel to the dead time programming resistor (RDT).
7	NC	No connection.
8	VDDI	Input-side power supply terminal; connect to a source of 4.5 to 5.5 V.
9	GNDB	Ground terminal for Driver B.
10	VOB	Driver B output (low-side driver).
11	VDDDB	Driver B power supply voltage terminal; connect to a source of 6.5 to 24 V.
12	NC	No connection.
13	NC	No connection.
14	GNDA	Ground terminal for Driver A.
15	VOA	Driver A output (high-side driver).
16	VDDA	Driver A power supply voltage terminal; connect to a source of 6.5 to 24 V.



Table 5.2. Si8231/4 PWM Input HS/LS Isolated Driver (SOIC-16). WB SOIC-14 with IS3 package designation, has pins 12 & 13 missing

Pin	Name	Description
1	PWM	PWM input.
2	NC	No connection.
3	VDDI	Input-side power supply terminal; connect to a source of 4.5 to 5.5 V.
4	GNDI	Input-side ground terminal.
5	DISABLE	Device Disable. When high, this input unconditionally drives outputs VOA, VOB LOW. It is strongly recommended that this input be connected to external logic level to avoid erroneous operation due to capacitive noise coupling.
6	DT	Dead time programming input. The value of the resistor connected from DT to ground sets the dead time between output transitions of VOA and VOB. Defaults to 400 ps dead time when connected to VDDI or left open (see 2.10 Programmable Dead Time and Overlap Protection). If improved noise immunity is desired, a 10 nF capacitor may be added in parallel to the dead time programming resistor (RDT).
7	NC	No connection.
8	VDDI	Input-side power supply terminal; connect to a source of 4.5 to 5.5 V.
9	GNDB	Ground terminal for Driver B.
10	VOB	Driver B output (low-side driver).
11	VDDB	Driver B power supply voltage terminal; connect to a source of 6.5 to 24 V.
12	NC	No connection.
13	NC	No connection.
14	GNDA	Ground terminal for Driver A.
15	VOA	Driver A output (high-side driver).
16	VDDA	Driver A power supply voltage terminal; connect to a source of 6.5 to 24 V.



Table 5.3. Si8232/5/7/8 Dual Isolated Driver (SOIC-16). WB SOIC-14 with IS3 package designation, has pins 12 & 13 missing

Pin	Name	Description
1	VIA	Non-inverting logic input terminal for Driver A.
2	VIB	Non-inverting logic input terminal for Driver B.
3	VDDI	Input-side power supply terminal; connect to a source of 4.5 to 5.5 V, (2.7 to 5.5 V for Si8237/8).
4	GNDI	Input-side ground terminal.
5	DISABLE	Device Disable. When high, this input unconditionally drives outputs VOA, VOB LOW. It is strongly recommended that this input be connected to external logic level to avoid erroneous operation due to capacitive noise coupling.
6	NC	No connection.
7	NC	No connection.
8	VDDI	Input-side power supply terminal; connect to a source of 4.5 to 5.5 V, (2.7 to 5.5 V for Si8237/8).
9	GNDB	Ground terminal for Driver B.
10	VOB	Driver B output.
11	VDDB	Driver B power supply voltage terminal; connect to a source of 6.5 to 24 V.
12	NC	No connection.
13	NC	No connection.
14	GNDA	Ground terminal for Driver A.
15	VOA	Driver A output.
16	VDDA	Driver A power supply voltage terminal; connect to a source of 6.5 to 24 V.

LGA-14 and QFN-14 (5 x 5 mm)

**Table 5.4. Si8233 Two-Input HS/LS Isolated Driver (14 LD LGA and QFN)**

Pin	Name	Description
GNDI	1	Input-side ground terminal.
VIA	2	Non-inverting logic input terminal for Driver A.
VIB	3	Non-inverting logic input terminal for Driver B.
VDDI	4	Input-side power supply terminal; connect to a source of 4.5 to 5.5 V.
DISABLE	5	Device Disable. When high, this input unconditionally drives outputs VOA, VOB LOW. It is strongly recommended that this input be connected to external logic level to avoid erroneous operation due to capacitive noise coupling.
DT	6	Dead time programming input. The value of the resistor connected from DT to ground sets the dead time between output transitions of VOA and VOB. Defaults to 400 ps dead time when connected to VDDI or left open (see 2.10 Programmable Dead Time and Overlap Protection). If improved noise immunity is desired, a 10 nF capacitor may be added in parallel to the dead time programming resistor (RDT).
VDDI	7	Input-side power supply terminal; connect to a source of 4.5 to 5.5 V.
GNDB	8	Ground terminal for Driver B.
VOB	9	Driver B output (low-side driver).
VDDB	10	Driver B power supply voltage terminal; connect to a source of 6.5 to 24 V.
NC	11	No connection.
GNDA	12	Ground terminal for Driver A.
VOA	13	Driver A output (high-side driver).
VDDA	14	Driver A power supply voltage terminal; connect to a source of 6.5 to 24 V.

LGA-14 and QFN-14 (5 x 5 mm)



Table 5.5. Si8234 PWM Input HS/LS Isolated Driver (14 LD LGA and QFN)

Pin	Name	Description
GNDI	1	Input-side ground terminal.
PWM	2	PWM input.
NC	3	No connection.
VDDI	4	Input-side power supply terminal; connect to a source of 4.5 to 5.5 V.
DISABLE	5	Device Disable. When high, this input unconditionally drives outputs VOA, VOB LOW. It is strongly recommended that this input be connected to external logic level to avoid erroneous operation due to capacitive noise coupling.
DT	6	Dead time programming input. The value of the resistor connected from DT to ground sets the dead time between output transitions of VOA and VOB. Defaults to 400 ps dead time when connected to VDDI or left open (see 2.10 Programmable Dead Time and Overlap Protection). If improved noise immunity is desired, a 10 nF capacitor may be added in parallel to the dead time programming resistor (RDT).
VDDI	7	Input-side power supply terminal; connect to a source of 4.5 to 5.5 V.
GNDB	8	Ground terminal for Driver B.
VOB	9	Driver B output (low-side driver).
VDDDB	10	Driver B power supply voltage terminal; connect to a source of 6.5 to 24 V.
NC	11	No connection.
GNDA	12	Ground terminal for Driver A.
VOA	13	Driver A output (high-side driver).
VDDA	14	Driver A power supply voltage terminal; connect to a source of 6.5 to 24 V.

LGA-14 and QFN-14 (5 x 5 mm)

GNDI	1	Si8235	14	VDDA
VIA	2		13	VOA
VIB	3		12	GNDA
VDDI	4		11	NC
DISABLE	5		10	VDDB
NC	6		9	VOB
VDDI	7		8	GNDB

Table 5.6. Si8235 Dual Isolated Driver (14 LD LGA and QFN)

Pin	Name	Description
GNDI	1	Input-side ground terminal.
VIA	2	Non-inverting logic input terminal for Driver A.
VIB	3	Non-inverting logic input terminal for Driver B.
VDDI	4	Input-side power supply terminal; connect to a source of 4.5 to 5.5 V.
DISABLE	5	Device Disable. When high, this input unconditionally drives outputs VOA, VOB LOW. It is strongly recommended that this input be connected to external logic level to avoid erroneous operation due to capacitive noise coupling.
NC	6	No connection.
VDDI	7	Input-side power supply terminal; connect to a source of 4.5 to 5.5 V.
GNDB	8	Ground terminal for Driver B.
VOB	9	Driver B output (low-side driver).
VDDB	10	Driver B power supply voltage terminal; connect to a source of 6.5 to 24 V.
NC	11	No connection.
GNDA	12	Ground terminal for Driver A.
VOA	13	Driver A output (high-side driver).
VDDA	14	Driver A power supply voltage terminal; connect to a source of 6.5 to 24 V.

6. Package Outlines

6.1 Package Outline: 16-Pin Wide Body SOIC

Figure 6.1 16-Pin Wide Body SOIC on page 41 illustrates the package details for the Si823x in a 16-Pin Wide Body SOIC. Table 6.1 Package Diagram Dimensions on page 41 lists the values for the dimensions shown in the illustration.

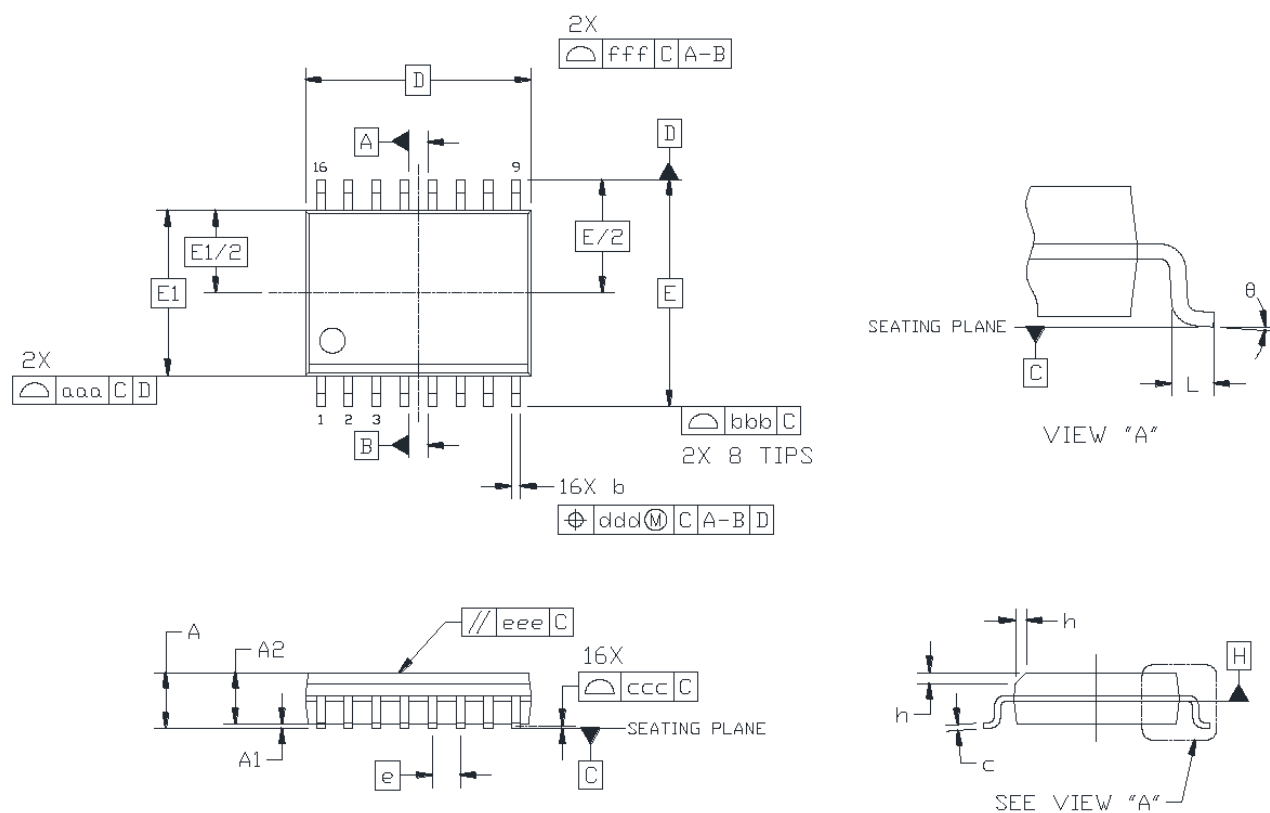


Figure 6.1. 16-Pin Wide Body SOIC

Table 6.1. Package Diagram Dimensions

Dimension	Min	Max
A	—	2.65
A1	0.10	0.30
A2	2.05	—
b	0.31	0.51
c	0.20	0.33
D	10.30 BSC	
E	10.30 BSC	
E1	7.50 BSC	
e	1.27 BSC	
L	0.40	1.27
h	0.25	0.75
θ	0°	8°

Dimension	Min	Max
aaa	—	0.10
bbb	—	0.33
ccc	—	0.10
ddd	—	0.25
eee	—	0.10
fff	—	0.20

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Outline MS-013, Variation AA.
4. Recommended reflow profile per JEDEC J-STD-020 specification for small body, lead-free components.

6.2 Package Outline: 14-Pin Wide Body SOIC

Figure 6.2 Si823x 14-pin WB SOIC Outline on page 43 illustrates the package details for the Si823x in a 14-Pin Wide Body SOIC. Table 6.2 Package Diagram Dimensions on page 43 lists the values for the dimensions shown in the illustration.

**Figure 6.2. Si823x 14-pin WB SOIC Outline****Table 6.2. Package Diagram Dimensions**

Dimension	MIN	MAX
A	—	2.65
A1	0.10	0.30
A2	2.05	—
b	0.31	0.51
c	0.20	0.33
D	10.30 BSC	
E	10.30 BSC	
E1	7.50 BSC	
e	1.27 BSC	
L	0.40	1.27
h	0.25	0.75
Θ	0°	8°
aaa	—	0.10
bbb	—	0.33
ccc	—	0.10
ddd	—	0.25
eee	—	0.10
fff	—	0.20

Dimension	MIN	MAX
Notes: 1. All dimensions shown are in millimeters (mm) unless otherwise noted. 2. Dimensioning and Tolerancing per ANSI Y14.5M-1994. 3. This drawing conforms to JEDEC Outline MS-013, Variation AA. 4. Recommended reflow profile per JEDEC J-STD-020 specification for small body, lead-free components.		

6.3 Package Outline: 16-Pin Narrow Body SOIC

Figure 6.3 16-pin Small Outline Integrated Circuit (SOIC) Package on page 45 illustrates the package details for the Si823x in a 16-pin narrow-body SOIC. Table 6.3 Package Diagram Dimensions on page 45 lists the values for the dimensions shown in the illustration.



Figure 6.3. 16-pin Small Outline Integrated Circuit (SOIC) Package

Table 6.3. Package Diagram Dimensions

Dimension	Min	Max	Dimension	Min	Max
A	—	1.75	L	0.40	1.27
A1	0.10	0.25	L2	0.25 BSC	
A2	1.25	—	h	0.25	0.50
b	0.31	0.51	θ	0°	8°
c	0.17	0.25	aaa	0.10	
D	9.90 BSC		bbb	0.20	
E	6.00 BSC		ccc	0.10	
E1	3.90 BSC		ddd	0.25	
e	1.27 BSC				

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MS-012, Variation AC.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

6.4 Package Outline: 14 LD LGA (5 x 5 mm)

Figure 6.4 Si823x LGA Outline on page 46 illustrates the package details for the Si823x in an LGA outline. Table 6.4 Package Diagram Dimensions on page 46 lists the values for the dimensions shown in the illustration.

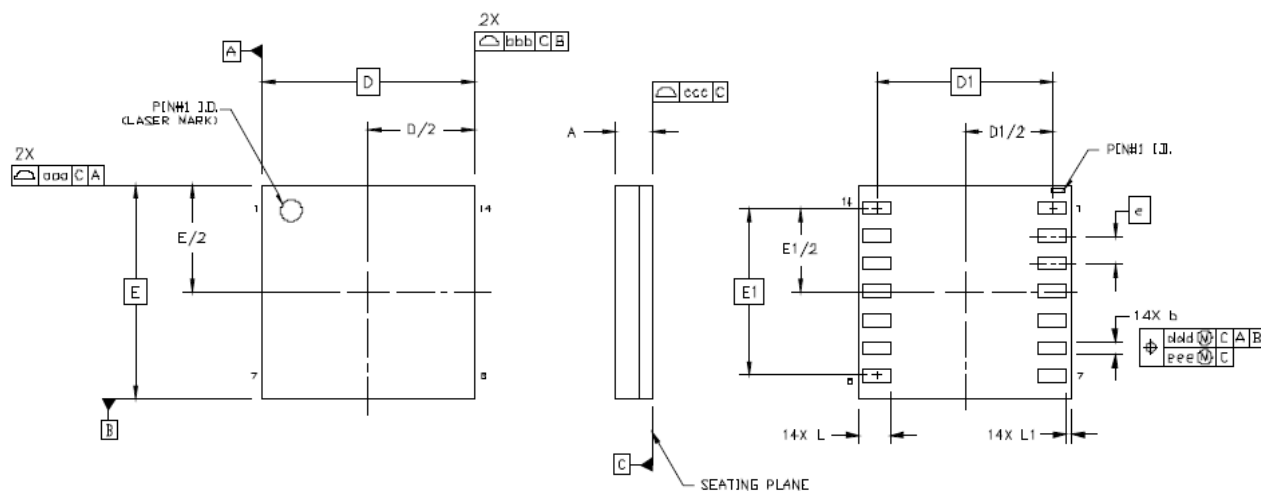


Figure 6.4. Si823x LGA Outline

Table 6.4. Package Diagram Dimensions

Dimension	MIN	NOM	MAX
A	0.74	0.84	0.94
b	0.25	0.30	0.35
D	5.00 BSC		
D1	4.15 BSC		
e	0.65 BSC		
E	5.00 BSC		
E1	3.90 BSC		
L	0.70	0.75	0.80
L1	0.05	0.10	0.15
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.15
eee	—	—	0.08

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

6.5 Package Outline: 14 LD QFN

Figure 6.5 Si823x 14-pin LD QFN Outline on page 47 illustrates the package details for the Si823x in an QFN outline. Table 6.5 Package Diagram Dimensions on page 47 lists the values for the dimensions shown in the illustration.



Figure 6.5. Si823x 14-pin LD QFN Outline

Table 6.5. Package Diagram Dimensions

Dimension	MIN	NOM	MAX
A	0.74	0.85	0.90
A1	0	0.025	0.05
b	0.25	0.30	0.35
D	5.00 BSC		
e	0.65 BSC		
E	5.00 BSC		
E1	3.60 BSC		
L	0.50	0.60	0.70
L1 ³	—	0.10 BSC	—
ccc	—	—	0.08
ddd	—	—	0.10

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. L1 shall not be less than 0.01 mm.

7. Land Patterns

7.1 Land Pattern: 16-Pin Wide Body SOIC

Figure 7.1 16-Pin SOIC Land Pattern on page 48 illustrates the recommended land pattern details for the Si823x in a 16-pin wide-body SOIC. Table 7.1 16-Pin Wide Body SOIC Land Pattern Dimensions on page 48 lists the values for the dimensions shown in the illustration.



Figure 7.1. 16-Pin SOIC Land Pattern

Table 7.1. 16-Pin Wide Body SOIC Land Pattern Dimensions

Dimension	Feature	(mm)
C1	Pad Column Spacing	9.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.90

Notes:

1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P1032X265-16AN for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

7.2 Land Pattern: 14-Pin Wide Body SOIC

Figure 7.2 14-Pin WB SOIC Land Pattern on page 49 illustrates the recommended land pattern details for the Si823x in a 14-pin Wide Body SOIC. Table 7.2 14-Pin WB SOIC Land Pattern Dimensions on page 49 lists the values for the dimensions shown in the illustration.



Figure 7.2. 14-Pin WB SOIC Land Pattern

Table 7.2. 14-Pin WB SOIC Land Pattern Dimensions

Dimension	Feature	(mm)
C1	Pad Column Spacing	9.70
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.60

Notes:

1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P1032X265-16AN for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

7.3 Land Pattern: 16-Pin Narrow Body SOIC

Figure 7.3 16-Pin Narrow Body SOIC PCB Land Pattern on page 50 illustrates the recommended land pattern details for the Si823x in a 16-pin narrow-body SOIC. Table 7.3 16-Pin Narrow Body SOIC Land Pattern Dimensions on page 50 lists the values for the dimensions shown in the illustration.



Figure 7.3. 16-Pin Narrow Body SOIC PCB Land Pattern

Table 7.3. 16-Pin Narrow Body SOIC Land Pattern Dimensions

Dimension	Feature	(mm)
C1	Pad Column Spacing	5.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.55

Notes:

1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P600X165-16N for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

7.4 Land Pattern: 14 LD LGA/QFN

Figure 7.4 14-Pin LGA/QFN Land Pattern on page 51 illustrates the recommended land pattern details for the Si823x in a 14-pin LGA/QFN. Table 7.4 14-Pin LGA/QFN Land Pattern Dimensions on page 51 lists the values for the dimensions shown in the illustration.

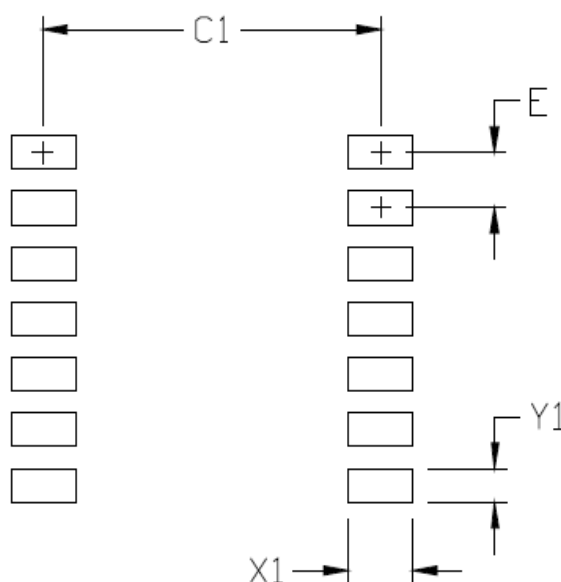


Figure 7.4. 14-Pin LGA/QFN Land Pattern

Table 7.4. 14-Pin LGA/QFN Land Pattern Dimensions

Dimension	(mm)
C1	4.20
E	0.65
X1	0.80
Y1	0.40

Notes:

General

1. All dimensions shown are in millimeters (mm).
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μ m minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8. Top Markings

8.1 Si823x Top Marking (14/16-Pin Wide Body SOIC)



Table 8.1. Top Marking Explanation (14/16-Pin Wide Body SOIC)

Line 1 Marking:	Base Part Number	Si823 = ISOdriver product series
	Ordering Options	Y = Peak output current
	See Ordering Guide for more information.	0, 1, 2, 7 = 0.5 A 3, 4, 5, 8 = 4.0 A U = UVLO level A = 5 V; B = 8 V; C = 10 V; D = 12.5 V V = Isolation rating B = 2.5 kV; C = 3.75 kV; D = 5.0 kV
Line 2 Marking:	YY = Year	Assigned by the Assembly House. Corresponds to the year and workweek of the mold date.
	WW = Workweek	
	TTTTTT = Mfg Code	Manufacturing Code from Assembly Purchase Order form.
Line 3 Marking:	Circle = 1.5 mm Diameter (Center Justified)	"e4" Pb-Free Symbol
	Country of Origin	TW = Taiwan (as shown), TH = Thailand
	ISO Code Abbreviation	

8.2 Si823x Top Marking (16-Pin Narrow Body SOIC)



Line 1 Marking:	Base Part Number	Si823 = ISOdriver product series
	Ordering Options	Y = Peak output current 0, 1, 2, 7 = 0.5 A 3, 4, 5, 8 = 4.0 A U = UVLO level A = 5 V; B = 8 V; C = 10 V; D = 12.5 V V = Isolation rating A = 1.0 kV; B = 2.5 kV; C = 3.75 kV
Line 2 Marking:	YY = Year	Assigned by the Assembly House. Corresponds to the year and workweek of the mold date.
	WW = Workweek	
	TTTTTT = Mfg Code	Manufacturing Code from Assembly Purchase Order form.

8.3 Si823x Top Marking (14 LD LGA/QFN)



Line 1 Marking:	Base Part Number	Si823 = ISOdriver product series
	Ordering Options See Ordering Guide for more information.	Y = Peak output current 0, 1, 2 = 0.5 A 3, 4, 5 = 4.0 A
Line 2 Marking:	Ordering options	U = UVLO level A = 5 V; B = 8 V; C = 10 V; D = 12.5 V V = Isolation rating A = 1.0 kV; B = 2.5 kV; C = 3.75 kV I = -40 to +125 °C ambient temperature range M = LGA package type M1 = QFN package type
Line 3 Marking:	TTTTTT	Manufacturing Code from Assembly
Line 4 Marking:	Circle = 1.5 mm diameter	Pin 1 identifier
	YYWW	Manufacturing date code

9. Revision History

Revision 2.15

September 2019

- Updated Section [1. Ordering Guide](#).

Revision 2.14

June 2019

- Added automotive grade OPN, Si8230BD-AS, to Ordering Guide for Automotive Grade OPNs.

Revision 2.13

September 2018

- Added automotive grade OPNs in Ordering Guide for Automotive Grade OPNs.
- Modified power equations in [2.7 Power Dissipation Considerations](#).
- Corrected typo for IDISABLE in [Table 3.1 Electrical Characteristics¹ on page 24](#).
- Reformatted [Table 3.5 VDE 0884-10 Insulation Characteristics¹ on page 30](#).
- Added Absolute Max rating of –2V/200 ns on output pins in [Table 3.8 Absolute Maximum Ratings¹ on page 32](#).
- Updated [7.2 Land Pattern: 14-Pin Wide Body SOIC](#).

Revision 2.12

May 2018

- Updated the Ordering Guide for Automotive-Grade OPN options.

Revision 2.1.1

January 2018

- Added new table to Ordering Guide for Automotive-Grade OPN options.

Revision 2.1

October 2017

- Added IS3 and IM1 packaging options
- Added IEC 62368-1 references throughout
- Changed max propagation delay spec from 60 ns to 45 ns based on new test limits
- Removed references to IEC 61010
- Removed references to IEC 60747, replaced with references to VDE 0884-10

Revision 2.0

August 7, 2017

Revision 1.9

July 7, 2017

- Updated [1. Ordering Guide](#) to designate tape and reel packaging option.

Revision 1.8

May 17, 2016

- Converted document from Framemaker to DITA.

Revision 1.7

- Updated [3.1 Test Circuits](#)
 - Added CQC certificate numbers.
- Updated [Table 3.3 Insulation and Safety-Related Specifications](#) on page 29
 - Updated Erosion Depth.
- Updated [Table 3.5 VDE 0884-10 Insulation Characteristics¹](#) on page 30
 - Updated V_{PR} for WBSOIC-16.
- Updated [Table 3.8 Absolute Maximum Ratings¹](#) on page 32
 - Removed I_o and added Peak Output Current specifications.
- Updated Equation 1.
- Updated [Figure 4.1 Si823x in Half-Bridge Application](#) on page 33.
- Updated [Figure 4.2 Si8232/5/7/8 in a Dual Driver Application](#) on page 34.
- Updated Ordering Guide [Table 1.1 Si823x Ordering Guide^{1, 2, 4}](#) on page 2

Revision 1.6

- Updated [Table 1.1 Si823x Ordering Guide^{1, 2, 4}](#) on page 2, Ordering Part Numbers.
- Added Revision D Ordering Part Numbers.
- Removed all Ordering Part Numbers of previous revisions.

Revision 1.5

- Updated [Table 3.1 Electrical Characteristics¹](#) on page 24, input and output supply current.
- Added references to AEC-Q100 qualified throughout.
- Changed all 60747-5-2 references to 60747-5-5.
- Added references to CQC throughout.
- Updated pin descriptions throughout.
 - Corrected dead time default to 400 ps from 1 ns.
- Updated [Table 1.1 Si823x Ordering Guide^{1, 2, 4}](#) on page 2, Ordering Part Numbers.
 - Removed moisture sensitivity level table notes.

Revision 1.4

- Updated [1. Ordering Guide](#).
 - Updated "3 V VDDI Ordering Options".

Revision 1.3

- Added Si8237/8 throughout.
- Updated [Table 3.1 Electrical Characteristics¹](#) on page 24.
- Updated [Figure 3.1 IOL Sink Current Test Circuit](#) on page 27.
- Updated [Figure 3.2 IOH Source Current Test Circuit](#) on page 27.
- Added [Figure 3.3 Common Mode Transient Immunity Test Circuit](#) on page 28.
- Updated Si823x Family Truth Table to include notes 1 and 2.
- Updated [2.10 Programmable Dead Time and Overlap Protection](#).
- Removed references to Figures 26A and 26B.
- Updated [Table 1.1 Si823x Ordering Guide^{1, 2, 4}](#) on page 2.
- Added Si8235-BA-C-IS1 ordering part number.
- Added table note.

Revision 1.2

- Updated [1. Ordering Guide](#).
 - Updated moisture sensitivity level (MSL) for all package types.
- Updated [Table 3.8 Absolute Maximum Ratings¹ on page 32](#).
 - Added junction temperature spec.
- Updated [3.1 Test Circuits](#) with new notes.
- Updated Figures [Figure 2.16 Output Sink Current vs. Supply Voltage on page 13](#), [Figure 2.14 Output Source Current vs. Supply Voltage on page 12](#), [Figure 2.17 Output Sink Current vs. Temperature on page 13](#), and [Figure 2.15 Output Source Current vs. Temperature on page 12](#) to reflect correct y-axis scaling.
- Updated [Figure 4.2 Si8232/5/7/8 in a Dual Driver Application on page 34](#).
- Updated .
- Updated [6.1 Package Outline: 16-Pin Wide Body SOIC](#).
- Updated [Table 6.1 Package Diagram Dimensions on page 41](#).
- Change references to 1.5 kV_{RMS} rated devices to 1.0 kV_{RMS} throughout.
- Updated [2.7 Power Dissipation Considerations](#).

Revision 1.1

- Updated .
 - Updated CMTI specification.
- Updated [Table 3.1 Electrical Characteristics¹ on page 24](#).
 - Updated CMTI specification.
- Updated [Table 3.5 VDE 0884-10 Insulation Characteristics¹ on page 30](#).
- Updated [4.2 Dual Driver](#).
- Updated [1. Ordering Guide](#).
- Replaced pin descriptions on page 1 with chip graphics.

Revision 1.0

- Updated Tables [3.1 Test Circuits](#), [Table 3.3 Insulation and Safety-Related Specifications on page 29](#), [Table 3.4 IEC 60664-1 Ratings on page 30](#), and [Table 3.5 VDE 0884-10 Insulation Characteristics¹ on page 30](#).
- Updated [1. Ordering Guide](#).
 - Added 5 V UVLO ordering options
- Added Device Marking sections.

Revision 0.3

- Moved Sections 2, 3, and 4 to after Section 5.
- Updated Tables [Table 5.4 Si8233 Two-Input HS/LS Isolated Driver \(14 LD LGA and QFN\) on page 38](#), [Table 5.5 Si8234 PWM Input HS/LS Isolated Driver \(14 LD LGA and QFN\) on page 39](#).
 - Removed Si8230, Si8231, and Si8232 from pinout and from title.
- Updated and added Ordering Guide footnotes.
- Updated UVLO specifications in [Table 3.1 Electrical Characteristics¹ on page 24](#).
- Added PWD and Output Supply Active Current specifications in [Table 3.1 Electrical Characteristics¹ on page 24](#).
- Updated and added typical operating condition graphs in [2.3 Typical Operating Characteristics \(0.5 Amp\)](#) and [2.4 Typical Operating Characteristics \(4.0 Amp\)](#).

Revision 0.2

- Updated all specs to reflect latest silicon revision.
- Updated [Table 3.1 Electrical Characteristics¹ on page 24](#) to include new UVLO options.
- Updated [Table 3.8 Absolute Maximum Ratings¹ on page 32](#) to reflect new maximum package isolation ratings
- Added Figures 34, 35, and 36.
- Updated Ordering Guide to reflect new package offerings.
- Added "Undervoltage Lockout (UVLO)" section to describe UVLO operation.

Revision 0.11

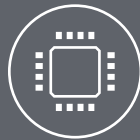
- Initial release.



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