LV8907UW

Sensor-less Three-phase Brushless DC Motor Controller, with Gate Drivers, for Automotive

ON Semiconductor®

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Overview

The LV8907 is a high performance, AEC-Q100 qualified, sensor-less three-phase BLDC motor controller with integrated gate drivers for driving external N-MOSFETs. An on-chip two-stage charge pump provides required gate voltage for a wide range of low $R_{DS(ON)}$ type external N-MOSFETs. The device offers a rich set of system protection and diagnostic functions such as over-current, over-voltage, short-circuit, under-voltage, over-temperature and many more. It supports open-loop as well as closed-loop speed control with user configurable startup, speed setting and proportional/integral (PI) control coefficients, making it suitable for a wide range of motor and load combinations. With a built-in linear regulator for powering external circuits, a watchdog timer, and a LIN (Local Interconnect Network) transceiver, the LV8907 offers a very small system solution.

The LV8907 stores system parameters in embedded one-time programmable (OTP) non-volatile memory in addition to RAM system memory. An SPI interface is provided for parameter setting and monitoring the system status. With the operating junction temperature tolerance up to 175ºC and electrically LIN compatible control signals (PWM and Enable), the LV8907 is an ideal solution for stand-alone BLDC motor control systems.

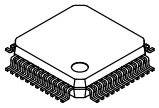
Features

- AEC-Q100 qualified and PPAP capable.
- Operating junction temperature up to 175ºC
- Operating voltage range from 5.5V to 20V with tolerance from 4.5V to 40V
- Embedded proprietary sensor-less trapezoidal and pseudo-sinusoidal commutation
- Supports open-loop as well as closed-loop speed control
- Integrated gate drivers for driving six N-MOSFETs
- Two-stage charge pump for continuous 100% duty cycle operation
- 5V/3.3V regulator, LIN transceiver and Watchdog timer applications using an external microcontroller.
- Configurable speed settings and PI control coefficients
- Various system protection features including:
  - Shoot through protection using configurable dead-time
  - Drain-source short detection
  - Cycle-by-cycle current limit and over-current shutdown
  - Over-voltage and under-voltage shutdown
  - Over-temperature warning and shutdown
  - Input PWM fault detection

Typical Applications

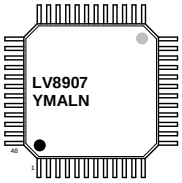
- Automotive pumps (Fuel, Oil, and Hydraulic)
- Fans (HVAC, Radiator, Battery Cooling, LED Headlight Cooling)
- White goods and industrial BLDC motor control

PACKAGE PICTURE



SQFP48K
7 mm x 7 mm

MARKING DIAGRAM



Y: production year
M: production month
A: assembly location
LN: lot number

ORDERING INFORMATION

Ordering Code:
LV8907UWR2G

Package
SQFP48K

Shipping (quantity/packing)
2500 per tape & reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D. http://www.onsemi.com/pub_link/Collateral/BRD8011-D.PDF

April 2016- Rev. 0

Publication Order Number:
LV8907UW/D

LV8907 BLOCK DIAGRAM

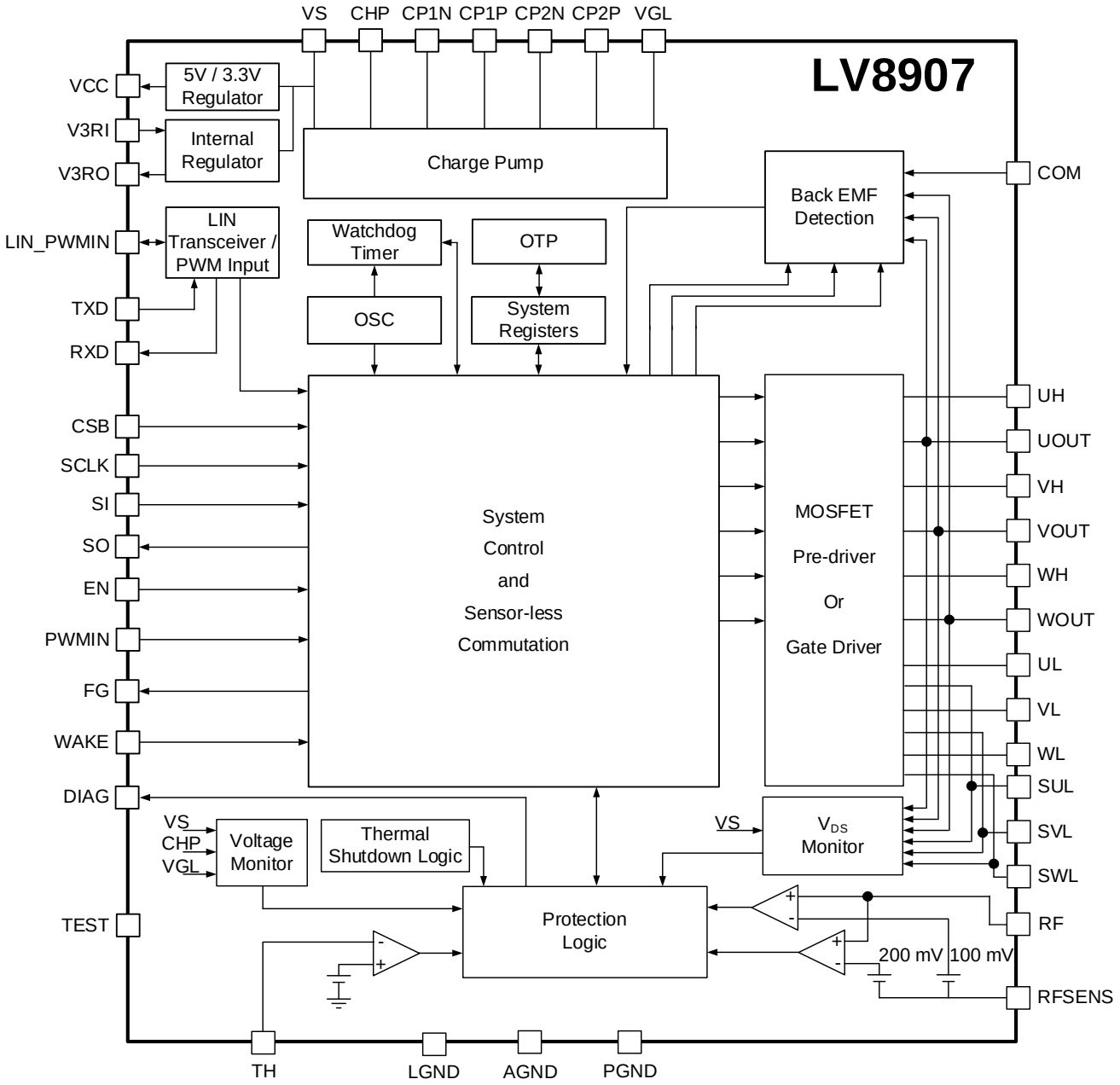


Figure 1: LV8907 Block Diagram

APPLICATION BLOCK DIAGRAMS

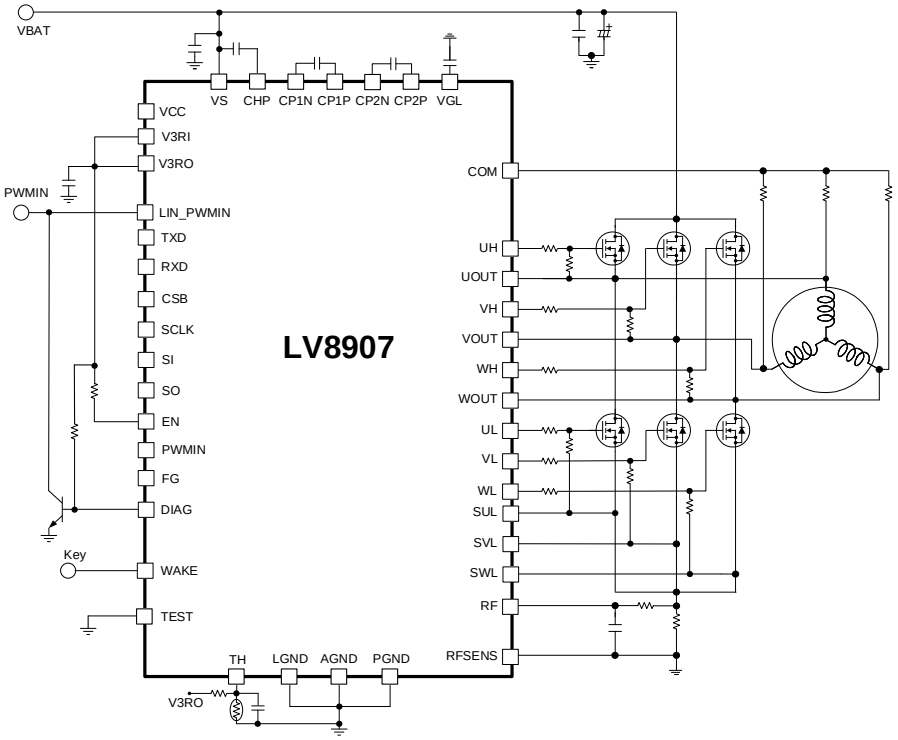


Figure 2: Example of Standalone Configuration

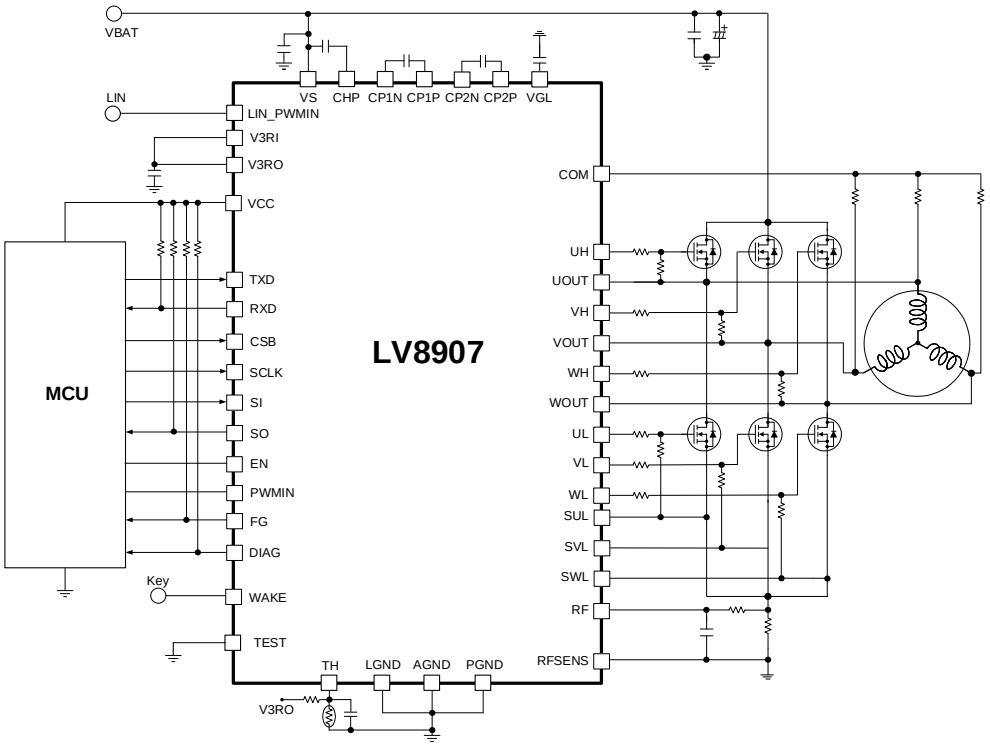


Figure 3: Example of LIN Based Control Configuration

PIN ASSIGNMENTS

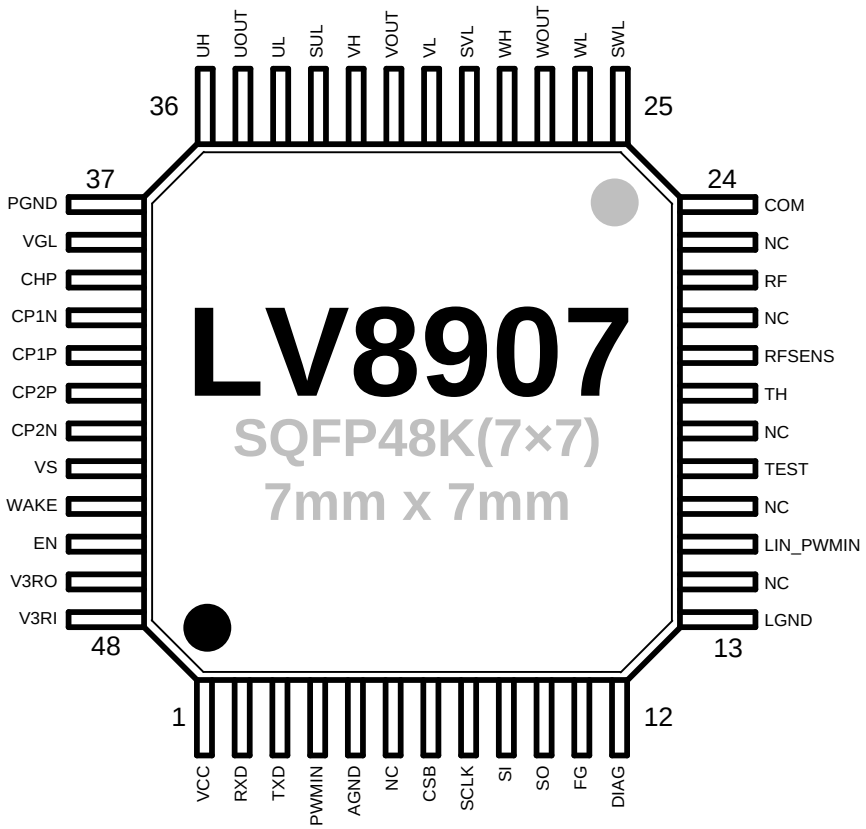


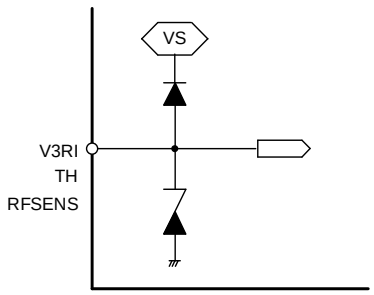
Figure 4: LV8907 Pinout

PIN DESCRIPTION

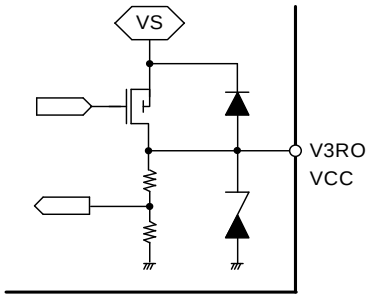
Pin Name	Pin No	Description	Page
VCC	1	5V or 3.3V regulator output pin. (Selected by internal register setting) Power supply for microcontroller. Connect capacitor to AGND for stability.	16
RXD	2	Open drain logic level output of LIN_PWMIN received data. Use pull-up to a voltage less than or equal to VS.	18
TXD	3	Logic level input of transmit data for LIN_PWMIN.	18
PWMIN	4	Digital level PWM input pin for direct drive or speed register selection details. Input polarity can be programmed for either active high or active low.	16
AGND	5	Analog GND pin.	
NC	6, 14, 16,18, 21, 23	No Connections	
CSB	7	Active low SPI interface chip selection pin.	20
SCLK	8	SPI interface clock input pin.	20
SI	9	Active high SPI interface serial data input pin.	20
SO	10	Open drain SPI interface serial data output pin.	20
FG	11	Open drain back-EMF transition output pin. The frequency division ratio is selectable via register settings.	18
DIAG	12	Programmable open drain diagnostic output.	18
LGND	13	LIN Block GND pin. Must be connected to AGND on the PCB.	
LIN_ PWMIN	15	LIN transceiver input/output. Register selectable as high voltage PWM input with a $V_{VS}/2$ threshold.	18
TEST	17	Factory test pin. Connect to GND.	
TH	19	Thermistor input pin for power stage temperature detection. If the input voltage is below the threshold voltage, an error is triggered. The error threshold is programmable. To disable tie to V3RO.	19
RFSENS	20	Shunt resistance reference pin. Connect this pin to the GND side of the Shunt resistor with Kelvin leads.	19
RF	22	Output current detect pin. Connect this pin to higher terminal of the shunt resistor with Kelvin leads.	19
COM	24	COM input pin. Connect this pin to the motor neutral point if available. This point may be derived from a resistive network with 1k resistors to the phases.	14
SUL SVL SWL	33 29 25	Current return path for low-side gate drive. Short circuit shutoff level is measured between this pin and its corresponding phase pin.	18
UL VL WL	34 30 26	Gate driver output pin for the low-side Nch Power FET. Use gate resistors for wave-shaping.	18
UOUT VOUT WOUT	35 31 27	Current return path for high-side gate drive and reference for high-side short circuit shut-off.	18
UH VH WH	36 32 28	Gate driver output pin for the high-side Nch Power FET. Use gate resistors for wave-shaping.	18
PGND	37	GND pin for the charge pump.	
VGL	38	Power supply pin for low-side gate drive. Connect decoupling capacitor between this pin and GND.	16
CHP	39	Power supply pin for high-side gate drive. Connect decoupling capacitor between this pin and VS.	16
CP1N	40	Charge transfer pin of the Charge pump (1N). Connect capacitor between CP1P and CP1N.	16
CP1P	41	Charge transfer pin of the Charge pump (1P). Connect capacitor between CP1P and CP1N.	16
CP2P	42	Charge transfer pin of the Charge pump (2P). Connect capacitor between CP2P and CP2N.	16
CP2N	43	Charge transfer pin of the Charge pump (2N). Connect capacitor between CP2P and CP2N.	16

Pin Name	Pin No	Description	Page
VS	44	Power supply pin.	15
WAKE	45	WAKE pin. “H” = Operating mode, “L” or “Open” = Sleep mode. In Sleep mode all gate drivers are high-impedance. To protect the power stage, pull-down resistors on the gate lines may be required.	15
EN	46	Motor stage Enable pin. “H” = Normal enabled mode; “L” or “Open” = Standby mode. In Standby mode all gate drivers driven low. Motor freewheeling.	15
V3RO	47	3V regulator output pin. Connect capacitor between this pin and AGND.	16
V3RI	48	3V regulator input pin (internally connected to ccontrol, and logic circuits). Connect to V3RO pin.	16

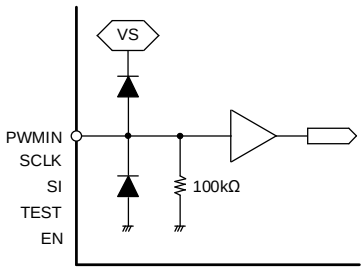
PIN CIRCUIT



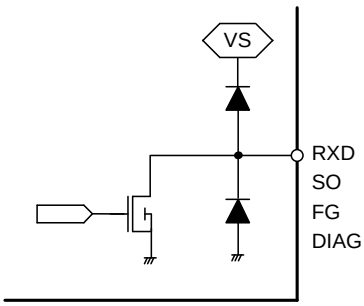
TYPE1: V3RI, TH, RFSENS



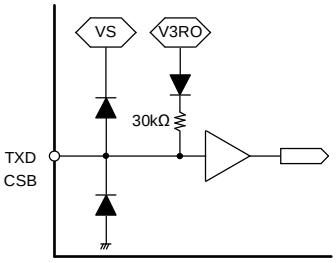
TYPE2: V3RO, VCC



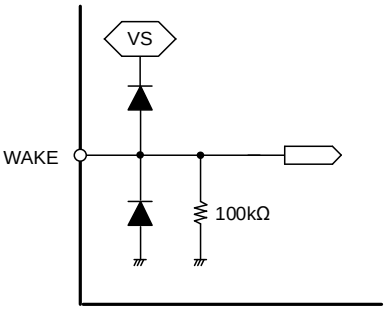
TYPE3: PWMIN, SCLK, SI, TEST, EN



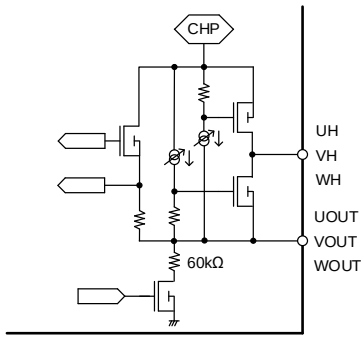
TYPE4: RXD, SO, FG, DIAG



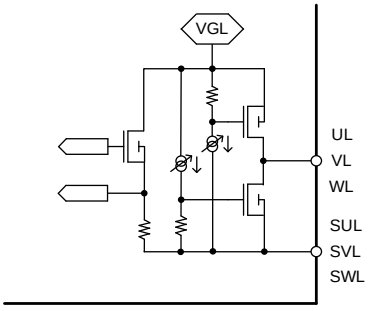
TYPE5: TXD, CSB



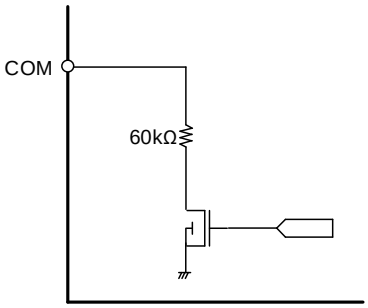
TYPE6: WAKE



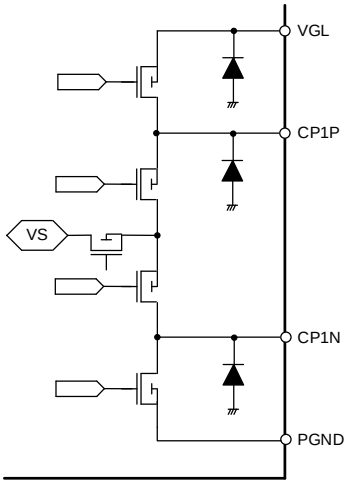
TYPE7: UH, VH, WH, UOUT, VOUT, WOUT



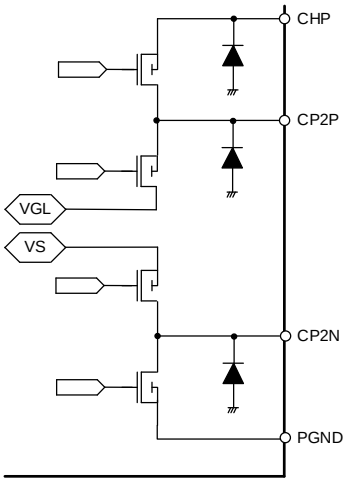
TYPE8: UL, VL, WL, SUL, SVL, SWL



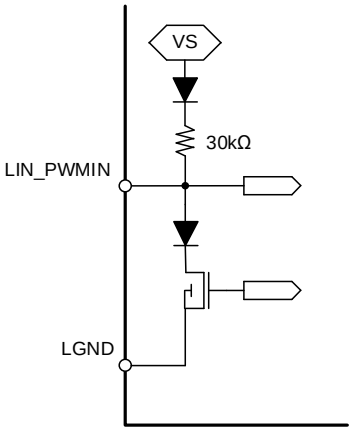
TYPE9: COM



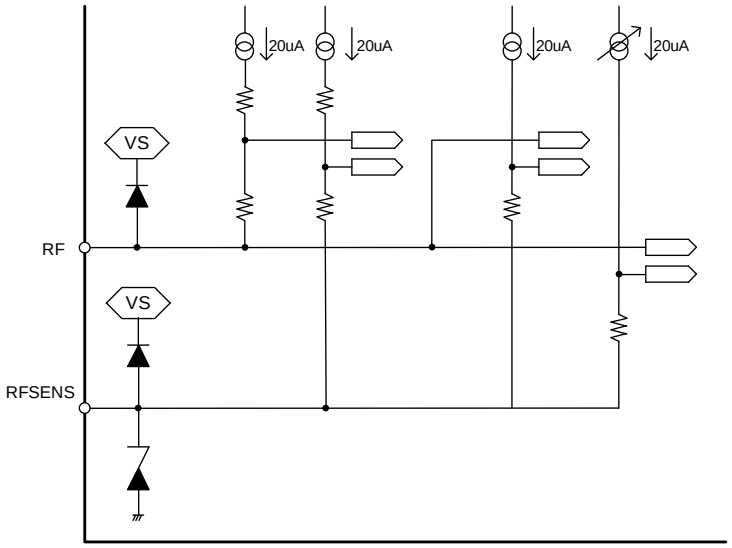
TYPE10: VGL, CP1P, CP1N, PGND



TYPE11: CHP, CP2P, CP2N, PGND



TYPE12: LIN_PWMIN, LGND



TYPE13: RF, RFSENS

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Parameter	Pins	Ratings	Unit
Supply voltage	VS	–0.3 to 40	V
Charge pump voltage (high side)	CHP	–0.3 to 40	V
Charge pump voltage (low side)	VGL	–0.3 to 16	V
Logic power supply	VR3I, VR3O	–0.3 to 3.6	V
5V Regulator voltage	VCC	–0.3 to 5.5	V
Digital I/O voltage1	WAKE,EN	–0.3 to 40	V
Digital I/O voltage2	CSB, SCLK, SI, PWMIN, TXD, TEST	–0.3 to 5.5	V
Digital output voltage	DIAG, FG, SO, RXD	–0.3 to 40	V
LIN bus voltage	LIN_PWMIN Voltage differential between Pins are 60V or less	–40 to 40	V
RF input voltage	RF	–3 to 3.6	V
RFSENS input voltage	RFSENS	–0.3 to 1.0	V
TH input voltage	TH	–0.3 to 3.6	V
Voltage Tolerance	UOUT, VOUT, WOUT, COM	–3 to 40	V
High-side output	UH, VH, WH	–3 to 40	V
Low-side output	UL, VL, WL	–3 to 16	V
Low-side Source output voltage	SUL, SVL, SWL	–3 to 3.6	V
Voltage between HS gate and phase	UH-UOUT,VH-VOUT,WH-WOUT	–0.3 to 40	V
Voltage between LS gate and source	UL-SUL, VL-SVL, WL-SWL	–0.3 to 16	V
Output current	UH,VH,WH,UL,VL,WL pulsed (duty5%)	50 400	mA
Open drain output current	DIAG, FG, SO, RXD	10	mA
Thermal Resistance ($R_{\theta jA}$)	with Board (Note 2)	47	°C/W
ESD Human Body Model	AEC Q100-002	2	kV
ESD Charged Device Model	AEC Q100-011	750	V
Storage temperature		–55 to 150	°C
Junction temperature		–40 to 150	°C
	(Note 3)	150 to 175	°C

Note 1: Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Note 2: 76.2 × 114.3 × 1.6mm, glass epoxy board

Note 3: Operation outside the Operating Junction temperature is not guaranteed. Operation above 150°C should not be considered without a written agreement from ON Semiconductor Engineering staff.

ELECTRICAL CHARACTERISTICS

Valid at a junction temperature range from −40°C to 150°C, for supply Voltage 6.0V≤VS≤20V.
Typical values at 25°C and VS=12V unless specified otherwise. (Note 4)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply-voltage range	VS		6	12	20	V
		Device fully functional.	5.5		20	V
		Full logic functionality, driver stage off.	4.5		40	V
Supply current into VS	I_{S1}	V3RO=V3RI		15	25	mA
	I_{S2}	Sleep Mode		40	80	μA
Operational junction Temperature	Topj		−40		150	°C
OUTPUT BLOCK (UH, VH, WH, UL, VL, WL)						
Low-side output On-resistance 1	RON(L1)	"L" level Io=10mA		6	15	Ω
Low-side output On-resistance 2	RON(L2)	"H" level Io=-10mA		12	22	Ω
High-side output On-resistance 1	RON(H1)	"L" level Io=10mA		6	15	Ω
High-side output On-resistance 2	RON(H2)	"H" level Io=-10mA		12	22	Ω
DRIVE OUTPUT BLOCK (PWM BLOCK)						
Drive output PWM frequency	fPWMO	PWMF=0 Low frequency mode	18.5	19.5	20.5	kHz
Output PWM Duty cycle resolution	ΔPWMDUTY	PWMF=0 Low frequency mode (Note 5)			0.2	%
3V CONSTANT VOLTAGE OUTPUT						
Output voltage	V3RO		3.135	3.3	3.465	V
Voltage regulation	ΔV3R1	VS=6.0 to 20V			50	mV
Load regulation	ΔV3REG2	Io=5mA to 25mA			50	mV
Current Limit	IV3RO	Not for external loads > 5mA	50			mA
VCC 5V CONSTANT VOLTAGE OUTPUT						
Output voltage	VC5RO	VS=6.0 to 20V	4.75	5.00	5.25	V
Voltage regulation	ΔVC5R1	VS=6.0 to 20V			50	mV
Load regulation	ΔVC5R2	Io=5mA to 25mA			50	mV
Current Limit	IVCC5V		50			mA
VCC 3V CONSTANT VOLTAGE OUTPUT						
Output voltage	VC3RO		3.135	3.3	3.465	V
Voltage regulation	ΔVC3R1	VS=6.0 to 20V			50	mV
Load regulation	ΔVC3R2	Io=5mA to 25mA			50	mV
Current Limit	IVCC3V3		50			mA
LOW-SIDE GATE VOLTAGE OUTPUT (VGL Pin)						
Low-side output voltage1	VGLH1	6.0 < VS ≤ 8.0V Io=−10mA	8.0	12.0	14.0	V
Low-side output voltage2	VGLH2	8.0 < VS ≤ 20V Io=−10mA	10.0	12.0	14.0	V

Parameter	Symbol	Condition	Min	Typ	Max	Unit
HIGH-SIDE OUTPUT VOLTAGE (CHP Pin)						
Internal charge pump oscillator frequency	FCP	SSCG=0	49.6	52.1	54.6	kHz
Boost voltage1	VGHH1	6.0 < VS ≤ 8.0V Io=−10mA	VS +6.0	VS +12.0	VS +14.0	V
Boost voltage2	VGHH2	8.0 < VS ≤ 20V Io=−10mA	VS +9.0	VS +12.0	VS +14.0	V
PWMIN INPUT PIN in low frequency mode						
Input PWM frequency range	fLPWM		5.3		1000	Hz
PWM signal timeout	TLPWMIN			210	220	ms
PWMIN INPUT PIN in High frequency mode						
Input PWM frequency range	fHPWM		0		18.5	kHz
DIGITAL INPUT PIN (CSB, TXD)						
High-level input voltage	VIH1		0.8×V3RO			V
Low-level input voltage	VIL1				0.2×V3RO	V
Input hysteresis voltage	VIHYS1		0.1	0.35	0.6×V3RO	V
Pull-up resistance.	RDVI1		15	30	60	KΩ
DIGITAL INPUT PIN (SCLK, SI, PWMIN, TEST)						
High-level input voltage	VIH2		0.8×V3RO			V
Low-level input voltage	VIL2				0.2×V3RO	V
Input hysteresis voltage	VIHYS2		0.1	0.35	0.6×V3RO	V
Pull-down resistance	RDVI2		50	100	200	KΩ
WAKE INPUT PIN						
High-level input voltage	VIH3		2.5			V
Low-level input voltage	VIL3				0.6	V
Internal Pull-down resistance	RDVI3		50	100	200	KΩ
EN INPUT PIN						
High-level input voltage	VIH4		0.8×V3RO			V
Low-level input voltage	VIL4				0.2×V3RO	V
Input hysteresis voltage	VIHYS4		0.1	0.35	0.6×V3RO	V
Pull-down resistance	RDVI4		50	100	200	KΩ
DIGITAL OUTPUT PIN (SO, FG, DIAG, RXD)						
Output voltage	VOL	Io=1mA pull-up current			0.2	V
Output leakage current	ILOLK				10	μA

Parameter	Symbol	Condition	Min	Typ	Max	Unit
CURRENT LIMIT / OVER-CURRENT PROTECTION (RF, RFSENS)						
Current limit voltage	VRF1	Voltage between RF and RFSENS	90	100	110	mV
Over-current detection Voltage threshold	VRF2	Voltage between RF and RFSENS	180	200	220	mV
EXTERNAL THERMAL PROTECTION (TH)						
Threshold Voltage Falling	VTH0 VTH1 VTH2 VTH3	THTH[1:0]=00 THTH[1:0]=01 THTH[1:0]=10 THTH[1:0]=11	−10%	0.35 0.30 0.25 0.20	+10%	V
Hysteresis range	VTHHYS		0.025	0.05	0.075	V
THERMAL PROTECTION						
Thermal warning temperature	 TTW0 TTW1	(Junction temperature) (Note5) TSTS=0 TSTS=1	 125 150			°C
Thermal warning temperature hysteresis	TTWHYS	(Junction temperature) (Note5)		25		°C
Thermal shutdown temperature	 TTSD0 TTSD1	(Junction temperature) (Note5) TSTS=0 TSTS=1	 150 175			°C
Thermal shutdown temperature hysteresis	TTSDHYS	(Junction temperature) (Note5)		25		°C
VOLTAGE MONITORING (VS, CHP, VGL, VCC)						
VS under-voltage detection	VSLV		4.8		5.1	V
VS under-voltage detection hysteresis	VSLVHYS		0.1	0.25	0.4	V
VS Over-voltage detection	VSHV		20		24	V
Over-voltage detection hysteresis	VSHVHYS		0.5	1.0	1.5	V
CHP under-voltage detection	CHPLV		VS+4.5		VS+5.5	V
CHP under-voltage detection hysteresis	CHPLVHYS		0.2	0.4	0.7	V
VGL under-voltage detection	VGLLV		4.5		5.5	V
VGL under-voltage detection hysteresis	VGLLVHYS		0.2	0.4	0.7	V
VCC3.3 under-voltage detection	VCLV3	REGSEL=0, VCCEN = 1, VCLVPO=0	2.3		2.7	V
VCC3.3 under-voltage detection hysteresis	VCLVHYS3	REGSEL=0, VCLVPO=0	0.1	0.25	0.4	V
VCC5.0 under-voltage detection	VCLV5	REGSEL=1, VCCEN = 1, VCLVPO=0	3.8		4.2	V
VCC5.0 under-voltage detection hysteresis	VCLVHYS5	REGSEL=1, VCLVPO=0	0.1	0.25	0.4	V

Parameter	Symbol	Condition	Min	Typ	Max	Unit
LIN_PWMIN PIN (LIN TRANSMITTER)						
LIN output current bus in dominant state	Ibus_pas_dom	Driver OFF Vbus=0V,VS=7V & 18V	−1			mA
LIN output current bus in recessive state	Ibus_pas_rec	Driver OFF Vbus=VS,VS=7V & 18V			20	uA
Short circuit current limitation	Ibus_lim	Driver ON Vbus=VS, VS=7V & 18V	40		200	mA
Internal Pull-up resistance	Rslave	VS=7V & 18V	20	30	47	kΩ
LIN_PWMIN PIN (LIN RECEIVER & PWMIN)						
High-level input voltage	Vbusdom	VS=7V & 18V	0.6×VS		VS	V
Low-level input voltage	Vbusrec	VS=7V & 18V	0		0.4×VS	V
Input hysteresis voltage	Vbushys	VS=7V & 18V	0.05×VS		0.2×VS	V
AC characteristics LIN_PWMIN PIN						
Duty cycle 1	D1	THrecmax=0.744VS THdommax=0.581VS VS=7.0V…18V, tbit=50μs D1=tBusrecmin/(2*tbit)	0.396		0.5	
Duty cycle 2	D2	THrecmin=0.422VS THdommin=0.284VS VS=7.6V…18V, tbit=50μs D1=tBusrecmax/(2*tbit)	0.5		0.581	
Duty cycle 3	D3	THrecmax=0.778VS THdommax=0.616VS VS=7.0V…18V, tbit=96μs D1=tBusrecmin/(2*tbit)	0.417		0.5	
Duty cycle 4	D4	THrecmin=0.389VS THdommin=0.251VS VS=7.6V…18V, tbit=96μs D1=tBusrecmax/(2*tbit)	0.5		0.59	
Propagation delay bus recessive to RXD=high	Trx_pdr	VS=7V & 18V			6	μs
Propagation delay bus dominant to RXD=low	Trx_pdf	VS=7V & 18V			6	μs
Symmetry of receiver propagation delay	Trx_sym	trx_pdr-Trxpdf	−2		2	μs
Normal Slope rise time 12	T_rise_norm 12	VS=12V,LINSLP=0 L1,L2 (Note 6)			22.5	μs
Normal Slope fall time 12	T_fall_norm 12	VS=12V,LINSLP=0 L1,L2 (Note 6)			22.5	μs
symmetry of Normal Slope 12	T_sym_norm 12	VS=12V,LINSLP=0 L1,L2 (Note 6)	−4		4	μs
Normal Slope rise time 3	T_rise_norm 3	VS=12V,LINSLP=0,L3 (Note 6)			27	μs
Normal Slope fall time 3	T_fall_norm 3	VS=12V,LINSLP=0,L3 (Note 6)			27	μs
symmetry of Normal Slope 3	T_sym_norm 3	VS=12V,LINSLP=0,L3 (Note 6)	−5		5	μs
Low Slope rise time	T_rise_low	VS=12V,LINSLP=1,L3 (Note 6)			62	μs
Low Slope fall time	T_fall_low	VS=12V,LINSLP=1,L3 (Note 6)			62	μs

Note 4: Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Note 5: Not tested in production. Guaranteed by design.

Note 6: Load conditions Rbus/Cbus: L1=1kΩ/1nF, L2=660Ω/6.8nF, L3=500Ω/10nF Typical Operating Conditions

DETAILED FUNCTIONAL DESCRIPTON

The LV8907 integrates full sensor-less brushless DC motor commutation and Proportional/Integral (PI) speed control. A robust startup algorithm combined with OTP registers for important system parameters make this IC a solution of choice for many BLDC applications which need to turn a motor in one direction only such as pumps, fans, etc. No detailed BLDC commutation knowledge is necessary.

Building a BLDC application with the LV8907 is even simpler than building a DC motor. Only a PWM pulse train is necessary to control the motor – either directly or via speed control. Switch-only applications are also possible. Speed and error information can be fed back to the control unit via FG and DIAG outputs.

If more complex operation and flexibility are required the LV8907 can be combined with a small microcontroller. The LV8907 implements motor commutation and includes all necessary support circuitry for the microcontroller such as:

- 5V/3.3V Power supply.
- Integrated watchdog timer.
- LIN Transceiver.
- External Temperature Sensor.

In case of system errors such as a missing control signal, or a watchdog error, the LV8907 includes auto-run settings. If one of those errors occur and connection to the microcontroller is lost, the motor can continue running at a pre-defined fixed duty cycle of 25%, 50%, 75% or 100%.

Motor Commutation

Motor position is detected using the BEMF of the un-driven phase of a rotating three-phase motor relative to its neutral point connected to COM. Once an adequate BEMF level has been detected voltages applied via PWM to the other two phases of the motor maintain rotation. The digital equivalent of the BEMF signal appears at FG.

Two different PWM patterns can be selected via register MRCONF12 to match motors with trapezoidal or sinusoidal BEMF.

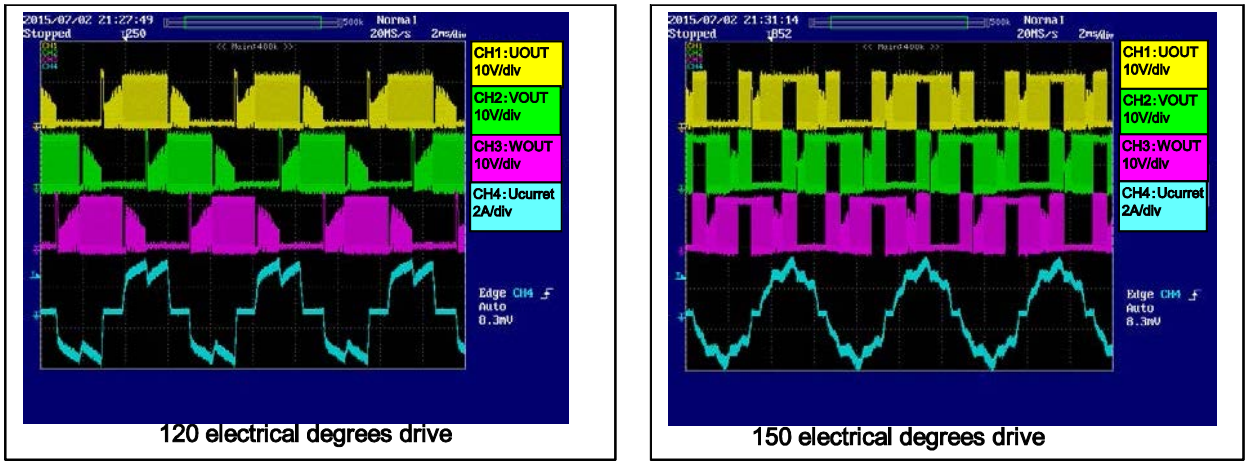


Figure 5: Trapezoidal vs. Sinusoidal Drive @ 50% Duty cycle
(CH1&3=Phase Voltage, CH2=Phase Current, CH4=Speed signal FG)

Figure 5 shows a comparison of a motor driven with normal trapezoidal commutation (left) vs. one driven with sinusoidal drive. With sinusoidal drive each phase is driven 150 electrical degrees with soft transitioning. This results in sinusoidal drive current with lower total harmonic distortion, reducing both torque ripple and noise. Trapezoidal drive results in a higher voltage across the motor phases and may be preferable for high torque and high speed operation.

Maximum Motor Speed

The maximum physical motor speed of the application is limited by the internal clock to approximately 48000 electrical RPM. If this is exceeded the LV8907 coasts the motor until BEMF detection and drive can resume.

Commutation Angle Adjustment

In trapezoidal commutation mode it is possible to advance the commutation angle by up to 28 electrical degrees as defined in register LASET. Early commutation adjusts the rotor magnetic field positioning and allows for higher motor speeds at the expense of efficiency. Advancing commutation can be done dynamically by a companion microcontroller.

Motor Startup

BEMF is used for rotor position sensing but for BEMF generation the motor has to be rotating. A stopped motor will initially be driven open-loop until BEMF can be detected.

Open-loop operation is motor parameter dependent. The most critical parameters depend on load and motor inertia. They are initial commutation frequency and PWM duty cycle (which affects motor flux density).

In the LV8907, the initial commutation frequency is programmed with register STOSC. Flux density is regulated by limiting startup current with a current ramp. During this ramp the current limit is increased in 16 steps from 0 to the maximum current defined by the external shunt. The ramp time from 105ms to 6.72s is

defined in register SSTT. Register SSTEN allows to disable the current ramp if necessary.
Fixed motor speed will be applied until either a valid BEMF has been detected in all three phases or the startup timer expires.

Motor Lock

This timer begins after the end of the current ramp and can be programmed from 420ms to 6.72s in register CPTM. If the timer expires a locked rotor error is flagged. In automatic retry mode, the LV8907 will restart after standby mode for time of eight times of CPTM.

Spin-up of Rotating Motors

The LV8907 can perform free-wheeling detection before applying the open loop spin-up algorithm described above. If the motor is already turning in the right direction the IC will continue with closed loop commutation. If the motor is turning in the wrong direction, the IC will wait for the motor to stop and then perform open-loop startup.

There are two scenarios where this behavior might not be desirable:

1. Fast Startup is required
   Free-wheeling detection takes up to one electrical revolution of the motor, which may be inacceptable for some applications. In this case free-wheeling detection can be disabled by setting FRREN. See section "Fast Startup" on page 18.
2. Wind-milling backwards
   Should the motor be driven by some external force as it is freewheeling in the wrong direction the LV8907 will potentially wait forever. Should start-up under these conditions be required, free-wheeling detection must be disabled as well.

Chip Activation, Shutdown and System States

After power up of VS and WAKE above 2.5V the LV8907 wakes up. Standby mode is entered after VS has exceeded 5.5V (min.).

A high level on WAKE > 2.5V (max.) activates the IC from sleep mode which enables the internal linear regulator at V3RO. Once the voltage on V3RO as sensed on V3RI has passed the power on reset (POR) threshold the system oscillator starts, and after 32 counts of the system clock (3.2µs typical) releases the internal digital reset which simultaneously starts the external regulator VCC and the charge-pump, and loads the system register contents from OTP into the internal registers. During the entire wake-up sequence of 8ms (typ.) DIAG is masked for charge-pump and VCC under-voltage. After wake-up is complete, the IC enters Standby mode and DIAG is activated to display internal errors. During Standby mode full SPI access is possible.
A high on EN takes the LV8907 from Standby to Normal mode. Normal mode allows motor control and SPI access is limited. A low on EN disables the motor stage regardless of the PWM input and returns the part back to Standby mode.
The IC is shut down by taking WAKE below 0.6V (min.). WAKE has priority over the state of EN, if EN hold functionality is desired; it needs to be implemented with an external diode from EN to WAKE.

System States

LV8907 has three operating modes. The operating modes are controlled by WAKE and EN.

Sleep mode
Sleep mode is a power saving mode. All circuits are powered down, charge pump is inactive and the SPI port is unusable. Activating WAKE allows the transition from the sleep mode to either Standby or Normal mode.

Standby mode
In Standby mode the OTP content has been transferred into the master-register. In this mode all outputs are turned off. Any internal writable register that is not locked can be configured by SPI interface.

Normal mode
In normal mode, outputs can be controlled and all blocks are active. All registers can be read through the SPI interface.

Mode	WAKE	EN	Internal bias	Logic	VCC	Charge pump	Drivers
Sleep	L	×	Disable	Reset	Disable	Disable	High-Z
Standby	H	L	Enable	Active	Enable	Enable	Low
Normal	H	H	Enable	Active	Enable	Enable	Enable

Supply Voltage Transients

The LV8907 is well suited to operate during typical automotive transients. It is fully functional during start-stop transients, as it maintains all specified parameters for supply voltages from 6V < VS < 20V. If the supply voltage falls below 5V, for example during cold-cranking, under-voltage error is flagged, but digital functionality is maintained until the internal regulator falls below its under-voltage lockout level of 2.2V. The VCC regulator must be configured for 3.3V if low transient operation is desired.

If over-voltage protection is enabled in MRCONF10 an over-voltage error is indicated if the supply rises beyond 20V(min). In both under- and over-voltage error modes, the power stage drivers UH, VH, WH and UL, VL, and

WL go low, turning the external power stage high-impedance and letting the motor freewheel. The LV8907 will re-engage the motor after conditions have returned to normal.

System Power Supplies

Three power supplies are integrated into the LV8907:

- An internal 3.3V regulator provides power to the digital and interface section.
- The VCC regulator can be configured to provide 5V or 3.3V to an external processor and other loads.
- A dual stage charge-pump allows 100% duty cycle operation and maintains full enhancement to the power stage at low input voltages.

Internal Regulator V3RO, V3RI

The internal regulator is supplied from VS, provides 3.3V at V3RO. V3RI is connected to the power supply inputs of the control and logic circuit blocks. V3RO and V3RI need to be connected externally and bypassed to the GND plane for stability. V3RO must not be used for external loads.

VCC Regulator

The VCC regulator may power external loads up to 50mA(max). VCC becomes active during Standby mode and can be configured via register VCCSEL to provide 5V or 3.3V. Under-voltage error is flagged if the output voltage drops below 4.2V in 5V operation, or 2.7V in 3.3V operation.

The VCC regulator can be enabled or disabled with register VCCEN.

Charge Pump Circuit for CHP and VGL

LV8907 has an integrated charge pump circuit for low-side and high-side pre-driver supply. Low side drive voltage at VGL is 12V(typ.) and high side drive voltage at CHP is VS+12V(typ.). For functionality see Figure 6.

Under-voltage protection for the low side drivers activates if VGL falls below 4.8V in which case the output FET's will be turned off and VGL under-voltage error is flagged in register MRDIAG. Over-voltage protection for the high side drivers activates if VS becomes greater than 20V(min). In that event the driver stage is disabled, over-voltage error is flagged in register MRDIAG, and both VGL and CHP are discharged to prevent output circuit destruction.

The charge pump circuit operates nominally at 52.1KHz. A SSCG function is provided to add a spread-spectrum component for EMI reduction.

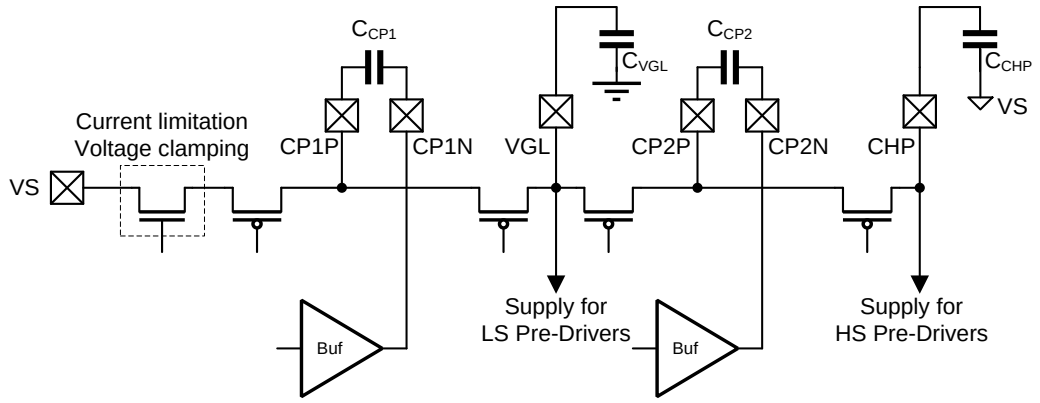


Figure 6: Charge Pump Circuit

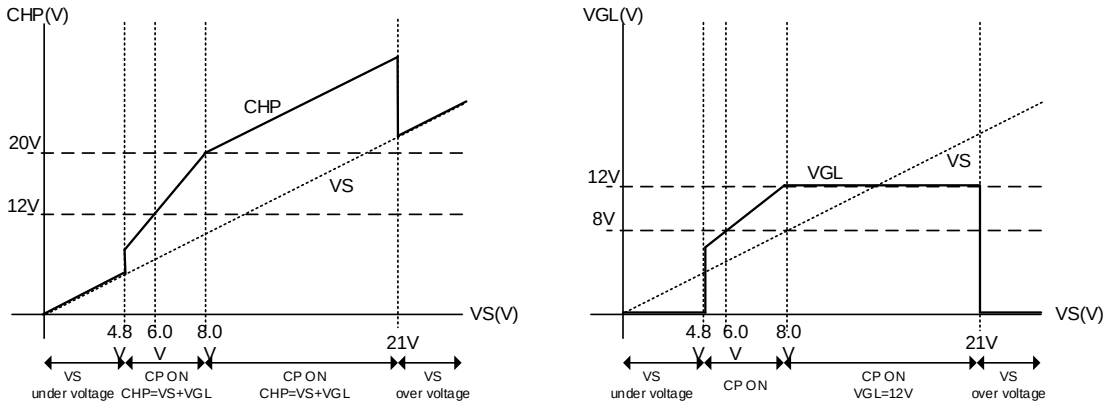


Figure 7: High Side and Low Side Gate Voltages

INPUT PWM and SPEED CONTROL

The LV8907 provides three speed control methods through the input PWM signal:

1. Direct PWM pass-through
2. Indirect PWM translation
3. Closed loop speed control

Direct PWM Pass-through

The input PWM frequency and duty cycle are directly fed to the power stage. This allows a companion microprocessor direct control over duty cycle and output frequency up to 18.5kHz. No input frequency detection takes place in this mode, so 100% and 0% duty cycle can be applied.
NOTE: It is important not to exceed 18.5kHz to maintain reliable back-EMF detection.
When the register bit PWMF is set 1, this control method is selected.

Indirect PWM Translation

This is the preferred mode for stand-alone operation. In this mode the input PWM signal is compared against minimum and maximum PWM frequency thresholds to allow for more robust operation. Frequencies above 1kHz are ignored and frequencies below 5.3Hz(typ.) are considered as 0% or 100% duty cycle (no frequency). The duty cycle of the PWM input signal is measured with a resolution of 9 bits. There is an inherent delay to detect and utilize this duty cycle information, the motor will not start. The delay time is determined by $T_{PWM} \times \left(1 + \frac{1}{8}\right)$. If faster start-up is necessary, see section "Fast Startup" below. If no frequency is detected after 210ms (typ.) the PWMPO flag is set in system warning register MRDIAG1. Even without PWM input the LV8907 can run as described below in section "Fast Startup".
If a valid frequency was detected, the LV8907 evaluates the input duty cycle and translates it into an output duty cycle as shown in Figure 8. The output PWM frequency is fixed to 19.5kHz (typ.).

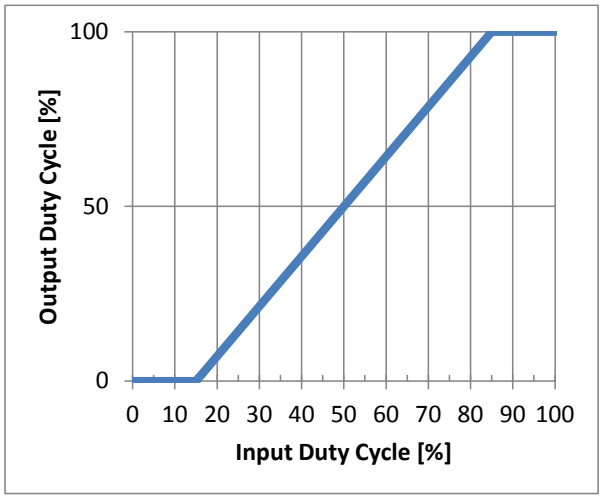


Figure 8: Duty Cycle Translation

Input duty cycles lower than 15% are considered a motor-off command and will also reset the error registers. Input to output duty cycle translation is described by the following formula:

$$d_{OUT} = \begin{cases} 0 & , \quad 0 \le d_{IN} \le 15 \\ \frac{10}{7}(d_{IN} - 15) & , \quad 15 < d_{IN} < 85 \\ 100 & , \quad 85 \le d_{IN} \le 100 \end{cases}$$

Closed loop speed control

For stand-alone operation, the LV8907 offers a PI controller for motor speed which is activated by clearing bit SCEN. Frequencies above 1kHz are ignored and frequencies below 5.3Hz(typ.) are considered as 0% or 100% duty cycle (no frequency). The output PWM frequency is fixed to 19.5kHz (typ.).

LV8907 provides nine target speed values which are stored in registers FGT0 to FGT8. In speed control mode the input PWM duty cycle is encoded as a selector for these registers as shown in Figure 9. A duty cycle hysteresis allows for stable register selection.

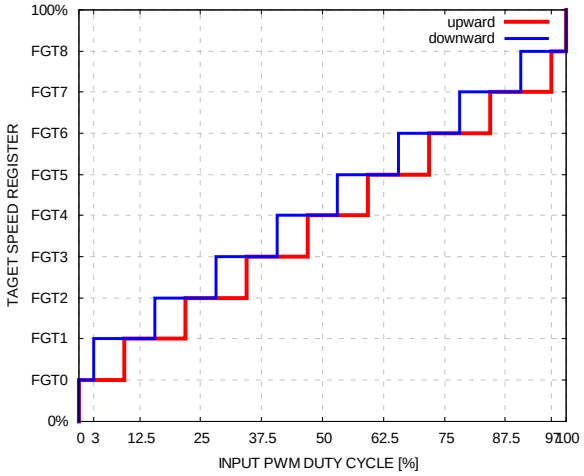


Figure 9: Target Speed Register Selection by Input PWM Duty Cycle

A duty cycle of 50% with a variation band of 6.25% for example will select the motor speed value stored in the 4th speed register FGT4. This allows for non-linear speed curves. When using a companion microcontroller it is possible to write to the speed register in real time during operation to achieve finer RPM resolution. For more information see section "Target speed setting" on page 33.

The Control algorithm

The LV8907 controls the motor speed by comparing the selected target speed to the actual motor speed and incorporating a PI controller with configurable gains for the P and I components which are stored in register MRSPCT0 and MRSPCT1 respectively.

Ramping of Speed Control Values

While tight control is required for optimal speed tracking, it may be undesirable during large input changes as it may lead to sudden supply loading, increasing noise and motor wear. To limit the slope of the control signal, register STEPSEL imposes a ramp on an input step to slew the speed response of the motor.

Decreasing motor speed too fast results in energy recuperation back into the system. To limit over-voltage during energy recuperation, the variable DWNSET allows either

1. to distribute the recuperation energy over a longer period of time or
2. to prevent energy recuperation entirely.

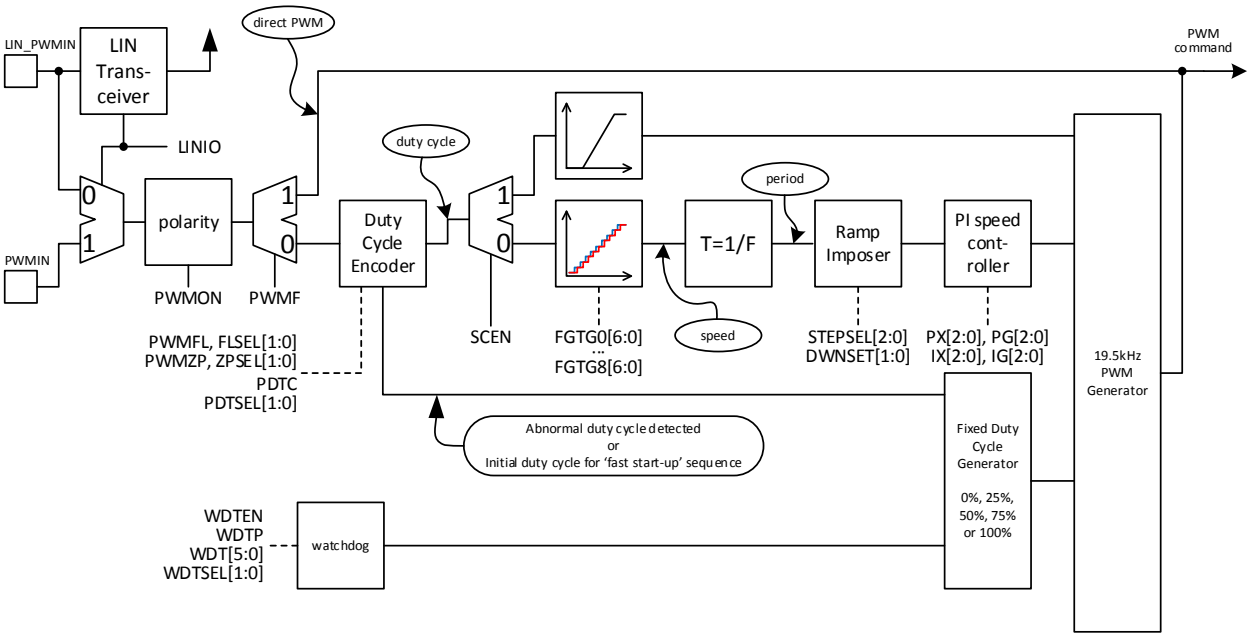


Figure 10: PWM Command Flow and Related Registers

Fast Startup

It may be desirable to have the motor start immediately after EN goes high and not wait for PWM input duty cycle evaluation. Two register settings enable motor operation during this evaluation time: bit PDTC determines if the motor should be running during this time at all, and PDTSEL selects a motor duty cycle of 25, 50, 75 or 100%. This is used as the initial value of the duty cycle command for the closed loop speed control mode. To guarantee smooth transition from fast startup to PWM operation it is important to apply a comparable external PWM duty cycle at startup. Also make sure that free-run detection is disabled (FRREN=1) to improve start-up speed.

Abnormal Duty Cycle Operation (100% or 0%)

For normal duty cycle controlled operation the PWM signal is expected to have a frequency between 5.3Hz and 1kHz. If no frequency is detected, the LV8907 will flag PWMO error and enter 0% or 100% duty cycle mode depending on the level of the PWM signal (all low or all high). Operation during this mode can be selected to be either no motor operation, or motor operation at a fixed motor duty cycle of 25, 50, 75 or 100% as defined by the variables PWMFL and FLSEL or PWMZP and ZPSEL. These PWM values do not enter into the speed control loop.

Speed Feedback FG

The motor speed is shown at open drain output FG where the transitions are direct representations of the BEMF signal transitions on the motor. The relationship between motor rotation and FG pulses is defined in register FGOF.

Fault Output DIAG

A low on open drain output DIAG indicates a system fault and a shutdown of the driver stage. Per default all system faults self-recover when the fault condition is removed. For some potentially destructive faults such as over-current, FET-short circuit and locked rotor conditions, it is possible to latch the fault condition. For more information on system diagnostics see section “System Errors and Warnings” on page 20.

LIN Transceiver

LIN_PWMIN can be used as a local interconnect network (LIN) 2.2A compatible LIN transceiver by setting the LINIO bit and connecting an external microcontroller to RXD and TXD. The microcontroller must handle the LIN communication and control the LV8907 through EN, PWMIN and the SPI interface. The LIN transceiver can be switched to low slope mode to reduce electromagnetic emissions by setting LINSLP=1. For more information on the automotive LIN bus protocol consult publicly available documentation.

Gate Drive Circuit

The gate drive circuit of the LV8907 includes 3 half-bridge drivers which control external N-Channel FETs for the motor phases U, V and W. The high side drivers UH, VH, WH switch their gate connection either to CHP or the respective phase connection UOUT, VOUT and WOUT. The low-side drivers are switched from VGL to the corresponding source connection SUL, SVL, SWL. Both high and low side switches are not current controlled. Slope control has to be implemented with external components.

Current shoot-through protection of the bridge-drivers is implemented by a dead-time counter that delays the turning- on of the complementary switch. The dead-time can be programmed from 100ns < t_{FDTI} < 3.2us into 5bit parameter FDTI.

To protect against external shorts the drain-source voltage of the active external Power FETs is monitored as well. 4 bit register FSCDL selects a short-circuit shutoff voltage 100mV < V_{FSCLD} < 1.6V. To suppress false triggering during the rising edge of FET activation, a four bit masking time can be programmed in FSCDT.

Current Limit and Over-current Shutoff

An integrated current sense amplifier implements current limiting and over-current shutoff by measuring the motor phase current across a single shunt between RF and RFSENS.

Figure 11 on page 19 shows a summary of the current limit and the over-current shutoff, and the descriptions for each function are in the following sections.

Cycle-by-cycle Current Limit

If the voltage between RF and RFSENS exceeds V_{RF1}=100mV(typ.), the active bridge is turned off until the next PWM period. To suppress switching transients a current limit blanking time 0.1us < t_{CLMASK} < 1.6us can be programmed into register CLMASK.

During soft-start this current limit is ramped from 0 to 100mV in 16 steps during a programmable time 105ms < t_{SSTT} < 6.71s as defined in register SSTT.

Over-current Shutoff

If the bit OCPEN is set and the voltage between RF and RFSENS exceeds V_{RF2} = 200mV(typ.), the LV8907 goes into over-current shutoff and all gate drivers are driving low turning the power FETs high-impedance. To suppress switching transients an over-current shutoff blanking time 0.2us < t_{OCMASK} < 3.2us can be programmed into register OCMASK.

Current	Purpose	Flag	Sense point	Threshold	Turn-off	Recovery
Cycle-by-cycle	Limiter	None	Sense Resistor VRF	100mV	PWM FET	Next PWM cycle
Short to VS	Protector	OCPO	Sense Resistor VRF	200mV	All FET	52.4ms later
		FSPO	FET VDS	configurable		
Short to GND	Protector	FSPO	FET VDS	configurable	All FET	52.4ms later

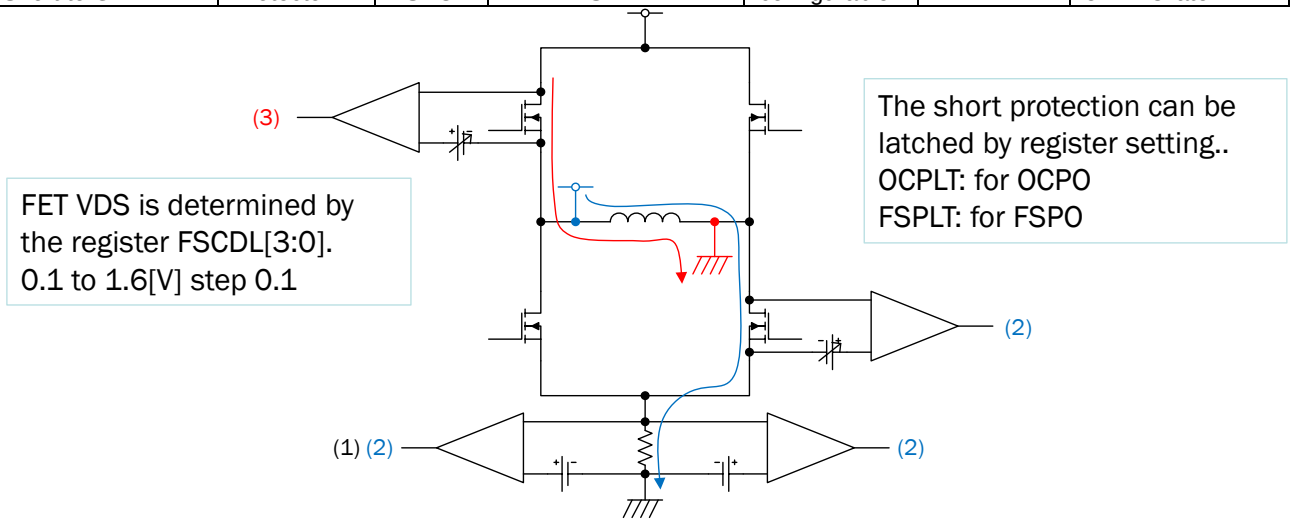


Figure 11: Current Limit vs. Over-current Shutoff

Temperature Sensing

The LV8907 measures internal die temperature and implements internal thermal warning and shutoff. It is also possible to protect external devices by monitoring the voltage at pin TH. Internal and external over-temperature can shut down the driver section.

Internal Over-temperature Measurement

A thermal warning is issued if the internal temperature of the device reaches approximately 25°C below the over-temperature shutoff level. The shutoff level is selected by bit TSTS as 150°C or 175°C(min).

External Over-temperature Shutoff

An analog comparator triggers external over-temperature error if the voltage at pin TH falls below the two bit programmable level 0.2V < V_{THTH} < 0.35V as defined by register THTH. For external temperature measurement connect a resistor between V3RO and TH and an NTC between TH and AGND. The programmed threshold voltage at V_{THTH} should be reached at the intended thermal shutdown temperature of the external component to be protected. During the over-temperature condition, the gate drivers are disabled and a flag, THPO in MRDIAG0 is set.

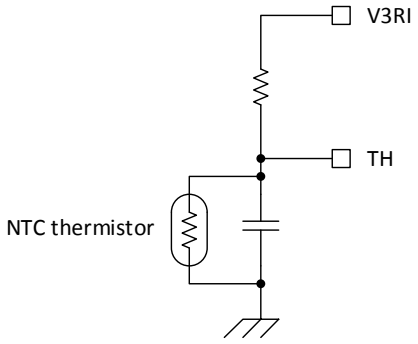


Figure 12: Example Circuit for External Temperature Sensing

Watchdog Operation

The LV8907 includes a watchdog timer to monitor a companion microcontroller and disable the motor if the microcontroller stops working properly. Bit WDTEN enables and disables the watchdog timer. Access to this bit can be blocked – see section “OTP Registers” on page 37 for details. The enabled watchdog will issue an error whenever the watchdog time 1.64ms < t_{WDT} < 104.96ms expires. A write of 00h to register MRST resets the watchdog timer.

A watchdog timeout can result in either a motor stop, or motor operation at four predefined duty cycles (25%, 50%, 75%, 100%) as defined by WDTP and WDTSEL. The duty cycle is directly applied to the power stage, not through the speed selection registers. The microprocessor is not re-set.

System Errors and Warnings

All system errors and most warnings cause a transition on DIAG. The polarity of this transition can be selected in bit DIAGSEL. The ability of stand-alone applications without microcontroller to react to errors and warnings is limited. For this case various auto-retry strategies are implemented.
If a companion microcontroller exists, more complex error handling is possible and DIAG should be connected to an interrupt input of the microcontroller.

Errors that may cause serious damage such as short-circuit, over-current and locked rotor can be latched by enabling the corresponding latch bit in MRCONF10. In this case the LV8907 will keep the output stage disabled until the latch is cleared by one of the following actions:

- Power on reset.
- EN low.
- Low frequency PWM less than 15% duty cycle.
- SPI write of FFh to MRRST.

If bit DLTO is set ONLY latched errors will cause a transition of DIAG. To detect the other less serious errors and warnings, the diagnostic registers MRDIAG0/MRDIAG1 have to be read regularly via SPI access.

Table 1) Error Register: MRDIAG0[7:0]

Bit	Error	Description	Maskable	Latchable	Self Recovery when latch function turned off
0	OCPO	Over-current Error	X	X	After 52.4ms (typ.) the motor will re-start.
1	VSLVPO	VS Under-voltage			Motor is re-started when voltage recovers.
2	VSOVPO	VS Over-voltage	X		Motor is re-started when voltage recovers.
3	CHPLVPO	CHP Under-voltage			Motor is re-started when voltage recovers.
4	VGLLVPO	VGL Under-voltage			Motor is re-started when voltage recovers.
5	FSPO	FET Short Circuit	X	X	After 52.4ms (typ.) the motor will re-start.
6	THPO	TH Over-temperature	X		Motor is re-started when temperature recovers.
7	CPO	Locked Rotor	X	X	Wait 8 t_{CPTM} periods (see “Motor Lock” on page 15)

See register MRCONF10 for error activation and masking and MRCONF11 for latching options.

Table 2) Warning Register: MRDIAG1[7:0]

Bit	Warning	Description	DIAG	Blankable	Effect
0	THWPO	Junction Temp. Warning	X	X	The IC has exceeded the warning temperature but stays in Normal operation.
1	THSPO	Junction Over-temperature	X		The IC has exceeded the shutoff temperature. Drivers are shut down during over-temperature.
2	WDTPO	Watchdog Timeout	X	X	Driver stage is shut off or continues with pre-selected duty cycle (25, 50, 75, 100%).
3	STUPO	Startup Operation			The motor is running open loop.
4	SPCO	Loss of speed lock			Target speed and actual speed are more than 6.25% different.
5	Internal Use				
6	VCLVPO	VCC under-voltage	X	X	Driver stage off.
7	PWMPO	PWM Input Fault	X		No PWM signal detected. Driver stage is shut off or continues with pre-selected duty cycle (25, 50, 75, 100%).

*An “X” in column “DIAG Blank” means that it is possible to prevent a warning from triggering DIAG see register MRCONF10 for details.

SPI Interface

In the LV8907 the SPI interface is used to perform general communications for status reporting, control and programming.

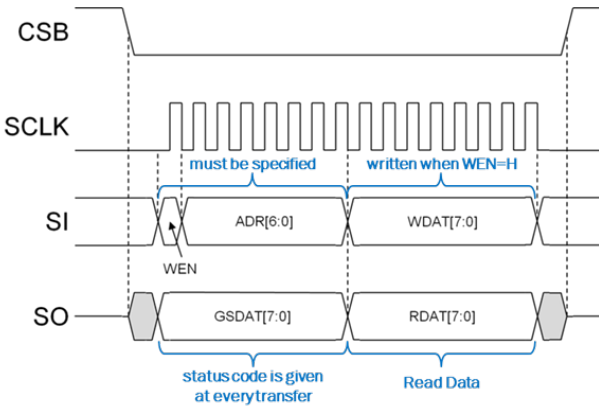


Figure 13: SPI Format

SPI communications with the LV8907 follows established industry standard practices including the use of WEN and start and stop bits as shown above. Data is transferred MSB first and both clock and data are transferred as 'true' data with the higher level indicating a logical 1 or true state. If WEN is LOW, the register data is transferred from LV8907 to the microcontroller. If WEN is HIGH, the register data is transferred from the microcontroller to the LV8907 register.

There are two items to be especially careful of with the general communication scheme:

(1) Communications must be full duplex and simultaneous. It is not allowed to send one transaction and then read data on a second transaction as the status register information will be updated on the first transaction and then be out of date for the second. Some systems break transactions into separate read and write operations which is not acceptable with the LV8907.

(2) It is important the system master uses the clock and data polarities and phases as shown above. Both the clock and data on some systems can be inverted for various reasons but must arrive at the LV8907 per the above drawing. Common errors include SCLK inversion such that the leading edge arrives as a downward transition rather than a rising edge, or having the data to clock phase incorrect. Data phase must be such that the data only changes during a clock falling edge and is completely stable during a clock rising edge. This means a good margin of one half of a bit time exists to eliminate transmission delay hazards.

The first byte returned on all transactions is always the status register, GSDAT, and contains information such as the busy flag during programming operations.

GSDAT[7:0]								
Bit 7	**6**	**5**	**4**	**3**	**2**	**1**	**Bit 0**	
ORBEN	STUPO	SACF	DIAGS	LATCH	OBSY	SMOD[1:0]		
						0	0	Sleep mode (MRACK[7:0]=FFh)
						0	1	Device start up time
						1	0	Standby mode
						1	1	Normal mode (MRACK [7:0]=55h)
0	x	x	0	0	0	x	x	Normal Operation
					1			OTP busy with read/write access
				1				Latched shutdown condition
			1					Failure Condition
		0						Last SPI access OK
		1						Last SPI access failed*
	0							Motor in Startup mode
	1							Motor in Normal drive mode
1								OTP integrity test mode

The following SPI failures are detectable and reported collectively in GSDAT as general SPI failures:

- Any access to an address which are outside the defined address space.
- The number of SCLK transitions is not 16 within one word transfer.
- Any access to MRCONF, MRACS, ORCONF, ORACS while OBSY=1 (during write operations)
- Write access to MRODL register while OBSY=1 (during write operations.)
- Write access to any of the main registers after setting MSAENB=1 (Implies MRxxxx registers are locked).
- Write access to any of the OTP registers after OSAENB=1 (Implies ORxxxx registers are locked). .
- Write access attempt to a read only or locked register.
- SI signal changed at positive edge of SCLK. (Incorrect data/sclk phase setup)

SPI Timing

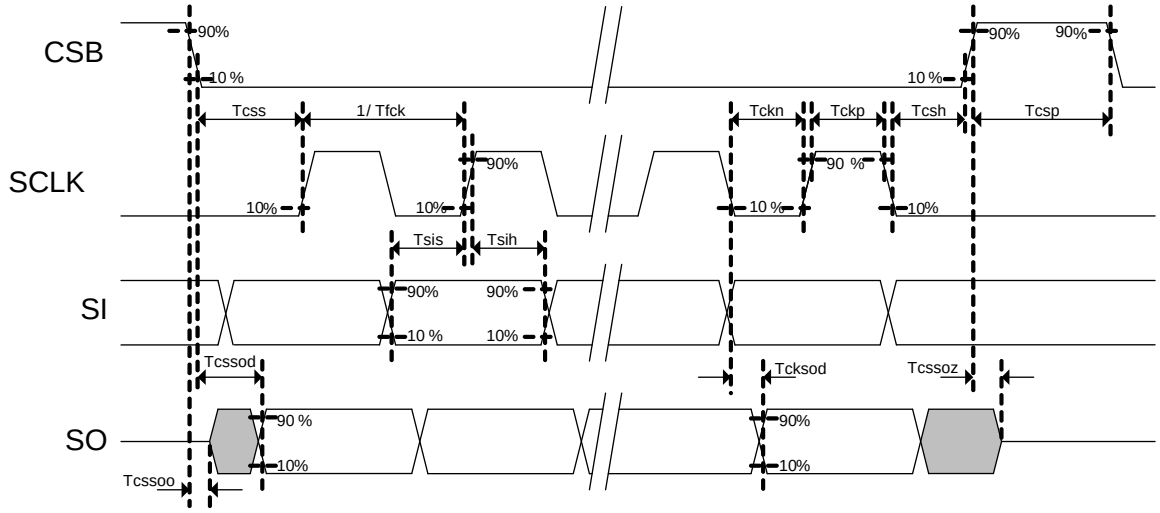


Figure 14: SPI Timing Chart

Tj=-40 to 150°C, VS=4.5 to 20V
Pull-up resistance of SO pin=2.4kΩ, Output load of SO pin=30pF

Symbol	Comment	Min	Typ	Max	Unit
Tfck	SCLK clock frequency			500	kHz
Tckp	SCLK high pulse width	950			ns
Tckn	SCLK low pulse width	950			ns
Tcss	CSB setup time	950			ns
Tcsh	CSB hold time	950			ns
Tcsp	CSB high pulse width	1900			ns
Tsis	SI setup time	450			ns
Tsih	SI hold time	450			ns
Tcssod	CSB fall edge to SO delay time			950	ns
Tcksod	SCLK fall edge to SO delay time			950	ns
Tcssoo	CSB fall edge to SO data out time	0			ns
Tcssoz	CSB rise edge to SO Hi-Z out time			950	ns

REGISTER DESCRIPTION

SPI Register Map

The SPI interface allows read access to the entire address space. The MASTER registers can only be written in Standby mode and then only if the write lock bit MSAENB has never been set high.

Addr	Register	Description	Write Enable	Standby Mode	Normal Mode
IC Setup Register					
00h	MRCONF0	Main function Free-run Detection ON/OFF setup	MSAENB	Read / Write	Read
01h	MRCONF1	PWM Input Specification	MSAENB	Read / Write	Read
02h	MRCONF2	Soft-start EN setup / FG output setup / Dead time setup	MSAENB	Read / Write	Read
03h	MRCONF3	PWM undetected operation mode setup Soft-start setting	MSAENB	Read / Write	Read
04h	MRCONF4	Activation frequency setup	MSAENB	Read / Write	Read
05h	MRCONF5	Current limit detection timing setup / Over-current detection setup	MSAENB	Read / Write	Read
06H	MRCONF5	For Internal Use Only	MSAENB	Read / Write	Read
07h	MRCONF7	Sync rectification setup Protection setup FET short Protection	MSAENB	Read / Write	Read
08h	MRCONF8	SSCG Protection setup Locking Protection Overheat protection	MSAENB	Read / Write	Read
09h	MRCONF9	WDT setup	MSAENB	Read / Write	Read
0Ah	MRCONF10	Error / warning masks and DIAG output setup	MSAENB	Read / Write	Read
0Bh	MRCONF11	Speed FB operation setup at deceleration WDT protection operation setup Latch setup	MSAENB	Read / Write	Read
0Ch	MRCONF12	Lead angle setup Silent drive setup STEP at the time of changing Speed FB target revolution	Always OK	Read / Write	Read / Write
Speed Control Setup					
10h	MRSPCT0	Proportional Gain Setup	Always OK	Read / Write	Read / Write
11h	MRSPCT1	Integral Gain Setup	Always OK	Read / Write	Read / Write
12h	MRSPCT2	3.125% Input PWM	Always OK	Read / Write	Read / Write
13h	MRSPCT3	12.5% Input PWM	Always OK	Read / Write	Read / Write
14h	MRSPCT4	25% Input PWM	Always OK	Read / Write	Read / Write
15h	MRSPCT5	37.5% Input PWM	Always OK	Read / Write	Read / Write
16h	MRSPCT6	50% Input PWM	Always OK	Read / Write	Read / Write
17h	MRSPCT7	62.5% Input PWM	Always OK	Read / Write	Read / Write
18h	MRSPCT8	75% Input PWM	Always OK	Read / Write	Read / Write
19h	MRSPCT9	87.5% Input PWM	Always OK	Read / Write	Read / Write
1Ah	MRSPCT10	96.875% Input PWM	Always OK	Read / Write	Read / Write

Addr	Register	Description	Write Enable	Standby Mode	Normal Mode
System Diagnostics and Test					
20h	MRACS	Lock Bits for OTP and Main Register write		Read	Read
30h	MRACK	SPI Operation Diagnostics	-	Read	Read
31h	MRODL	OTP data READ	Always OK	Read / Write	Read
32h	MRRST	For WDT/Protection Reset	Always OK	Read / Write	Read / Write
33h	MRORB	For OTP Zapping check	Always OK	Read / Write	Read
34h	MRDIAG0	Protection status check	-	Read	Read
35h	MRDIAG1	Protection status check	-	Read	Read
38h	TEST1	Production test register 1			
…					
3C	TEST5	Production test register 5			
OTP Memory Section					
40h	ORCONF0	Default states of MRCONF0 – MRCONF12			
…					
4Ch	ORCONF12	transferred upon startup			
50h	ORSPCT0	Default states of MRSPCT0 – MRSPCT10			
…					
5Ah	ORSPCT10	transferred upon startup			
60h	ORACS	Default states of MRACS			

Motor Configuration Register Overview

ADDR[6:0]	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00h	MRCONF0	FRMD	FRREN	SCEN	PWMF	REGSEL	VCEN	LINSLP	LINIO
01h	MRCONF1	FLSEL[1:0]		ZPSEL[1:0]		PWMFL	PWMZP	PDTC	PWMON
02h	MRCONF2	SSTEN	FGOF[1:0]		FDTI[4:0]				
03h	MRCONF3	PDTSEL[1:0]		SSTT[5:0]					
04h	MRCONF4	STOSC[7:0]							
05h	MRCONF5	CLMASK[3:0]				OCMASK[3:0]			
06h	MRCONF6	Internal Use Only							
07h	MRCONF7	SYNCEN	PPDOSEL	FSCDT[1:0]		FSCDL[3:0]			
08h	MRCONF8	SSCG	CPTM[3:0]				THTH[1:0]		TSTS
09h	MRCONF9	WDTEN	WDTP	WDT[5:0]					
0Ah	MRCONF10	VCLVPEN	CPEN	THWEN	THPEN	FSPEN	OVPEN	OCPEN	DIAGSEL
0Bh	MRCONF11	DWNSET[1:0]		WDTSEL[1:0]		CPLT	FSPLT	OCPLT	DLTO
0Ch	MRCONF12	STEPSEL[2:0]			SLMD	LASET[3:0]			

MRCONF0

Address = 00h				Standby Mode: **Read/Write** Normal Mode: **Read Only**			
Bit 7	**6**	**5**	**4**	**3**	**2**	**1**	**Bit 0**
FRMD	FRREN	SCEN	PWMF	REGSEL	VCEN	LINSLP	LINIO

FRMD: Forward / reverse selection

The physical motor rotation direction depends on the wiring of the three phases.
FRMD=1 reverses the motor direction.

FRREN: Free-run detection enable

Decides if the LV8907 does a BEMF detection before attempting to start the motor open-loop excitation and commutation.

FRREN=0 Motor will start with a BEMF detection.
FRREN=1 Motor will start open loop with startup parameters.

SCEN: Speed feedback control enable

This bit selects the LV8907 internal speed feedback control or PWM pass-through. Speed feedback control is active when SCEN=0. RPM is selected from input duty cycle as shown in Figure 9 on page 17.
SCEN=1: The closed loop speed control is inactivated.

PWMF: PWM input frequency selection

Decides the PWM input frequency range and PWM translation configuration.
PWMF=0: Indirect PWM translation or closed loop speed control. Valid PWM input frequency from 5.3Hz to 1kHz.
PWMF=1: Direct PWM pass-through. Valid PWM input frequency up to 18.5kHz. In this mode the PWM frequency is directly fed to the power stage. Internal closed loop speed control cannot be used.

The following table shows the configuration summary based on the combination of SCEN and PWMF.

SCEN	PWMF	Speed control	Input PWM frequency range [Hz]	Output PWM frequency
0	0	closed loop	5.3 to 1000	19.5 [kHz]
1	0	indirect translated	5.3 to 1000	19.5 [kHz]
0	1	direct pass-through	up to 18500	same as input
1	1	direct pass-through	up to 18500	same as input

REGSEL: VCC Voltage selection (5V/3.3V)

REGSEL=0 VCC output set to 3.3V.
REGSEL=1 VCC output set to 5V.

VCEN: VCC regulator enable

VCEN=0 VCC is off.
VCEN=1 VCC is active.

LINSLP: LIN slope mode setup

To improve EMI performance the LIN switching slope can be reduced.
LINSLP=0 Normal LIN rise-time.
LINSLP=1 Rise time increased by 1/3.

LINIO: External input system selection

LV8907 has an embedded LIN physical layer which can also be used as a PWM input channel.
LINIO=0 LIN_PWMIN is in PWM input mode.
LINIO=1 The LIN transceiver is active and the PWM signal is taken from PWMIN.

MRCONF1

Address = 01h				Standby Mode: **Read/Write** Normal Mode: **Read Only**			
Bit 7	**6**	**5**	**4**	**3**	**2**	**1**	**Bit 0**
FLSEL[1,0]		ZPSEL[1,0]		PWMFL	PWMZP	PDTC	PWMON

FLSEL: 100% PWM input duty cycle motor operation

If 100% PWM input duty cycle was detected (no PWM frequency) and PWMFL is set, the motor is driven with the duty cycle programmed into FLSEL as shown in the following table.

FLSEL[1]	FLSEL[0]	Motor Duty Cycle[%]
0	0	25
0	1	50
1	0	75
1	1	100

ZPSEL: 0% PWM input duty cycle motor operation

If 0% PWM input duty cycle is detected (no PWM frequency) and PWMZP is set, the motor is driven with the duty cycle programmed into ZPSEL as shown in the following table.

ZPSEL[1]	ZPSEL[0]	Motor Duty Cycle[%]
0	0	25
0	1	50
1	0	75
1	1	100

PWMFL: Operation mode selection at PWM input duty cycle = 100%

If 100% PWM input duty cycle was detected the motor will be
PWMFL=0: turned off.
PWMFL=1: driven with the duty cycle defined by FLSEL.

PWMZP: Operation mode selection at PWM input duty cycle = 0%

If 0% PWM input duty cycle is detected the motor will be.
PWMZP=0: turned off.
PWMZP=1: driven with the duty cycle defined by ZPSEL.

PDTC: Fast Startup operation mode

During the first 200ms after EN high, while the PWM signal is still being measured, the motor can be either
PDTC=0: turned off.
PDTC=1: driven with the duty cycle defined by PDTSEL (MRCONF3[7,6])

PWMON: PWM input signal level

Decides whether the PWM input signal is active low, or active high.
PWMON=0: PWM input signal is active high.
PWMON=1: PWM input signal is active low.

MRCONF2

Address = 02h				Standby Mode: **Read/Write** Normal Mode: **Read Only**			
Bit 7	**6**	**5**	**4**	**3**	**2**	**1**	**Bit 0**
SSTEN	FGOF[1,0]		FDTI[4:0]				

SSTEN: Soft-start function enable

Soft-start (current ramp) allows slow startup of motors with higher inertia. The soft-start algorithm ramps the current limit from 0 to max current in 16 steps during soft-start time t_{SST} which is programmed in register MRCONF3.
SSTEN=0 Soft-start is OFF.
SSTEN=1 Soft-start is active.

Note that soft-start typically begins after duty cycle detection. If no duty cycle operation is selected (PDTC=1) Soft-start will begin after reset.

FGOF: FG signal output frequency selection

The FG signal is a representation of a successfully detected back-EMF transition which occurs three times during every electrical revolution. It is possible to divide that frequency as described in the following table.

FGOF[1]	FGOF[0]	FG output mode
0	0	One transition per back-EMF detection.
0	1	One pulse per electrical revolution.
1	0	One transition every two BEMF det.
1	1	One pulse every two elec. Revolutions.

FDTI: Dead time setting

During phase switching between supply and GND it is possible for both low- and high-side drivers to be temporarily on at the same time causing large current spikes. Register FDTI defines a dead time during which both drivers will be kept off during these transitions.

FDTI[4]	FDTI[3]	FDTI[2]	FDTI[1]	FDTI[0]	Dead time[us]
0	0	0	0	0	3.2
0	0	0	0	1	3.1
FDTI					3.2 - FDTI/10
1	1	1	1	0	0.2
1	1	1	1	1	0.1

MRCONF3

Address = 03h				Standby Mode: **Read/Write** Normal Mode: **Read Only**			
Bit 7	**6**	**5**	**4**	**3**	**2**	**1**	**Bit 0**
PDTSEL[1,0]		SSTT[5:0]					

PDTSEL: Fast Start-up motor operation.

If bit PDTC is set the motor is driven with the duty cycle programmed into PDTSEL as shown in the following table, as soon as EN is high. This feature is bridging the initial 200ms of operation until a valid PWM duty cycle can be decoded.

PDTSEL[1]	PDTSEL[0]	Motor Duty Cycle[%]
0	0	25
0	1	50
1	0	75
1	1	100

SSTT: Soft-start time setting

Soft-start allows startup of motors with higher inertia by ramping the current. The soft-start algorithm divides the current limit voltage 100mV (Typ.) into 16 sections and increases the value from 6.25mV to 100mV to switch over the current limit value. The soft start can be set from 0.1s < tSSTT < 6.71s as shown in the table below:

SSTT[5]	SSTT[4]	SSTT[3]	SSTT[2]	SSTT[1]	SSTT[0]	Soft-start time[s]
0	0	0	0	0	0	0.105
0	0	0	0	0	1	0.21
SSTT						0.105 · (1 + SSTT)
1	1	1	1	1	0	6.615
1	1	1	1	1	1	6.72

MRCONF4

Address = 04h							Standby Mode: **Read/Write** Normal Mode: **Read Only**	
Bit 7	**6**	**5**	**4**	**3**	**2**	**1**	**Bit 0**	
STOSC[7:0]								Startup commutation period [ms]
0	0	0	0	0	0	0	0	0.82
STOSC								0.82×(1+STOSC)
1	1	1	1	1	1	1	1	209.92

This register defines the rotation frequency f_{STOSC} at which the motor should be turned during open-loop startup. If a BEMF signal can be detected the IC will commutate to the next energization pattern by using the zero-crossing as its reference. If no BEMF can be detected the IC will commutate to the next energization pattern with the frequency programmed into STOSC. Open-loop startup continues for the time programmed into CPTM (MRCONF8[6:3]) If no BEMF is detected during that time a locked rotor error is indicated.

MRCONF5

Address = 05h							Standby Mode: **Read/Write** Normal Mode: **Read Only**
Bit 7	**6**	**5**	**4**	**3**	**2**	**1**	**Bit 0**
CLMASK[4:0]				OCMASK[4:0]			

CLMASK: Current limit mask time setting

In order to prevent noise and glitches from causing false current limiting, a mask time can be programmed.

CLMASK[3]	CLMASK [2]	CLMASK [1]	CLMASK [0]	Mask Time[us]
0	0	0	0	0.1
0	0	0	1	0.2
CLMASK				0.1+CLMASK/10
1	1	1	0	1.5
1	1	1	1	1.6

OCMASK: Over-current detection Mask time setting

The time to detect over-current can be programmed with OCMASK.

OCMASK[3]	OCMASK [2]	OCMASK [1]	OCMASK [0]	Mask Time[us]
0	0	0	0	0.2
0	0	0	1	0.4
OCMASK				0.2 · (1+OCMASK)
1	1	1	0	3.0
1	1	1	1	3.2

MRCONF6

Address = 06h — Standby Mode: **Read/Write**; Normal Mode: **Read Only**

Bit 7	6	5	4	3	2	1	Bit 0
SROFFT[3-0]				CRMASK[3-0]			

Internal use only.

MRCONF7

Address = 07h — Standby Mode: **Read/Write**; Normal Mode: **Read Only**

Bit 7	6	5	4	3	2	1	Bit 0
SYNCEN	PPDOSEL	FSCDT[1:0]		FSCDL[3:0]			

SYNCEN: Synchronous rectification enable

Defines synchronous rectification mode for the output stage. In synchronous rectification the high and low side switches are always switched in complementary mode = if one switch is on, the other one is off . In a-synchronous rectification both complementary switches may be off and the motor current is circling through the body diodes.
SYNCEN=0 Synchronous rectification is ON.
SYNCEN=1 Synchronous rectification is OFF.

PPDOSEL: DIAG output selection at PWM input abnormality

D6 of the main register MRCONF7 can be used to reflect abnormal detection result to DIAG pin at the time of PWM input abnormal detection (0% or 100% detection).
PPDOSEL=0 PWM abnormal input detection result is reflected to DIAG pin when

PPDOSEL=1 and it is not reflected to DIAG pin when.

FSCDT: FET Short protection detection time setting

By monitoring FET Vds, the time from FET's ON signal output until detecting Shorted status can be set with D5 and D4 of MRCONF7. Please refer to the table below for settable time:

FSCDT[1]	FSCDT [0]	Detection time[us]
0	0	3.2
0	1	6.4
1	0	9.6
1	1	12.8

FSCDL: FET Short protection detection voltage setting

Vds voltage to detect FET Short status can be set with D3~D0 of MRCONF7. Please refer to the table below for available voltages:

FSCDL [3]	FSCDL[2]	FSCDL [1]	FSCDL [0]	Vth[V]
0	0	0	0	0.1
0	0	0	1	0.2
FSCDL				0.1+FSCDL/10
1	1	1	0	1.5
1	1	1	1	1.6

MRCONF8

Address = 08h — Standby Mode: **Read/Write**; Normal Mode: **Read Only**

Bit 7	6	5	4	3	2	1	Bit 0
SSCG	CPTM[3-0]				THTH[1,0]		TSTS

SSCG: Charge Pump Spread Spectrum

The Charge pump may have radiation noise issues due to switching at 52.1kHz(typ.). By activating SSCG it is possible to disperse frequency components of the charge pump switching frequency. The frequency will vary 20%.

SSCG=0: Spread spectrum OFF
SSCG=1: Spread spectrum ON

CPTM: Open Loop Startup Timeout

A locked rotor protection circuit is embedded in order to protect IC and Motor during locked rotor conditions. A locked rotor is detected by counting the time the IC is in Start-up mode (without back-EMF detection) If no back-EMF is detected for the time programmed into CPTM register the motor is turned off and a locked rotor is flagged.
In Auto recovery mode the motor will remain off for eight times the Open Loop Startup Timeout before another startup is attempted.

CPTM [3]	CPTM [2]	CPTM [1]	CPTM [0]	Detection/Restart time[s]
0	0	0	0	0.42 / 3.36
0	0	0	1	0.84 / 6.72
CPTM				0.42 · (1+CPTM) / 3.36 · (1+CPTM)
1	1	1	0	6.3 / 50.4
1	1	1	1	6.72 / 53.76

THTH: Threshold for External Thermometer Input

LV8907 has an embedded comparator to monitor the external power FET's temperature using an external thermistor. If the voltage at TH drops below the threshold level (shown in the table), the external over-temperature protection is activated, the output gate driver stage is turned off and the THPO error flag is set.

THTH[1]	THTH [0]	V_{TH}[V]
0	0	0.35
0	1	0.30
1	0	0.25
1	1	0.20

TSTS: Junction temperature warning and shutoff levels

The LV8907 monitors its own junction temperature to protect against over-temperature damage. Two different warning and shut-off levels can be selected:

TSTS=0: Over-temperature warning occurs at 125℃(typ.), shutdown at 150℃(typ.).
TSTS=1: Over-temperature warning occurs at 150℃(typ.), shutdown at 175℃(typ.).

MRCONF9

Address = 09h				Standby Mode: **Read/Write** Normal Mode: **Read Only**			
Bit 7	**6**	**5**	**4**	**3**	**2**	**1**	**Bit 0**
WDTEN	WDTP	WDT[5:0]					

WDTEN: Watchdog enable

This bit can enable or disable the watchdog. For increased system robustness it is possible to permanently lock access to this bit. See OTP section for more details.
WDTEN=1 Watchdog is active.
WDTEN=0 Watchdog is disabled.

WDTP: Operation against watchdog timeout

Operation mode against watchdog time can be selected.
WDTP=0 Motor off.
WDTP=1 Motor is driven with the PWM duty cycle as defined by WDTSEL (MRCONF11[5,4]).

WDT: Watchdog timer setting

The end time of the watchdog timer is defined by register WDT.

WDT [5]	WDT [4]	WDT [3]	WDT [2]	WDT [1]	WDT [0]	Detection Time[ms]
0	0	0	0	0	0	1.64
0	0	0	0	0	1	3.28
WDT						1.64 · (1+WDT)
1	1	1	1	1	0	103.32
1	1	1	1	1	1	104.96

MRCONF10

Address = 0Ah				Standby Mode: **Read/Write** Normal Mode: **Read Only**			
Bit 7	**6**	**5**	**4**	**3**	**2**	**1**	**Bit 0**
VCLVPEN	CPEN	THWEN	THPEN	FSPEN	OVPEN	OCPEN	DIAGSEL

xEN: Error and warning mask

The higher seven bit in this register allows enabling and disabling of various errors and warnings. A one in the register masks the error, a zero activates the protection. The following errors and warnings can be masked:

- VCLVPEN = 0: VCC Under-voltage protection enabled
- CPEN = 0: Motor block protection enabled
- THWEN = 0: Thermal warning output enabled
- THPEN = 0: Thermal protection enabled
- FSPEN = 0: FET short protection enabled
- OVPEN = 0: Over-voltage protection enabled
- OCPEN = 0: Over-current protection enabled

DIAGSEL: Diagnosis output polarity selection

This bit selects the polarity of the DIAG signal
DIAGSEL=0 The DIAG pin is active low.
DIAGSEL=1 The DIAG pin is active high and draws pull-down current when off.

MRCONF11

Address = 0Bh				Standby Mode: **Read/Write** Normal Mode: **Read Only**			
Bit 7	**6**	**5**	**4**	**3**	**2**	**1**	**Bit 0**
DWNSET[1,0]		WDTSEL[1,0]		CPLT	FSPLT	OCPLT	DLTO

DWNSET: Mode setting at the time of speed feedback deceleration

During speed control mode, motor deceleration can lead to energy recuperation and temporary voltage spikes. DWNSET allows for various degrees of energy recuperation:

- Normal Mode
  Results in a tightest control and maximum energy recuperation. The application circuit has to be able to absorb the energy generated.
- Sync OFF Mode
  The motor is essentially not driven until it has reached the target speed. This does not feed any energy back into the supply, but may take a long time if motor inertia is high and losses are low.
- Slow Response Mode
  This mode is essentially imposing a slow deceleration ramp on the control speed. The energy recuperated is similar to Normal Mode but spread over a longer period of time reducing the voltage overshoot.

DWNSET[1]	DWNSET [0]	Mode
0	0	Normal Mode
0	1	Sync OFF Mode
1	0	Slow Response Mode (PROT/32)
1	1	Normal Mode

WDTSEL: Operation mode selection after a Watchdog timeout

Bit WDTP (MRCONF9[6]) defines if a Watchdog timeout causes Halt mode (0% drive) or Drive mode.

When Drive mode is selected the motor duty cycle is defined by WDTSEL as shown in the table below.

WDTSEL[1]	WDTSEL[0]	Duty[%]
0	0	25
0	1	50
1	0	75
1	1	100

xPLT: Protection Latch selection

The faults of the motor block, FET Short and over-current can cause intolerable large-current. To prevent repeated current flow during re-try attempts, it is possible to latch these errors. The LV8907 will remain disabled until the latch is cleared by the register MRRST.

CPLT=0 Auto recover after a motor block.
CPLT=1 Latch the IC off after a motor block.

FSPLT=0 Auto recover after a FET short.
FSPLT=1 Latch the IC off after a FET short.

OCPLT=0 Auto recover after over-current.
OCPLT=1 Latch the IC off after over-current.

DLTO: Diagnostic output mode selection

Selects which errors/warnings will actually trigger a DIAG transition.

DLTO=0: Trigger DIAG for any non-masked error or warning.
DLTO=1: Trigger DIAG only for latched errors as defined by xPLT above.

MRCONF12

Address = 0Ch				Standby Mode: **Read/Write** Normal Mode: **Read/Write***			
Bit 7	**6**	**5**	**4**	**3**	**2**	**1**	**Bit 0**
STEPSEL[2-0]			SLMD	LASET[3-0]			

*Note: This register is writeable in Normal mode.

STEPSEL: Ramp imposed on speed control changes

In speed control mode, large steps in motor target speed can cause excessive current spikes, noise and wear on the mechanical components. The LV8907 allows to impose a limit on the difference between target speed and actual speed such that every electrical revolution only a fraction of the previous rotational (PROT) speed is allowed to change. This limit is defined by STEPSEL in register MRCONF12[7-5].

Note: During closed loop speed control optimization and/or evaluation, it might be useful to turn off this ramp imposing (STEPSEL[2:0]= 0b000).

Figure 15 shows the RPM ramping response to an input step for six different ramp settings for instance.

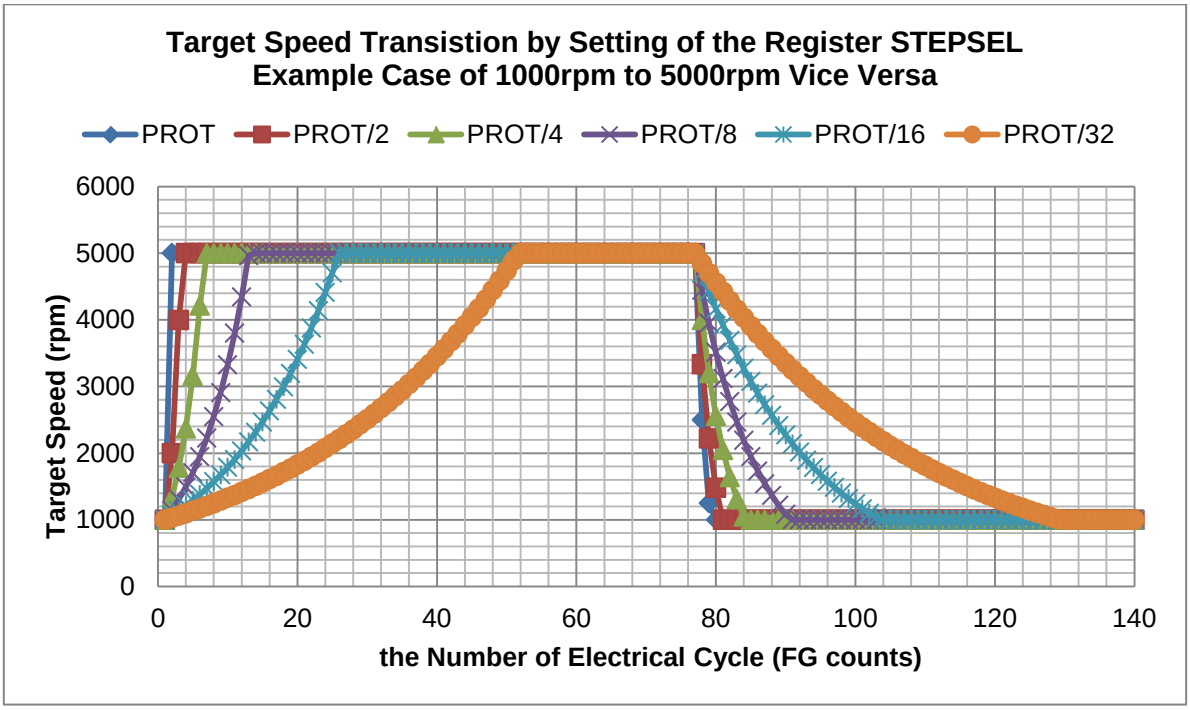


Figure 15: Speed Control Input Ramp of Different STEPSEL Settings

STEPSEL[2]	STEPSEL[1]	STEPSEL[0]	Step Mode
0	0	0	PROT (Current electrical speed at FG)
0	0	1	PROT/2
0	1	0	PROT/4
0	1	1	PROT/8
1	0	0	PROT/16
1	0	1	PROT/32
1	1	0	PROT
1	1	1	PROT

SLMD: Sinusoidal vs. trapezoidal drive mode selection

This bit selects whether the motor phases are driven with a trapezoidal or pseudo-sinusoidal signal.

SLMD=0 Trapezoidal drive with 120 degrees energization.
SLMD=1 Sinusoidal drive with 150 degrees energization.

LASET: Lead angle setting

In trapezoidal drive mode it is possible to advance the commutation point towards zero-crossing of the back-EMF signal. This helps to achieve back-EMF field-weakening for higher rotational speeds and to compensate for delays in high speed operation.

LASET [3]	LASET [2]	LASET [1]	LASET [0]	Lead Angle[deg]
0	0	0	0	0
0	0	0	1	1.875
LASET				LASET · 1.875
1	1	1	0	26.25
1	1	1	1	28.125

Speed Control Register Overview

ADDR[6:0]	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
10h	MRSPCT0	-	PX[2:0]			-	PG[2:0]		
11h	MRSPCT1	-	IX[2:0]			-	IG[2:0]		
12h	MRSPCT2	-	FGT0[6:0]						
13h	MRSPCT3	-	FGT1[6:0]						
14h	MRSPCT4	-	FGT2[6:0]						
15h	MRSPCT5	-	FGT3[6:0]						
16h	MRSPCT6	-	FGT4[6:0]						
17h	MRSPCT7	-	FGT5[6:0]						
18h	MRSPCT8	-	FGT6[6:0]						
19h	MRSPCT9	-	FGT7[6:0]						
1Ah	MRSPCT10	-	FGT8[6:0]						

Speed control loop gain setting

Closed loop motor rotation speed controller (PI) is provided. The block diagram is shown in Figure 16. Where,

TAG: target speed (period)
PROT: previous speed feedback (period)
Int: previous sum
K: scaling factor

$$K = \frac{VS}{128 \times 512}$$

Proportional Gain can be set with PX and PG of MRSPCT0 where the total gain is the product of both components PG and PX. Integral Gain can be set with IX, and IG of MRSPCT1 respectively. These P and I parameters can be changed while a motor is running (i.e. EN = HIGH). MRSPCT0 must be written, followed by writing MRSPCT1 through SPI. To update the P and I parameters of the control logic block simultaneously, MRSPCT0 code is suspended until MRSPCT1 is written. The calculation operates every FG cycle. The period is measured by 104kHz clock.

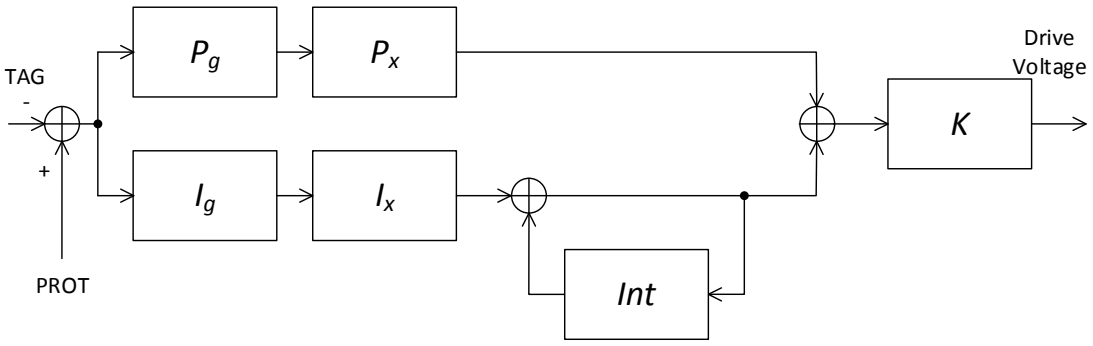


Figure 16: PI Speed Controller Block Diagram

PX, IX [2]	PX, IX [1]	PX, IX [0]	Gain
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	0

PG, IG [2]	PG, IG [1]	PG, IG [0]	Gain
0	0	0	1
0	0	1	7/8
0	1	0	6/8
0	1	1	5/8
1	0	0	4/8
1	0	1	3/8
1	1	0	2/8
1	1	1	1/8

The proportional gain is a product of PX and PG, and the integrator gain is a product of IX and IG.

	Px Ix		Pg Ig	
Value	Factor	Setting	Factor	Setting
0.125	x1	0	x1/8	7
0.250	x1	0	x2/8	6
0.250	x2	1	x1/8	7
0.375	x1	0	x3/8	5
0.500	x1	0	x4/8	4
0.500	x2	1	x2/8	6
0.500	x4	2	x1/8	7
0.625	x1	0	x5/8	3
0.750	x1	0	x6/8	2
0.750	x2	1	x3/8	5
0.875	x1	0	x7/8	1
1.000	x1	0	x1	0
1.000	x2	1	x4/8	4
1.000	x4	2	x2/8	6
1.000	x8	3	x1/8	7
1.250	x2	1	x5/8	3
1.500	x2	1	x6/8	2
1.500	x4	2	x3/8	5
1.750	x2	1	x7/8	1
2.000	x16	4	x1/8	7
2.000	x2	1	x1	0
2.000	x4	2	x4/8	4
2.000	x8	3	x2/8	6
2.500	x4	2	x5/8	3
3.000	x4	2	x6/8	2
3.000	x8	3	x3/8	5
3.500	x4	2	x7/8	1
4.000	x16	4	x2/8	6
4.000	x32	5	x1/8	7
4.000	x4	2	x1	0
4.000	x8	3	x4/8	4
5.000	x8	3	x5/8	3
6.000	x16	4	x3/8	5
6.000	x8	3	x6/8	2
7.000	x8	3	x7/8	1
8.000	x16	4	x4/8	4
8.000	x32	5	x2/8	6
8.000	x64	6	x1/8	7
8.000	x8	3	x1	0
10.000	x16	4	x5/8	3
12.000	x16	4	x6/8	2
12.000	x32	5	x3/8	5
14.000	x16	4	x7/8	1
16.000	x16	4	x1	0
16.000	x32	5	x4/8	4
16.000	x64	6	x2/8	6
20.000	x32	5	x5/8	3
24.000	x32	5	x6/8	2
24.000	x64	6	x3/8	5
28.000	x32	5	x7/8	1
32.000	x32	5	x1	0
32.000	x64	6	x4/8	4
40.000	x64	6	x5/8	3
48.000	x64	6	x6/8	2
56.000	x64	6	x7/8	1
64.000	x64	6	x1	0

Thus, there are some duplication with responding to the combination of X and G.

Target speed setting

There are two ways of setting a target speed with speed control active (SCEN=0):

1. By using a companion microprocessor to write the speed value directly into the Speed Control Register via SPI.
2. By applying a low frequency PWM input which selects a target speed from the Speed Control Register.

SPI Speed Control

For SPI speed control the companion microprocessor should apply a fixed duty cycle PWM signal to the LV8907 PWMIN pin. An input duty cycle of 12.5% would then select speed register MRSPCT3 as shown in the table below. By writing RPM values to register MRSPCT3 via SPI, the speed can be controlled directly.

PWM Speed Control

PWM input frequency must be in Low frequency mode (PWMF=0). In this mode the PWM input duty cycle is measured and used to select a target speed from the Speed Control Registers MRSPCT2..10. Note that 0% and 100% input duty cycle will be flagged as a "PWM Input Fault"

Input Duty Cycle(%) (center value of the range)	Register
0	0% Duty Operation*
(3.125)	MRSPCT2
12.5	MRSPCT3
25	MRSPCT4
37.5	MRSPCT5
50	MRSPCT6
62.5	MRSPCT7
75	MRSPCT8
87.5	MRSPCT9
(96.875)	MRSPCT10
100	100% Duty Operation*

*See page 18: Abnormal Duty Cycle Operation (100% or 0%)

There is a hysteresis of 6.25% duty cycle around each typical value resulting in the duty cycle thresholds depicted in Figure 9 on page 17.
The motor speed is defined as ERPM (Electrical Revolutions Per Minute). To calculate the physical rotational speed RPM of the motor divide ERPM by the number of pole pairs of the motor. Each of the nine registers (FGT0[6:0] to FGT8[6:0]) selected by the input PWM above has 7 bits to program ERPM in a piecewise exponential function.

Preset Target Speed RPM in Electrical Cycle	Register FGTx[6:0] Speed Index Code
400	4 (0x04)
… one step 200 …	… one step 1 …
13,200	68 (0x44)
… one step 400 …	… one step 1 …
17,600	79 (0x4F)
… one step 800 …	… one step 1 …
24,000	87 (0x57)
… one step 2,000 …	… one step 1 …
40,000	95 (0x5F)

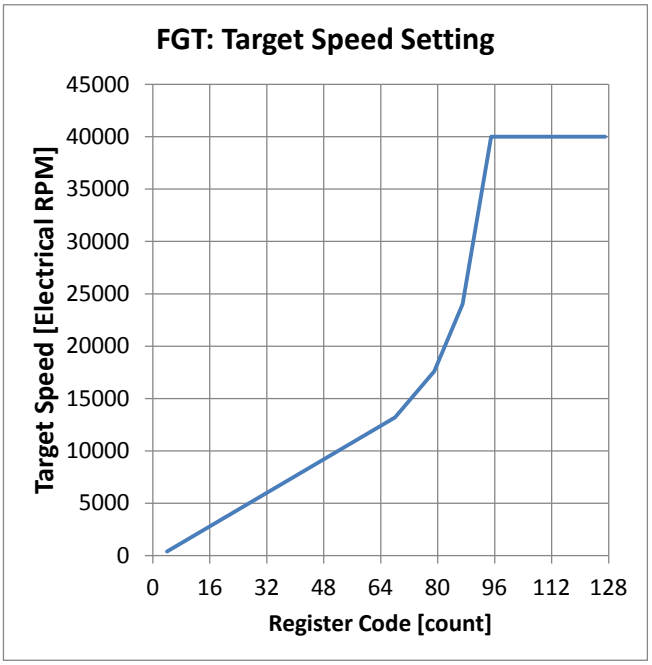


Figure 17: Speed Register Contents vs. Electrical RPM

MRACS

Address = 20h				Standby Mode: **Read Only** Normal Mode: **Read Only**			
Bit 7	**6**	**5**	**4**	**3**	**2**	**1**	**Bit 0**
0	0	0	0	0	0	OSAENB	MSAENB

This read-only register controls SPI access to the Master Registers and OTP Registers. Its contents are transferred from OTP Register ORACS at device startup.

OSANEB: OTP Register access enable

Controls write access to the OTP registers.
OSAENB=0: Write access permitted.
OSAENB=1: Write access denied.

MSANEB: Master Register access enable

Controls write access to the Master registers.
OSAENB=0: Write access permitted.
OSAENB=1: Write access denied.

MRACK

Address = 30h				Standby Mode: **Read Only** Normal Mode: **Read Only**			
Bit 7	**6**	**5**	**4**	**3**	**2**	**1**	**Bit 0**
0	1	0	1	0	1	0	1

This read only register is used to check IC and SPI interface. 55h is read from this register in standby and normal mode, FFh during sleep mode.

MRODL

Address = 31h							Standby Mode: **Read/Write** Normal Mode: **Read Only**	
Bit 7	**6**	**5**	**4**	**3**	**2**	**1**	**Bit 0**	
MRODL[7:0]								
0	0	0	0	0	0	0	0	OTP download

A write access of 00h to this register initiates a copy operation of OTP data to the Master Register. This register is blocked if OBSY is high.

MRRST

Address = 32h							Standby Mode: **Read/Write** Normal Mode: **Read/Write**	
Bit 7	**6**	**5**	**4**	**3**	**2**	**1**	**Bit 0**	
MRRST[7:0]								
0	0	0	0	0	0	0	0	Reset Watchdog Timer
1	1	1	1	1	1	1	1	Reset Error Latch

This register is used to reset the watch dog timer or the error latch.

- Writing 00h to this register will reset the watch dog timer.
- Writing FFh will reset the protection latch.

MRORB

Address = 33h				Standby Mode: **read/write** Normal Mode: **read Only**			
Bit 7	**6**	**5**	**4**	**3**	**2**	**1**	**Bit 0**
0	0	0	0	0	0	ORBEN	ORBLV

This register modifies the OTP readout threshold. After programming the OTP registers should be verified by reading them with the readout thresholds set low and high to detect false zeros and ones. See “OTP Programming” on page 38.

ORBEN: Selects the margin read mode.

ORBEN = 0: Normal mode.
ORBEN = 1: Margin read mode.

ORBLV: Selects the OTP readout threshold.

ORBLV = 0: Low level margin check
ORBLV = 1: High level margin check

MRDIAG0

Address = 34h				Standby Mode: **Read Only** Normal Mode: **Read Only**			
Bit 7	**6**	**5**	**4**	**3**	**2**	**1**	**Bit 0**
CPO	THPO	FSPO	VGLLVPO	CHPLVPO	VSOVPO	VSLVPO	OCPO

Registers MRDIAG0 and MRDIAG1 indicate the system errors and/or warnings.

CPO: Locked rotor protection output

No back EMF was detected during the entire open-loop startup time as programmed in CPTM on page 29. Either the rotor is blocked, or startup parameters are not correct. The drivers are disabled.

THPO: Thermal protection output

The external temperature sensor input TH threshold was triggered. If the voltage at pin TH is lower than programmed in THTH on page 29 the drivers will shut down. Tie TH to V3RO to disable this function.

FSPO: FET Short protection output

The drain-source voltage threshold across one of the external power FETs has been exceeded during operation. The threshold voltage is programmed in register FSCDL. Errors are suppressed for a blanking time as programmed in register FSCDT.
For the high-side FETs this voltage is measured between pin VS and the corresponding phase connection UOUT, VOUT, WOUT. For the low-side FETs it is measured between the phase connection and the pins SUL, SVL and SWL. Make sure to minimize potential voltage drops in the sense paths.

VGLLVPO: VGL Low voltage protection output

The voltage at VGL has dropped below 5.5V(max). The drivers are disabled to protect against low gate enhancement.

CHPLVPO: CHP Low voltage protection output

The voltage between VS and VCP has dropped below 5.5V(max). The drivers are disabled to protect against low gate enhancement.

VSOVPO: VS Over-voltage protection output

The voltage at VS has exceeded 20V(min). The driver stage and the charge pump are disabled to protect against over-voltage at the charge-pump.

VSLVPO: VS Low voltage protection output

The voltage at VS has fallen below 5.1V(max). The driver stage is disabled to protect against internal threshold issues.

VOCPO: Over-current protection output

The voltage between current sense pins RFSENS and RF has exceeded 200mV for longer than the over-current limit mask time programmed in OCMASK in register MRCONF5 on page 27. The driver stage is disabled to protect against damage.

MRDIAG1

Address = 35h				Standby Mode: **Read Only** Normal Mode: **Read Only**			
Bit 7	**6**	**5**	**4**	**3**	**2**	**1**	**Bit 0**
PWMPO	VCLVPO	-	SPCO	STUPO	WDTPO	THSPO	THWPO

Registers MRDIAG0 and MRDIAG1 indicate the system errors and/or warnings.

PWMPO: PWM input abnormal protection output

The PWM input does not oscillate with the appropriate frequency or is steady high (100%) or low (0%). Depending on the settings in register MRCONF1 on page 25 the driver stage will turn off, or operate at a predefined duty cycle (emergency mode).

VCLVPO: VCC reduced voltage protection output

VCC under-voltage error. Depending on the setting of MRCONF0 on page MRCONF0 VCC is either 5V(typ.) or 3.3V(typ.). Under-voltage is flagged if VCC falls below 4.2V(max.) or 2.7V(max.) respectively.

SPCO: Speed error out of the range

SPCO = 0, when the absolute value of the speed error is equal to or less than target $\times \frac{1}{16}$

SPCO = 1, when the absolute value of the speed error is greater than target $\times \frac{1}{16}$

STUPO: Start-up status output

This flag indicates open-loop startup operation. No back EMF has been detected, yet.

WDTPO: Watch dog timer protection output

The watchdog has timed out. This flag will be high if the watchdog was not re-set during the time defined by MRCONF9 on page 29. If the watchdog is enabled the driver stage will either be off or run in emergency mode with the settings defined by MRCONF11 on page 30.

Flag WDTPO is high even if the watchdog is disabled.

THSPO: Junction temperature thermal protection output

The IC temperature is too high and the drivers are shut off. The over-temperature shutoff level is defined by MRCONF8 on page 28 to be either 150ºC(min.) or 175ºC(min.).

THWPO: Junction temperature thermal warning output

The IC temperature has exceeded the warning level. The over-temperature warning level is defined by MRCONF8 on page 28 to be either 125ºC(min.) or 150ºC(min.).

OTP Registers

The OTP Registers contain the default values of the system registers. These registers are always readable via SPI in either Standby or Normal modes. During device startup these default values are copied from the OTP bank (SPI addresses 40h to 60h) to the Master register bank (SPI addresses 00h to 20h). The OTP registers should only be programmed once during IC initialization, during normal operation only the Master Registers are accessed and modified. It is possible to block programming of the OTP section by setting the OSANB bit in the ORACS Register of the OTP.

For detailed information on the content of the OTP see the corresponding Master Register descriptions in the previous section. Master registers from 30h to 35h shown below are autonomous and have no equivalent position in the OTP as they report various internal data and status information.

ADDR[6:0]	Bank	OTP Register	Function	Master Register	ADDR[6:0]
40h	0d[0]	ORCONF0		MRCONF0	00h
41h	0d[1]	ORCONF1		MRCONF1	01h
42h	0d[2]	ORCONF2		MRCONF2	02h
43h	0d[3]	ORCONF3		MRCONF3	03h
44h	0d[4]	ORCONF4		MRCONF4	04h
45h	1d[0]	ORCONF5		MRCONF5	05h
47h	1d[2]	ORCONF7		MRCONF7	07h
48h	1d[3]	ORCONF8		MRCONF8	08h
49h	1d[4]	ORCONF9		MRCONF9	09h
4Ah	2d[0]	ORCONF10		MRCONF10	0Ah
4Bh	2d[1]	ORCONF11		MRCONF11	0Bh
4Ch	2d[2]	ORCONF12	…corresponds to…	MRCONF12	0Ch
50h	2d[3]	ORSPCT0		MRSPCT0	10h
51h	2d[4]	ORSPCT1		MRSPCT1	11h
52h	3d[0]	ORSPCT2		MRSPCT2	12h
53h	3d[1]	ORSPCT3		MRSPCT3	13h
54h	3d[2]	ORSPCT4		MRSPCT4	14h
55h	3d[3]	ORSPCT5		MRSPCT5	15h
56h	3d[4]	ORSPCT6		MRSPCT6	16h
57h	4d[0]	ORSPCT7		MRSPCT7	17h
58h	4d[1]	ORSPCT8		MRSPCT8	18h
59h	4d[2]	ORSPCT9		MRSPCT9	19h
5Ah	4d[3]	ORSPCT10		MRSPCT10	1Ah
60h	4d[4]	ORACS	WRITE protection	MRACS	20h
_	_	_	SPI Status Register	MRACK	30h
_	_	_	Initiates a bank write	MRODL	31h
_	_	_	Watchdog Reset	MRRST	32h
_	_	_	Margin read checks	MRORB	33h
_	_	_	Diagnostic Flags	MRDIAG0	34h
_	_	_	Diagnostic Flags	MRDIAG1	35h

OTP data download

The OTP register data is typically transferred into the main registers at device startup (From sleep to standby transition). This operation takes up to 110us. A high OBSY flag in the first returned byte during a SPI transaction indicates this.

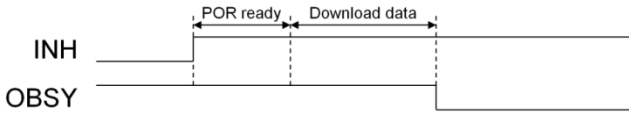


Figure 18: OTP data download timing at startup

An OTP download can also actively be initiated by writing 00h to register MRODL. This command requires monitoring the OBSY flag. Don't perform specific register access (MRCONF, MRSPCT, ORCONF, ORSPCT, ORACS) until the OBSY flag is cleared.

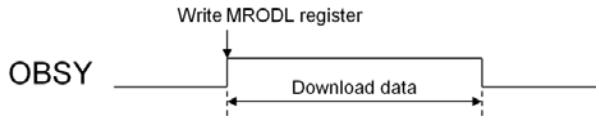


Figure 19: OTP data download timing after an MRODL command

OTP Programming Overall

Figure 20 shows overall of the OTP memory write and verify flow. It consists of preparation, write and three times of data integrity verification.

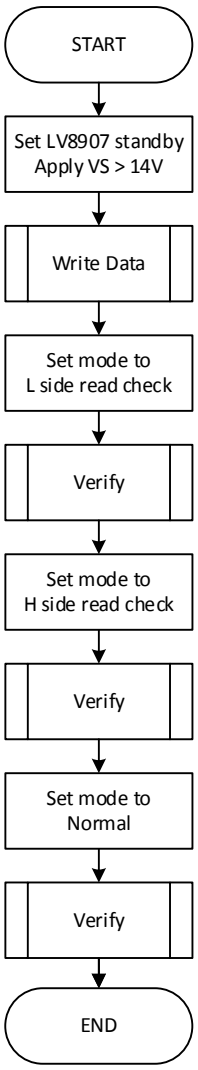


Figure 20 OTP Memory Write and Verify Flow

OTP Programming

The OTP registers can be programmed in Standby mode only while the write lock bit OSAENB is set 0. And, the supply voltage at pin VS must be more than 14V. The actual write operation to the OTP memory will be done, when the state change from 0 to 1 is commanded. Once the bit state is changed to 1, it cannot be change back to 0. The number of writing is limited to one per bit.

The OTP memory consists of five memory banks. The bank contains five register bytes. The bank is filled by five SPI write transactions. When the last address register in each bank is received, the busy-flag OBSY will be set and those five bytes will be programmed permanently into the corresponding OTP bank. The OBSY flag will be reset at the end of the write cycle. OBSY is in GSDAT register. To get GSDAT, SPI accesses to the register MRACK is recommended. MRACK doesn't interfere with the programming operation.

MRCONF, MRSPCT, ORCONF, ORSPCT, ORACS registers cannot be accessed during an OTP write cycle.

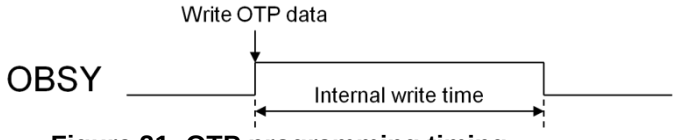


Figure 21: OTP programming timing

The programming takes 25ms maximum. To simplify operation, a waiting for 25ms plus margin can be applicable instead of a polling of the flag OBSY. (Figure 22)

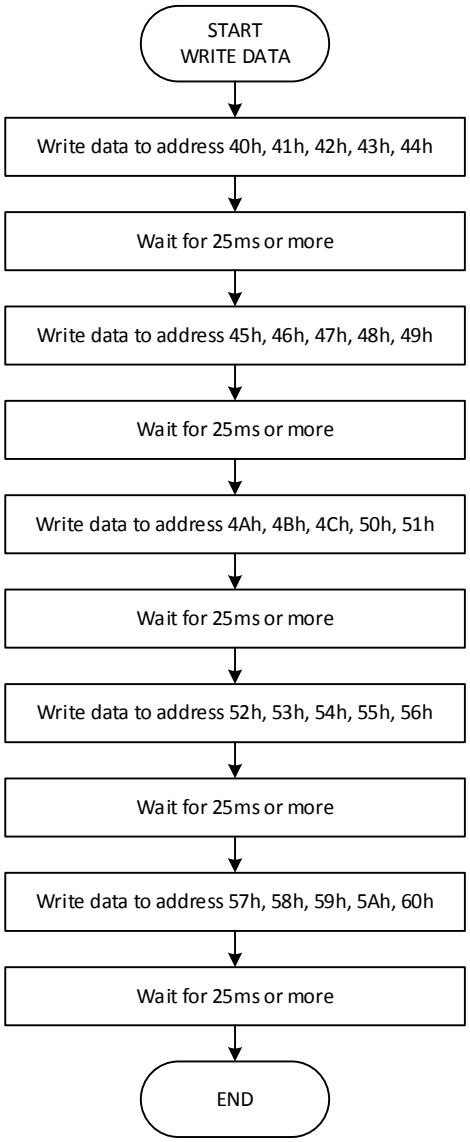


Figure 22 OTP Memory Write Operation

OTP data integrity verification

In order to verify that the OTP programming operation was successful. It is strongly recommended to do an OTP margin check: To do this, the OTP registers are downloaded into the main register bank with minimum and maximum readout thresholds. This OTP download is forced by writing 00h to register MRODL. The readout threshold is set in register MRORB.

OTP Margin read check sequence after programmed:

1. Set OTP readout threshold "low" by setting ORBEN=1 and ORBLV=0 in register MRORB
2. Execute OTP download command by writing 00h to MRODL.
3. Verify that the main register contents are consistent with the programmed OTP data.
4. Set OTP readout threshold "high" by setting ORBEN=1 and ORBLV=1 in register MRORB
5. Execute OTP download command by writing 00h to MRODL.
6. Verify that the main register contents are consistent with the programmed OTP data.
7. Return OTP threshold to normal by setting ORBEN=0 and ORBLV=0.
8. Execute OTP download command.
9. Verify that the main register contents are consistent with the programmed OTP data.

Locking OTP register contents

MSAENB bit and OSAENB bit of ORACS register are used in order to prevent write-access of main- and OTP registers respectively.

CAUTION: Inadvertent writing of these bits will permanently lock the corresponding register blocks from any further write access. Should only be set at end of development cycles.

ORACS

Address = 60h				Standby Mode: **Read/Write** Normal Mode: **Read Only**			
Bit 7	**6**	**5**	**4**	**3**	**2**	**1**	**Bit 0**
0	0	0	0	0	0	OSAENB	MSAENB

This register is used in order to permanently prevent write access to the OTP and/or main registers. This register data is transferred into MRACS register.

OSAENB D[1]: Controls write access to the OTP registers.

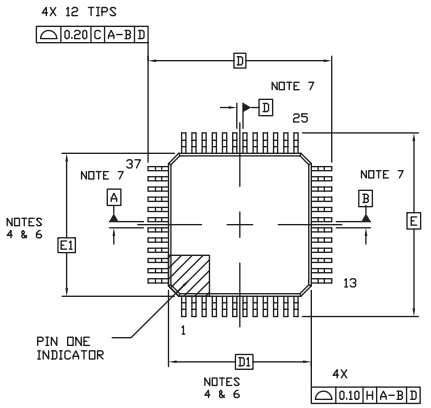
OSAENB=0: Write access permitted.
OSAENB=1: Write access denied.

MSAENBD[0]: This bit is used in order to prevent write access to the main registers.

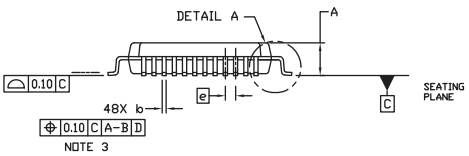
MSAENB=0: Write access permitted.
MSAENB=1: Write access denied.

PACKAGE DIMENSIONS

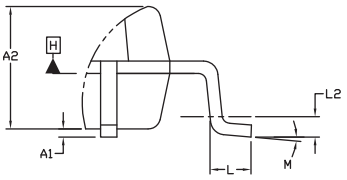
SPQFP48 7x7 / SQFP48K
CASE 131AN
ISSUE A



TOP VIEW



SIDE VIEW

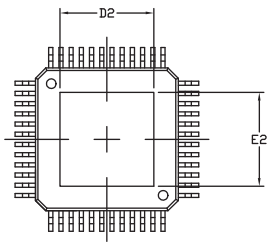


DETAIL A

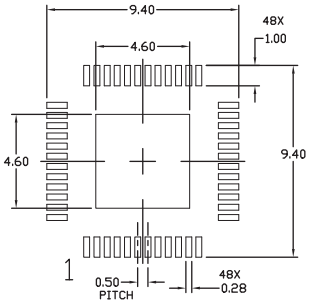
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL BE 0.08 MAX. AT MMC. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.25 PER SIDE. DIMENSIONS D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE INCLUDING MOLD MISMATCH.
5. THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE SIZE BY AS MUCH AS 0.15.
6. DATUMS A-B AND D ARE DETERMINED AT DATUM PLANE H.
7. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
8. DIMENSIONS D AND E TO BE DETERMINED AT DATUM PLANE C.

	MILLIMETERS	
DIM	MIN.	MAX.
A	---	1.70
A1	0.00	0.15
A2	1.50 REF	
b	0.15	0.26
D	9.00 BSC	
D1	7.00 BSC	
D2	4.60 REF	
E	9.00 BSC	
E1	7.00 BSC	
E2	4.60 REF	
e	0.50 BSC	
L	0.30	0.70
L2	0.25 BSC	
M	0°	10°



BOTTOM VIEW



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