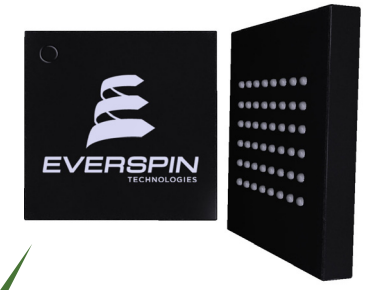
MR256A08B

32K x 8 MRAM

FEATURES

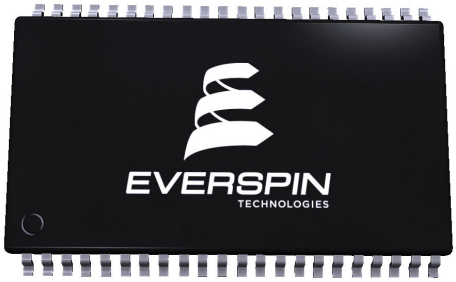
- 3.3 Volt power supply
- Fast 35 ns read/write cycle
- SRAM compatible timing
- Native non-volatility
- Unlimited read & write endurance
- Data always non-volatile for >20-years at temperature
- Commercial and industrial temperatures
- **RoHS-Compliant** TSOP2, BGA and SOIC packages



RoHS

BENEFITS

- One memory replaces FLASH, SRAM, EEPROM and BBSRAM in system for simpler, more efficient design
- Improves reliability by replacing battery-backed SRAM



INTRODUCTION

The **MR256A08B** is a 262,144-bit magnetoresistive random access memory (MRAM) device organized as 32,768 words of 8 bits. The MR256A08B offers SRAM compatible 35ns read/write timing with unlimited endurance. Data is always non-volatile for greater than 20-years. Data is automatically protected on power loss by low-voltage inhibit circuitry to prevent writes with voltage out of specification. The MR256A08B is the ideal memory solution for applications that must permanently store and retrieve critical data and programs quickly.

The **MR256A08B** is available in a small footprint 400-mil, 44-lead plastic small-outline TSOP type-2 package, an 8 mm x 8 mm, 48-pin ball grid array (BGA) package or a 32-lead SOIC package. All package footprints are compatible with similar low-power SRAM products and other non-volatile RAM products.

The **MR256A08B** provides highly reliable data storage over a wide range of temperatures. The product is offered with commercial temperature (0 to +70 °C) and industrial temperature (-40 to +85 °C) range options.

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1. DEVICE PIN ASSIGNMENT

Figure 1.1 Block Diagram

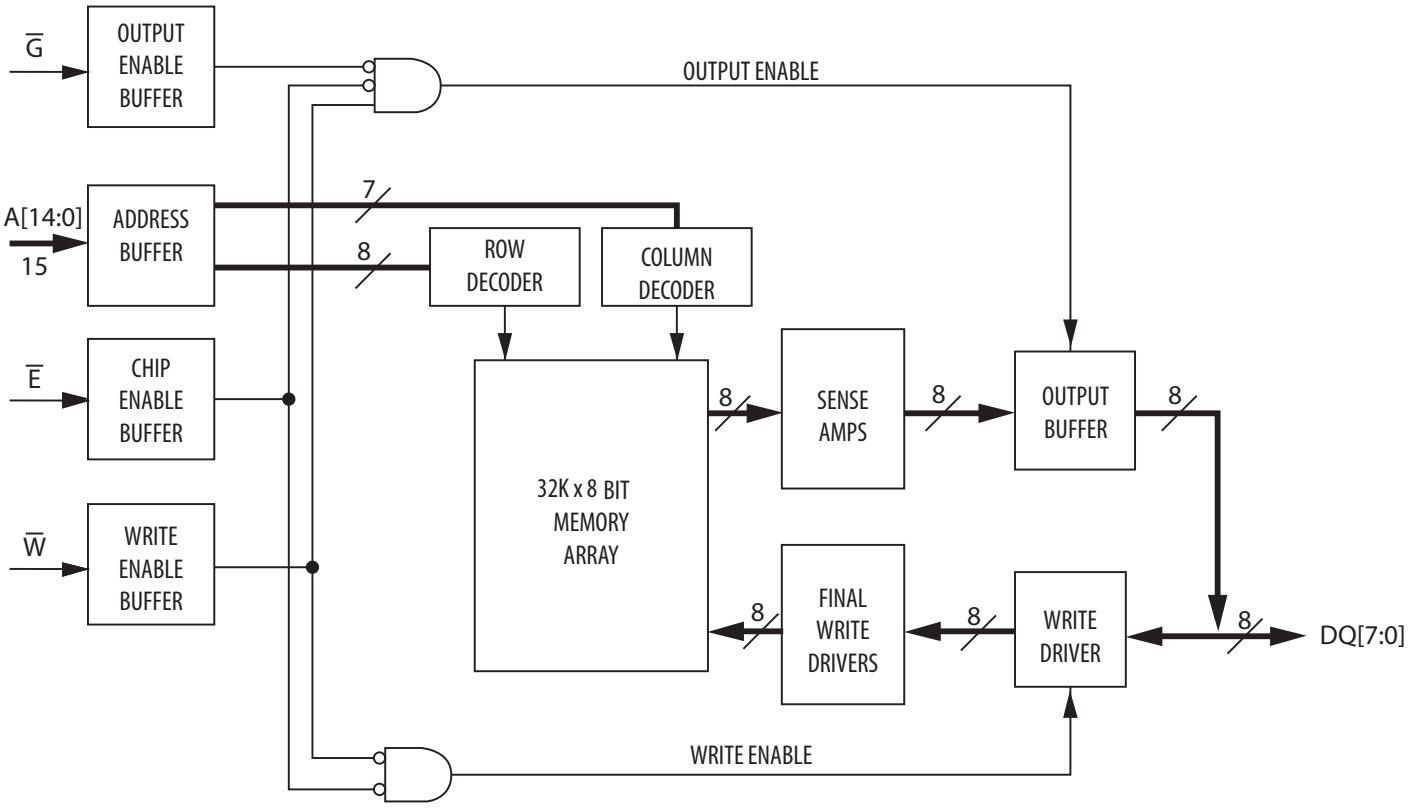
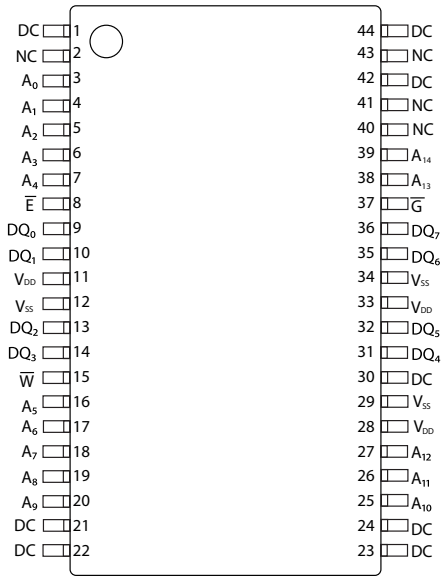


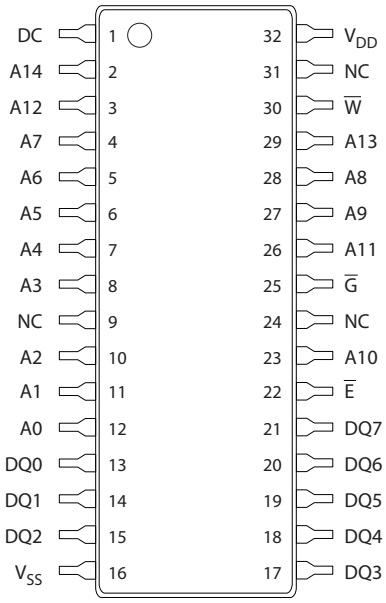
Table 1.1 Pin Functions

Signal Name	Function
A	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQ	Data I/O
V_{DD}	Power Supply
V_{SS}	Ground
DC	Do Not Connect
NC	No Connection - Pin 2, 40, 41,43 (TSOPII); Ball D3, G2, H1, H6, (BGA) Reserved For Future Expansion

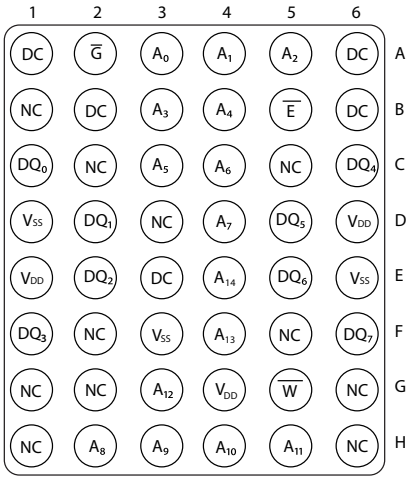
Figure 1.2 Pin Diagrams for Available Packages (Top View)



44 Pin TSOP2



32 Pin SOIC



48 Pin FBGA

Table 1.2 Operating Modes

$\overline{E}$[1]	$\overline{G}$[1]	$\overline{W}$[1]	Mode	V_{DD} Current	DQ[7:0][2]
H	X	X	Not selected	I_{SB1}, I_{SB2}	Hi-Z
L	H	H	Output disabled	I_{DDR}	Hi-Z
L	L	H	Byte Read	I_{DDR}	D_{Out}
L	X	L	Byte Write	I_{DDW}	D_{in}

[1] H = high, L = low, X = don't care

[2] Hi-Z = high impedance

2. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

This device contains circuitry to protect the inputs against damage caused by high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage greater than maximum rated voltages to these high-impedance (Hi-Z) circuits.

The device also contains protection against external magnetic fields. Precautions should be taken to avoid application of any magnetic field more intense than the maximum field intensity specified in the maximum ratings.

Table 2.1 Absolute Maximum Ratings[1]

Parameter	Symbol	Value	Unit
Supply voltage[2]	V_{DD}	-0.5 to 4.0	V
Voltage on an pin[2]	V_{IN}	-0.5 to V_{DD} + 0.5	V
Output current per pin	I_{OUT}	±20	mA
Package power dissipation [3]	P_D	0.600	W
Temperature under bias MR256A08B (Commercial) MR256A08BC (Industrial)	T_{BIAS}	 -10 to 85 -45 to 95	°C
Storage Temperature	T_{stg}	-55 to 150	°C
Lead temperature during solder (3 minute max)	T_{Lead}	260	°C
Maximum magnetic field during write MR256A08B (All Temperatures)	H_{max_write}	2000	A/m
Maximum magnetic field during read or standby	H_{max_read}	8000	A/m

[1] Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to recommended operating conditions. Exposure to excessive voltages or magnetic fields could affect device reliability.

[2] All voltages are referenced to V_{SS}.

[3] Power dissipation capability depends on package characteristics and use environment.

Table 2.2 Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Power supply voltage	V_{DD}	3.0 [1]	3.3	3.6	V
Write inhibit voltage	V_{WI}	2.5	2.7	3.0 [1]	V
Input high voltage	V_{IH}	2.2	-	V_{DD} + 0.3 [2]	V
Input low voltage	V_{IL}	-0.5 [3]	-	0.8	V
Temperature under bias MR256A08B (Commercial) MR256A08BC (Industrial)	T_A	 0 -40		 70 85	°C

[1] There is a 2 ms startup time once V_{DD} exceeds $V_{DD,}$(min). See **Power Up and Power Down Sequencing** below.

[2] V_{IH}(max) = V_{DD} + 0.3 V_{DC}; V_{IH}(max) = V_{DD} + 2.0 V_{AC} (pulse width ≤ 10 ns) for I ≤ 20.0 mA.

[3] V_{IL}(min) = -0.5 V_{DC} ; V_{IL}(min) = -2.0 V_{AC} (pulse width ≤ 10 ns) for I ≤ 20.0 mA.

Power Up and Power Down Sequencing

The MRAM is protected from write operations whenever V_{DD} is less than V_{WI}. As soon as V_{DD} exceeds V_{DD}(min), there is a startup time of 2 ms before read or write operations can start. This time allows memory power supplies to stabilize.

The $\overline{E}$ and $\overline{W}$ control signals should track V_{DD} on power up to V_{DD}- 0.2 V or V_{IH} (whichever is lower) and remain high for the startup time. In most systems, this means that these signals should be pulled up with a resistor so that signal remains high if the driving signal is Hi-Z during power up. Any logic that drives $\overline{E}$ and $\overline{W}$ should hold the signals high with a power-on reset signal for longer than the startup time.

During power loss or brownout where V_{DD} goes below V_{WI}, writes are protected and a startup time must be observed when power returns above V_{DD}(min).

Figure 2.1 Power Up and Power Down Diagram

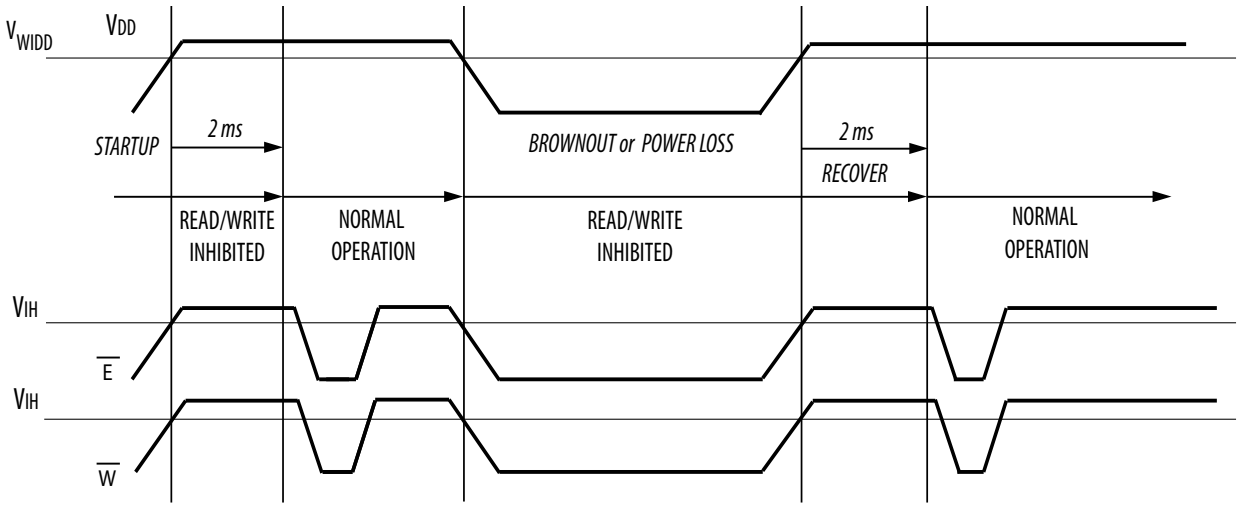


Table 2.3 DC Characteristics

Parameter	Symbol	Min	Typical	Max	Unit
Input leakage current	$I_{lkg(I)}$	-	-	±1	µA
Output leakage current	$I_{lkg(O)}$	-	-	±1	µA
Output low voltage (I_{OL} = +4 mA) (I_{OL} = +100 µA)	V_{OL}	-	-	0.4 V_{SS} + 0.2	V
Output high voltage (I_{OL} = -4 mA) (I_{OL} = -100 µA)	V_{OH}	2.4 V_{DD} - 0.2	-	-	V

Table 2.4 Power Supply Characteristics

Parameter	Symbol	Typical	Max	Unit
AC active supply current - read modes[1] (I_{OUT}= 0 mA, V_{DD}= max)	I_{DDR}	25	30	mA
AC active supply current - write modes[1] (V_{DD}= max)	I_{DDW}	55	65	mA
AC standby current (V_{DD}= max, $\overline{E} = V_{IH}$) *no other restrictions on other inputs*	I_{SB1}	6	7	mA
CMOS standby current ($E \geq V_{DD}$ - 0.2 V and $V_{In} \leq V_{SS}$ + 0.2 V or $\geq V_{DD}$ - 0.2 V) ($\overline{V}_{DD}$ = max, f = 0 MHz)	I_{SB2}	5	6	mA

[1] All active current measurements are measured with one address transition per cycle and at minimum cycle time.

3. TIMING SPECIFICATIONS

Table 3.1 Capacitance[1]

Parameter	Symbol	Typical	Max	Unit
Address input capacitance	C_{In}	-	6	pF
Control input capacitance	C_{In}	-	6	pF
Input/Output capacitance	$C_{I/O}$	-	8	pF

[1] f = 1.0 MHz, dV = 3.0 V, T_A = 25 °C, periodically sampled rather than 100% tested.

Table 3.2 AC Measurement Conditions

Parameter	Value	Unit
Logic input timing measurement reference level	1.5	V
Logic output timing measurement reference level	1.5	V
Logic input pulse levels	0 or 3.0	V
Input rise/fall time	2	ns
Output load for low and high impedance parameters	See Figure 3.1	
Output load for all other timing parameters	See Figure 3.2	

Figure 3.1 Output Load Test Low and High

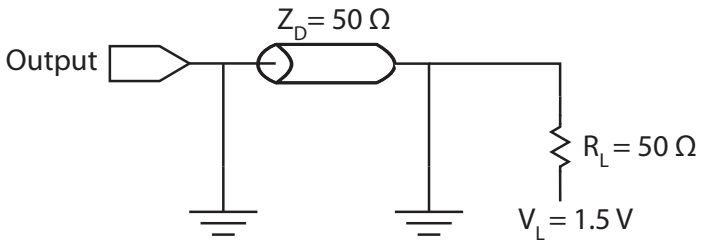
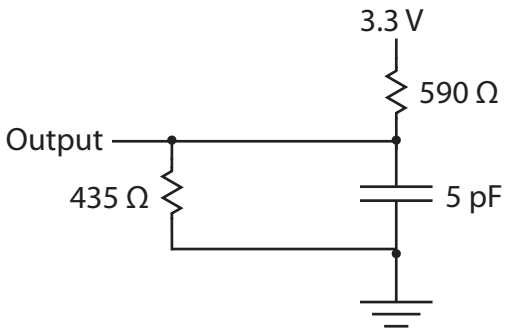


Figure 3.2 Output Load Test All Others



Read Mode

Table 3.3 Read Cycle Timing[1]

Parameter	Symbol	Min	Max	Unit
Read cycle time	t_{AVAV}	35	-	ns
Address access time	t_{AVQV}	-	35	ns
Enable access time[2]	t_{ELQV}	-	35	ns
Output enable access time	t_{GLQV}	-	15	ns
Output hold from address change	t_{AXQX}	3	-	ns
Enable low to output active[3]	t_{ELQX}	3	-	ns
Output enable low to output active[3]	t_{GLQX}	0	-	ns
Enable high to output Hi-Z[3]	t_{EHQZ}	0	15	ns
Output enable high to output Hi-Z[3]	t_{GHQZ}	0	10	ns

1 $\overline{W}$ is high for read cycle. Power supplies must be properly grounded and decoupled, and bus contention conditions must be minimized or eliminated during read or write cycles.

2 Addresses valid before or at the same time $\overline{E}$ goes low.

3 This parameter is sampled and not 100% tested. Transition is measured ±200 mV from the steady-state voltage.

Figure 3.3A Read Cycle 1

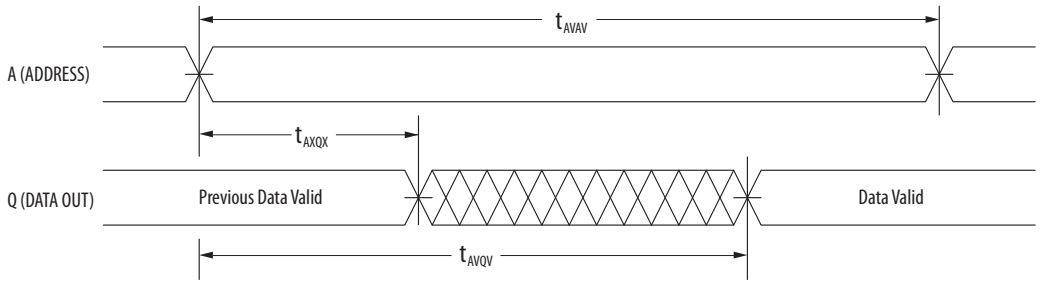


Figure 3.3B Read Cycle 2

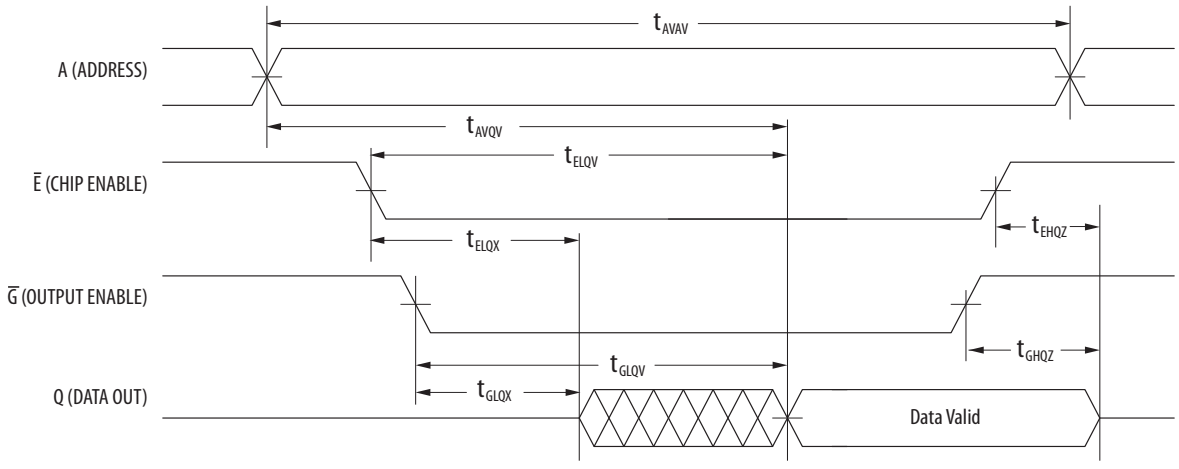


Table 3.4 Write Cycle Timing 1 ($\overline{W}$ Controlled)[1]

Parameter	Symbol	Min	Max	Unit
Write cycle time[2]	t_{AVAV}	35	-	ns
Address set-up time	t_{AVWL}	0	-	ns
Address valid to end of write ($\overline{G}$ high)	t_{AVWH}	18	-	ns
Address valid to end of write ($\overline{G}$ low)	t_{AVWH}	20	-	ns
Write pulse width ($\overline{G}$ high)	t_{WLWH} t_{WLEH}	15	-	ns
Write pulse width ($\overline{G}$ low)	t_{WLWH} t_{WLEH}	15	-	ns
Data valid to end of write	t_{DVWH}	10	-	ns
Data hold time	t_{WHDX}	0	-	ns
Write low to data Hi-Z[3]	t_{WLQZ}	0	12	ns
Write high to output active[3]	t_{WHQX}	3	-	ns
Write recovery time	t_{WHAX}	12	-	ns

[1] All writes occur during the overlap of $\overline{E}$ low and $\overline{W}$ low. Power supplies must be properly grounded and decoupled and bus contention conditions must be minimized or eliminated during read and write cycles. If $\overline{G}$ goes low at the same time or after $\overline{W}$ goes low, the output will remain in a high impedance state. After $\overline{W}$ or $\overline{E}$ has been brought high, the signal must remain in steady-state high for a minimum of 2 ns. The minimum time between $\overline{E}$ being asserted low in one cycle to $\overline{E}$ being asserted low in a subsequent cycle is the same as the minimum cycle time allowed for the device.

[2] All write cycle timings are referenced from the last valid address to the first transition address.

[3] This parameter is sampled and not 100% tested. Transition is measured ±200 mV from the steady-state voltage. At any given voltage or temperature, $t_{WLQZ}(max) < t_{WHQX}(min)$

Figure 3.4 Write Cycle Timing 1 ($\overline{W}$ Controlled)

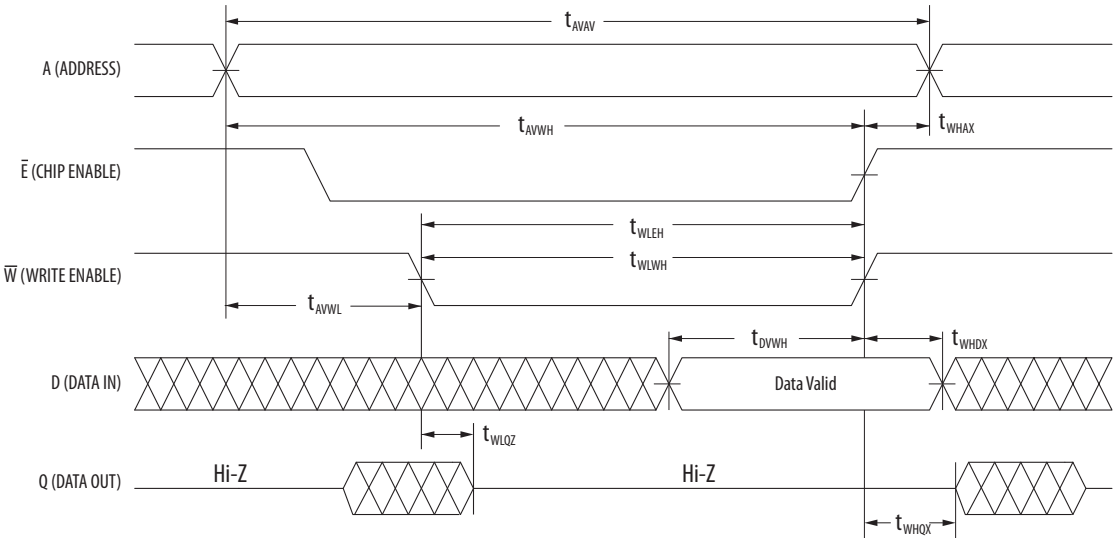


Table 3.5 Write Cycle Timing 2 ($\overline{E}$ Controlled)[1]

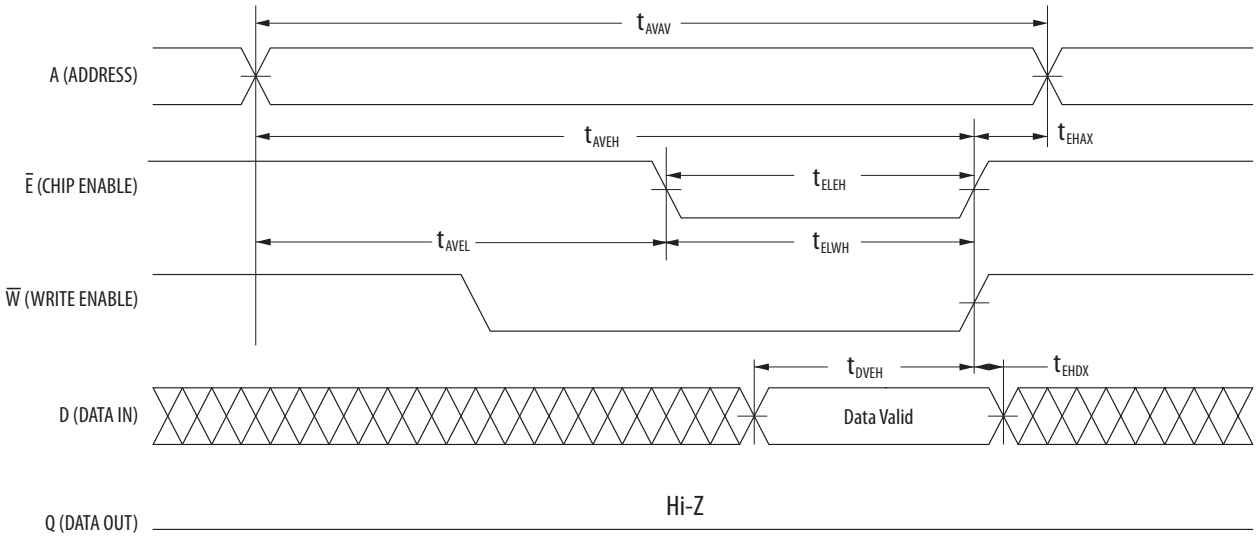
Parameter	Symbol	Min	Max	Unit
Write cycle time[2]	t_{AVAV}	35	-	ns
Address set-up time	t_{AVEL}	0	-	ns
Address valid to end of write ($\overline{G}$ high)	t_{AVEH}	18	-	ns
Address valid to end of write ($\overline{G}$ low)	t_{AVEH}	20	-	ns
Enable to end of write ($\overline{G}$ high)	t_{ELEH} t_{ELWH}	15	-	ns
Enable to end of write ($\overline{G}$ low)[3]	t_{ELEH} t_{ELWH}	15	-	ns
Data valid to end of write	t_{DVEH}	10	-	ns
Data hold time	t_{EHDX}	0	-	ns
Write recovery time	t_{EHAX}	12	-	ns

[1] All writes occur during the overlap of $\overline{E}$ low and $\overline{W}$ low. Power supplies must be properly grounded and decoupled and bus contention conditions must be minimized or eliminated during read and write cycles. If $\overline{G}$ goes low at the same time or after $\overline{W}$ goes low, the output will remain in a high impedance state. After $\overline{W}$ or $\overline{E}$ has been brought high, the signal must remain in steady-state high for a minimum of 2 ns. The minimum time between $\overline{E}$ being asserted low in one cycle to $\overline{E}$ being asserted low in a subsequent cycle is the same as the minimum cycle time allowed for the device.

[2] All write cycle timings are referenced from the last valid address to the first transition address.

[3] If $\overline{E}$ goes low at the same time or after $\overline{W}$ goes low, the output will remain in a high-impedance state. If $\overline{E}$ goes high at the same time or before $\overline{W}$ goes high, the output will remain in a high-impedance state.

Figure 3.5 Write Cycle Timing 2 ($\overline{E}$ Controlled)



4. ORDERING INFORMATION

Figure 4.1 Part Numbering System

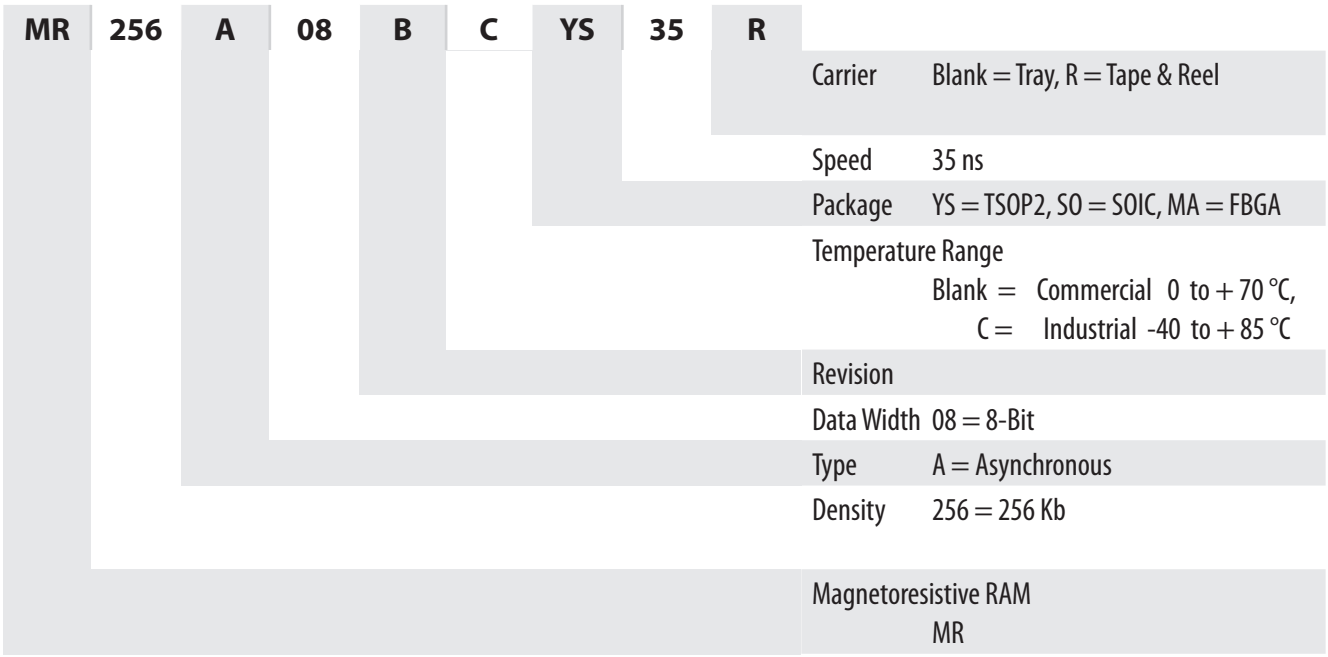


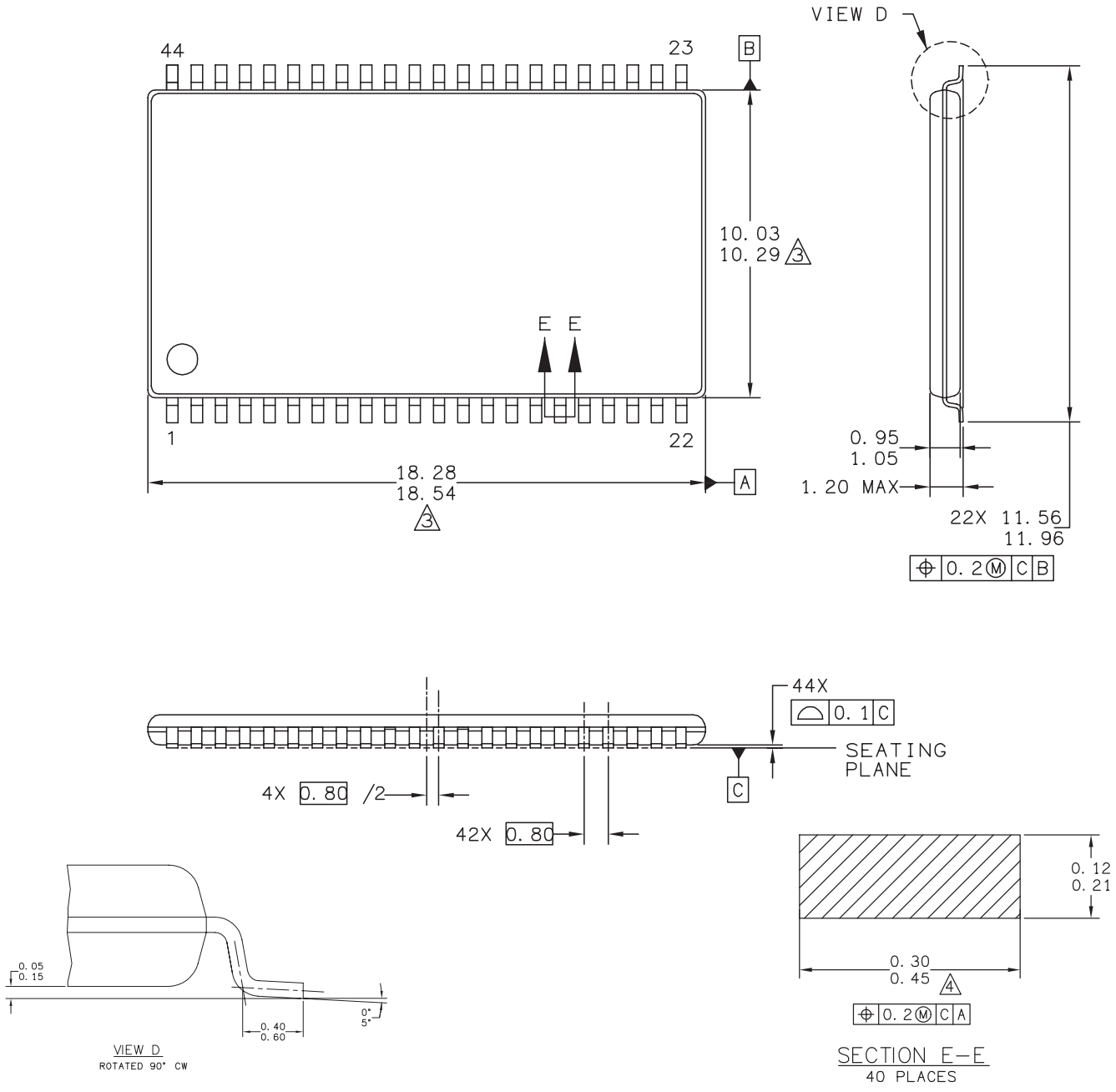
Table 4.1 Available Parts

Part Number	Description	Package	Ship Pack	Temp Rating
MR256A08BYS35	3.3 V 32Kx8 MRAM Commercial	44-TSOP	Tray	0 to +70 °C
MR256A08BCYS35	3.3 V 32Kx8 MRAM Industrial	44-TSOP	Tray	-40 to +85 °C
MR256A08BYS35R	3.3 V 32Kx8 MRAM Commercial	44-TSOP	Tape and Reel	0 to +70 °C
MR256A08BCYS35R	3.3 V 32Kx8 MRAM Industrial	44-TSOP	Tape and Reel	-40 to +85 °C
MR256A08BMA35	3.3 V 32Kx8 MRAM Commercial	48-BGA	Tray	0 to +70 °C
MR256A08BCMA35	3.3 V 32Kx8 MRAM Industrial	48-BGA	Tray	-40 to +85 °C
MR256A08BMA35R	3.3 V 32Kx8 MRAM Commercial	48-BGA	Tape and Reel	0 to +70 °C
MR256A08BCMA35R	3.3 V 32Kx8 MRAM Industrial	48-BGA	Tape and Reel	-40 to +85 °C
MR256A08BSO35	3.3 V 32Kx8 MRAM Commercial	32-SOIC	Tray	0 to +70 °C
MR256A08BCSO35 [1]	3.3 V 32Kx8 MRAM Industrial	32-SOIC	Tray	-40 to +85 °C

[1] Preliminary Product: This product is classified as Preliminary until the completion of all qualification tests. The specifications in this data sheet are intended to be final but are subject to change. Please check the Everspin web site www.everspin.com for the latest information on product status.

5. MECHANICAL DRAWING

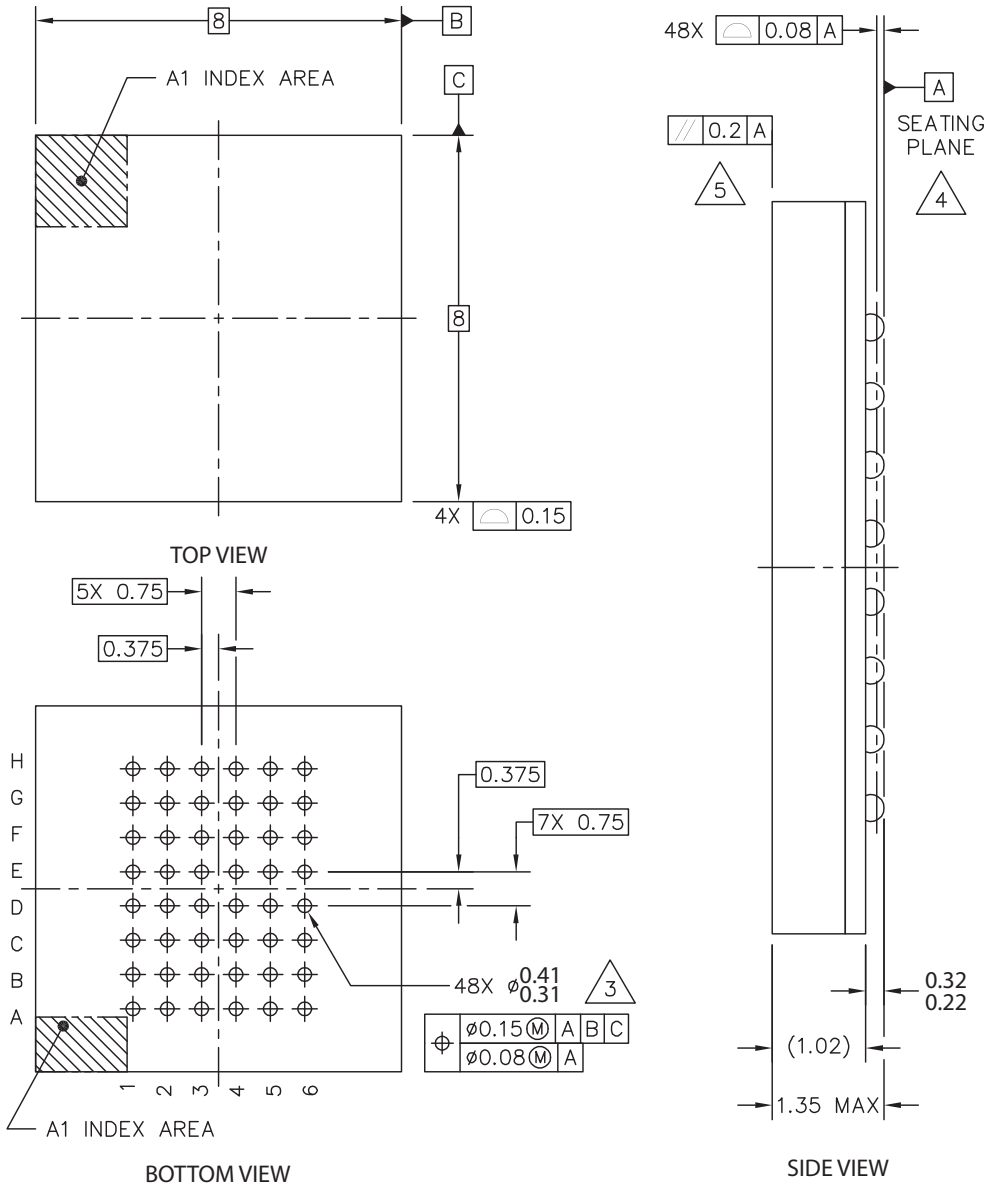
Figure 5.1 TSOP2



Print Version Not To Scale

1. Dimensions and tolerances per ASME Y14.5M - 1994.
2. Dimensions in Millimeters.
3. Dimensions do not include mold protrusion.
4. Dimension does not include DAM bar protrusions.
   DAM Bar protrusion shall not cause the lead width to exceed 0.58.

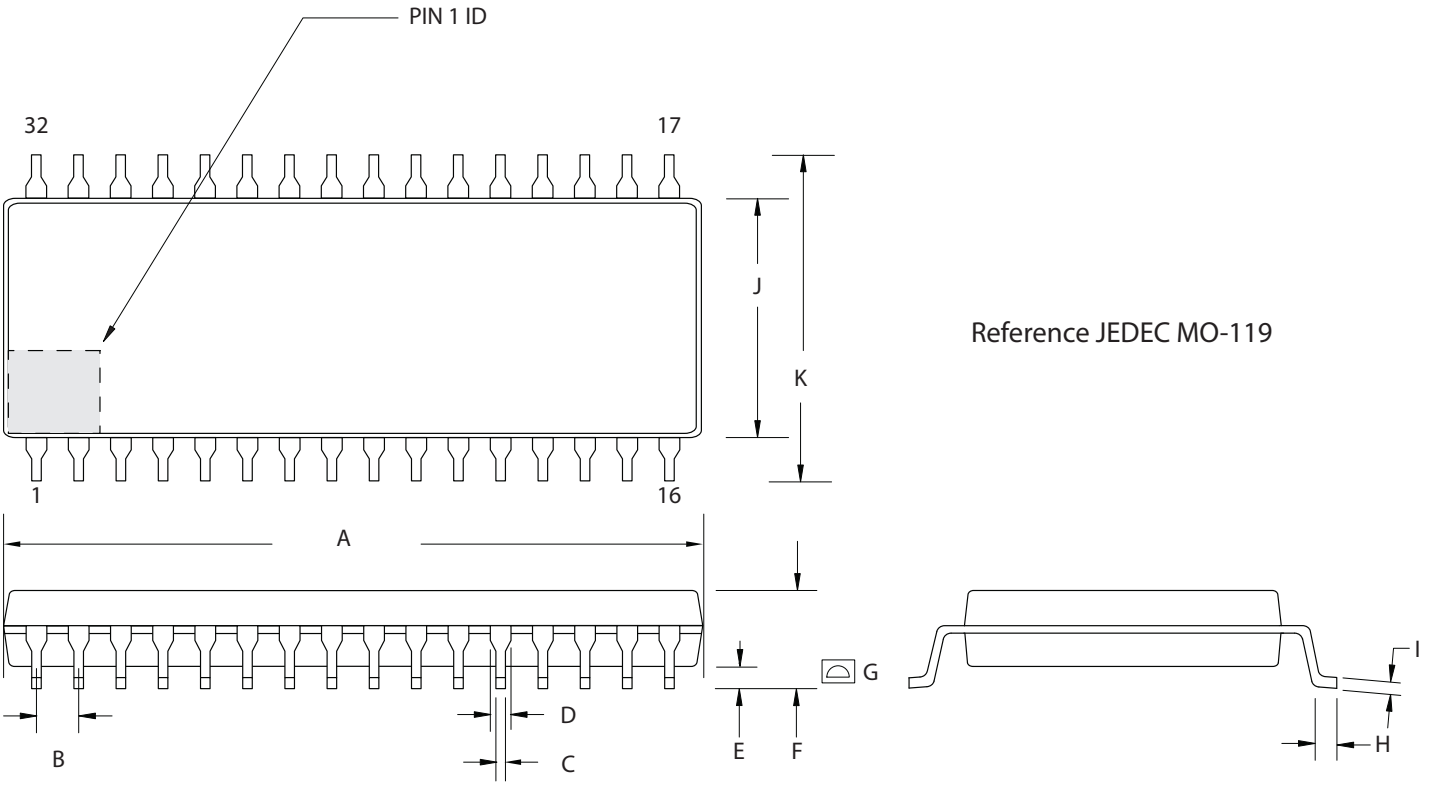
Figure 5.2 FBGA



Print Version Not To Scale

1. Dimensions in Millimeters.
2. Dimensions and tolerances per ASME Y14.5M - 1994.
3. Maximum solder ball diameter measured parallel to DATUM A
4. DATUM A, the seating plane is determined by the spherical crowns of the solder balls.
5. Parallelism measurement shall exclude any effect of mark on top surface of package.

Figure 5.3 SOIC



Unit	A	B	C	D	E	F	G	H	I	J	K
mm - Min	20.574	1.00	0.355	0.66	0.101	2.286	Radius	0.533	0.152	7.416	10.287
- Max	20.878	1.50	0.508	0.81	0.254	2.540	0.101	1.041	0.304	7.594	10.642
inch - Min	0.810	0.04	0.14	0.026	0.004	0.09	Radius	0.021	0.006	0.292	0.405
- Max	0.822	0.06	0.02	0.032	0.010	0.10	0.0040	0.041	0.012	0.299	0.419

6. REVISION HISTORY

Revision	Date	Description of Change
0	Sept 12, 2008	Initial Advance Information Release
1	Mar 25, 2009	Add Industrial and Automotive Temperature Options
2	August 16, 2011	Removed Automotive temperature options. Included SOIC package. Revised formatting
3	October 28, 2011	Changed TSOP-II to TSOP2. Changed logo to new EST Logo. Revisions to Available Parts, Table 4.1: Added Industrial Temp Grade option in SOIC package. Deleted Tape & Reel pack option for all SOIC packaged parts.
4	Dec 16, 2011	Figure 2.1 cosmetic update. Figure 5.2 BGA package outline drawing revised for package ball size.

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File Name:
MR256A08B_Datasheet_EST355_Rev4.pdf

Стандарт Электрон Связь

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