

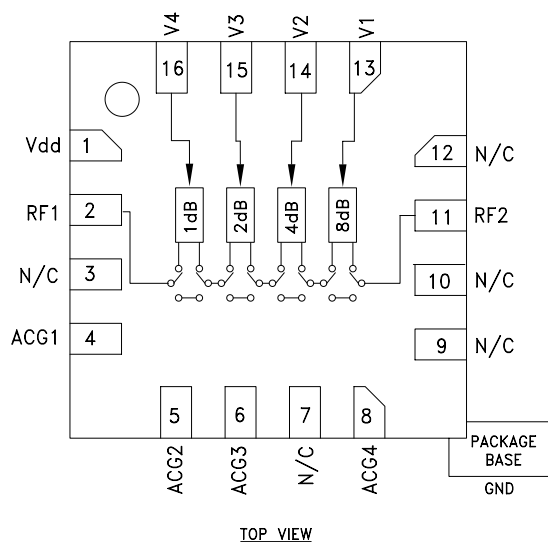
1 dB LSB SILICON MMIC 4-BIT DIGITAL POSITIVE CONTROL ATTENUATOR, 0.1 - 8 GHz

Typical Applications

The HMC540SLP3E is ideal for both RF and IF applications:

- Cellular Infrastructure
- Wireless Infrastructure
- Microwave Radio & VSAT
- Test Equipment and Sensors

Functional Diagram



Features

- 1 dB LSB Steps to 15 dB
- ± 0.2 dB Typical Step Error
- Low Insertion Loss: ≤ 1 dB
- High IP3: +56 dBm
- Single Control Line Per Bit
- TTL/CMOS Compatible Control
- Single +3.3/+5V Supply
- 3x3 mm SMT Package
- ESD rating: Class 2 (2kV HBM)
- Drop-in Replacement for HMC540LP3E

General Description

The HMC540SLP3E is a broadband 4-bit Silicon IC digital attenuator in a low cost leadless surface mount package. This single positive control line per bit digital attenuator utilizes off chip AC ground capacitors for near DC operation, making it suitable for a wide variety of RF and IF applications. Covering 0.1 to 8 GHz, the insertion loss is less than 1 dB typical. The attenuator bit values are 1 (LSB), 2, 4 and 8 dB for a total attenuation of 15 dB. Attenuation accuracy is excellent at ± 0.2 dB typical step error. The attenuator also features a IIP3 of +56dBm. Four TTL/CMOS control inputs are used to select each attenuation state. It can operate with a single Vdd ranging from +3.3V to 5V.

Electrical Specifications,

$T_A = +25^\circ\text{C}$, With $V_{dd} = +5\text{V}$ & $V_{ctl} = 0/+5\text{V}$ (Unless Otherwise Noted)

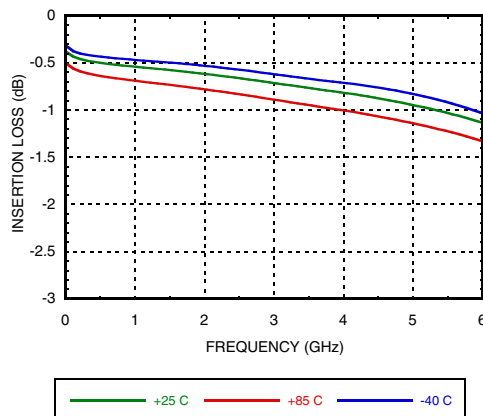
| Parameter | Frequency (GHz) | Min. | Typ. | Max. | Units |
|---|-----------------|-----------------|-------------------------------------|------|-------|
| Insertion Loss | 0.1 - 2.0 GHz | | 0.7 | 1.1 | dB |
| | 2.0 - 3.0 GHz | | 0.8 | 1.3 | dB |
| | 3.0 - 4.0 GHz | | 0.8 | 1.6 | dB |
| | 4.0 - 5.5 GHz | | 1.0 | 2.6 | dB |
| | 5.5 - 8.0 GHz | | 1.7 | 3.0 | dB |
| Attenuation Range | 0.1 - 8 GHz | | 15 | | dB |
| Return Loss (RF1 & RF2, All Atten. States) | 0.1 - 3.5 GHz | | 22 | | dB |
| | 3.5 - 5.5 GHz | | 17 | | dB |
| | 5.5 - 8 GHz | | 12 | | dB |
| Attenuation Accuracy: (Referenced to Insertion Loss) | All States | 0.1 - 1.0 GHz | ± (0.2 + 2% of Atten. Setting) Max. | | dB |
| | | 1.0 - 4.0 GHz | ± (0.2 + 3% of Atten. Setting) Max. | | dB |
| | | 4.0 - 5.0 GHz | ± (0.3 + 5% of Atten. Setting) Max. | | dB |
| | | 5.0 - 5.5 GHz | ± (0.4 + 8% of Atten. Setting) Max. | | dB |
| | | 5.5 GHz - 8 GHz | ± (0.5 + 9% of Atten. Setting) Max. | | dB |

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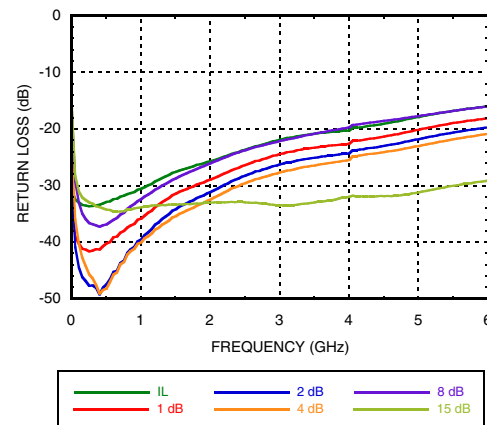
| Parameter | Frequency (GHz) | Min. | Typ. | Max. | Units |
|---|-----------------|---------------------------------------|----------|------|-------|
| Input Power for 0.1 dB Compression | 0.1 - 8 GHz | | 31 | | dBm |
| Input Third Order Intercept Point (Two-Tone Input Power= 12 dBm Each Tone) | 0.1 - 8 GHz | REF - 4 dB States 5 - 15 dB States | 57 55 | | dBm |
| Switching Characteristics | DC - 8 GHz | | | | |
| tRISE, tFALL (10/90% RF) | | | 45 | | ns |
| tON, tOFF (50% CTL to 10/90% RF) | | | 129 | | ns |

Frequency Response Plots up to 6 GHz

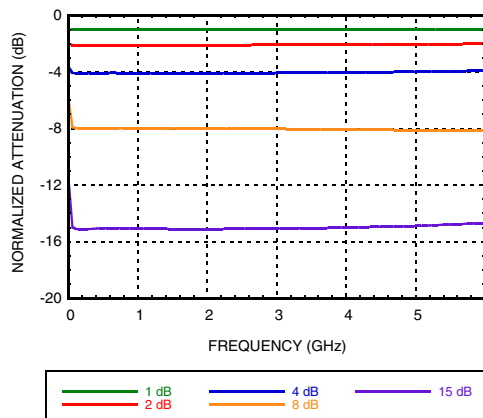
Insertion Loss



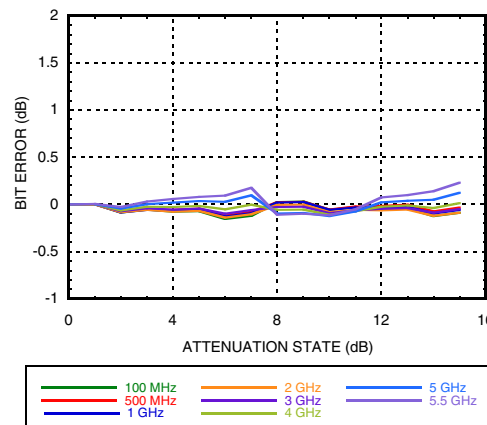
Return Loss RF1, RF2 (Only Major States are Shown)



Normalized Attenuation (Only Major States are Shown)



Bit Error vs. Attenuation State



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**1 dB LSB SILICON MMIC 4-BIT DIGITAL
POSITIVE CONTROL ATTENUATOR, 0.1 - 8 GHz**

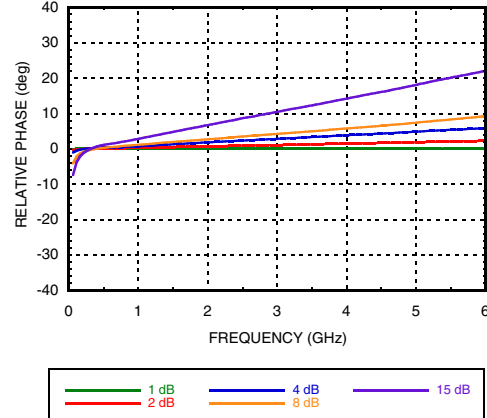
Bit Error vs. Frequency

(Only Major States are Shown)

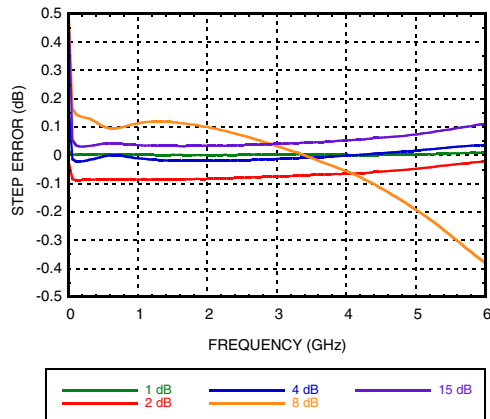


Relative Phase vs. Frequency

(Only Major States are Shown)



Step Error vs Frequency (Major States)

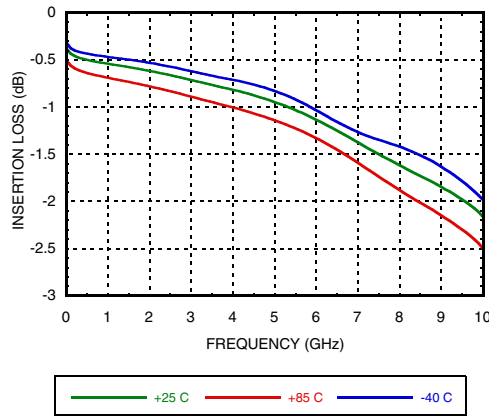


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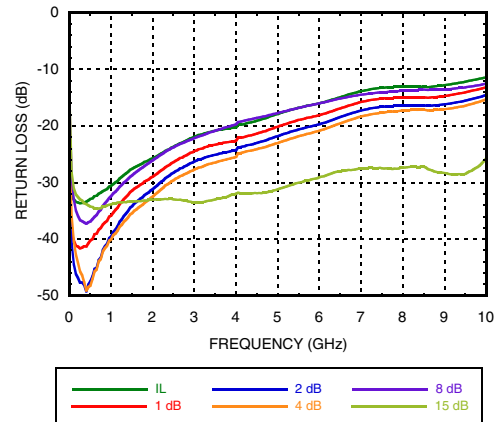
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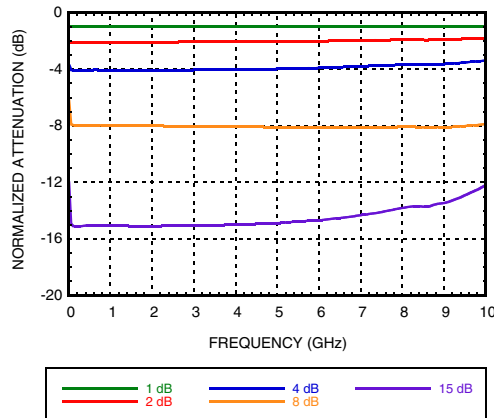
**Frequency Response Plots up to 10 GHz
Insertion Loss**



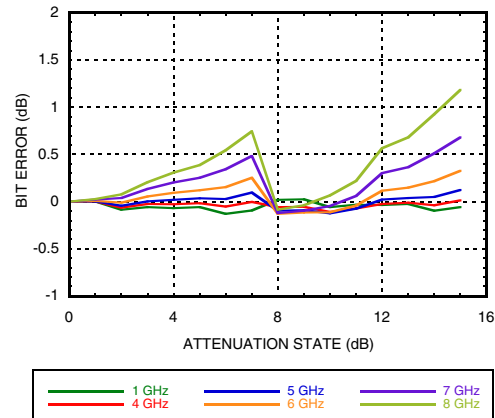
**Return Loss RF1, RF2
(Only Major States are Shown)**



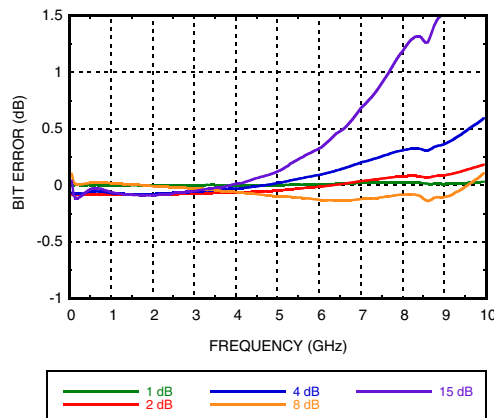
**Normalized Attenuation
(Only Major States are Shown)**



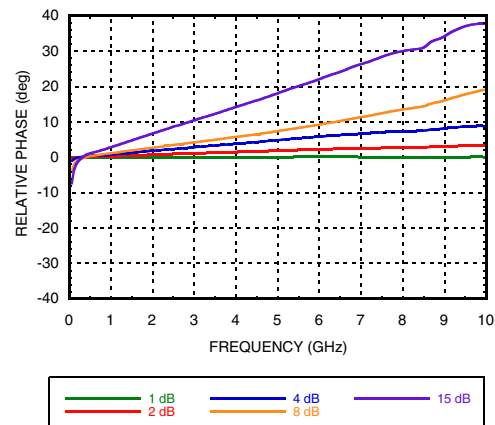
Bit Error vs. Attenuation State



**Bit Error vs. Frequency
(Only Major States are Shown)**



**Relative Phase vs. Frequency
(Only Major States are Shown)**

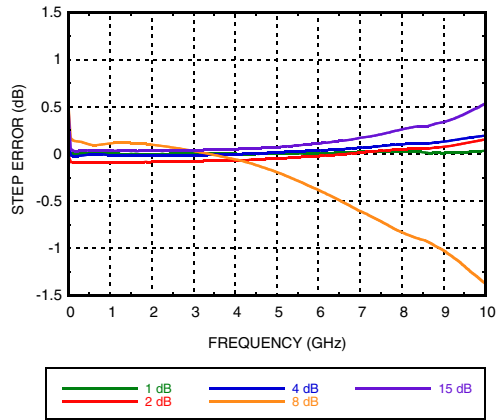


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Step Error vs Frequency (Major States)

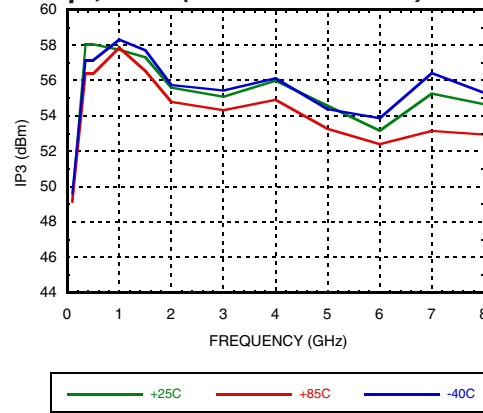


1 dB LSB SILICON MMIC 4-BIT DIGITAL POSITIVE CONTROL ATTENUATOR, 0.1 - 8 GHz

**Power Handling up to 8 GHz
Input Third Order Intercept Point over
Temp., 5V (100 MHz - 8 GHz)**



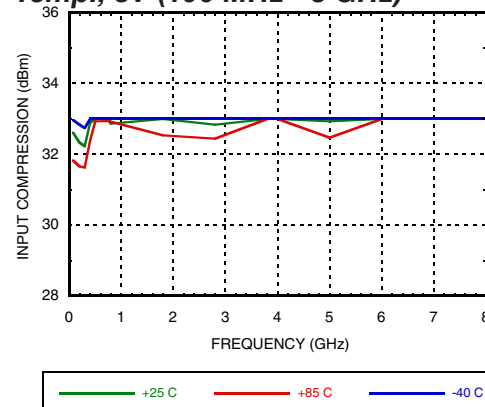
**Input Third Order Intercept Point over
Temp., 3.3V (100 MHz - 8 GHz)**



**0.1 and 1 dB Input Compression Point, 5V
(100 MHz - 8 GHz)**



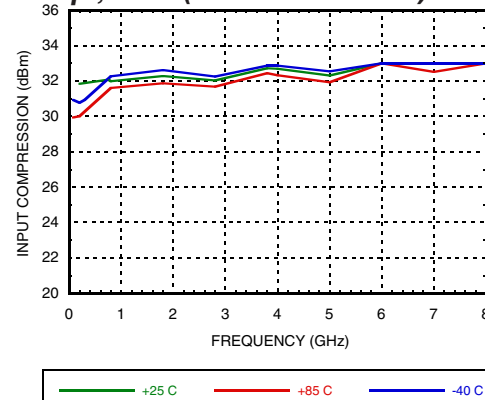
**1 dB Input Compression Point, Over
Temp., 5V (100 MHz - 8 GHz)**



**0.1 and 1 dB Input Compression Point,
3.3V (100 MHz - 8 GHz)**



**1 dB Input Compression Point, Over
Temp., 3.3V (100 MHz - 8 GHz)**



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Absolute Maximum Ratings

| | |
|---|-------------------|
| RF Input Power at 85 °C | +27 dBm |
| RF Input Power at 105 °C | +25 dBm |
| Bias Voltage (Vdd) | -0.3V to 5.4V |
| Control Voltage Range (V1 to V4) | -0.3V to Vdd +.5V |
| Channel Temperature | 140 °C |
| Thermal Resistance (at maximum power dissipation) | 110 °C/W |
| ESD Sensitivity (HBM) | Class 2 |
| Storage Temperature | -65 to +150 °C |

Recommended Operation Ratings

| | |
|----------------------------------|----------------|
| RF Input Power at 85 °C | +24 dBm |
| RF Input Power at 105 °C | +23 dBm |
| Bias Voltage (Vdd) | 3V to 5.4V |
| Control Voltage Range (V1 to V4) | 0 to Vdd |
| Operating Temperature | -40 to +105 °C |



ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Bias Voltage & Current

| Vdd (V) | Idd (Typ.) (mA) |
|---------|-----------------|
| +3.3 | 0.14 |
| +5.0 | 0.17 |

Control Voltage

| State | Vdd = +3.3V | Vdd = +5V |
|-------|--------------------|---------------------|
| Low | 0 to 0.5V @ < 1 uA | 0 to +0.8V @ < 1 uA |
| High | 2 to 3.3V @ 25 uA | 2 to 5V @ 35 uA |

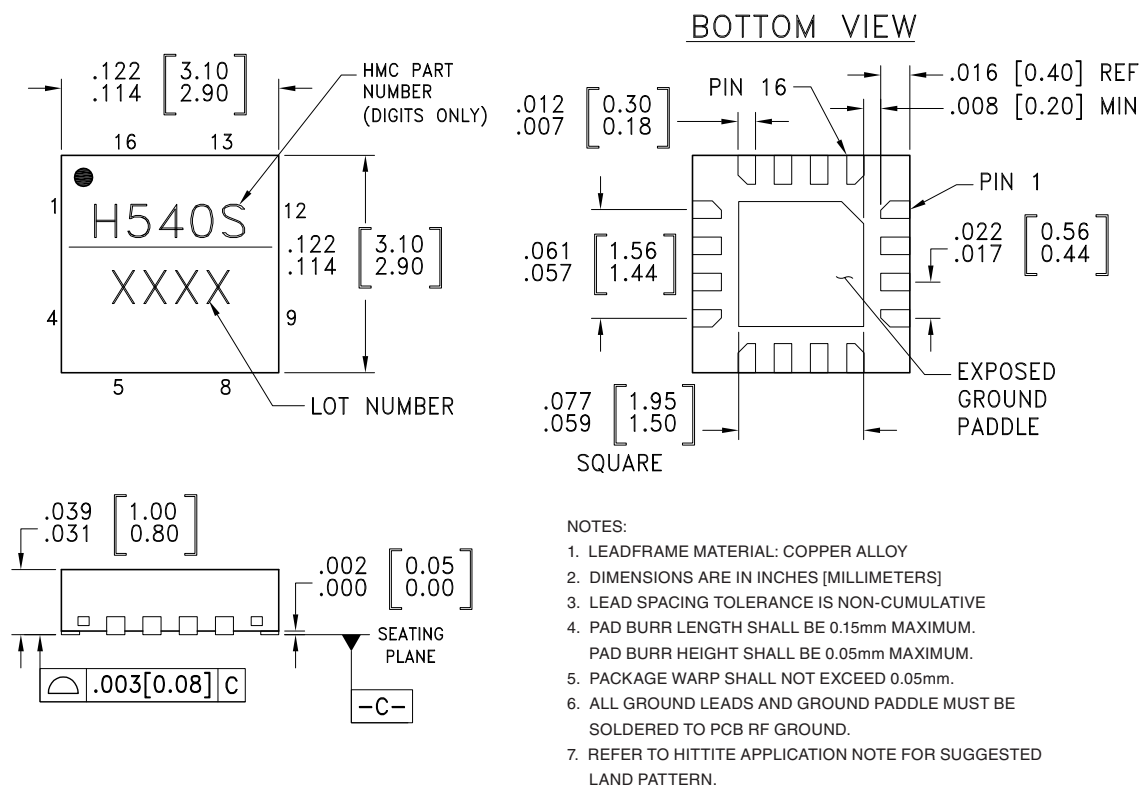
Truth Table

| Control Voltage Input | | | | Attenuation State RF1 - RF2 |
|-----------------------|------------|------------|------------|--------------------------------|
| V1 8 dB | V2 4 dB | V3 2 dB | V4 1 dB | |
| High | High | High | High | Reference I.L. |
| High | High | High | Low | 1 dB |
| High | High | Low | High | 2 dB |
| High | Low | High | High | 4 dB |
| Low | High | High | High | 8 dB |
| Low | Low | Low | Low | 15 dB |

Any combination of the above states will provide an attenuation approximately equal to the sum of the bits selected.

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Outline Drawing



Package Information

| Part Number | Package Body Material | Lead Finish | MSL Rating | Package Marking ^[3] |
|-------------|--|---------------|---------------------|--------------------------------|
| HMC540SLP3E | RoHS-compliant Low Stress Injection Molded Plastic | 100% matte Sn | MSL3 ^[2] | H540S XXXX |

[1] Max peak reflow temperature of 235 °C

[2] Max peak reflow temperature of 260 °C

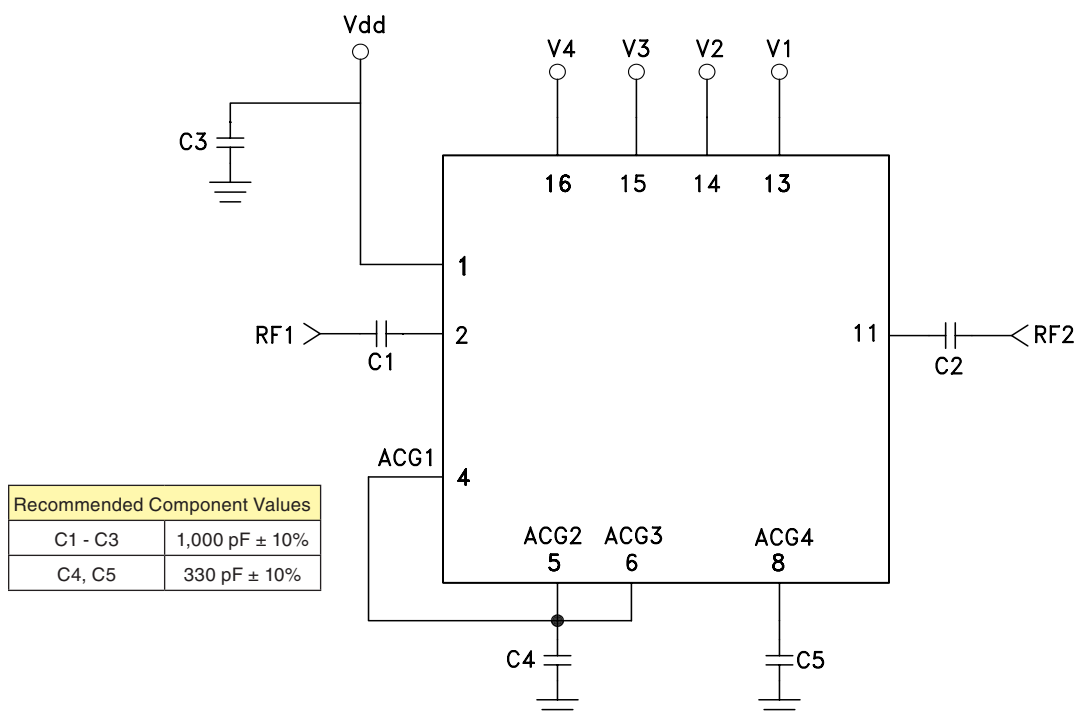
[3] 4-Digit lot number XXXX

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Pin Descriptions

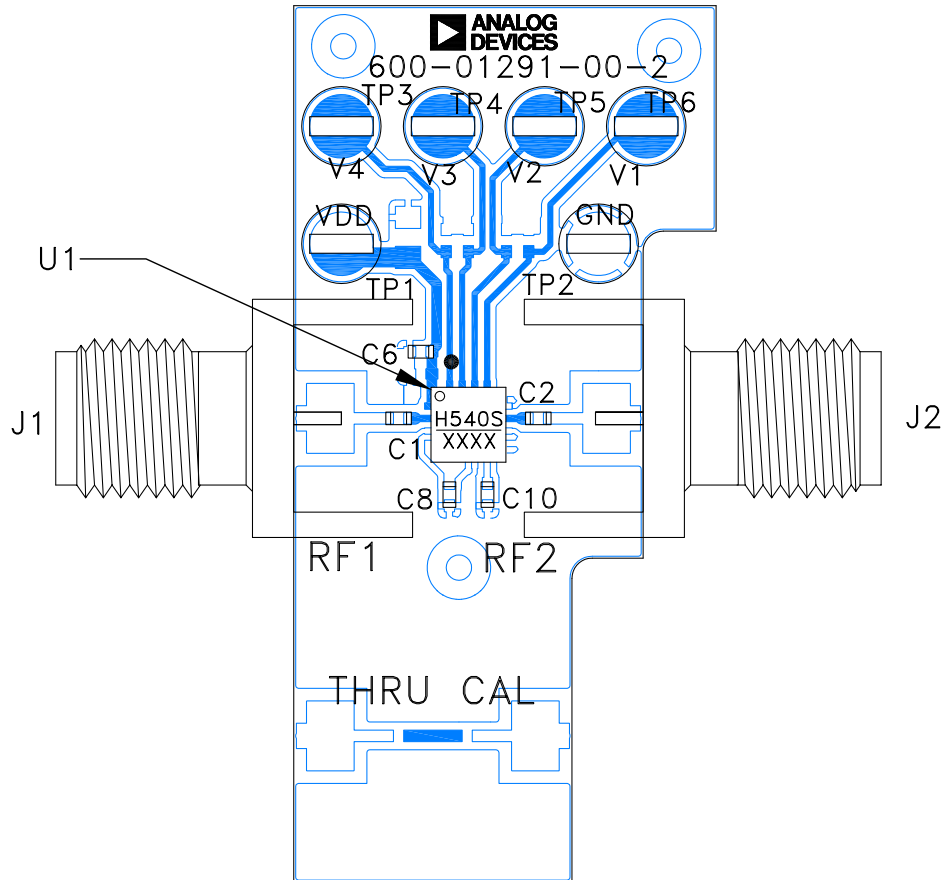
| Pin Number | Function | Description | Interface Schematic |
|-----------------|-------------|---|---------------------|
| 1 | Vdd | Supply Voltage. | |
| 2, 11 | RF1, RF2 | This pin is DC coupled and matched to 50 Ohm. Blocking capacitors are required. Select value based on lowest frequency of operation. | |
| 3, 7, 9, 10, 12 | N/C | These pins should be connected to PCB RF ground to maximize performance. | |
| 4 - 6, 8 | ACG1 - ACG4 | External capacitor to ground is required. Select value for lowest frequency of operation. Place capacitor as close to pins as possible. | |
| 13 - 16 | V1 - V4 | See truth table and control voltage table. | |
| | GND | Package bottom has an exposed metal paddle that must be connected to RF/DC Ground. | |

Application Circuit



1 dB LSB SILICON MMIC 4-BIT DIGITAL POSITIVE CONTROL ATTENUATOR, 0.1 - 8 GHz

Evaluation PCB



List of Materials for Evaluation PCB EV1HMC540SLP3^[1]

| Item | Description |
|------------|--------------------------------|
| J1, J2 | PCB Mount SMA Connector |
| TP1 - TP6 | Thru Hole Mount Test Point |
| C1, C2, C6 | 1000 pF Capacitor, 0402 Pkg. |
| C8, C10 | 330 pF Capacitor, 0402 Pkg. |
| U1 | HMC540SLP3E Digital Attenuator |
| PCB [2] | 600-01291-00 Evaluation PCB |

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Analog Devices upon request.



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