MICROCHIP TC4426A/TC4427A/TC4428A

1.5A Dual High-Speed Power MOSFET Drivers

Features:

- High Peak Output Current – 1.5A
- Wide Input Supply Voltage Operating Range:
  - 4.5V to 18V
- High Capacitive Load Drive Capability – 1000 pF in 25 ns (typ.)
- Short Delay Times – 30 ns (typ.)
- Matched Rise, Fall and Delay Times
- Low Supply Current:
  - With Logic '1' Input – 1 mA (typ.)
  - With Logic '0' Input – 100 μA (typ.)
- Low Output Impedance – 7Ω (typ.)
- Latch-Up Protected: Will Withstand 0.5A Reverse Current
- Input Will Withstand Negative Inputs Up to 5V
- ESD Protected – 4 kV
- Pin-compatible with TC426/TC427/TC428 and TC4426/TC4427/TC4428
- Space-saving 8-Pin MSOP and 8-Pin 6x5 DFN Packages

Applications:

- Switch Mode Power Supplies
- Line Drivers
- Pulse Transformer Drive

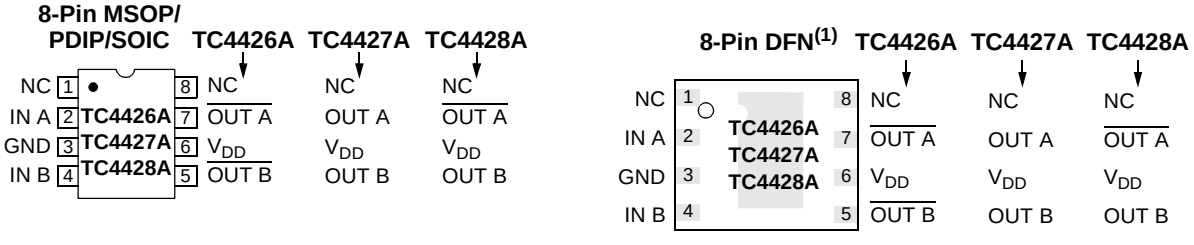
General Description:

The TC4426A/TC4427A/TC4428A are improved versions of the earlier TC4426/TC4427/TC4428 family of MOSFET drivers. In addition to matched rise and fall times, the TC4426A/TC4427A/TC4428A devices have matched leading and falling edge propagation delay times.

These devices are highly latch-up resistant under any conditions within their power and voltage ratings. They are not subject to damage when up to 5V of noise spiking (of either polarity) occurs on the ground pin. They can accept, without damage or logic upset, up to 500 mA of reverse current (of either polarity) being forced back into their outputs. All terminals are fully protected against Electrostatic Discharge (ESD) up to 4 kV.

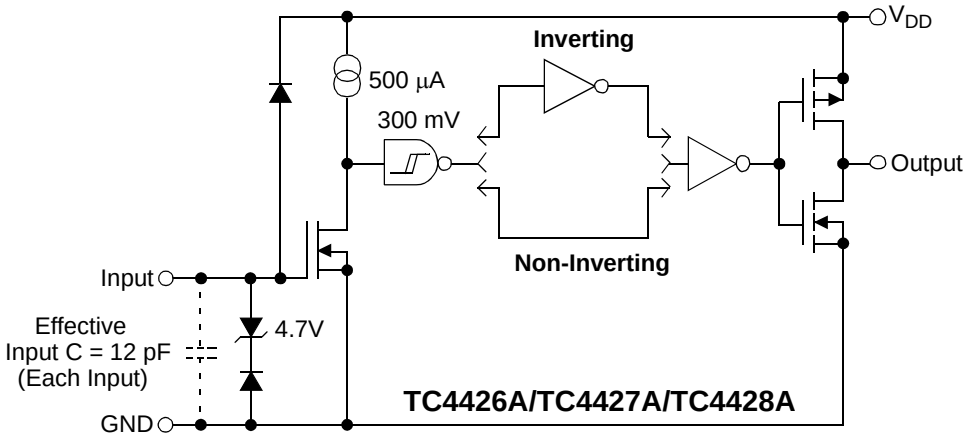
The TC4426A/TC4427A/TC4428A MOSFET drivers can easily charge/discharge 1000 pF gate capacitances in under 30 ns. These devices provide low enough impedances in both the on and off states to ensure the MOSFET's intended state will not be affected, even by large transients.

Package Types



Note 1: Exposed pad of the DFN package is electrically isolated.

Functional Block Diagram



Note 1: TC4426A has two inverting drivers, while the TC4427A has two non-inverting drivers. The TC4428A has one inverting and one non-inverting driver.

2: Ground any unused driver input.

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Supply Voltage ..... +22V
Input Voltage, IN A or IN B
..... (V_{DD} + 0.3V) to (GND – 5V)
Package Power Dissipation ($T_A \leq 70°C$)
DFN ..... **Note 2**
MSOP ..... 340 mW
PDIP ..... 730 mW
SOIC ..... 470 mW

† **Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, over operating temperature range with 4.5V $\leq V_{DD} \leq$ 18V.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Input						
Logic '1', High Input Voltage	V_{IH}	2.4	—	—	V	
Logic '0', Low Input Voltage	V_{IL}	—	—	0.8	V	
Input Current	I_{IN}	–1.0 –10	— —	+1.0 +10	µA	$0V \leq V_{IN} \leq V_{DD}$
Output						
High Output Voltage	V_{OH}	V_{DD} – 0.025	—	—	V	DC Test
Low Output Voltage	V_{OL}	—	—	0.025	V	DC Test
Output Resistance	R_O	— — — —	7 7 8 8	9 10 11 12	Ω	I_{OUT} = 10 mA, V_{DD} = 18V, T_A = +25°C 0°C $\leq T_A \leq$ +70°C -40°C $\leq T_A \leq$ +85°C -40°C $\leq T_A \leq$ +125°C
Peak Output Current	I_{PK}	—	1.5	—	A	V_{DD} = 18V
Latch-Up Protection Withstand Reverse Current	I_{REV}	—	> 0.5	—	A	Duty cycle $\leq$ 2%, t $\leq$ 300 µsec V_{DD} = 18V
Switching Time (Note 1)						
Rise Time	t_R	— — — —	25 27 29 30	35 40 40 40	ns	T_A = +25°C 0°C $\leq T_A \leq$ +70°C -40°C $\leq T_A \leq$ +85°C -40°C $\leq T_A \leq$ +125°C, **Figure 4-1**
Fall Time	t_F	— — — —	25 27 29 30	35 40 40 40	ns	T_A = +25°C 0°C $\leq T_A \leq$ +70°C -40°C $\leq T_A \leq$ +85°C -40°C $\leq T_A \leq$ +125°C, **Figure 4-1**
Delay Time	t_{D1}	— — — —	30 33 35 38	35 40 45 50	ns	T_A = +25°C 0°C $\leq T_A \leq$ +70°C -40°C $\leq T_A \leq$ +85°C -40°C $\leq T_A \leq$ +125°C, **Figure 4-1**
Delay Time	t_{D2}	— — — —	30 33 35 38	35 40 45 50	ns	T_A = +25°C 0°C $\leq T_A \leq$ +70°C -40°C $\leq T_A \leq$ +85°C -40°C $\leq T_A \leq$ +125°C, **Figure 4-1**
Power Supply						
Power Supply Current	I_S	— —	1.0 0.1	2.0 0.2	mA	V_{IN} = 3V (Both inputs) V_{IN} = 0V (Both inputs), V_{DD} = 18V

Note 1: Switching times ensured by design.
2: Package power dissipation is dependent on the copper pad area on the PCB.

TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, all parameters apply with 4.5V ≤ V_{DD} ≤ 18V.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range (C)	T_A	0	—	+70	°C	
Specified Temperature Range (E)	T_A	-40	—	+85	°C	
Specified Temperature Range (V)	T_A	-40	—	+125	°C	
Maximum Junction Temperature	T_J	—	—	+150	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Package Thermal Resistances						
Thermal Resistance, 8L-6x5 DFN	θ_{JA}	—	33.2	—	°C/W	
Thermal Resistance, 8L-MSOP	θ_{JA}	—	206	—	°C/W	
Thermal Resistance, 8L-PDIP	θ_{JA}	—	125	—	°C/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	155	—	°C/W	

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, over operating temperature range with 4.5V $\leq V_{DD} \leq$ 18V.

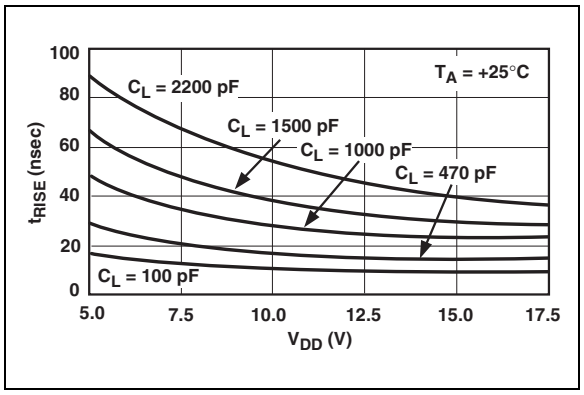


FIGURE 2-1: *Rise Time vs. Supply Voltage.*

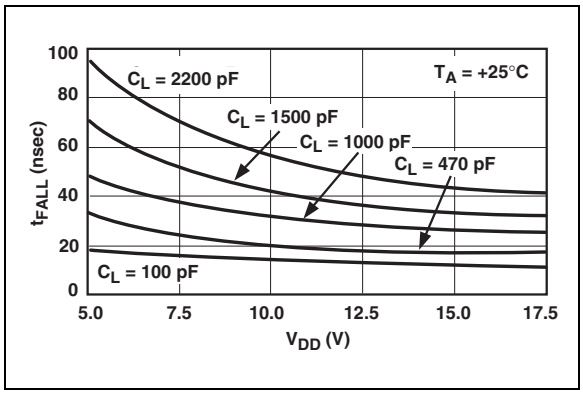


FIGURE 2-4: *Fall Time vs. Supply Voltage.*

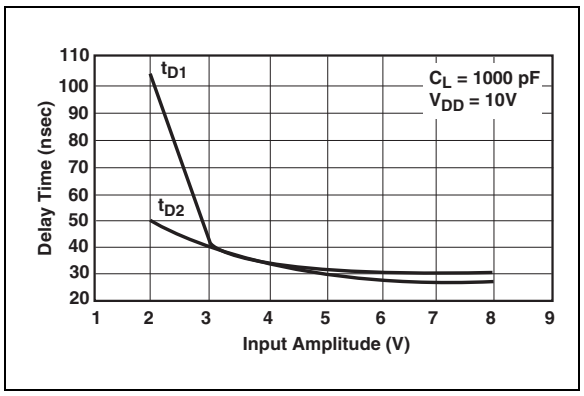


FIGURE 2-2: *Delay Time vs. Input Amplitude.*

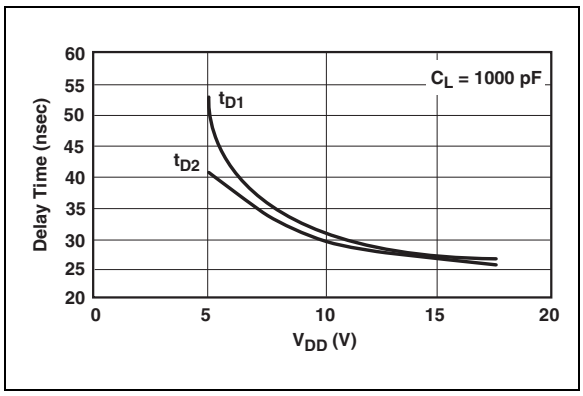


FIGURE 2-5: *Propagation Delay Time vs. Supply Voltage.*

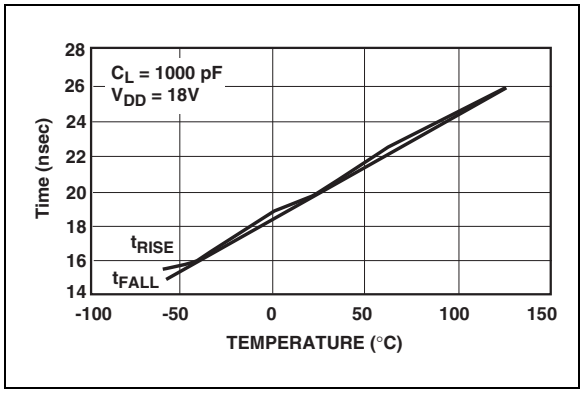


FIGURE 2-3: *Rise and Fall Times vs. Temperature.*

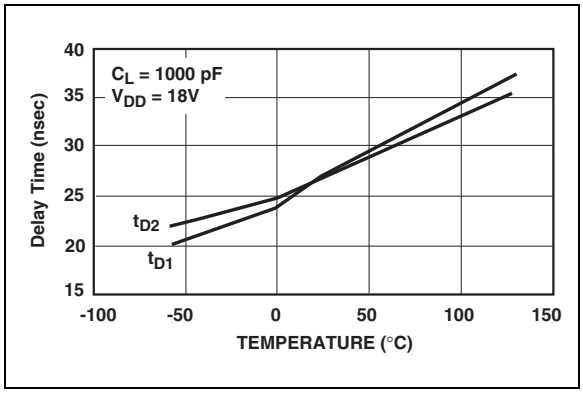


FIGURE 2-6: *Propagation Delay Time vs. Temperature.*

Note: Unless otherwise indicated, over operating temperature range with 4.5V ≤ V_{DD} ≤ 18V.

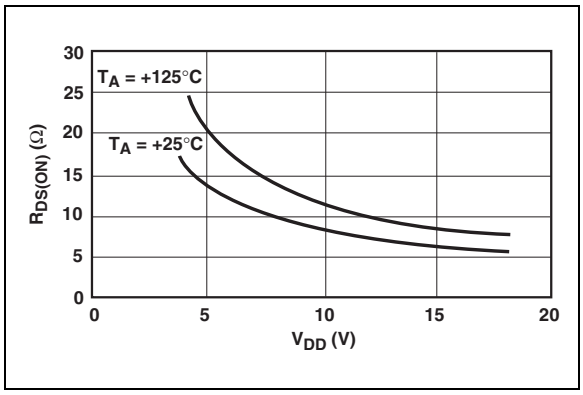


FIGURE 2-7: *High-State Output Resistance.*

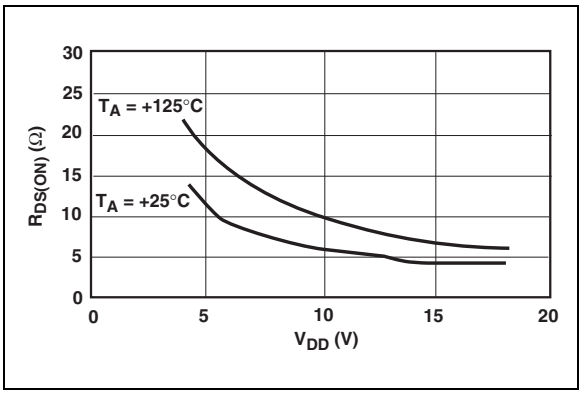


FIGURE 2-10: *Low-State Output Resistance.*

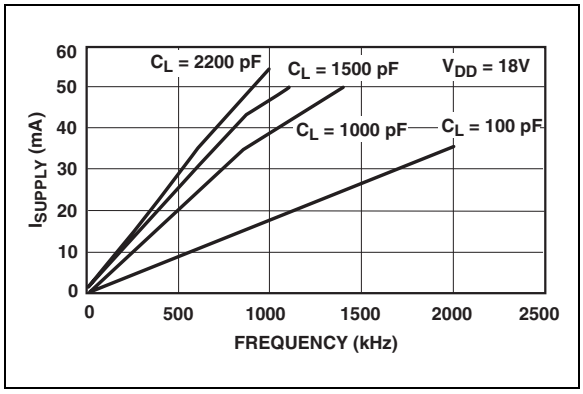


FIGURE 2-8: *Supply Current vs. Frequency.*

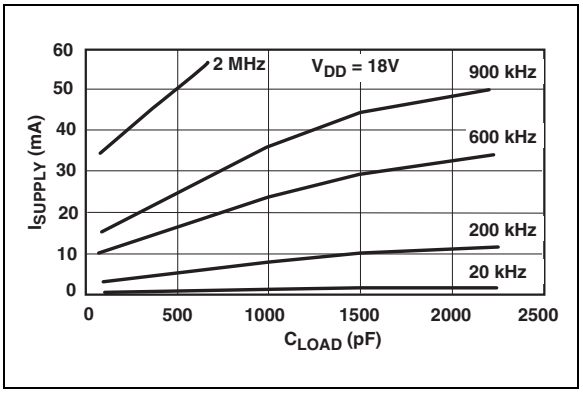


FIGURE 2-11: *Supply Current vs. Capacitive Load.*

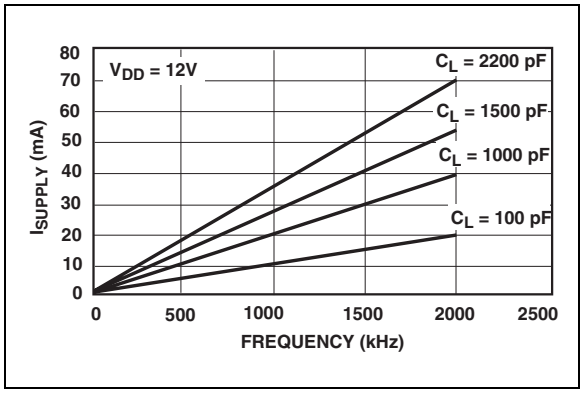


FIGURE 2-9: *Supply Current vs. Frequency.*

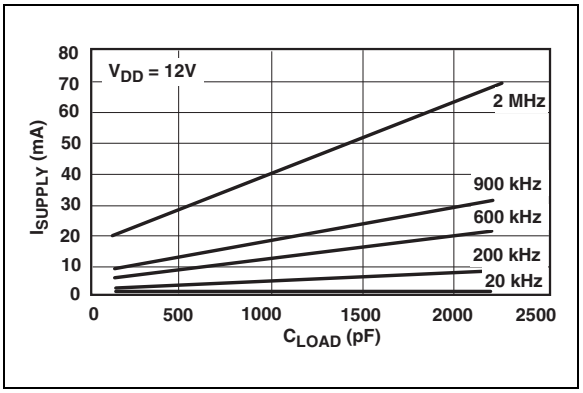


FIGURE 2-12: *Supply Current vs. Capacitive Load.*

Note: Unless otherwise indicated, over operating temperature range with 4.5V $\leq V_{DD} \leq$ 18V.

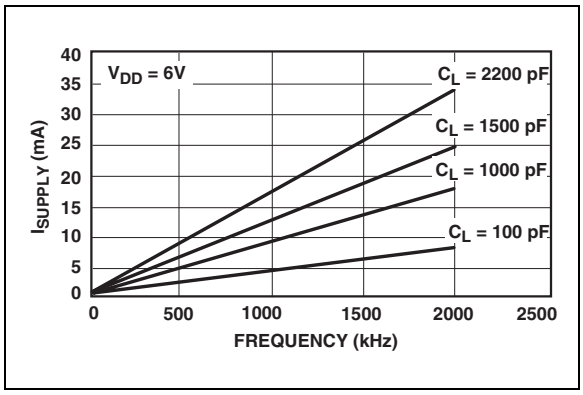


FIGURE 2-13: *Supply Current vs. Frequency.*

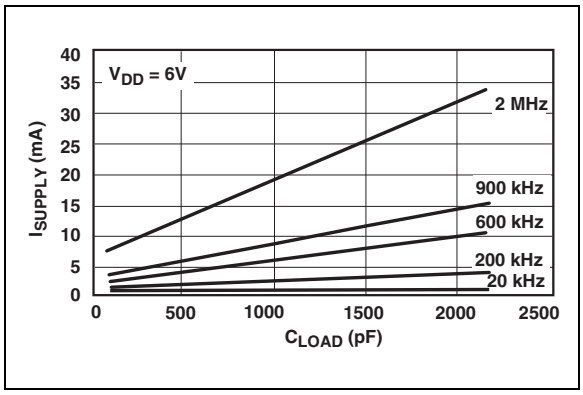


FIGURE 2-15: *Supply Current vs. Capacitive Load.*

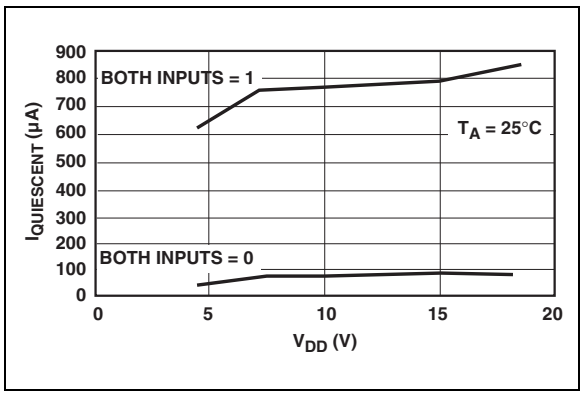


FIGURE 2-14: *Quiescent Supply Current vs. Voltage.*

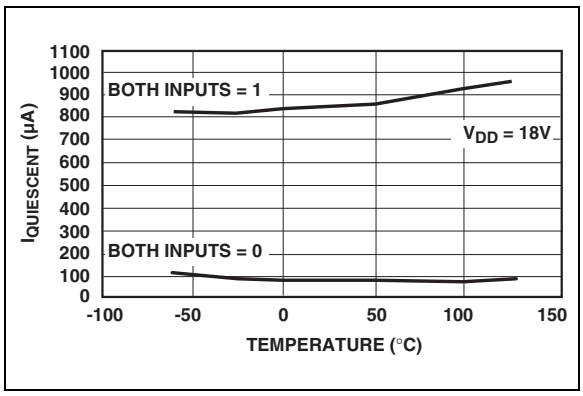


FIGURE 2-16: *Quiescent Supply Current vs. Temperature.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

8-Pin PDIP/ MSOP/SOIC	8-Pin DFN	Symbol	Description
1	1	NC	No connection
2	2	IN A	Input A
3	3	GND	Ground
4	4	IN B	Input B
5	5	OUT B	Output B
6	6	V_{DD}	Supply input
7	7	OUT A	Output A
8	8	NC	No connection
—	PAD	NC	Exposed Metal Pad

Note 1: Duplicate pins must be connected for proper operation.

3.1 Inputs A and B

MOSFET driver inputs A and B are high-impedance, TTL/CMOS compatible inputs. These inputs also have 300 mV of hysteresis between the high and low thresholds that prevents output glitching, even when the rise and fall time of the input signal is very slow.

3.2 Ground (GND)

The ground pin is the return path for both the bias current and the high peak current that discharges the external load capacitance. The ground pin should be tied into a ground plane or have a very short trace to the bias supply source return.

3.3 Output A and B

MOSFET driver outputs A and B are low-impedance, CMOS push-pull style outputs. The pull-down and pull-up devices are of equal strength, making the rise and fall times equivalent.

3.4 Supply Input (V_{DD})

The V_{DD} input is the bias supply for the MOSFET driver and is rated for 4.5V to 18V, with respect to the ground pin. The V_{DD} input should be bypassed with local ceramic capacitors. The value of these capacitors should be chosen based on the capacitive load that is being driven.

3.5 Exposed Metal Pad

The exposed metal pad of the 6x5 DFN package is not internally connected to any potential. Therefore, this pad can be connected to a ground plane or other copper plane on a printed circuit board, to aid in heat removal from the package.

4.0 APPLICATIONS INFORMATION

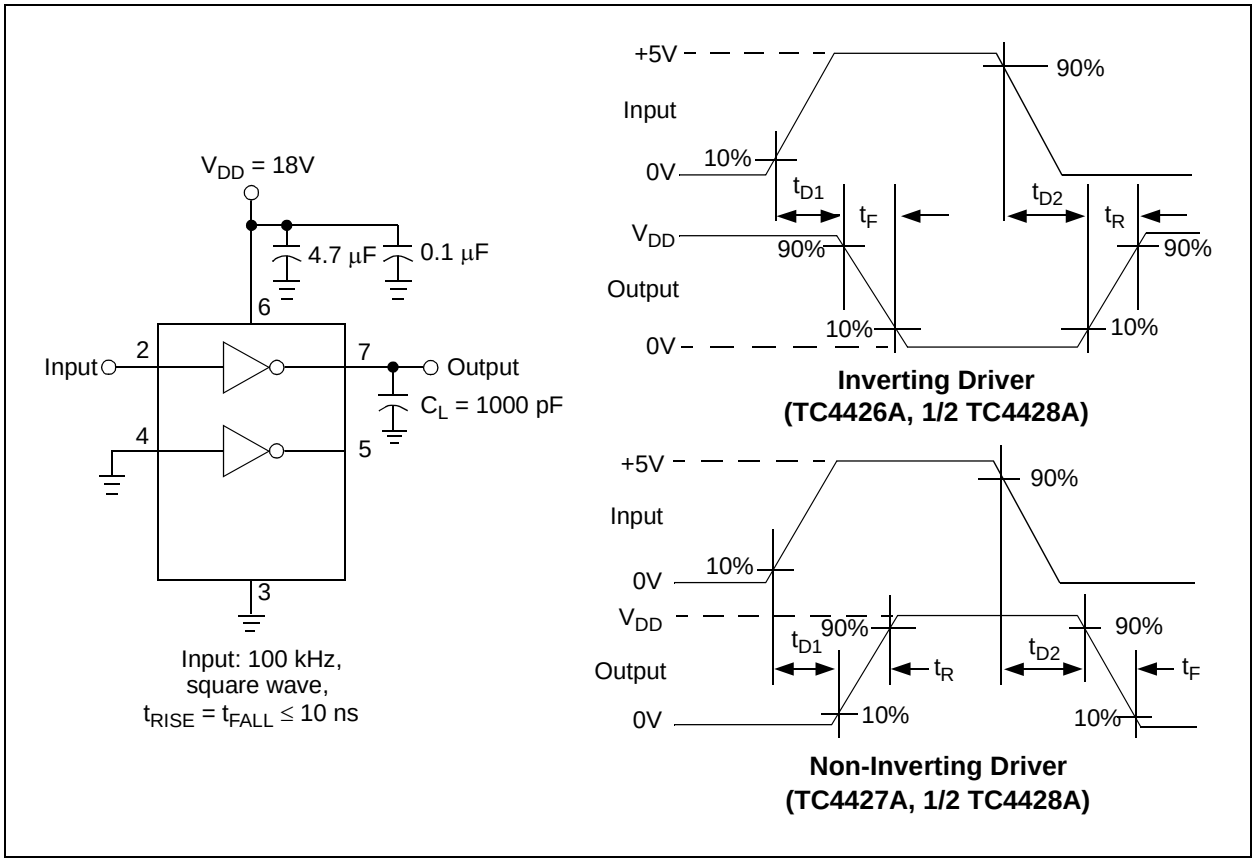
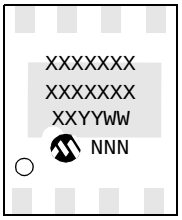


FIGURE 4-1: *Switching Time Test Circuit.*

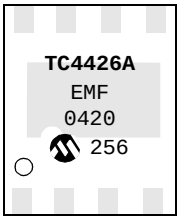
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

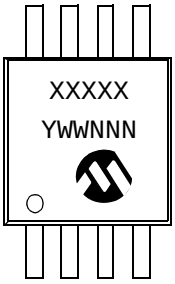
8-Lead DFN



Example:

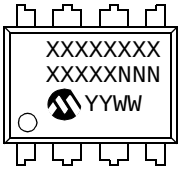


8-Lead MSOP

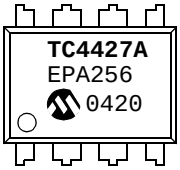


Example:

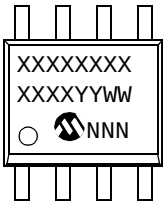
8-Lead PDIP (300 mil)



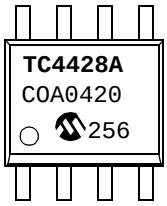
Example:



8-Lead SOIC (150 mil)



Example:

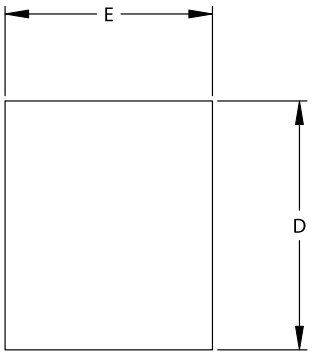


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

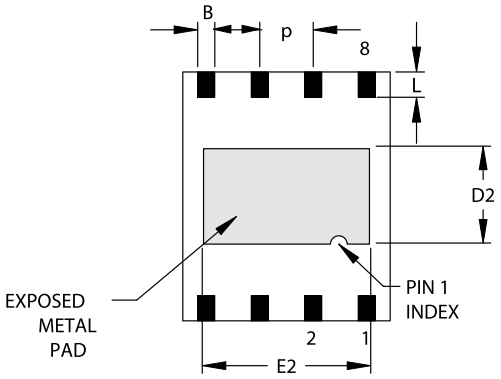
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Plastic Dual Flat No Lead Package (MF) 6x5 mm Body (DFN-S) – Saw Singulated

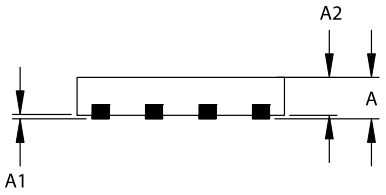
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

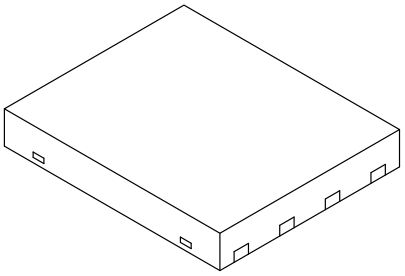


TOP VIEW



BOTTOM VIEW





Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050 BSC			1.27 BSC	
Overall Height	A	.033	.035	.037	0.85	0.90	0.95
Package Thickness	A2	.031	.035	.037	0.80	0.89	0.95
Standoff	A1	.000	.0004	.002	0.00	0.01	0.05
Base Thickness	A3	.007	.008	.009	0.17	0.20	0.23
Overall Length	E	.195	.197	.199	4.95	5.00	5.05
Exposed Pad Length	E2	.152	.157	.163	3.85	4.00	4.15
Overall Width	D	.234	.236	.238	5.95	6.00	6.05
Exposed Pad Width	D2	.089	.091	.093	2.25	2.30	2.35
Lead Width	B	.014	.016	.019	0.35	0.40	0.47
Lead Length	L	.024		.026	0.60		0.65

Notes:

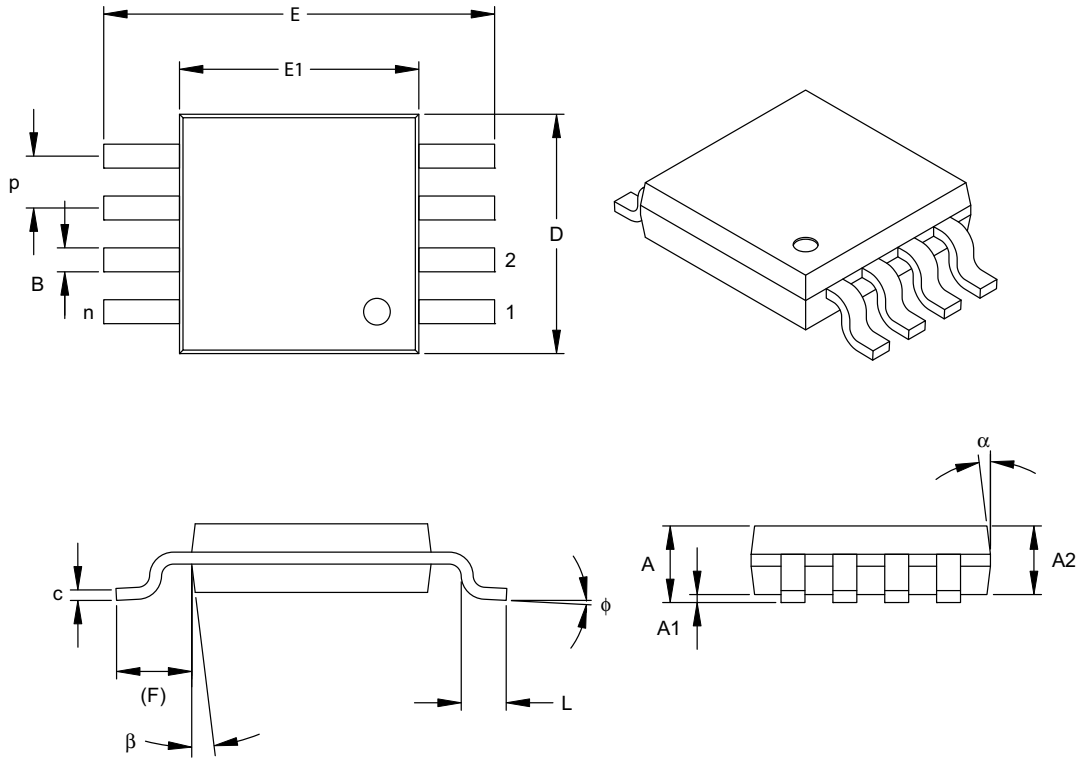
JEDEC equivalent: MO-220

Drawing No. C04-122

Revised 11/3/03

8-Lead Plastic Micro Small Outline Package (UA) (MSOP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.026 BSC			0.65 BSC	
Overall Height	A	-	-	.043	-	-	1.10
Molded Package Thickness	A2	.030	.033	.037	0.75	0.85	0.95
Standoff	A1	.000	-	.006	0.00	-	0.15
Overall Width	E		.193 TYP.			4.90 BSC	
Molded Package Width	E1		.118 BSC			3.00 BSC	
Overall Length	D		.118 BSC			3.00 BSC	
Foot Length	L	.016	.024	.031	0.40	0.60	0.80
Footprint (Reference)	F		.037 REF			0.95 REF	
Foot Angle	ϕ	0°	-	8°	0°	-	8°
Lead Thickness	c	.003	.006	.009	0.08	-	0.23
Lead Width	B	.009	.012	.016	0.22	-	0.40
Mold Draft Angle Top	α	5°	-	15°	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°	5°	-	15°

*Controlling Parameter

Notes:

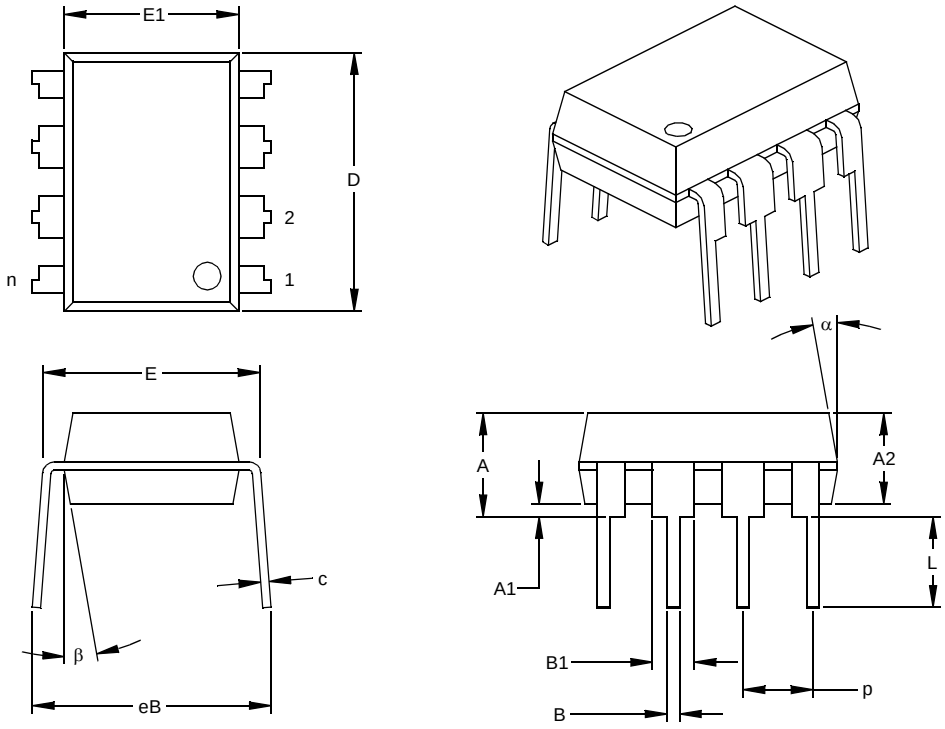
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MO-187

Drawing No. C04-111

8-Lead Plastic Dual In-line (PA) – 300 mil (PDIP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

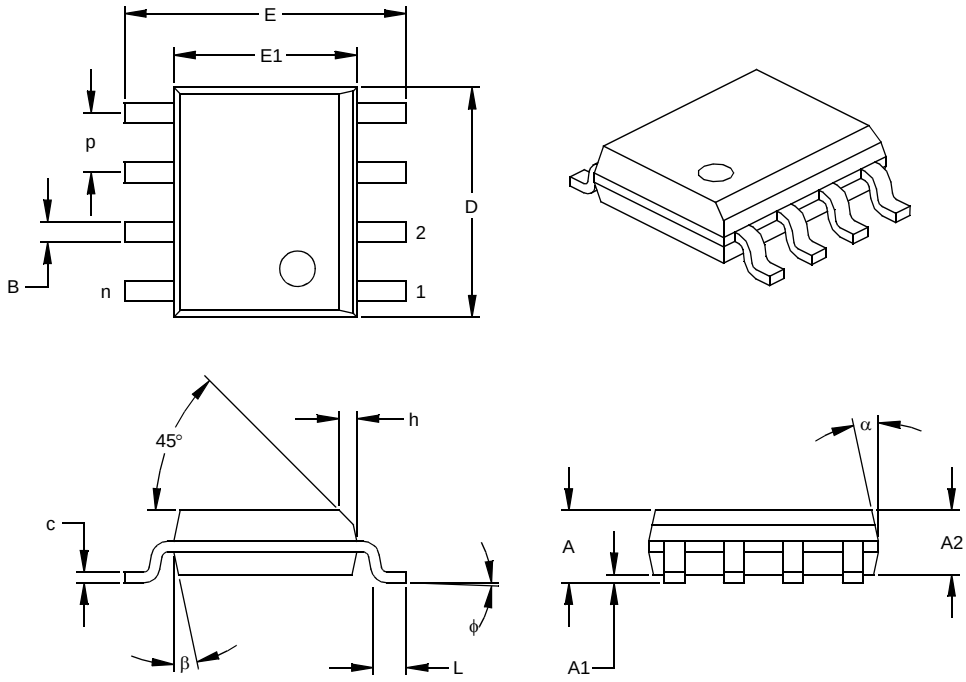


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

***** Controlling Parameter
§ Significant Characteristic
Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-018

8-Lead Plastic Small Outline (OA) – Narrow, 150 mil (SOIC)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

***** Controlling Parameter

§ Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.

JEDEC Equivalent: MS-012

Drawing No. C04-057

6.0 REVISION HISTORY

Revision G (December 2012)

Added a note to each package outline drawing.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	XX	XXX	X
Device	Temperature Range	Package	Tape & Reel	PB Free

Device:	TC4426A: 1.5A Dual MOSFET Driver, Inverting TC4427A: 1.5A Dual MOSFET Driver, Non-Inverting TC4428A: 1.5A Dual MOSFET Driver, Complementary
Temperature Range:	C = 0°C to +70°C (PDIP & SOIC Only) E = -40°C to +85°C V = -40ºC to +125°C
Package:	MF = Dual, Flat, No-Lead (6X5 mm Body), 8-lead MF713 = Dual, Flat, No-Lead (6X5 mm Body), 8-lead (Tape and Reel) PA = Plastic DIP (300 mil Body), 8-lead OA = Plastic SOIC, (150 mil Body), 8-lead OA713 = Plastic SOIC, (150 mil Body), 8-lead (Tape and Reel) UA = Plastic Micro Small Outline (MSOP), 8-lead UA713 = Plastic Micro Small Outline (MSOP), 8-lead (Tape and Reel)

Examples:

a) TC4426ACOA: 1.5A Dual Inverting MOSFET driver, 0°C to +70°C, 8LD SOIC package.

b) TC4426AEOA: 1.5A Dual Inverting MOSFET driver, -40°C to +85°C, 8LD SOIC package.

c) TC4426AEMF: 1.5A Dual Inverting MOSFET driver, -40°C to +85°C, 8LD DFN package.

a) TC4427ACPA: 1.5A Dual Non-Inverting MOSFET driver, 0°C to +70°C, 8LD PDIP package.

b) TC4427AEPA: 1.5A Dual Non-Inverting MOSFET driver, -40°C to +85°C, 8LD PDIP package.

c) TC4427AVMF713: 1.5A Dual Non-Inverting MOSFET driver, -40°C to +125°C, 8LD DFN package, Tape and Reel.

a) TC4428AEPA: 1.5A Dual Complementary MOSFET driver, -40°C to +85°C, 8LD PDIP package.

b) TC4428ACOA713: 1.5A Dual Complementary MOSFET driver, 0°C to +70°C 8LD SOIC package, Tape and Reel.

c) TC4428AVMF: 1.5A Dual Complementary MOSFET driver, -40°C to +125°C, 8LD DFN package.

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2. The Microchip Worldwide Site (www.microchip.com)

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

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