IS61VPS102436A IS61LPS102436A
IS61VPS204818A IS61LPS204818A

1Mb x 36, 2Mb x 18
36Mb SYNCHRONOUS PIPELINED, SINGLE CYCLE DESELECT STATIC RAM

JUNE 2010

FEATURES

- Internal self-timed write cycle
- Individual Byte Write Control and Global Write
- Clock controlled, registered address, data and control
- Burst sequence control using MODE input
- Three chip enable option for simple depth expansion and address pipelining
- Common data inputs and data outputs
- Auto Power-down during deselect
- Single cycle deselect
- Snooze MODE for reduced-power standby
- Power Supply

  LPS: V_{DD} 3.3V ± 5%, V_{DDQ} 3.3V/2.5V ± 5%

  VPS: V_{DD} 2.5V ± 5%, V_{DDQ} 2.5V ± 5%
- JEDEC 100-Pin TQFP and 165-ball PBGA packages
- Lead-free available

DESCRIPTION

The *ISSI* IS61LPS/VPS102436A and IS61LPS/VPS 204818A are high-speed, low-power synchronous static RAMs designed to provide burstable, high-performance memory for communication and networking applications. The IS61LPS/VPS102436A is organized as 1,048,476 words by 36 bits. The IS61LPS/VPS204818A is organized as 2M-word by 18 bits. Fabricated with *ISSI*'s advanced CMOS technology, the device integrates a 2-bit burst counter, high-speed SRAM core, and high-drive capability outputs into a single monolithic circuit. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input.

Write cycles are internally self-timed and are initiated by the rising edge of the clock input. Write cycles can be one to four bytes wide as controlled by the write control inputs.

Separate byte enables allow individual bytes to be written. The byte write operation is performed by using the byte write enable ($\overline{BWE}$) input combined with one or more individual byte write signals ($\overline{BWx}$). In addition, Global Write ($\overline{GW}$) is available for writing all bytes at one time, regardless of the byte write controls.

Bursts can be initiated with either $\overline{ADSP}$ (Address Status Processor) or $\overline{ADSC}$ (Address Status Cache Controller) input pins. Subsequent burst addresses can be generated internally and controlled by the $\overline{ADV}$ (burst address advance) input pin.

The mode pin is used to select the burst sequence order, Linear burst is achieved when this pin is tied LOW. Interleave burst is achieved when this pin is tied HIGH or left floating.

FAST ACCESS TIME

Symbol	Parameter	200	166	Units
t_{KQ}	Clock Access Time	3.1	3.5	ns
t_{KC}	Cycle Time	5	6	ns
	Frequency	200	166	MHz

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b.) the user assume all such risks; and
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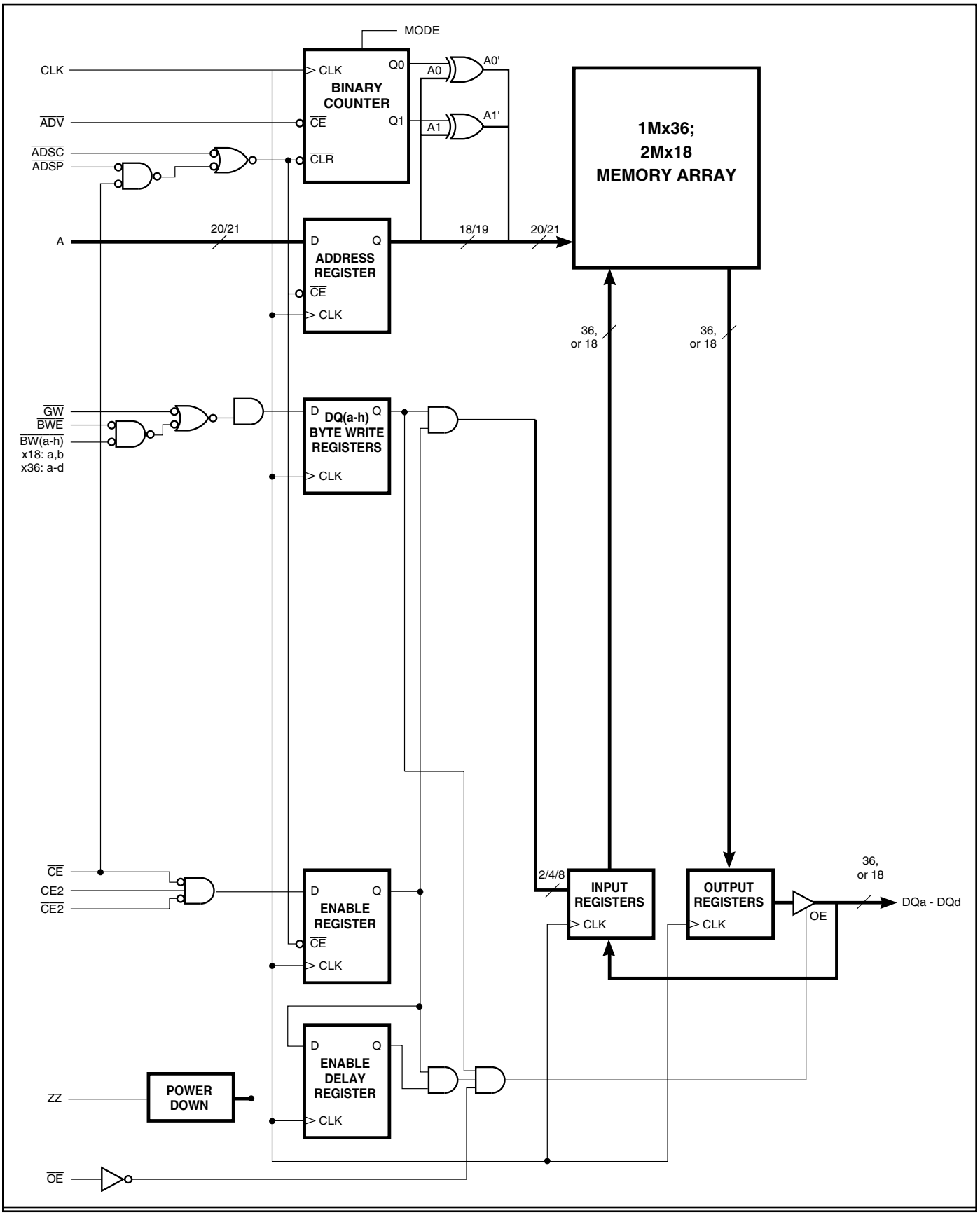
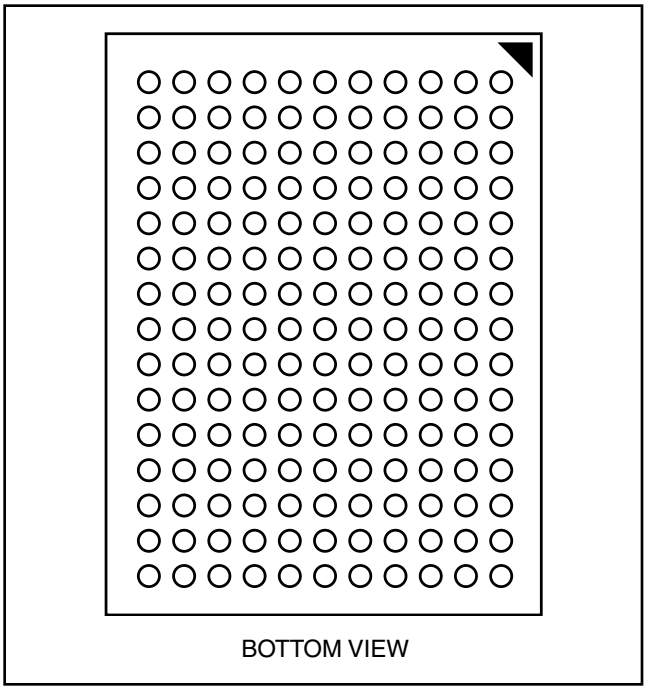
BLOCK DIAGRAM



165-PIN BGA

165-Ball, 13x15 mm BGA
1mm Ball Pitch, 11x15 Ball Array



BOTTOM VIEW

165 PBGA PACKAGE PIN CONFIGURATION

1M x 36 (TOP VIEW)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A	$\overline{CE}$	$\overline{BWc}$	$\overline{BWb}$	$\overline{CE2}$	$\overline{BWE}$	$\overline{ADSC}$	$\overline{ADV}$	A	NC
B	NC	A	CE2	$\overline{BWd}$	$\overline{BWa}$	CLK	$\overline{GW}$	$\overline{OE}$	$\overline{ADSP}$	A	NC
C	DQPc	NC	V_{DDQ}	Vss	Vss	Vss	Vss	Vss	V_{DDQ}	NC	DQPb
D	DQc	DQc	V_{DDQ}	V_{DD}	Vss	Vss	Vss	V_{DD}	V_{DDQ}	DQb	DQb
E	DQc	DQc	V_{DDQ}	V_{DD}	Vss	Vss	Vss	V_{DD}	V_{DDQ}	DQb	DQb
F	DQc	DQc	V_{DDQ}	V_{DD}	Vss	Vss	Vss	V_{DD}	V_{DDQ}	DQb	DQb
G	DQc	DQc	V_{DDQ}	V_{DD}	Vss	Vss	Vss	V_{DD}	V_{DDQ}	DQb	DQb
H	NC	NC	NC	V_{DD}	Vss	Vss	Vss	V_{DD}	NC	NC	ZZ
J	DQd	DQd	V_{DDQ}	V_{DD}	Vss	Vss	Vss	V_{DD}	V_{DDQ}	DQa	DQa
K	DQd	DQd	V_{DDQ}	V_{DD}	Vss	Vss	Vss	V_{DD}	V_{DDQ}	DQa	DQa
L	DQd	DQd	V_{DDQ}	V_{DD}	Vss	Vss	Vss	V_{DD}	V_{DDQ}	DQa	DQa
M	DQd	DQd	V_{DDQ}	V_{DD}	Vss	Vss	Vss	V_{DD}	V_{DDQ}	DQa	DQa
N	DQPd	NC	V_{DDQ}	Vss	NC	A	NC	Vss	V_{DDQ}	NC	DQPa
P	NC	NC	A	A	NC	A_1*	NC	A	A	A	A
R	MODE	A	A	A	NC	A_0*	NC	A	A	A	A

Note: * A_0 and A_1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.

PIN DESCRIPTIONS

Symbol	Pin Name
A	Address Inputs
A0, A1	Synchronous Burst Address Inputs
$\overline{ADV}$	Synchronous Burst Address Advance
$\overline{ADSP}$	Address Status Processor
$\overline{ADSC}$	Address Status Controller
$\overline{GW}$	Global Write Enable
CLK	Synchronous Clock
$\overline{CE}$, $\overline{CE2}$, CE2	Synchronous Chip Select
$\overline{BW}$x (x=a,b,c,d)	Synchronous Byte Write Controls

Symbol	Pin Name
$\overline{BWE}$	Byte Write Enable
$\overline{OE}$	Output Enable
ZZ	Power Sleep Mode
MODE	Burst Sequence Selection
NC	No Connect
DQx	Data Inputs/Outputs
DQPx	Data Inputs/Outputs
V_{DD}	3.3V/2.5V Power Supply
V_{DDQ}	Isolated Output Power Supply 3.3V/2.5V
Vss	Ground

165 PBGA PACKAGE PIN CONFIGURATION

2M x 18 (TOP VIEW)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A	$\overline{CE}$	$\overline{BWb}$	NC	$\overline{CE2}$	$\overline{BWE}$	$\overline{ADSC}$	$\overline{ADV}$	A	A
B	NC	A	CE2	NC	$\overline{BWa}$	CLK	$\overline{GW}$	$\overline{OE}$	$\overline{ADSP}$	A	NC
C	NC	NC	V_{DDQ}	Vss	Vss	Vss	Vss	Vss	V_{DDQ}	NC	DQPa
D	NC	DQb	V_{DDQ}	V_{DD}	Vss	Vss	Vss	V_{DD}	V_{DDQ}	NC	DQa
E	NC	DQb	V_{DDQ}	V_{DD}	Vss	Vss	Vss	V_{DD}	V_{DDQ}	NC	DQa
F	NC	DQb	V_{DDQ}	V_{DD}	Vss	Vss	Vss	V_{DD}	V_{DDQ}	NC	DQa
G	NC	DQb	V_{DDQ}	V_{DD}	Vss	Vss	Vss	V_{DD}	V_{DDQ}	NC	DQa
H	NC	NC	NC	V_{DD}	Vss	Vss	Vss	V_{DD}	NC	NC	ZZ
J	DQb	NC	V_{DDQ}	V_{DD}	Vss	Vss	Vss	V_{DD}	V_{DDQ}	DQa	NC
K	DQb	NC	V_{DDQ}	V_{DD}	Vss	Vss	Vss	V_{DD}	V_{DDQ}	DQa	NC
L	DQb	NC	V_{DDQ}	V_{DD}	Vss	Vss	Vss	V_{DD}	V_{DDQ}	DQa	NC
M	DQb	NC	V_{DDQ}	V_{DD}	Vss	Vss	Vss	V_{DD}	V_{DDQ}	DQa	NC
N	DQPb	NC	V_{DDQ}	Vss	NC	A	NC	Vss	V_{DDQ}	NC	NC
P	NC	NC	A	A	NC	A_1*	NC	A	A	A	A
R	MODE	A	A	A	NC	A_0*	NC	A	A	A	A

Note: * A_0 and A_1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.

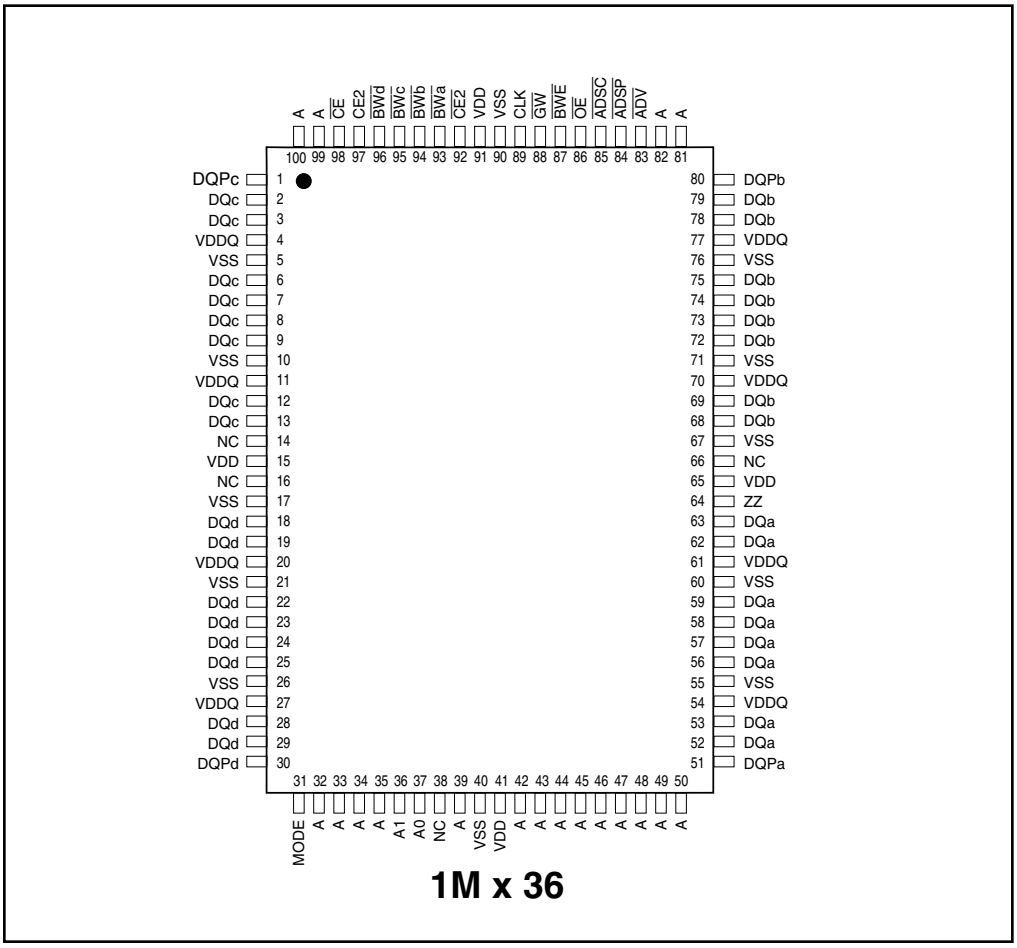
PIN DESCRIPTIONS

Symbol	Pin Name
A	Address Inputs
A0, A1	Synchronous Burst Address Inputs
$\overline{ADV}$	Synchronous Burst Address Advance
$\overline{ADSP}$	Address Status Processor
$\overline{ADSC}$	Address Status Controller
$\overline{GW}$	Global Write Enable
CLK	Synchronous Clock
$\overline{CE}$, $\overline{CE2}$, CE2	Synchronous Chip Select
$\overline{BW}$x (x=a,b)	Synchronous Byte Write Controls

Symbol	Pin Name
$\overline{BWE}$	Byte Write Enable
$\overline{OE}$	Output Enable
ZZ	Power Sleep Mode
MODE	Burst Sequence Selection
NC	No Connect
DQx	Data Inputs/Outputs
DQPx	Data Inputs/Outputs
V_{DD}	3.3V/2.5V Power Supply
V_{DDQ}	Isolated Output Power Supply 3.3V/2.5V
Vss	Ground

PIN CONFIGURATION

100-PIN TQFP



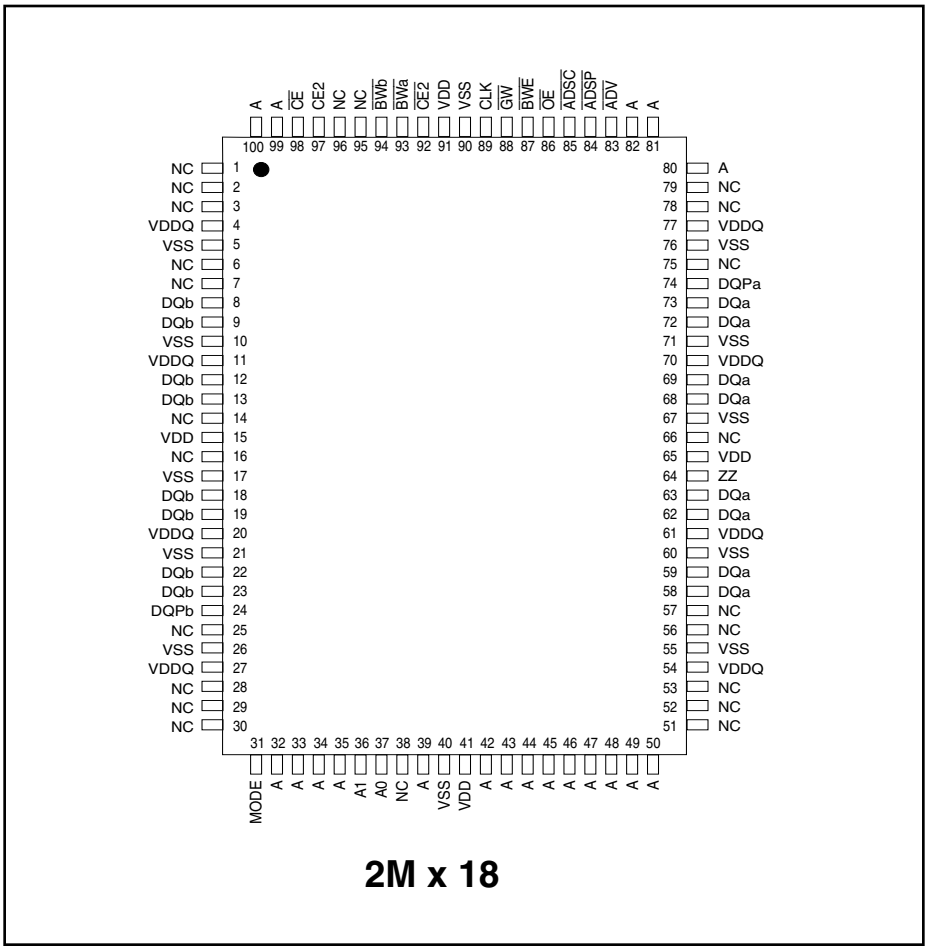
PIN DESCRIPTIONS

A0, A1	Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus.
A	Synchronous Address Inputs
$\overline{ADSC}$	Synchronous Controller Address Status
$\overline{ADSP}$	Synchronous Processor Address Status
$\overline{ADV}$	Synchronous Burst Address Advance
$\overline{BWa}$-$\overline{BWd}$	Synchronous Byte Write Enable
$\overline{BWE}$	Synchronous Byte Write Enable
$\overline{CE}$, $\overline{CE2}$, CE2	Synchronous Chip Enable
CLK	Synchronous Clock

DQa-DQd	Synchronous Data Input/Output
DQPa-DQPd	Parity Data Input/Output
$\overline{GW}$	Synchronous Global Write Enable
MODE	Burst Sequence Mode Selection
$\overline{OE}$	Output Enable
V_{DD}	3.3V/2.5V Power Supply
V_{DDQ}	Isolated Output Buffer Supply: 3.3V/2.5V
Vss	Ground
ZZ	Snooze Enable

PIN CONFIGURATION

100-PIN TQFP



2M x 18

PIN DESCRIPTIONS

A0, A1	Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus.
A	Synchronous Address Inputs
$\overline{ADSC}$	Synchronous Controller Address Status
$\overline{ADSP}$	Synchronous Processor Address Status
$\overline{ADV}$	Synchronous Burst Address Advance
$\overline{BWa}$-$\overline{BWb}$	Synchronous Byte Write Enable
$\overline{BWE}$	Synchronous Byte Write Enable
$\overline{CE}$, CE2, $\overline{CE2}$	Synchronous Chip Enable
CLK	Synchronous Clock
DQa-DQb	Synchronous Data Input/Output

DQPa-DQPb	Parity Data I/O; DQPa is parity for DQa1-8; DQPb is parity for DQb1-8
$\overline{GW}$	Synchronous Global Write Enable
MODE	Burst Sequence Mode Selection
$\overline{OE}$	Output Enable
V_{DD}	3.3V/2.5V Power Supply
V_{DDQ}	Isolated Output Buffer Supply: 3.3V/2.5V
Vss	Ground
ZZ	Snooze Enable

TRUTH TABLE[1-8] (3CE option)

OPERATION	ADDRESS	$\overline{CE}$	$\overline{CE2}$	CE2	ZZ	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselect Cycle, Power-Down	None	H	X	X	L	X	L	X	X	X	L-H	High-Z
Deselect Cycle, Power-Down	None	L	X	L	L	L	X	X	X	X	L-H	High-Z
Deselect Cycle, Power-Down	None	L	H	X	L	L	X	X	X	X	L-H	High-Z
Deselect Cycle, Power-Down	None	L	X	L	L	H	L	X	X	X	L-H	High-Z
Deselect Cycle, Power-Down	None	L	H	X	L	H	L	X	X	X	L-H	High-Z
Snooze Mode, Power-Down	None	X	X	X	H	X	X	X	X	X	X	High-Z
Read Cycle, Begin Burst	External	L	L	H	L	L	X	X	X	L	L-H	Q
Read Cycle, Begin Burst	External	L	L	H	L	L	X	X	X	H	L-H	High-Z
Write Cycle, Begin Burst	External	L	L	H	L	H	L	X	L	X	L-H	D
Read Cycle, Begin Burst	External	L	L	H	L	H	L	X	H	L	L-H	Q
Read Cycle, Begin Burst	External	L	L	H	L	H	L	X	H	H	L-H	High-Z
Read Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	L	L-H	Q
Read Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	H	L-H	High-Z
Read Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	L	L-H	Q
Read Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	H	L-H	High-Z
Write Cycle, Continue Burst	Next	X	X	X	L	H	H	L	L	X	L-H	D
Write Cycle, Continue Burst	Next	H	X	X	L	X	H	L	L	X	L-H	D
Read Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	L	L-H	Q
Read Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	H	L-H	High-Z
Read Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	L	L-H	Q
Read Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	H	L-H	High-Z
Write Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	L	X	L-H	D
Write Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	L	X	L-H	D

NOTE:

1. X means "Don't Care." H means logic HIGH. L means logic LOW.
2. For $\overline{WRITE}$, L means one or more byte write enable signals ($\overline{BWa-h}$) and $\overline{BWE}$ are LOW or $\overline{GW}$ is LOW. $\overline{WRITE}$ = H for all $\overline{BWx}$, $\overline{BWE}$, $\overline{GW}$ HIGH.
3. $\overline{BWa}$ enables WRITEs to DQa's and DQPa. $\overline{BWb}$ enables WRITEs to DQb's and DQPb. $\overline{BWc}$ enables WRITEs to DQc's and DQPc. $\overline{BWd}$ enables WRITEs to DQd's and DQPd. DQPa-DQPd are available on the x36 version.
4. All inputs except $\overline{OE}$ and ZZ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
5. Wait states are inserted by suspending burst.
6. For a WRITE operation following a READ operation, $\overline{OE}$ must be HIGH before the input data setup time and held HIGH during the input data hold time.
7. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
8. $\overline{ADSP}$ LOW always initiates an internal READ at the L-H edge of CLK. A WRITE is performed by setting one or more byte write enable signals and $\overline{BWE}$ LOW or $\overline{GW}$ LOW for the subsequent L-H edge of CLK. See WRITE timing diagram for clarification.

TRUTH TABLE[1-8] (1CE option)

NEXT CYCLE	ADDRESS	$\overline{CE}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	DQ
Deselected	None	H	X	L	X	X	X	High-Z
Read, Begin Burst	External	L	L	X	X	X	L	Q
Read, Begin Burst	External	L	L	X	X	X	H	High-Z
Write, Begin Burst	External	L	H	L	X	L	X	D
Read, Begin Burst	External	L	H	L	X	H	L	Q
Read, Begin Burst	External	L	H	L	X	H	H	High-Z
Read, Continue Burst	Next	X	H	H	L	H	L	Q
Read, Continue Burst	Next	X	H	H	L	H	H	High-Z
Read, Continue Burst	Next	H	X	H	L	H	L	Q
Read, Continue Burst	Next	H	X	H	L	H	H	High-Z
Write, Continue Burst	Next	X	H	H	L	L	X	D
Write, Continue Burst	Next	H	X	H	L	L	X	D
Read, Suspend Burst	Current	X	H	H	H	H	L	Q
Read, Suspend Burst	Current	X	H	H	H	H	H	High-Z
Read, Suspend Burst	Current	H	X	H	H	H	L	Q
Read, Suspend Burst	Current	H	X	H	H	H	H	High-Z
Write, Suspend Burst	Current	X	H	H	H	L	X	D
Write, Suspend Burst	Current	H	X	H	H	L	X	D

NOTE:
1. X means "Don't Care." H means logic HIGH. L means logic LOW.
2. For $\overline{WRITE}$, L means one or more byte write enable signals ($\overline{BWa}$-h) and $\overline{BWE}$ are LOW or $\overline{GW}$ is LOW. $\overline{WRITE}$ = H for all $\overline{BWx}$, $\overline{BWE}$, $\overline{GW}$ HIGH.
3. $\overline{BWa}$ enables WRITEs to DQa's and DQPa. $\overline{BWb}$ enables WRITEs to DQb's and DQPb. $\overline{BWc}$ enables WRITEs to DQc's and DQPc. $\overline{BWd}$ enables WRITEs to DQd's and DQPd. DQPa-DQPd are available on the x36 version.
4. All inputs except $\overline{OE}$ and ZZ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
5. Wait states are inserted by suspending burst.
6. For a WRITE operation following a READ operation, $\overline{OE}$ must be HIGH before the input data setup time and held HIGH during the input data hold time.
7. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
8. $\overline{ADSP}$ LOW always initiates an internal READ at the L-H edge of CLK. A WRITE is performed by setting one or more byte write enable signals and $\overline{BWE}$ LOW or $\overline{GW}$ LOW for the subsequent L-H edge of CLK. See WRITE timing diagram for clarification.

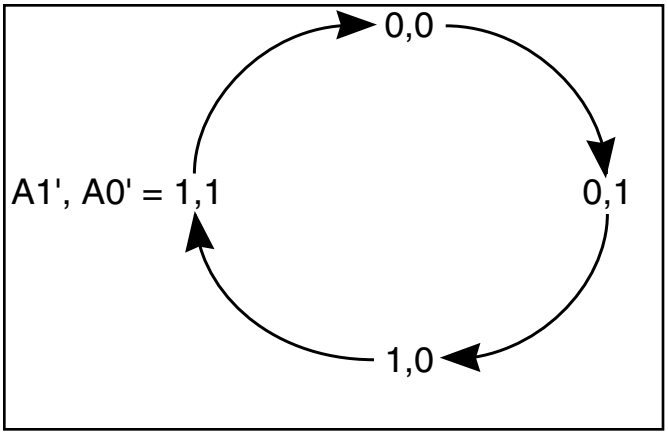
PARTIAL TRUTH TABLE

Function	$\overline{GW}$	$\overline{BWE}$	$\overline{BWa}$	$\overline{BWb}$	$\overline{BWc}$	$\overline{BWd}$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write Byte 1	H	L	L	H	H	H
Write All Bytes	H	L	L	L	L	L
Write All Bytes	L	X	X	X	X	X

INTERLEAVED BURST ADDRESS TABLE (MODE = V_{DD} or No Connect)

External Address A1 A0	1st Burst Address A1 A0	2nd Burst Address A1 A0	3rd Burst Address A1 A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

LINEAR BURST ADDRESS TABLE (MODE = VSS)



ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–55 to +150	°C
P_D	Power Dissipation	1.6	W
I_{OUT}	Output Current (per I/O)	100	mA
V_{IN}, V_{OUT}	Voltage Relative to Vss for I/O Pins	–0.5 to V_{DDQ} + 0.5	V
V_{IN}	Voltage Relative to Vss for for Address and Control Inputs	–0.5 to V_{DD} + 0.5	V
V_{DD}	Voltage on V_{DD} Supply Relative to Vss	–0.5 to 4.6	V

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. This device contains circuity to protect the inputs against damage due to high static voltages or electric fields; however, precautions may be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.
3. This device contains circuitry that will ensure the output devices are in High-Z at power up.

OPERATING RANGE (IS61LPSXXXXX)

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Commercial	0°C to +70°C	3.3V ± 5%	3.3V / 2.5V ± 5%
Industrial	–40°C to +85°C	3.3V ± 5%	3.3V / 2.5V ± 5%

OPERATING RANGE (IS61VPSXXXXX)

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Commercial	0°C to +70°C	2.5V ± 5%	2.5V ± 5%
Industrial	–40°C to +85°C	2.5V ± 5%	2.5V ± 5%

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

			3.3V		2.5V		
Symbol	Parameter	Test Conditions	Min.	Max.	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –4.0 mA (3.3V) I_{OH} = –1.0 mA (2.5V)	2.4	—	2.0	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 8.0 mA (3.3V) I_{OL} = 1.0 mA (2.5V)	—	0.4	—	0.4	V
V_{IH}	Input HIGH Voltage		2.0	V_{DD} + 0.3	1.7	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage		-0.3	0.8	-0.3	0.7	V
I_{LI}	Input Leakage Current	$V_{SS} \le V_{IN} \le V_{DD}$(1)	-5	5	-5	5	µA
I_{LO}	Output Leakage Current	$V_{SS} \le V_{OUT} \le V_{DDQ}$, $\overline{OE} = V_{IH}$	-5	5	-5	5	µA

POWER SUPPLY CHARACTERISTICS(1) (Over Operating Range)

				-200 MAX		-166 MAX		
Symbol	Parameter	Test Conditions	Temp. range	x18	x36	x18	x36	Unit
I_{CC}	AC Operating Supply Current	Device Selected, $\overline{OE} = V_{IH}$, ZZ ≤ V_{IL}, All Inputs ≤ 0.2V or ≥ V_{DD} – 0.2V, Cycle Time ≥ t_{KC} min.	Com.	450	450	400	400	mA
			Ind.	475	475	450	450	
			typ.(2)	390		340		
I_{SB}	Standby Current TTL Input	Device Deselected, V_{DD} = Max., All Inputs ≤ V_{IL} or ≥ V_{IH}, ZZ ≤ V_{IL}, f = Max.	Com.	150	150	140	140	mA
			Ind.	160	160	150	150	
I_{SBI}	Standby Current CMOS Input	Device Deselected, V_{DD} = Max., $V_{IN} \le V_{SS}$ + 0.2V or ≥V_{DD} – 0.2V f = 0	Com.	110	110	110	110	mA
			Ind.	140	140	140	140	
			typ.(2)	75		75		

Note:

1. MODE pin has an internal pullup and should be tied to V_{DD} or V_{SS}. It exhibits ±100µA maximum leakage current when tied to ≤ V_{SS} + 0.2V or ≥ V_{DD} – 0.2V.
2. Typical values are measured at Vcc = 3.3V, T_A = 25°C and not 100% tested.

CAPACITANCE[1,2]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Input/Output Capacitance	V_{OUT} = 0V	8	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{DD} = 3.3V.

3.3V I/O AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	1.5 ns
Input and Output Timing and Reference Level	1.5V
Output Load	See Figures 1 and 2

AC TEST LOADS

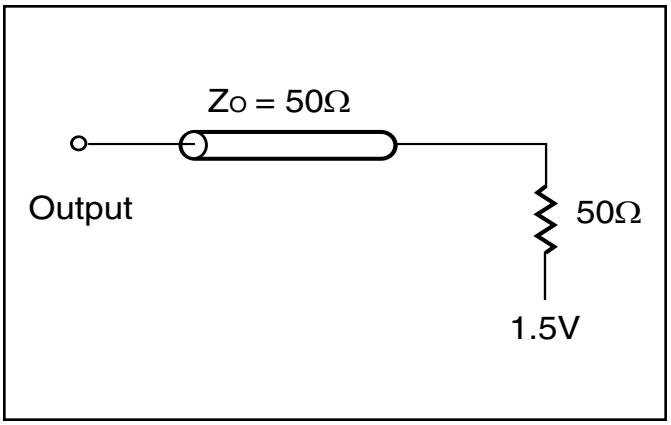


Figure 1

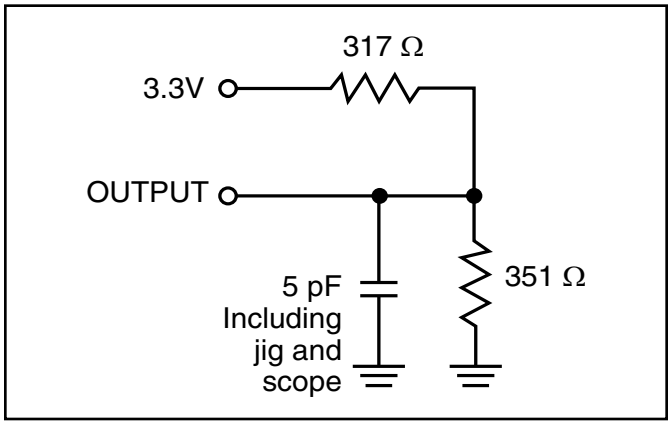


Figure 2

2.5V I/O AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 2.5V
Input Rise and Fall Times	1.5 ns
Input and Output Timing and Reference Level	1.25V
Output Load	See Figures 3 and 4

2.5 I/O OUTPUT LOAD EQUIVALENT

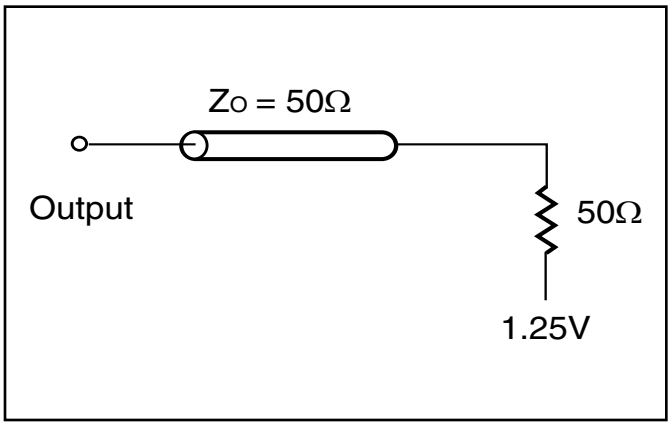


Figure 3

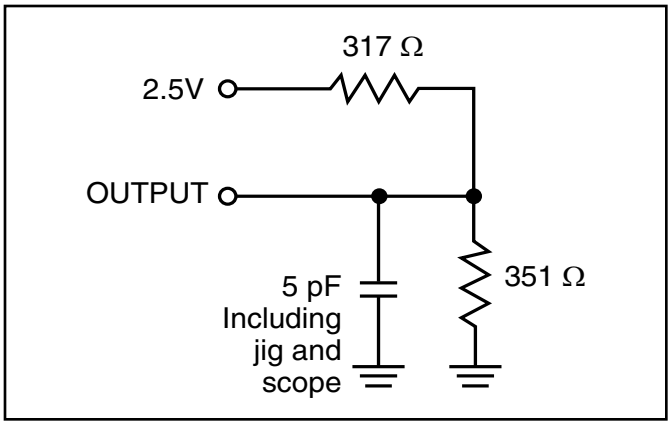


Figure 4

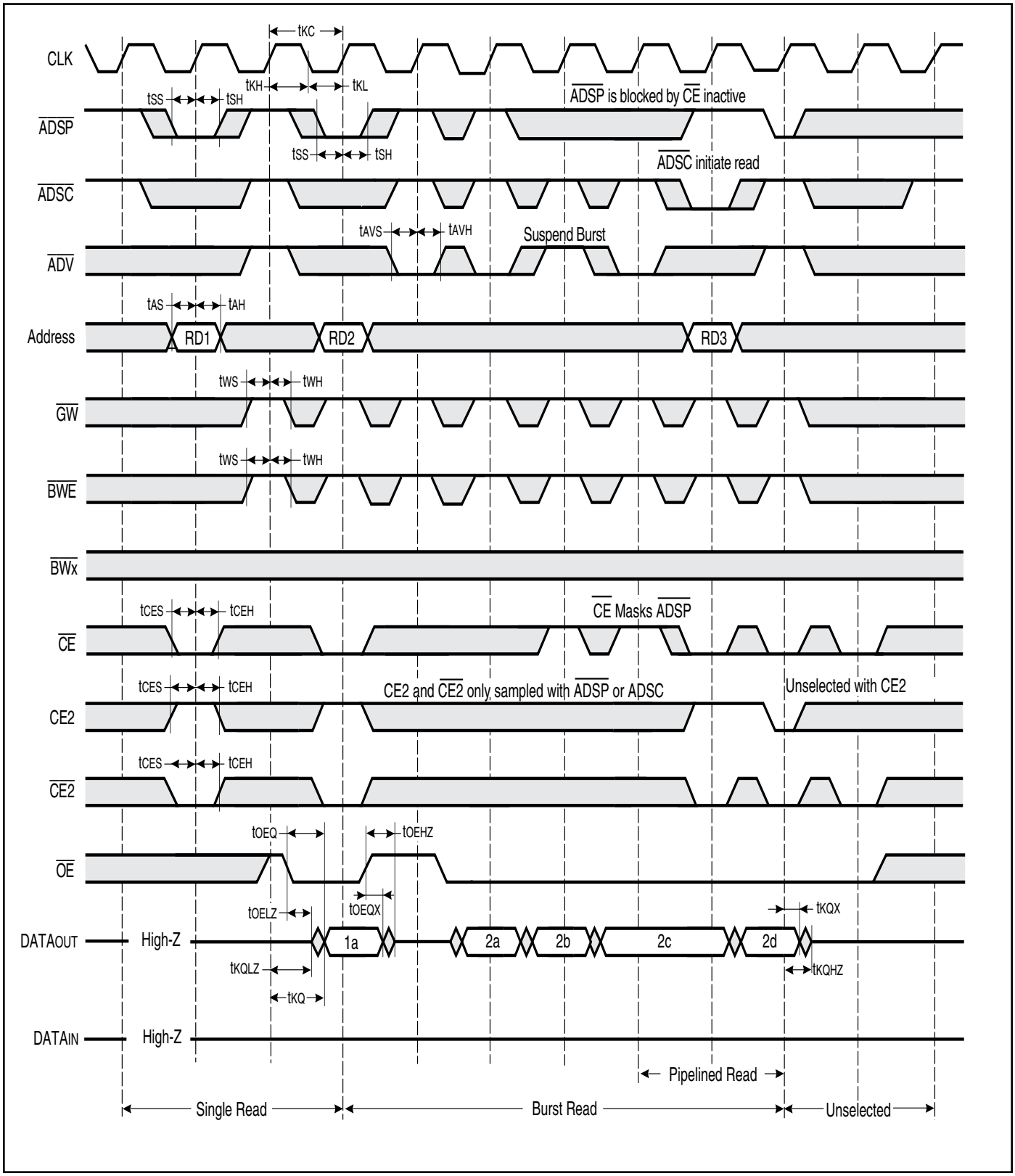
READ/WRITE CYCLE SWITCHING CHARACTERISTICS (Over Operating Range)

		-200		-166		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
f_{MAX}	Clock Frequency	—	200	—	166	MHz
t_{KC}	Cycle Time	5	—	6	—	ns
t_{KH}	Clock High Time	2	—	2.4	—	ns
t_{KL}	Clock Low Time	2	—	2.4	—	ns
t_{KQ}	Clock Access Time	—	3.1	—	3.5	ns
t_{KQX}[2]	Clock High to Output Invalid	1.5	—	1.5	—	ns
t_{KQLZ}[2,3]	Clock High to Output Low-Z	1	—	1	—	ns
t_{KQHZ}[2,3]	Clock High to Output High-Z	—	3.0	—	3.4	ns
t_{OEQ}	Output Enable to Output Valid	—	3.1	—	3.5	ns
t_{OEQX}[2]	Output Disable to Output Invalid	0	—	0	—	ns
t_{OELZ}[2,3]	Output Enable to Output Low-Z	0	—	0	—	ns
t_{OEHZ}[2,3]	Output Disable to Output High-Z	—	3.0	—	3.4	ns
t_{AS}	Address Setup Time	1.4	—	1.5	—	ns
t_{SS}	Address Status Setup Time	1.4	—	1.5	—	ns
t_{WS}	Read/Write Setup Time	1.4	—	1.5	—	ns
t_{CES}	Chip Enable Setup Time	1.4	—	1.5	—	ns
t_{AVS}	Address Advance Setup Time	1.4	—	1.5	—	ns
t_{DS}	Data Setup Time	1.4	—	1.5	—	ns
t_{AH}	Address Hold Time	0.4	—	0.5	—	ns
t_{SH}	Address Status Hold Time	0.4	—	0.3	—	ns
t_{WH}	Write Hold Time	0.4	—	0.5	—	ns
t_{CEH}	Chip Enable Hold Time	0.4	—	0.5	—	ns
t_{AVH}	Address Advance Hold Time	0.4	—	0.5	—	ns
t_{DH}	Data Hold Time	0.4	—	0.5	—	ns
t_{PDS}	ZZ High to Power Down	—	2	—	2	cyc
t_{PUS}	ZZ Low to Power Down	—	2	—	2	cyc

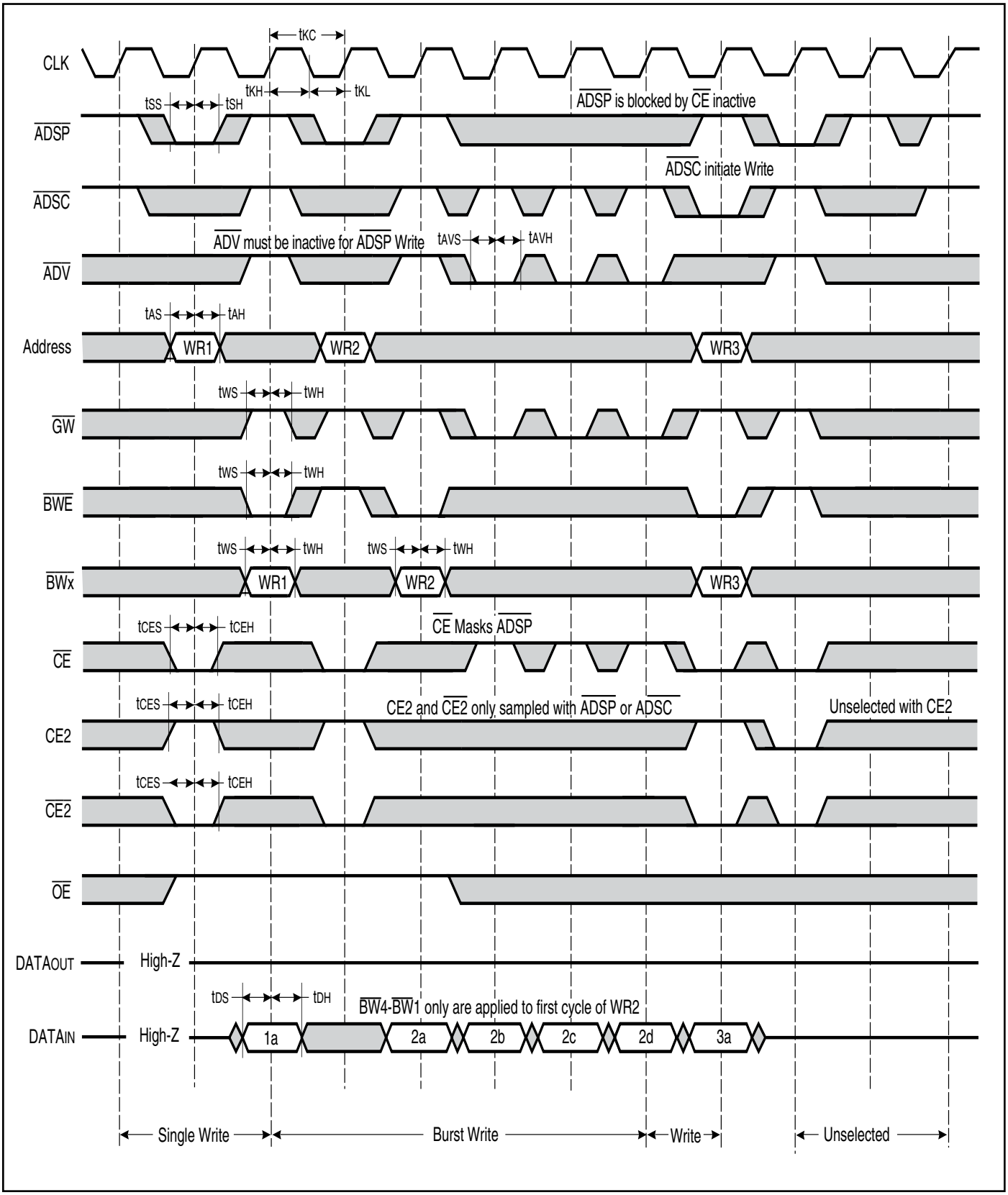
Note:

1. Configuration signal MODE is static and must not change during normal operation.
2. Guaranteed but not 100% tested. This parameter is periodically sampled.
3. Tested with load in Figure 2.

READ/WRITE CYCLE TIMING



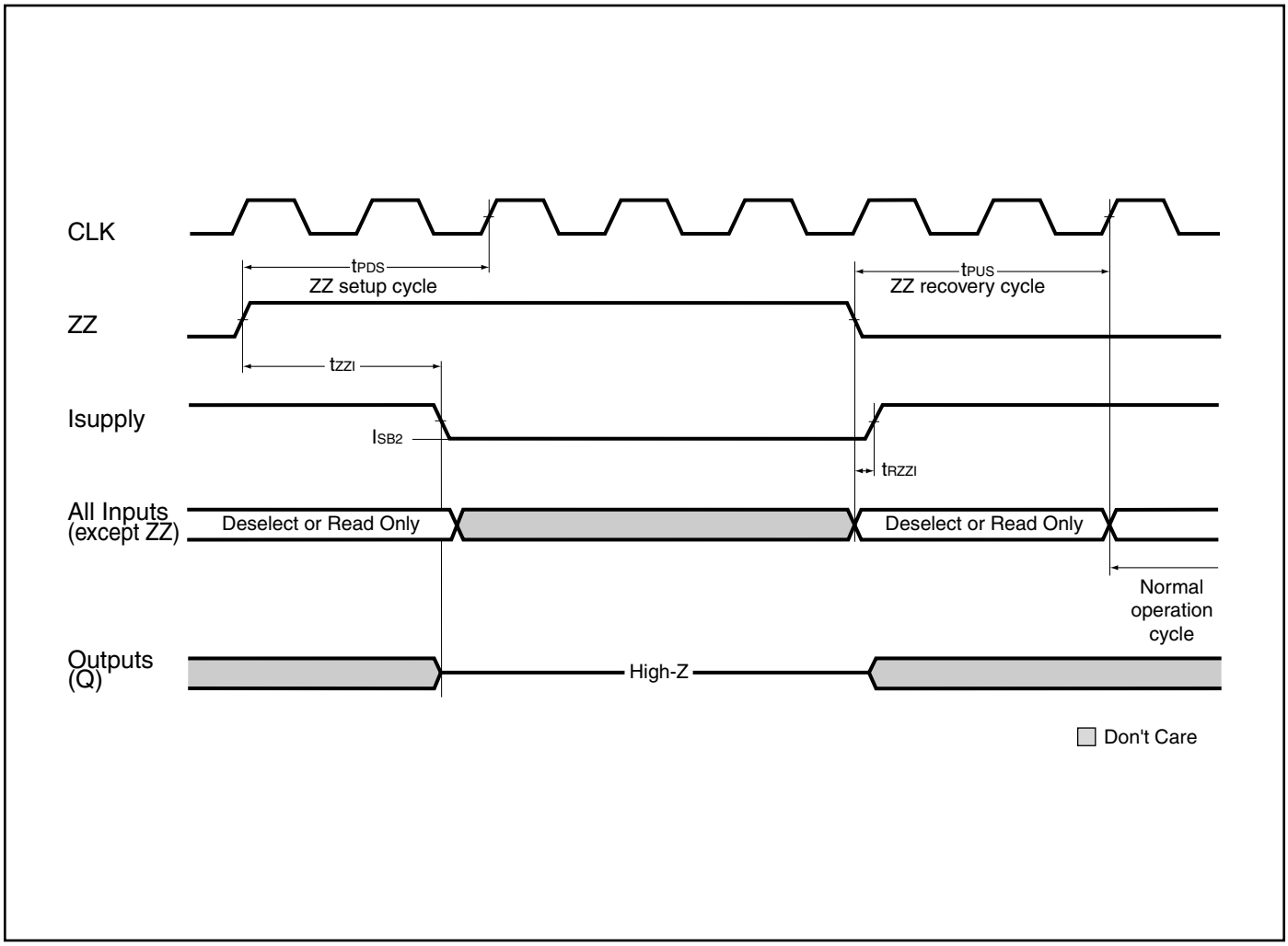
WRITE CYCLE TIMING



SNOOZE MODE ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Temperature	Conditions	Min.	Max.	Unit
I_{SB2}	Current during SNOOZE MODE	Com. Ind.	ZZ ≥ Vih	— —	60 90	mA
t_{PDS}	ZZ active to input ignored			—	2	cycle
t_{PUS}	ZZ inactive to input sampled			2	—	cycle
t_{ZZI}	ZZ active to SNOOZE current			—	2	cycle
t_{RZZI}	ZZ inactive to exit SNOOZE current			0	—	ns

SNOOZE MODE TIMING



ORDERING INFORMATION (3.3V core/2.5V-3.3V I/O)

Commercial Range: 0°C to +70°C

Configuration	Frequency	Order Part Number	Package
1Mx36			
	166	IS61LPS102436A-166TQ	100 TQFP
		IS61LPS102436A-166TQL	100 TQFP, Lead-free
		IS61LPS102436A-166B3	165 PBGA
2Mx18			
	166	IS61LPS204818A-166TQ	100 TQFP
		IS61LPS204818A-166TQL	100 TQFP, Lead-free
		IS61LPS204818A-166B3	165 PBGA

Industrial Range: -40°C to +85°C

Configuration	Frequency	Order Part Number	Package
1Mx36			
	166	IS61LPS102436A-166TQI	100 TQFP
		IS61LPS102436A-166TQLI	100 TQFP, Lead-free
		IS61LPS102436A-166B3I	165 PBGA
		IS61LPS102436A-166B3LI	165 PBGA, Lead-free
2Mx18			
	166	IS61LPS204818A-166TQI	100 TQFP
		IS61LPS204818A-166B3I	165 PBGA

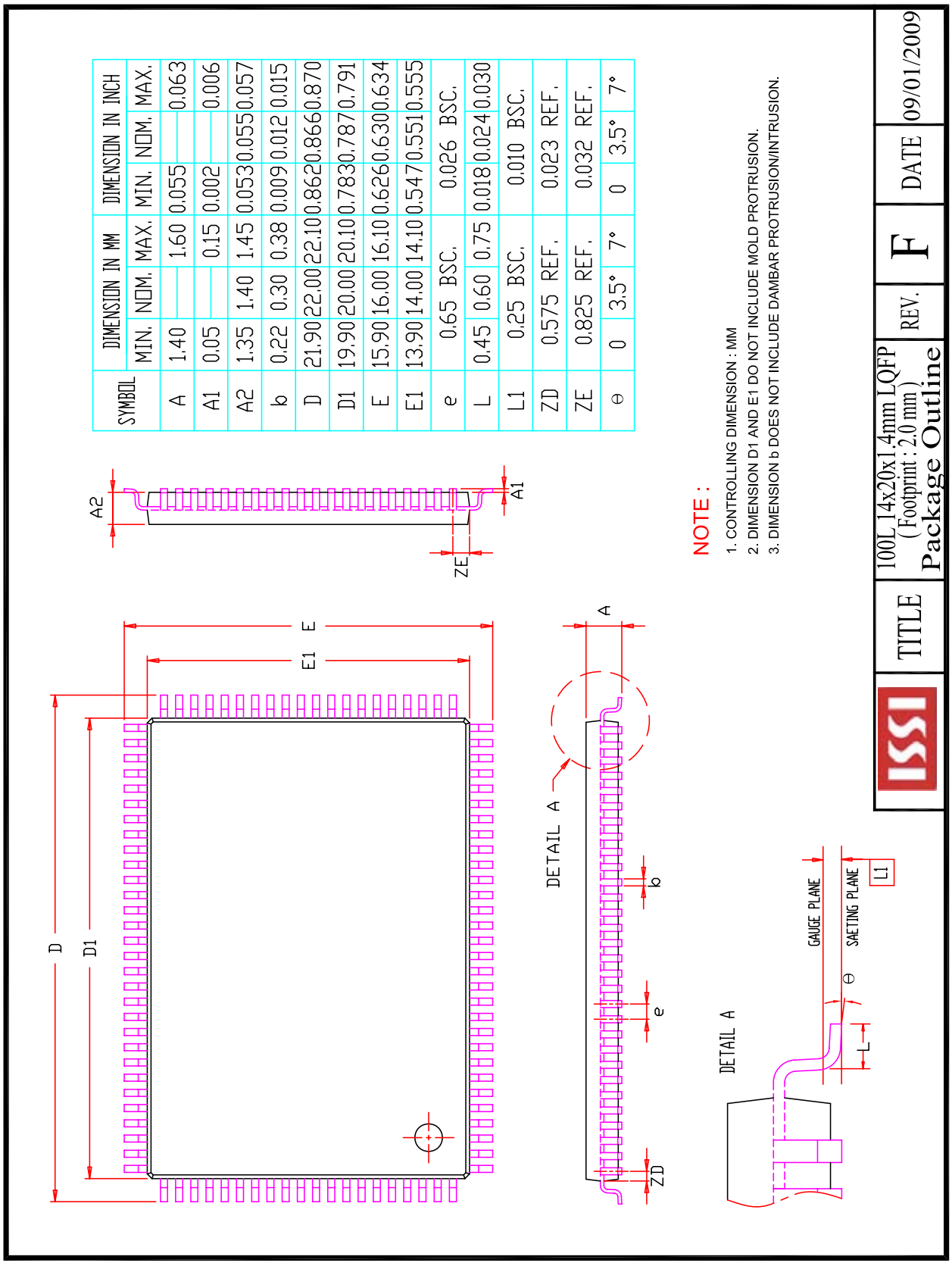
ORDERING INFORMATION (2.5V core/2.5V I/O)

Commercial Range: 0°C to +70°C

Configuration	Frequency	Order Part Number	Package
1Mx36			
	166	IS61VPS102436A-166TQ	100 TQFP
		IS61VPS102436A-166TQL	100 TQFP, Lead-free
		IS61VPS102436A-166B3	165 PBGA
2Mx18			
	166	IS61VPS204818A-166TQ	100 TQFP
		IS61VPS204818A-166TQL	100 TQFP, Lead-free
		IS61VPS204818A-166B3	165 PBGA

Industrial Range: -40°C to +85°C

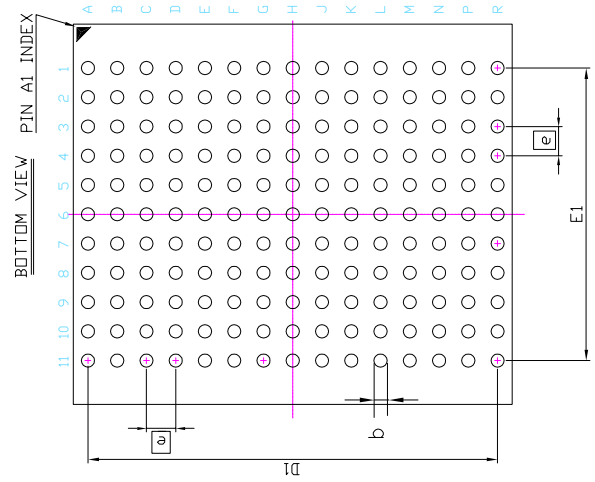
Configuration	Frequency	Order Part Number	Package
2Mx18			
	166	IS61VPS204818A-166TQI	100 TQFP
		IS61VPS204818A-166B3I	165 PBGA

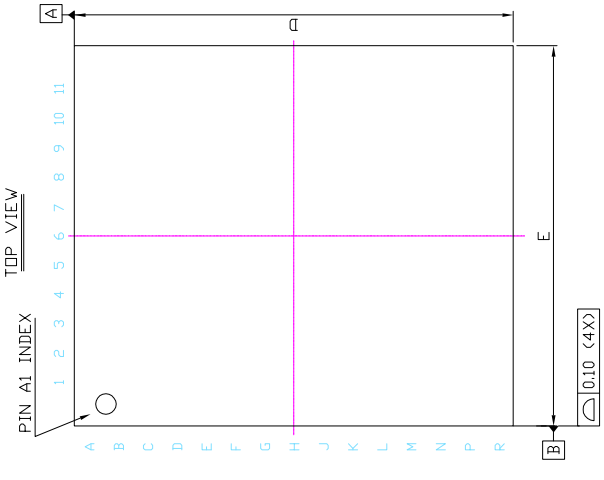

SYMBOL
DIMENSION IN MM
MIN. NOM. MAX.
DIMENSION IN INCH
MIN. NOM. MAX.
A 1.40 — 1.60 0.055 — 0.063
A1 0.05 — 0.15 0.002 — 0.006
A2 1.35 1.40 1.45 0.053 0.055 0.057
b 0.22 0.30 0.38 0.009 0.012 0.015
D 21.90 22.00 22.10 0.862 0.866 0.870
D1 19.90 20.00 20.10 0.783 0.787 0.791
E 15.90 16.00 16.10 0.626 0.630 0.634
E1 13.90 14.00 14.10 0.547 0.551 0.555
e 0.65 BSC. 0.026 BSC.
L 0.45 0.60 0.75 0.018 0.024 0.030
L1 0.25 BSC. 0.010 BSC.
ZD 0.575 REF. 0.023 REF.
ZE 0.825 REF. 0.032 REF.
θ 0 3.5° 7° 0 3.5° 7°
NOTE :
1. CONTROLLING DIMENSION : MM
2. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.
TITLE
100L 14x20x1.4mm LQFP
(Footprint : 2.0 mm)
Package Outline
REV. F
DATE 09/01/2009
280-600-011 REV. A
A2
A1
ZE
D
D1
E
E1
DETAIL A
A
b
e
ZD
GAUGE PLANE
SEATING PLANE
θ
L
L1

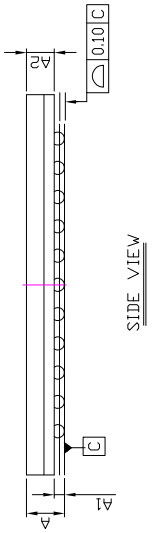
SYM.	DIMENSION (mm)			DIMENSION (inch)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A1	0.25	0.35	0.40	0.010	0.014	0.016
A2	—	0.79	—	—	0.031	—
b	0.40	0.45	0.50	0.016	0.018	0.020
D	14.90	15.00	15.10	0.587	0.591	0.594
D1	13.90	14.00	14.10	0.547	0.551	0.555
E	12.90	13.00	13.10	0.508	0.512	0.516
E1	9.90	10.00	10.10	0.390	0.394	0.398
e	1.00 BSC			0.039 BSC		

NOTE :

1. CONTROLLING DIMENSION : MM .







ISSI	TITLE	165L 13x15mm TF-BGA Package Outline	REV.	B	DATE	08/28/2008

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