FP31QF

2-Watt HFET

The Communications Edge ™

Product Information

Product Features

- 50 – 4000 MHz
- 18 dB Gain @ 900 MHz
- +34 dBm P1dB
- +46 dBm Output IP3
- High Drain Efficiency
- Lead free/RoHS-compliant 6mm 28-pin QFN package
- MTTF > 100 years

Applications

- Mobile Infrastructure
- CATV / DBS
- W-LAN / ISM
- RFID
- Defense / Homeland Security
- Fixed Wireless

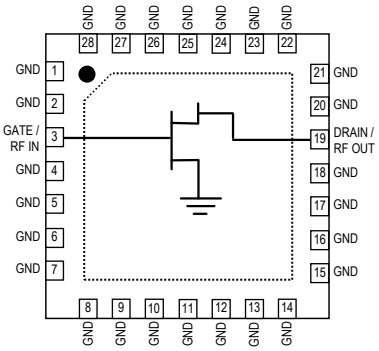
Product Description

The FP31QF is a high performance 2-Watt HFET (Heterostructure FET) in a low-cost lead-free/RoHS-compliant 28-pin 6x6 mm QFN (Quad Flatpack, No-Lead) surface-mount package. This device works optimally at a drain bias of +9 V and 450 mA to achieve +46 dBm output IP3 performance and an output power of +34 dBm at 1-dB compression.

The device conforms to WJ Communications' long history of producing high reliability and quality components. The FP31QF has an associated MTTF of a minimum of 100 years at a mounting temperature of 85 °C. All devices are 100% RF & DC tested.

The product is targeted for use as driver amplifiers for wireless infrastructure where high performance and high efficiency are required.

Functional Diagram



Function	Pin No.
Gate / RF Input	3
Drain / RF Output	19
Ground	All other pins & backside copper

Specifications

DC Parameter	Units	Min	Typ	Max
Saturated Drain Current, I_{dss}	mA		1170	
Transconductance, G_m	mS		590	
Pinch Off Voltage, V_p (1)	V		-2.0	

RF Parameter (2)	Units	Min	Typ	Max
Operational Bandwidth	MHz	50		4000
Test Frequency	MHz		800	
Small Signal Gain	dB		18	
Maximum Stable Gain	dB		24	
Output P1dB	dBm		+34	
Output IP3 (3)	dBm		+46	
Noise Figure	dB		3.5	

1. Pinch-off voltage is measured when I_{ds} = 4.8 mA.
2. Test conditions unless otherwise noted: T = 25 °C, V_{DS} = 9 V, I_{DQ} = 450 mA, in a tuned application circuit with $Z_L = Z_{LOPT}$, $Z_S = Z_{SOPT}$ (optimized for output power).
3. 3OIP measured with two tones at an output power of +18 dBm/tone separated by 1 MHz. The suppression on the largest IM3 product is used to calculate the 3OIP using a 2:1 rule.

Typical Performance (4)

Parameter	Units	Typical			
Frequency	MHz	915	1960	2140	2450
Gain	dB	18	13.5	13	12
S11	dB	-20	-20	-18	-18
S22	dB	-12	-11	-24	-15
Output P1dB	dBm	+34	+33.8	+33.2	+33.5
Output IP3 (3)	dBm	+46	+46.8	+46.6	+46.8
Noise Figure	dB	3.5	4.5	4.6	4.6
IS-95 Channel Power @ -45 dBc ACPR	dBm	+27.8	+27.3		
W-CDMA Ch. Power @ -45 dBc ACLR	dBm			+25	
Drain Voltage (5)	V	+9			
Drain Current (5)	mA	450			

4. Typical parameters represent performance in an application circuit.
5. Empirical measurements showed optimal power performance at a drain voltage = 9 volts at 450 mA. Because the FP31QF is a discrete device, users can choose their own bias configuration. Performance may vary from the data shown depending on the biasing conditions. To achieve a minimum 1 million hours MTTF rating, the biasing condition should maintain a junction temperature below 160 °C over all operating temperatures. This can be approximated by (drain voltage) x (drain current) x 17.5 °C/W + (maximum operating temperature).

Absolute Maximum Rating

Parameter	Rating
Operating Case Temperature	-40 to +85 °C
Storage Temperature	-55 to +125 °C
DC Power	7.5 W
RF Input Power (continuous)	6 dB above Input P1dB
Drain to Gate Voltage, V_{dg}	+16 V
Junction Temperature	+220 °C

Operation of this device above any of these parameters may cause permanent damage.

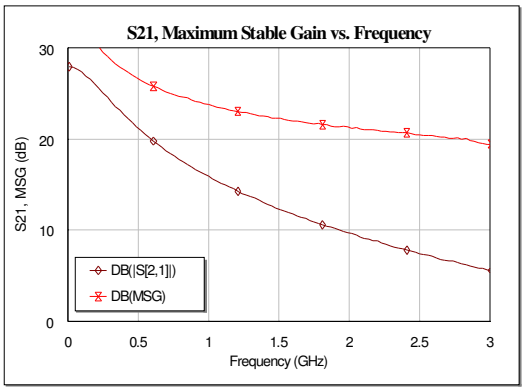
Ordering Information

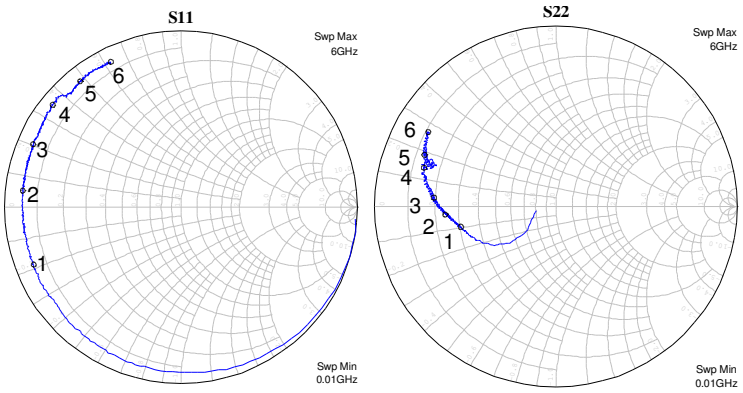
Part No.	Description
FP31QF-F	2-Watt HFET (lead-free/RoHS-compliant 6mm QFN package)
FP31QF-PCB900	870 – 960 MHz Application Circuit
FP31QF-PCB1900	1930 – 1990 MHz Application Circuit
FP31QF-PCB2140	2110 – 2170 MHz Application Circuit

Specifications and information are subject to change without notice

Typical Device Data

S-Parameters (V_{DS} = +9 V, I_{DS} = 450 mA, T = 25 °C, calibrated to device leads)





Note:
Measurements were made on the packaged device in a test fixture with 50 ohm input and output lines.
The S-parameters shown are the de-embedded data down to the device leads and represents typical performance of the device.

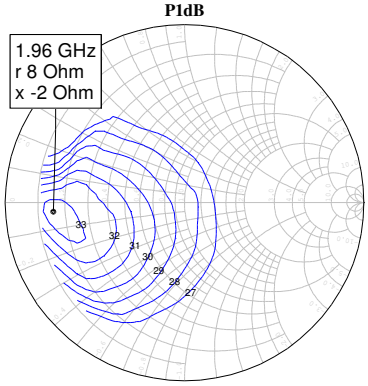
Freq (MHz)	S11 (mag)	S11 (ang)	S21 (mag)	S21 (ang)	S12 (mag)	S12 (ang)	S22 (mag)	S22 (ang)
50	0.985	-21.82	24.458	166.25	0.006	76.01	0.096	-110.34
250	0.936	-88.63	17.968	128.52	0.020	43.34	0.329	-135.13
500	0.913	-128.61	11.520	104.42	0.025	22.03	0.431	-151.01
750	0.899	-148.43	8.132	90.03	0.026	10.75	0.465	-158.3
1000	0.900	-160.54	6.225	79.35	0.026	4.56	0.490	-162.14
1250	0.900	-169.15	4.988	70.50	0.025	0.35	0.514	-163.92
1500	0.900	-176.01	4.125	62.56	0.025	-2.975	0.532	-166.86
1750	0.905	178.53	3.504	55.28	0.024	-4.91	0.560	-168.72
2000	0.909	172.99	3.046	47.93	0.023	-5.54	0.587	-170.95
2250	0.910	168.27	2.656	41.65	0.022	-4.44	0.606	-172.86
2500	0.914	164.14	2.349	34.95	0.021	-1.12	0.629	-175.13
2750	0.914	160.09	2.117	28.98	0.021	5.24	0.656	-177.13
3000	0.915	156.76	1.897	23.31	0.022	12.75	0.671	-179.41
3250	0.922	153.22	1.721	17.69	0.026	23.36	0.695	177.36
3500	0.926	149.22	1.563	11.97	0.034	32.54	0.720	175.05
3750	0.941	144.67	1.433	6.20	0.058	34.08	0.734	171.21
4000	0.943	140.45	1.318	0.98	0.102	23.74	0.768	165.82

Device S-parameters are available for download off of the website at: http://www.wj.com

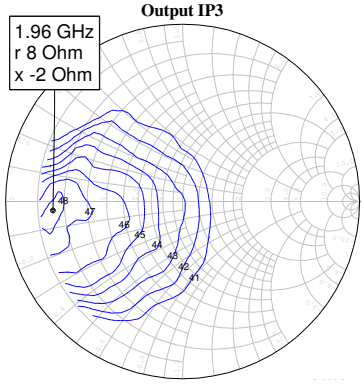
Load-Pull Data at 1.96 and 2.14 GHz

(V_{ds} = 8 V, I_{ds} = 500 mA, 25 °C, Z_S = 50 Ω, calibrated to device pins)

Freq (GHz)	ZS (Ω)	ZL (Ω)	Gain (dB)	P1dB (dBm)	OIP3 (dBm)	PAE (%)
1.96	5 + j0	8 - j2	18.5	+34	+48	49
2.14	5 - j2	8 - j3	18.0	+34	+48	50



P1dB max (1.96 GHz) = +34 dBm at Z_L = 8 - j2 Ω



OIP3 max (1.96 GHz) = +48 dBm at Z_L = 8 - j2 Ω

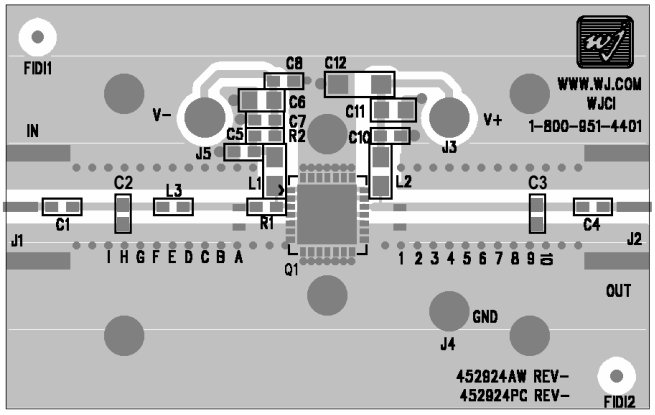
Application Circuit: 870 – 960 MHz (FP31QF-PCB900)

The application circuit is matched for output power.

Typical RF Performance

Drain Bias = +9 V, I_{ds} = 450 mA, 25 °C

Frequency	MHz	870	915	960
S21 – Gain	dB	18.3	18	17.7
S11 – Input Return Loss	dB	-15	-20	-16
S22 – Output Return Loss	dB	-9.3	-12	-16
Output P1dB	dBm	+33.9	+34	+33.7
Output IP3 (+18 dBm / tone, 1 MHz spacing)	dBm		+46	
Noise Figure	dB	3.4	3.5	3.5
IS-95 Channel Power @ -45 dBc ACPR	dBm		+27.8	

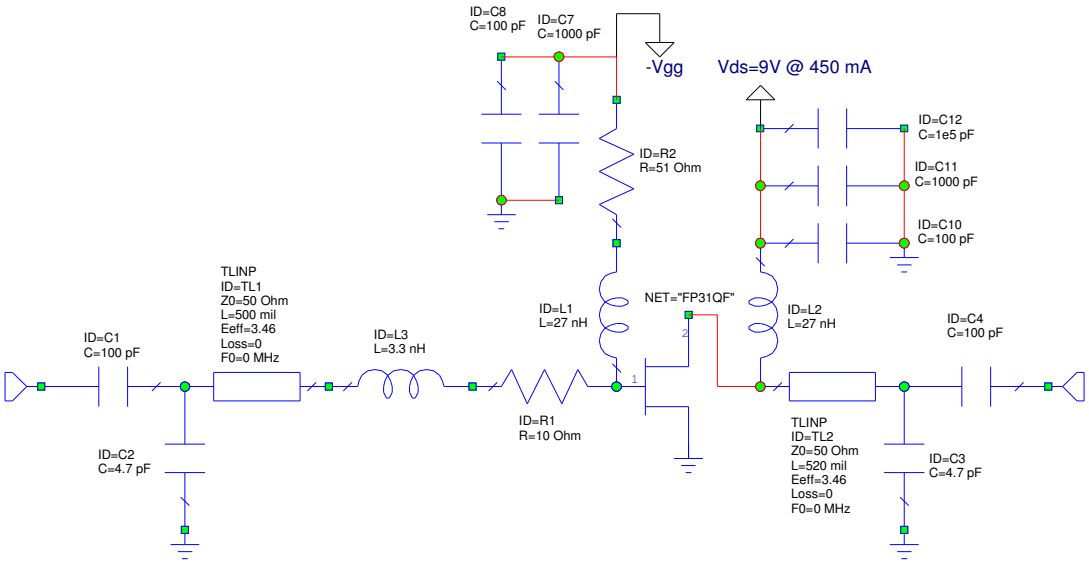


Circuit Board Material: .014" FR-4 (ε_r = 4.6),
4 layers (other layers added for rigidity), .062" total thickness, 1 oz copper
The main microstrip line has a line impedance of 50 Ω.

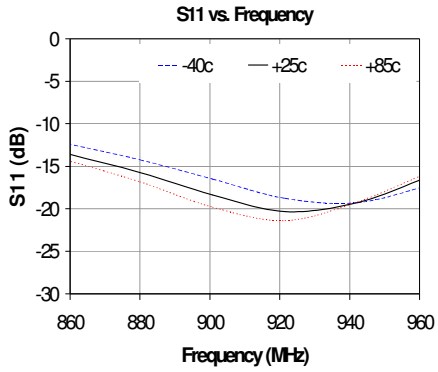
Bill of Materials

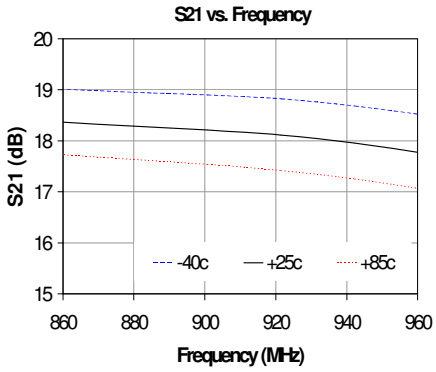
Ref. Desig.	Value	Part style	Size
C1, C4, C8, C10	100 pF	Chip capacitor	0603
C2, C3	4.7 pF	Chip capacitor	0603
C7, C11	1000 pF	Chip capacitor	0603
C12	0.1 µF	Chip capacitor	1206
L1, L2	27 nH	Wirewound chip inductor	0805
L3	3.3 nH	Multilayer chip inductor	0603
R1	10 Ω	Chip resistor	0603
R2	51 Ω	Chip resistor	0603
Q1	FP31QF	WJ 2W HFET	QFN 6x6
C5, C6		Do Not Place	

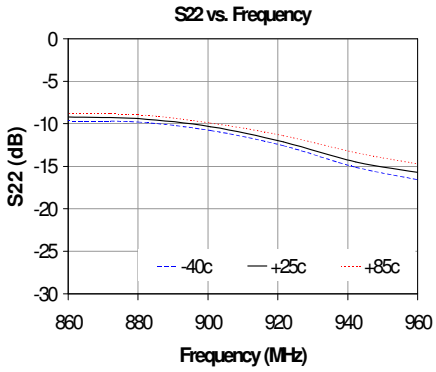
- The C2 and C3 placements are at silk screen markers, "H" and "9.5", respectively.
- The via hole spacing along the main microstrip line is .040".
- The distance from the edge of the FP31QF to the closer edge of L3 is .305".
- The transmission line lengths shown in the schematic are from the FP31QF device edge to the component edge.

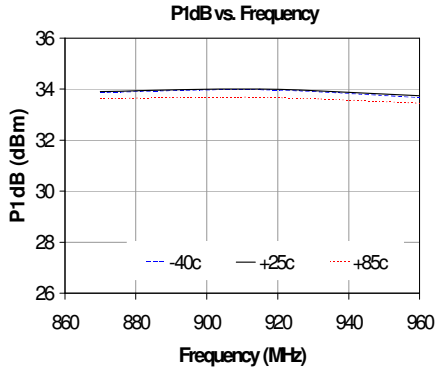


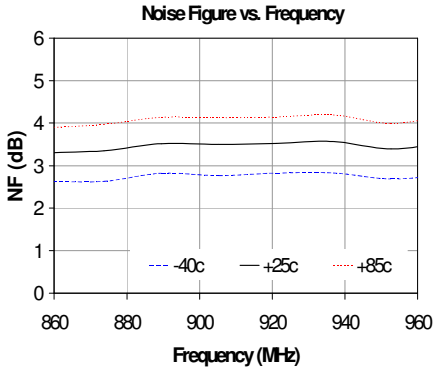
FP31QF-PCB900 Application Circuit Performance Plots

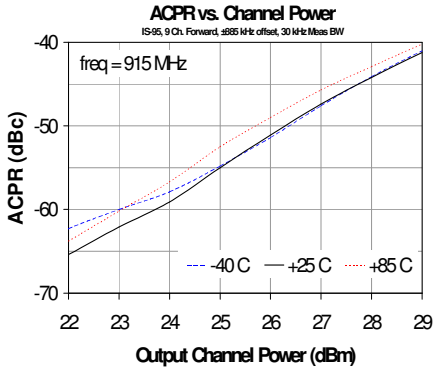


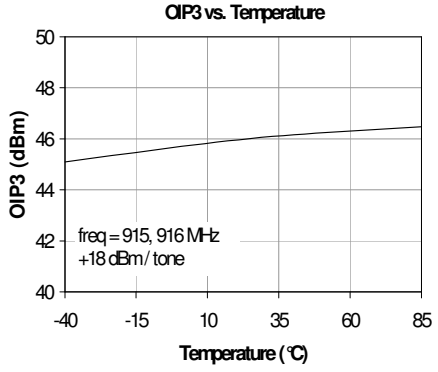


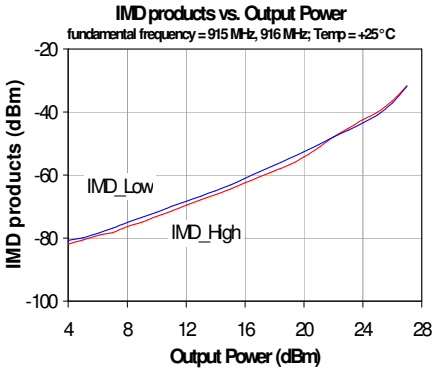


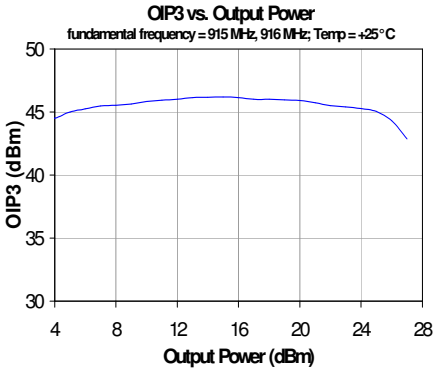


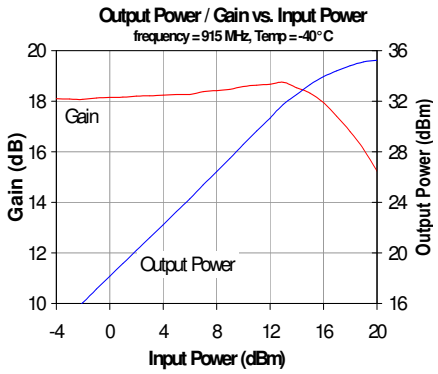


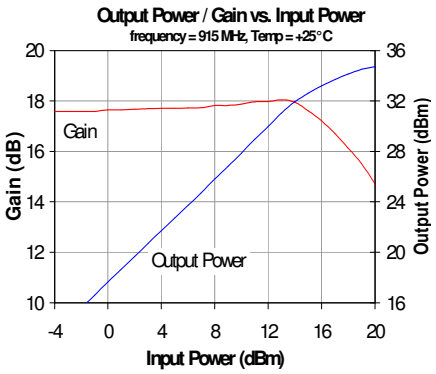


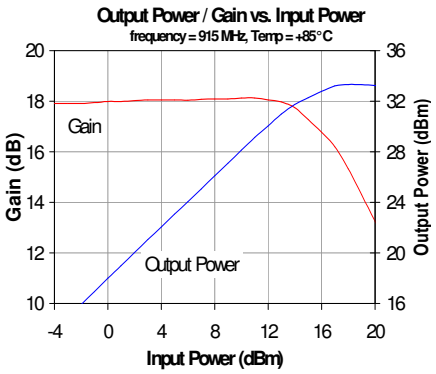












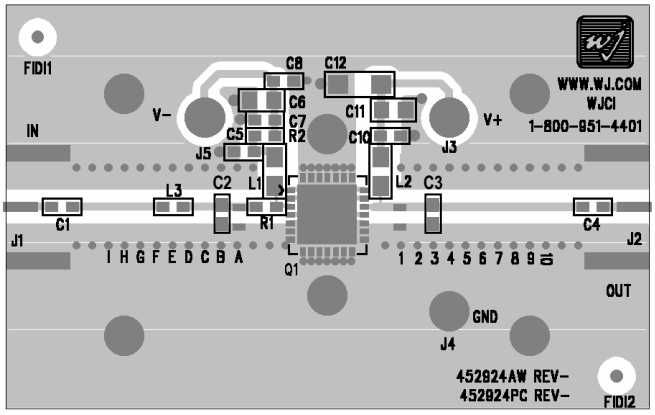
Application Circuit: 1930 – 1960 MHz (FP31QF-PCB1900)

The application circuit is matched for output power.

Typical RF Performance

Drain Bias = +9 V, I_{ds} = 450 mA, 25 °C

Frequency	MHz	1930	1960	1990
S21 – Gain	dB	14	13.8	13.8
S11 – Input Return Loss	dB	-17	-21	-27
S22 – Output Return Loss	dB	-11	-11	-13
Output P1dB	dBm	+33.5	+33.8	+33.8
Output IP3 (+18 dBm / tone, 1 MHz spacing)	dBm		+46.8	
Noise Figure	dB	4.3	4.5	4.4
IS-95 Channel Power @ -45 dBc ACPR	dBm		+27.3	

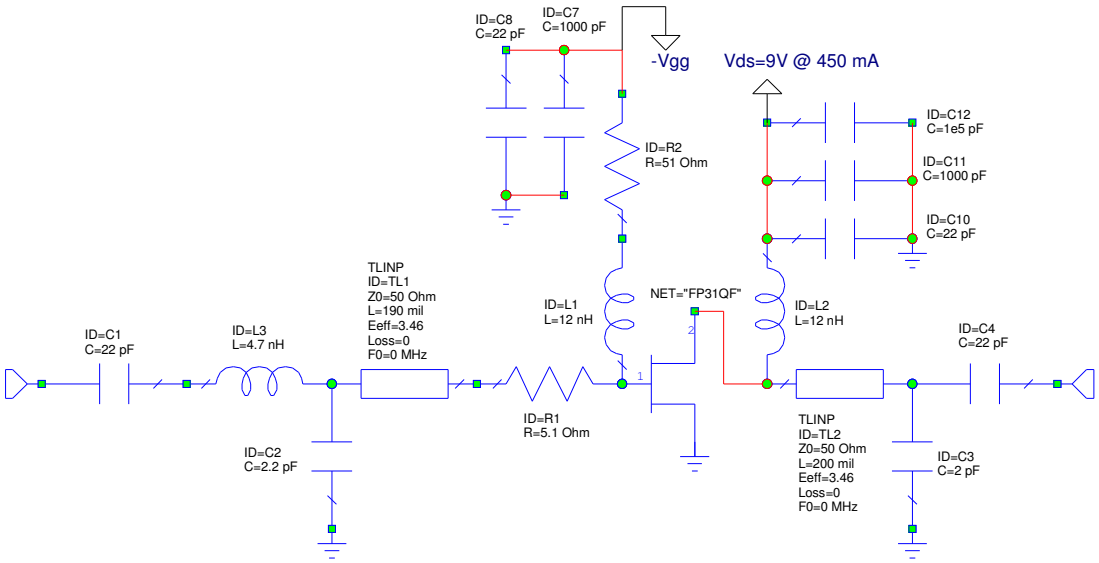


Circuit Board Material: .014" FR-4 (ε_r = 4.6),
4 layers (other layers added for rigidity), .062" total thickness, 1 oz copper
The main microstrip line has a line impedance of 50 Ω.

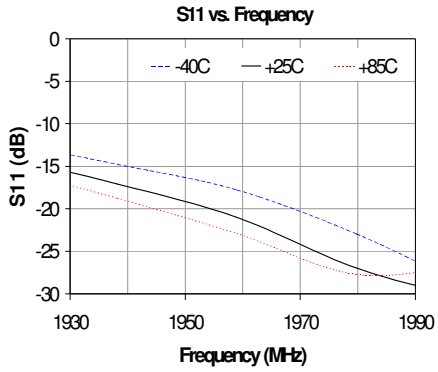
Bill of Materials

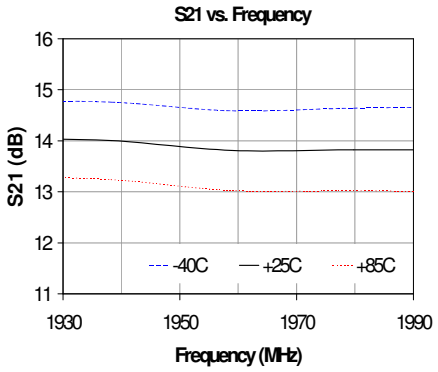
Ref. Desig.	Value	Part style	Size
C1, C4, C8, C10	22 pF	Chip capacitor	0603
C2	2.2 pF	Chip capacitor	0603
C3	2.0 pF	Chip capacitor	0603
C7, C11	1000 pF	Chip capacitor	0603
C12	0.1 µF	Chip capacitor	1206
L1, L2	12 nH	Wirewound chip inductor	0805
L3	4.7 nH	Multilayer chip inductor	0603
R1	5.1 Ω	Chip resistor	0603
R2	51 Ω	Chip resistor	0603
Q1	FP31QF	WJ 2W HFET	QFN 6x6
C5, C6		Do Not Place	

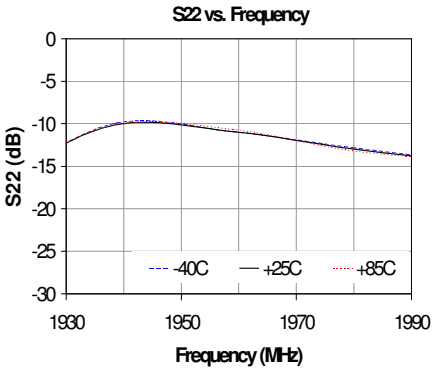
- The C2 and C3 placements are at silk screen markers, "B" and "3", respectively.
- The via hole spacing along the main microstrip line is .040".
- The distance from the edge of the FP31QF to the closer edge of L3 is .305".
- The transmission line lengths shown in the schematic are from the FP31QF device edge to the component edge.

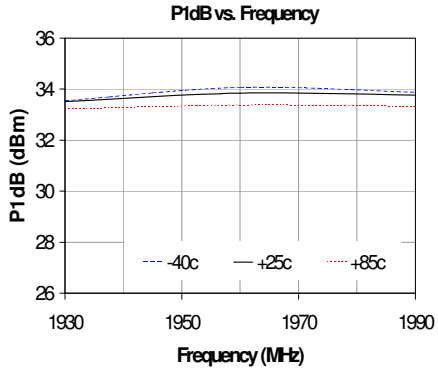


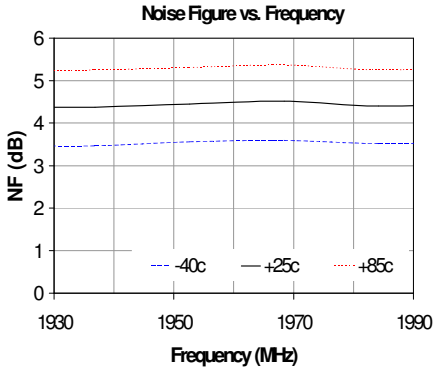
FP31QF-PCB1900 Application Circuit Performance Plots

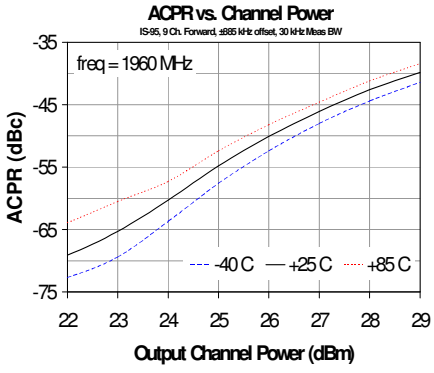


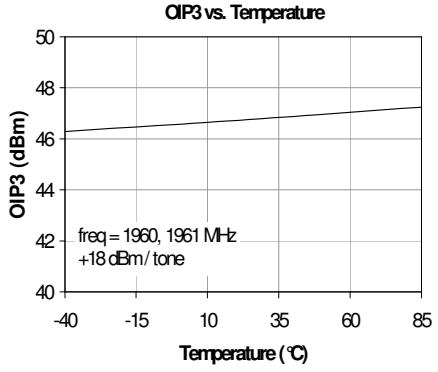


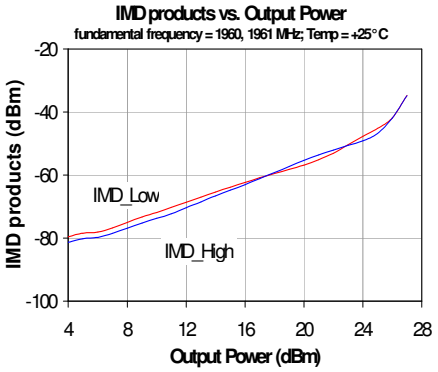


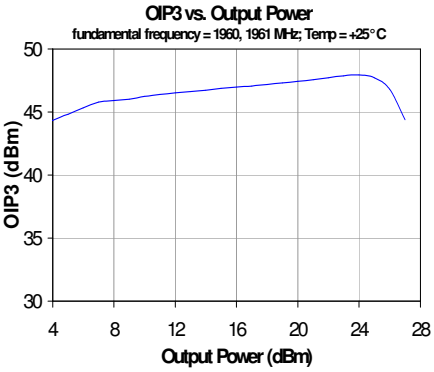


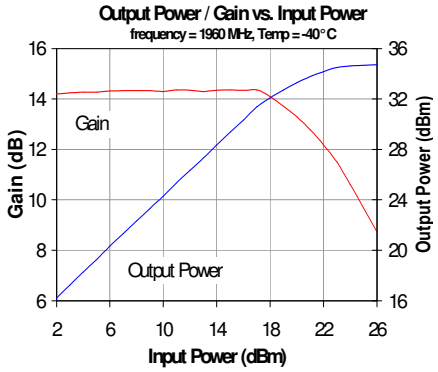


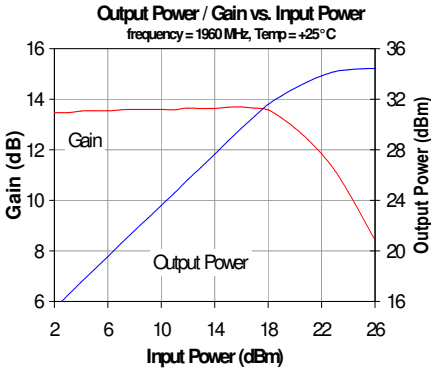


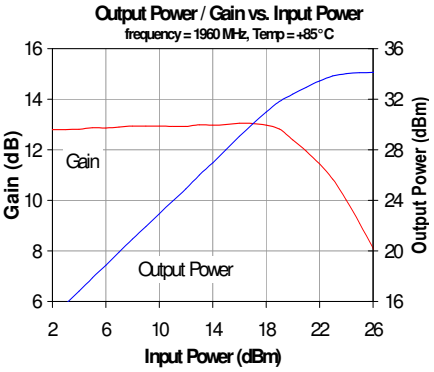












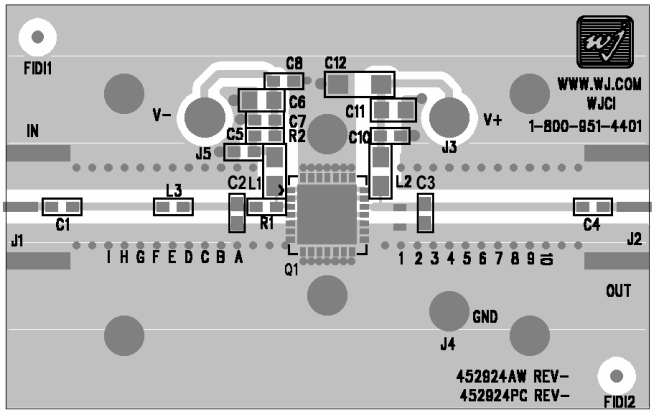
Application Circuit: 2110 – 2170 MHz (FP31QF-PCB2140)

The application circuit is matched for output power.

Typical RF Performance

Drain Bias = +9 V, I_{ds} = 450 mA, 25 °C

Frequency	MHz	2110	2140	2170
S21 – Gain	dB	13.2	13.3	13.1
S11 – Input Return Loss	dB	-17	-19	-16
S22 – Output Return Loss	dB	-14	-24	-18
Output P1dB	dBm	+33.6	+33.2	+33.3
Output IP3 (+18 dBm / tone, 1 MHz spacing)	dBm		+46.6	
Noise Figure	dB	4.7	4.6	4.9
IS-95 Channel Power @ -45 dBc ACPR	dBm		+25	

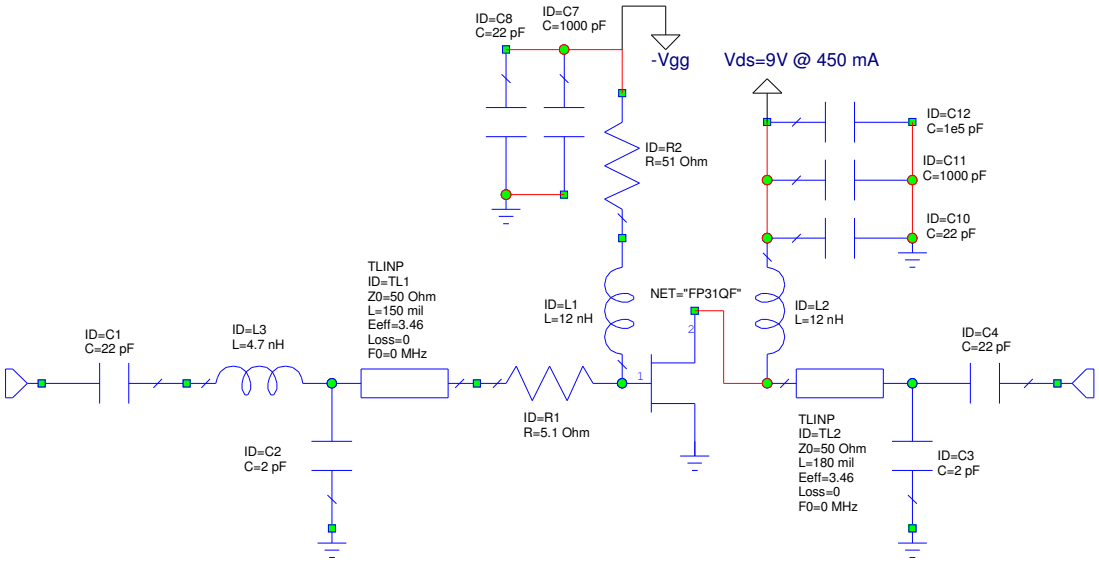


Circuit Board Material: .014" FR-4 (ε_r = 4.6),
4 layers (other layers added for rigidity), .062" total thickness, 1 oz copper
The main microstrip line has a line impedance of 50 Ω.

Bill of Materials

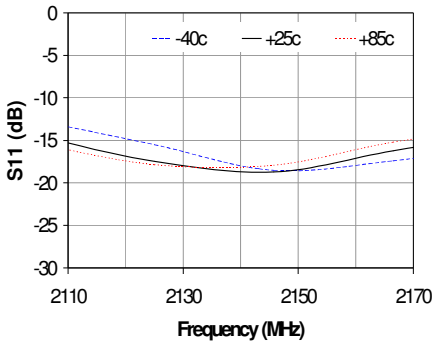
Ref. Desig.	Value	Part style	Size
C1, C4, C8, C10	22 pF	Chip capacitor	0603
C2, C3	2 pF	Chip capacitor	0603
C7, C11	1000 pF	Chip capacitor	0603
C12	0.1 µF	Chip capacitor	1206
L1, L2	12 nH	Wirewound chip inductor	0805
L3	4.7 nH	Multilayer chip inductor	0603
R1	5.1 Ω	Chip resistor	0603
R2	51 Ω	Chip resistor	0603
Q1	FP31QF	WJ 2W HFET	QFN 6x6
C5, C6		Do Not Place	

- The C2 and C3 placements are at silk screen markers, "A" and "2.5", respectively.
- The via hole spacing along the main microstrip line is .040".
- The distance from the edge of the FP31QF to the closer edge of L3 is .305".
- The transmission line lengths shown in the schematic are from the FP31QF device edge to the component edge.

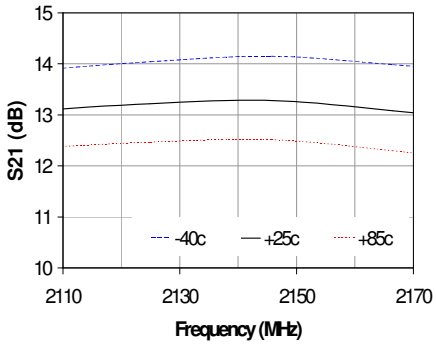


FP31QF-PCB2140 Application Circuit Performance Plots

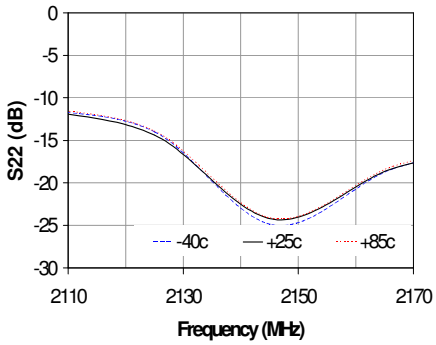
S11 vs. Frequency



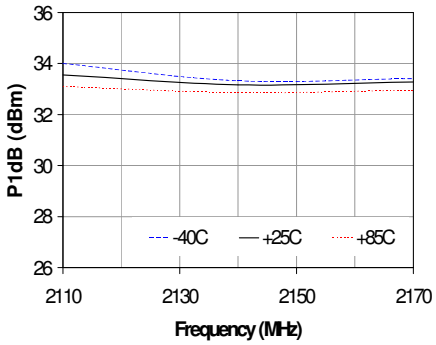
S21 vs. Frequency



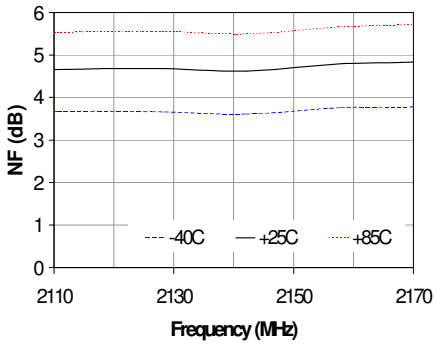
S22 vs. Frequency



P1dB vs. Frequency

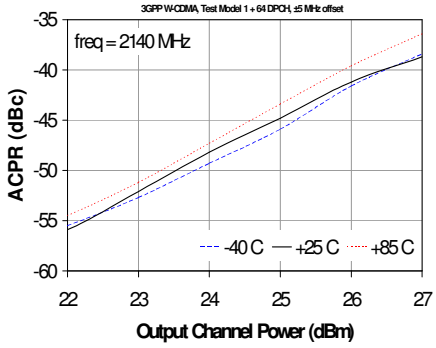


Noise Figure vs. Frequency

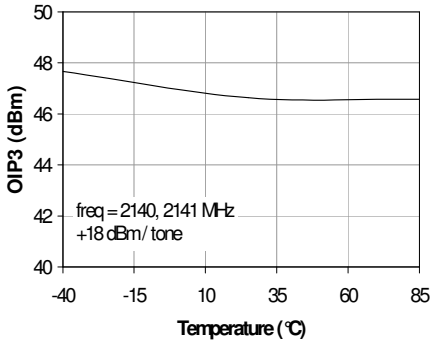


ACPR vs. Channel Power

3GPP W-CDMA Test Model 1 + 64 DPCH, ±5 MHz offset

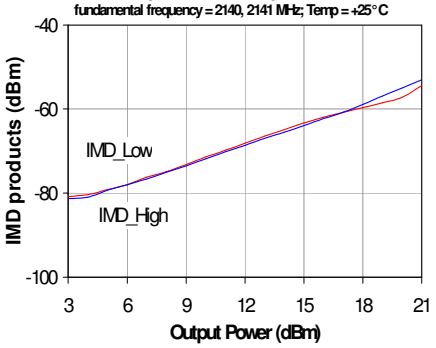


OIP3 vs. Temperature



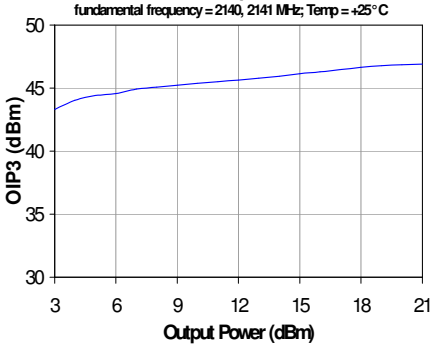
IMD products vs. Output Power

fundamental frequency = 2140, 2141 MHz; Temp = +25°C



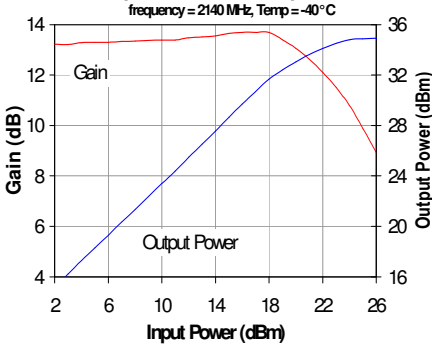
OIP3 vs. Output Power

fundamental frequency = 2140, 2141 MHz; Temp = +25°C



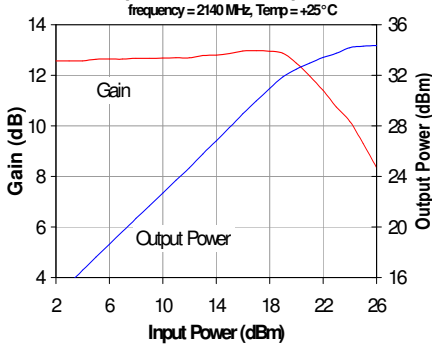
Output Power / Gain vs. Input Power

frequency = 2140 MHz, Temp = -40°C



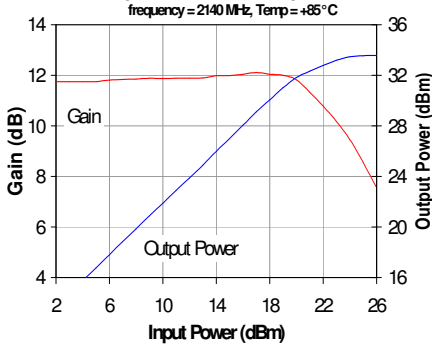
Output Power / Gain vs. Input Power

frequency = 2140 MHz, Temp = +25°C



Output Power / Gain vs. Input Power

frequency = 2140 MHz, Temp = +85°C



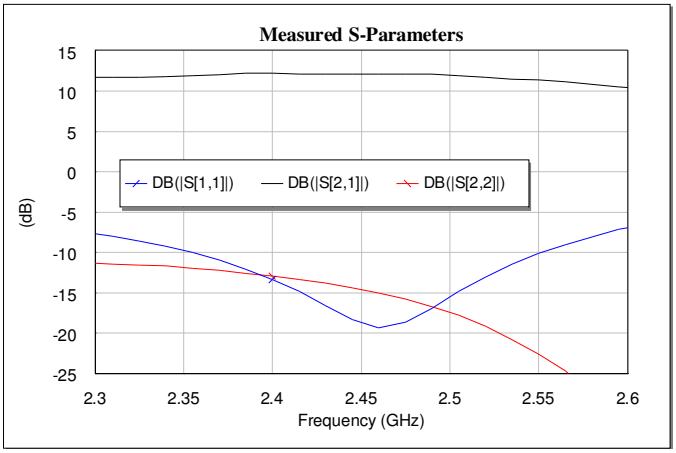
Reference Design: 2400 – 2500 MHz

The application circuit is matched for output power.

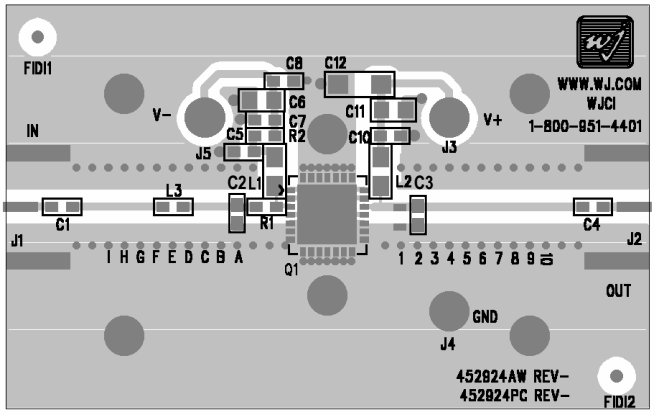
Typical RF Performance

Drain Bias = +9 V, I_{ds} = 450 mA, 25 °C

Frequency	MHz	2400	2500
S21 – Gain	dB	12.1	12.0
S11 – Input Return Loss	dB	-13	-16
S22 – Output Return Loss	dB	-13	-17
Output P1dB	dBm	+33.5	
Output IP3 (+18 dBm / tone, 1 MHz spacing)	dBm	+46.8	
Noise Figure	dB	4.6	



The 2.4 – 2.5 GHz Reference Circuit is shown for design purposes only. An evaluation board is not readily available for this application. The reader can obtain any FP31QF evaluation board and modify it with the circuit shown to achieve the performance shown in this reference design.

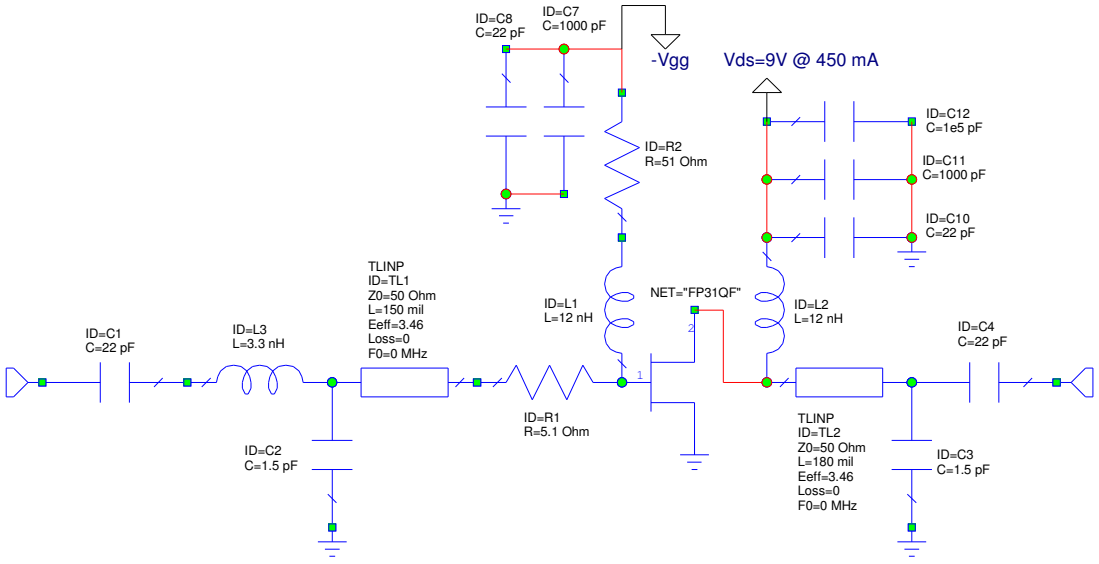


Circuit Board Material: .014" FR-4 (ε_r = 4.6),
4 layers (other layers added for rigidity), .062" total thickness, 1 oz copper
The main microstrip line has a line impedance of 50 Ω.

Bill of Materials

Ref. Desig.	Value	Part style	Size
C1, C4, C8, C10	22 pF	Chip capacitor	0603
C2, C3	1.5 pF	Chip capacitor	0603
C7, C11	1000 pF	Chip capacitor	0603
C12	0.1 µF	Chip capacitor	1206
L1, L2	12 nH	Wirewound chip inductor	0805
L3	3.3 nH	Multilayer chip inductor	0603
R1	5.1 Ω	Chip resistor	0603
R2	50 Ω	Chip resistor	0603
Q1	FP31QF	WJ 2W HFET	QFN 6x6
C5, C6		Do Not Place	

- The C2 and C3 placements are at silk screen markers, "A" and "2", respectively.
- The via hole spacing along the main microstrip line is .040".
- The distance from the edge of the FP31QF to the closer edge of L3 is .305".
- The transmission line lengths shown in the schematic are from the FP31QF device edge to the component edge.



Reference Design: 3500 MHz

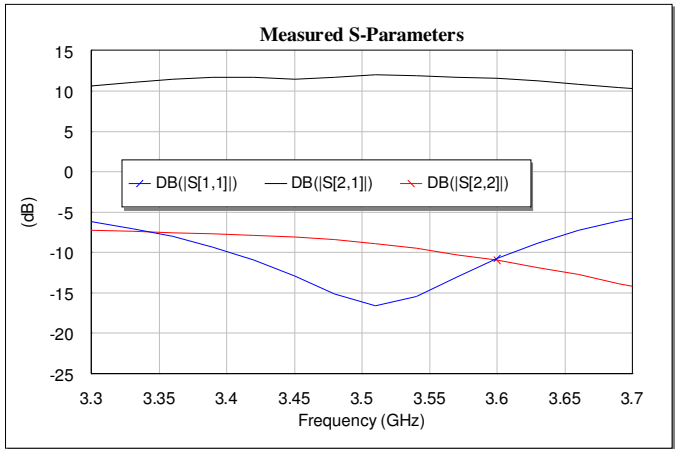
The application circuit is matched for output power.

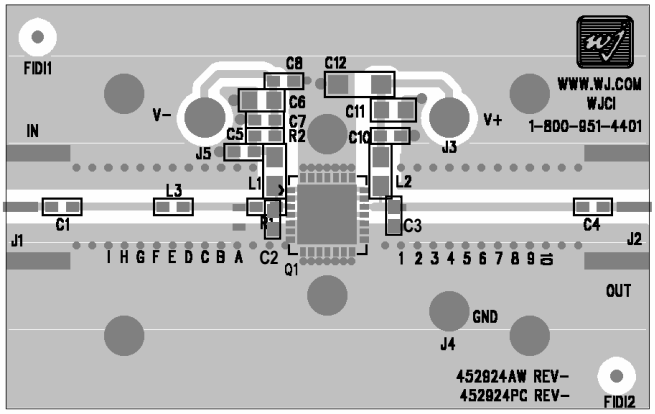
Typical RF Performance

Drain Bias = +9 V, I_{ds} = 450 mA, 25 °C

Frequency	MHz	3500
S21 – Gain	dB	11.9
S11 – Input Return Loss	dB	-16
S22 – Output Return Loss	dB	-8.8
Output P1dB	dBm	+33.5
Output IP3 (+18 dBm / tone, 1 MHz spacing)	dBm	+45

The 3.5 GHz Reference Circuit is shown for design purposes only. An evaluation board is not readily available for this application. The reader can obtain any FP31QF evaluation board and modify it with the circuit shown to achieve the performance shown in this reference design.



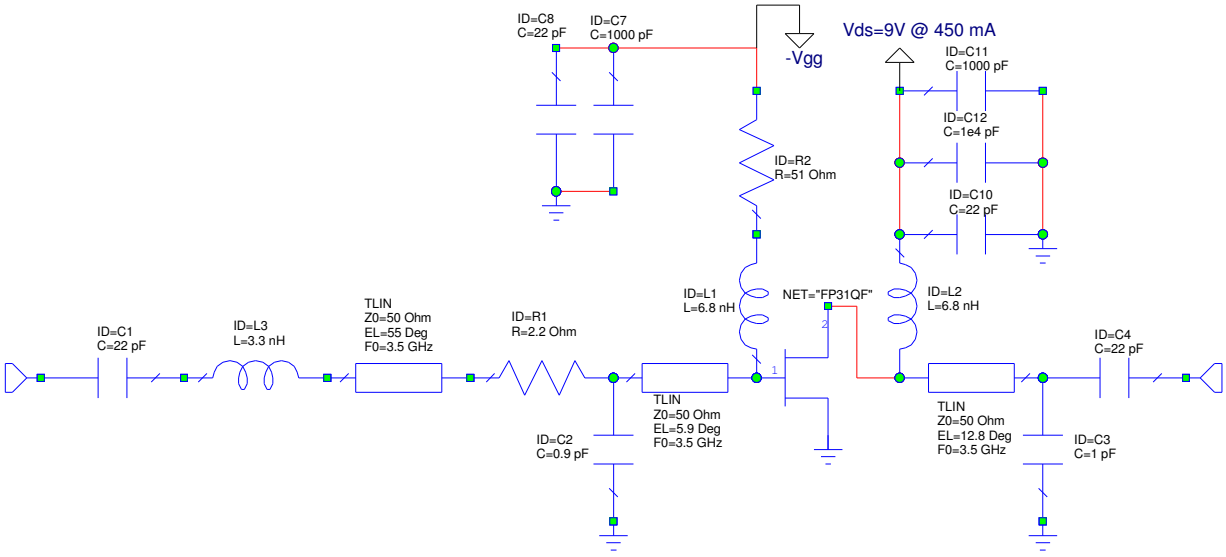


Circuit Board Material: .014" FR-4 (ε_r = 4.6),
4 layers (other layers added for rigidity), .062" total thickness, 1 oz copper
The main microstrip line has a line impedance of 50 Ω.

Bill of Materials

Ref. Desig.	Value	Part style	Size
C1, C4, C8, C10	22 pF	Chip capacitor	0603
C2	0.9 pF	Chip capacitor	0603
C3	1.0 pF	Chip capacitor	0603
C7, C11	1000 pF	Chip capacitor	0603
C12	0.1 µF	Chip capacitor	1206
L1, L2	6.8 nH	Wirewound chip inductor	0805
L3	3.3 nH	Multilayer chip inductor	0603
R1	2.2 Ω	Chip resistor	0603
R2	50 Ω	Chip resistor	0603
Q1	FP31QF	WJ 2W HFET	QFN 6x6
C5, C6		Do Not Place	

- Both the C2 and C3 placements are between the first and second via locations along the main microstrip line leading from the FP31QF device. Further descriptions are shown in the diagram on the left.
- The via hole spacing along the main microstrip line is .040".
- The distance from the edge of the FP31QF to the closer edge of L3 is .305".
- The transmission line lengths shown in the schematic are from the FP31QF device edge to the component edge.



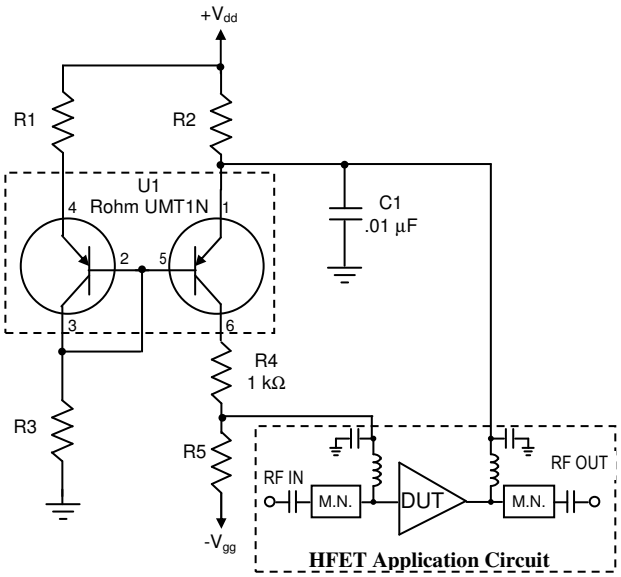
Application Note: Constant-Current Active-Biasing

Special attention should be taken to properly bias the FP31QF. Power supply sequencing is required to prevent the device from operating at 100% Idss for a prolonged period of time and possibly causing damage to the device. It is recommended that for the safest operation, the negative supply be "first on and last off." With a negative gate voltage present, the drain voltage can then be applied to the device. The gate voltage can then be adjusted to have the device be used at the proper quiescent bias condition.

An optional active-bias current mirror is recommended for use with the application circuits shown this datasheet. Generally in a laboratory environment, the gate voltage is adjusted until the drain draws the recommended operating current. The gate voltage required can vary slightly from device to device because of device pinchoff variation, while also varying slightly over temperature.

The active-bias circuit, shown on the right, uses dual PNP transistors to provide a constant drain current into the FP31QF, while also eliminating the effects of pinchoff variation. This configuration is best suited for applications where the intended output power level of the amplifier is backed off at least 6 dB away from its compression point. With the implementation of the circuit, lower P1dB values may be measured for a Class-AB amplifier, where the device will attempt to source more drain current while the circuit tries to provide a constant drain current. The circuit should be connected directly in line with where the voltage supplies would be normally connected with the amplifier circuit, as shown the diagram. Any required matching circuitry remains the same, although it is not shown in the diagram. This recommended active-bias constant-current circuit adds 7 components to the parts count for implementation, but should cost only an extra $0.144 to realize ($0.10 for U1, $0.0029 for R1, R3, R4, R5, $0.024 for R2, and $0.0085 for C1).

Temperature compensation is achieved by tracking the voltage variation with the temperature of the emitter-to-base junction of the two PNP transistors. As a 1st order approximation, this is achieved by using matched transistors with approximately the same Ibe current. Thus the transistor emitter voltage adjusts the HFET gate voltage so that the device draws a constant current, regardless of the temperature. A Rohm dual transistor - UMT1N - is recommended for cost, minimal board space requirements, and to minimize the variation between the two transistors. Minimizing the variability between the base-to-emitter junctions allow more accuracy in setting the current draw. More details can be found in a separate application note "Active-bias Constant-current Source Recommended for HFETs" found on the WJ website.



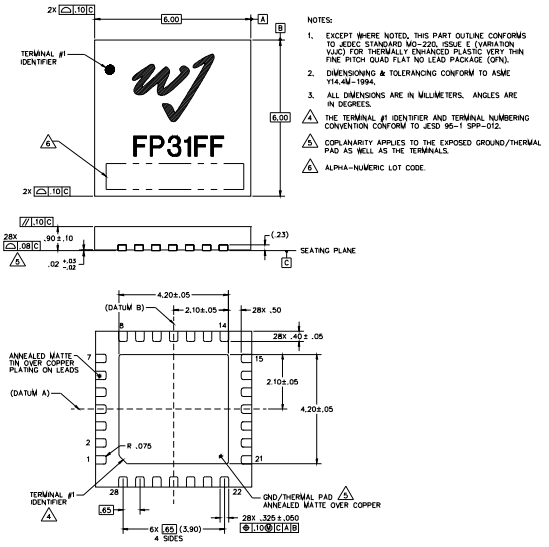
Parameter	FP31QF
Pos Supply, Vdd	+9 V
Neg Supply, Vgg	-5 V
Vds	+8.75. V
Ids	450 mA
R1	62 Ω
R2*	0.56 Ω
R3	2 kΩ
R4	1 kΩ
R5	1 kΩ

*R2 should be of size 1206 to dissipate 0.113 Watts. This should be of 1% tolerance. Two 1.1 Ω resistors in parallel of size 0805 can also be used.

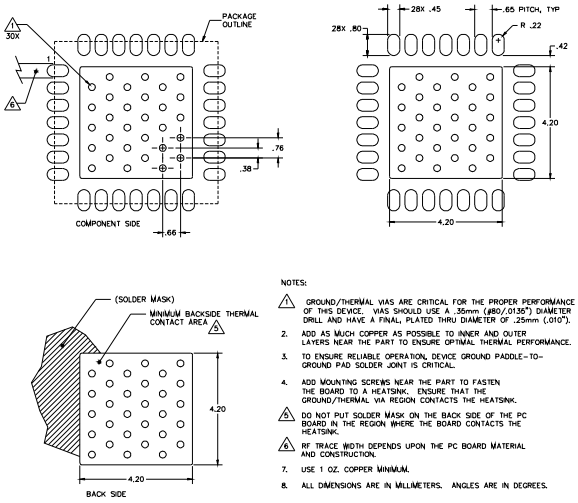
FP31QF-F Mechanical Information

This package is lead-free/RoHS-compliant. It is compatible with both lead-free (maximum 260 °C reflow temperature) and leaded (maximum 245 °C reflow temperature) soldering processes. The plating material on the pins is annealed matte tin over copper.

Outline Drawing



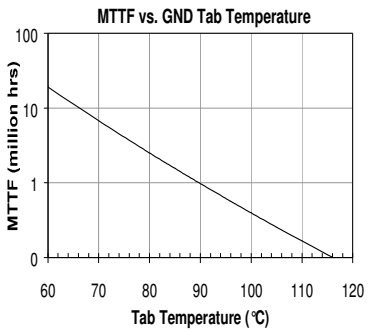
Mounting Configuration / Land Pattern



Thermal Specifications

Parameter	Rating
Operating Case Temperature	-40 to +85 °C
Thermal Resistance, Rth (1)	17.5 °C/W
Junction Temperature, Tj (2)	156 °C

1. The thermal resistance is referenced from the hottest part of the junction to the ground copper on the backside.
2. This corresponds to the typical drain biasing condition of +9V, 450 mA at an 85°C case temperature. A minimum MTTF of 1 million hours is achieved for junction temperatures below 160 °C.



Product Marking

The component will be lasermarked with a "FP31FF" product label with an alphanumeric lot code on the top surface of the package. The obsolete tin-lead package is marked with an "FP31QF" designator followed by an alphanumeric lot code.

Tape and reel specifications for this part will be located on the website in the "Application Notes" section.

ESD / MSL Information

Caution! ESD sensitive device.

ESD Rating: Class 1C
Value: Passes ≥ 1000V to <2000V
Test: Human Body Model (HBM)
Standard: JEDEC Standard JESD22-A114

ESD Rating: Class IV
Value: Passes ≥ 1000V
Test: Charged Device Model (CDM)
Standard: JEDEC Standard JESD22-C101

MSL Rating: Level 2 at +260 °C convection reflow
Standard: JEDEC Standard J-STD-020

Functional Pin Layout

Pin	FUNCTION
3	Gate /RF Input
19	Drain / RF Output

The backside paddle is the Source and should be grounded for thermal and electrical purposes. All other pins should be grounded on the PCB.

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Электронная почта: sales@st-electron.ru

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