SC16C554B/554DB

5 V, 3.3 V and 2.5 V quad UART, 5 Mbit/s (max.) with 16-byte FIFOs

Rev. 4 — 8 June 2010 **Product data sheet**

1. General description

The SC16C554B/554DB is a 4-channel Universal Asynchronous Receiver and Transmitter (QUART) used for serial data communications. Its principal function is to convert parallel data into serial data and vice versa. The UART can handle serial data rates up to 5 Mbit/s. It comes with an Intel (16 mode) or Motorola (68 mode) interface.

The SC16C554B/554DB is pin compatible with the ST16C554 and TL16C554 and it will power-up to be functionally equivalent to the 16C454. Programming of control registers enables the added features of the SC16C554B/554DB. Some of these added features are the 16-byte receive and transmit FIFOs, four receive trigger levels. The SC16C554B/554DB also provides DMA mode data transfers through FIFO trigger levels and the $\overline{\text{TXRDY}}$ and $\overline{\text{RXRDY}}$ signals. ($\overline{\text{TXRDY}}$ and $\overline{\text{RXRDY}}$ signals are not available in the HVQFN48 package.) On-board status registers provide the user with error indications, operational status, and modem interface control. System interrupts may be tailored to meet user requirements. An internal loopback capability allows on-board diagnostics.

The SC16C554B/554DB operates at 5 V, 3.3 V and 2.5 V, and the industrial temperature range, and is available in plastic PLCC68, LQFP64, LQFP80, and HVQFN48 packages. On the HVQFN48 package only, channel C has all the modem pins. Channels A and B have only $\overline{\text{RTS}}$n and $\overline{\text{CTS}}$n pins and channel D does not have any modem pin.

2. Features and benefits

- 4 channel UART
- 5 V, 3.3 V and 2.5 V operation
- Industrial temperature range (−40 °C to +85 °C)
- The SC16C554B is pin and software compatible with the industry-standard ST16C454/554, ST68C454/554, ST16C554, TL16C554
- The SC16C554DB is pin and software compatible with ST16C554D, and software compatible with ST16C454/554, ST16C554, TL16C554
- Up to 5 Mbit/s data rate at 5 V and 3.3 V, and 3 Mbit/s at 2.5 V
- 5 V tolerant on input only pins[1]
- 16-byte transmit FIFO
- 16-byte receive FIFO with error flags
- Programmable auto-$\overline{\text{RTS}}$ and auto-$\overline{\text{CTS}}$
  - In auto-$\overline{\text{CTS}}$ mode, $\overline{\text{CTS}}$ controls transmitter
  - In auto-$\overline{\text{RTS}}$ mode, RX FIFO contents and threshold control $\overline{\text{RTS}}$

1. For data bus pins D7 to D0, see Table 24 “Limiting values”.

- Automatic hardware flow control ($\overline{RTS}$/$\overline{CTS}$)
- Software selectable baud rate generator
- Four selectable Receive FIFO interrupt trigger levels
- Standard modem interface
- Standard asynchronous error and framing bits (Start, Stop, and Parity Overrun Break)
- Transmit, Receive, Line Status, and Data Set interrupts independently controlled
- Fully programmable character formatting:
  - 5-bit, 6-bit, 7-bit, or 8-bit characters
  - Even, odd, or no-parity formats
  - 1, $1^1\diagup_2$, or 2-stop bit
  - Baud generation (DC to 5 Mbit/s)
- False start-bit detection
- Complete status reporting capabilities
- 3-state output TTL drive capabilities for bidirectional data bus and control bus
- Line break generation and detection
- Internal diagnostic capabilities:
  - Loopback controls for communications link fault isolation
- Prioritized interrupt system controls
- Modem control functions ($\overline{CTS}$, $\overline{RTS}$, $\overline{DSR}$, $\overline{DTR}$, $\overline{RI}$, $\overline{CD}$).

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
SC16C554BIB64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
SC16C554BIB80	LQFP80	plastic low profile quad flat package; 80 leads; body 12 × 12 × 1.4 mm	SOT315-1
SC16C554BIBM	LQFP64	plastic low profile quad flat package; 64 leads; body 7 × 7 × 1.4 mm	SOT414-1
SC16C554BIBS	HVQFN48	plastic thermal enhanced very thin quad flat package; no leads; 48 terminals; body 6 × 6 × 0.85 mm	SOT778-3
SC16C554DBIA68	PLCC68	plastic leaded chip carrier; 68 leads	SOT188-2
SC16C554DBIB64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2

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4. Block diagram

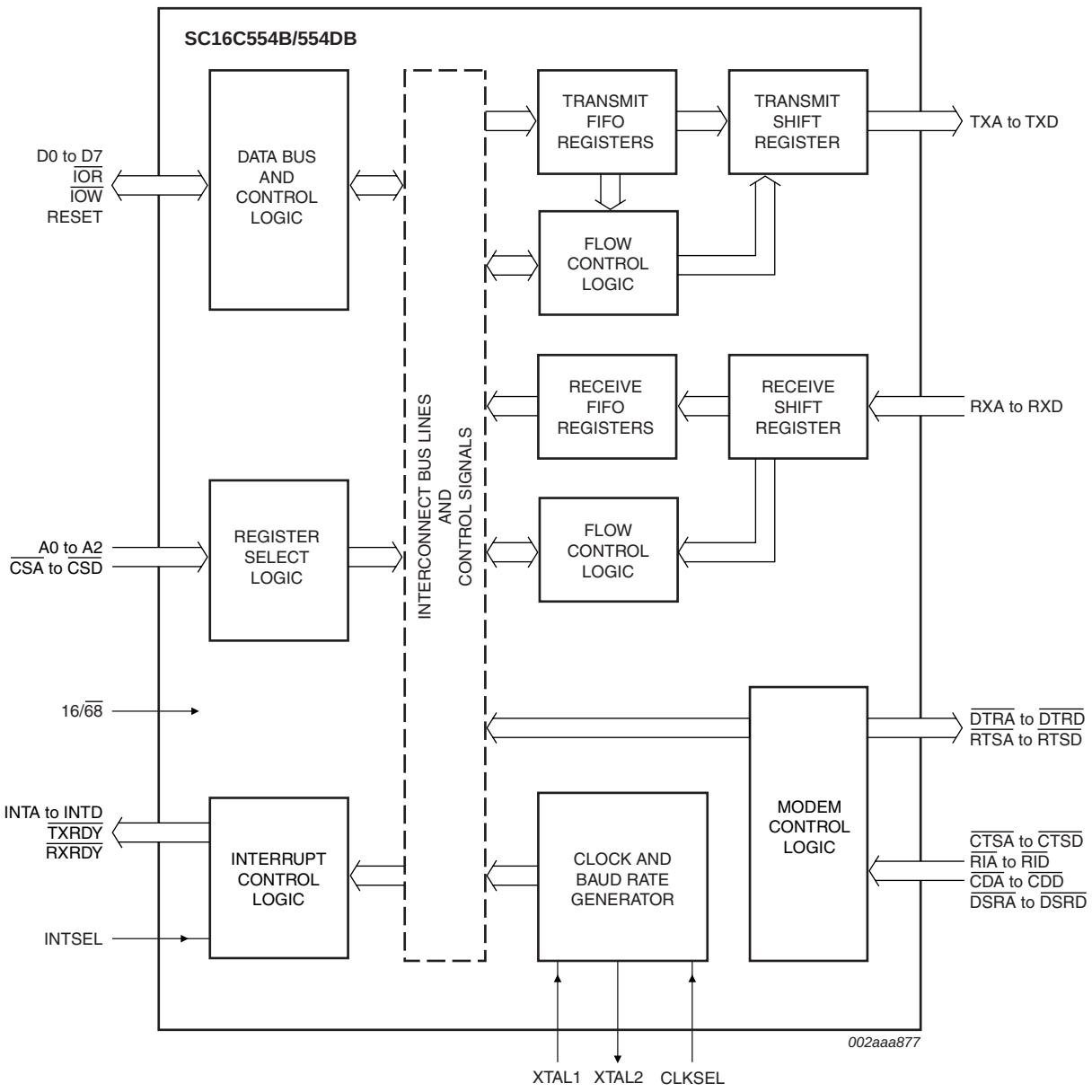


Fig 1. Block diagram of SC16C554B/554DB (16 mode)

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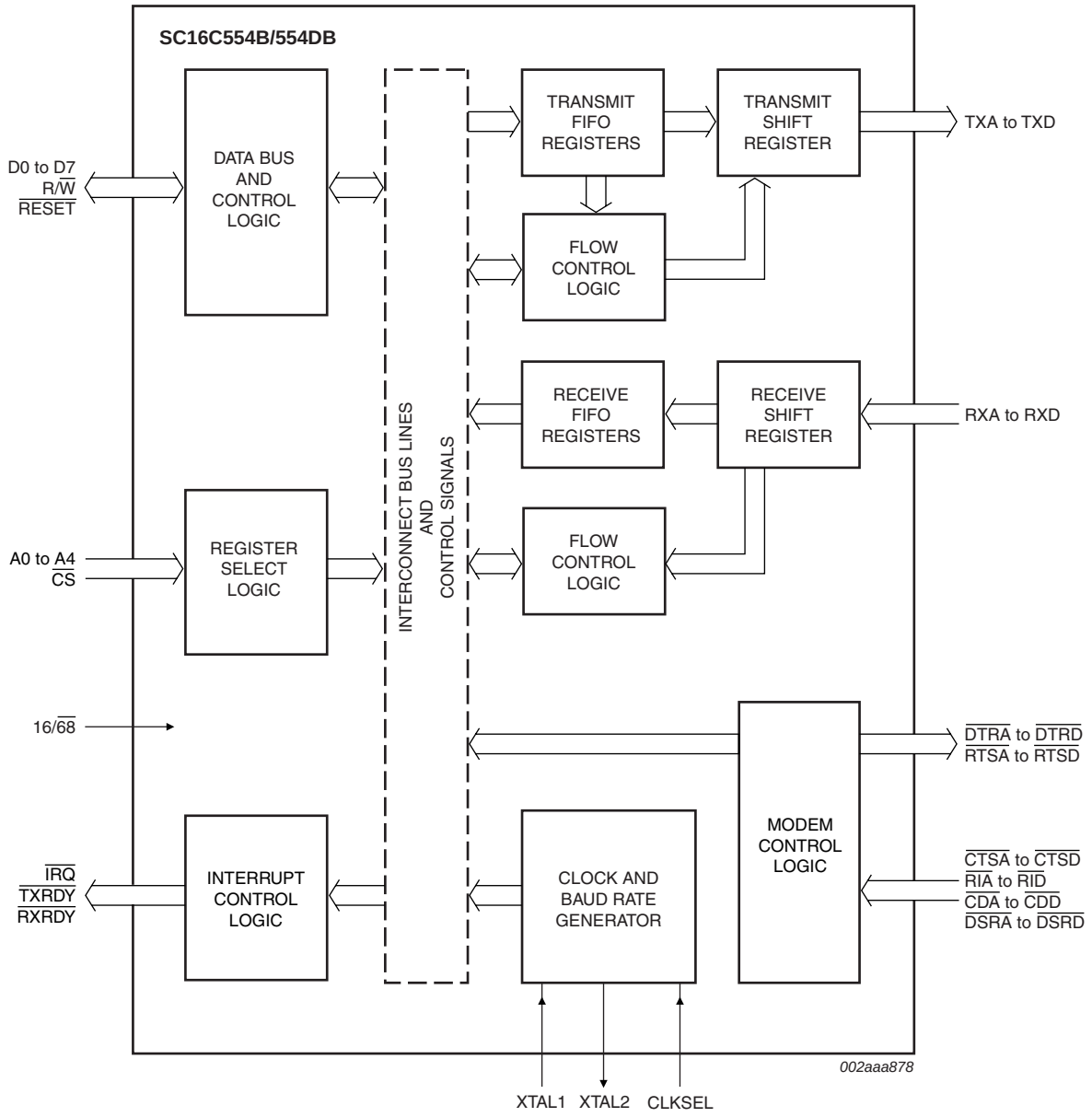


Fig 2. Block diagram of SC16C554B/554DB (68 mode)

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5. Pinning information

5.1 Pinning

5.1.1 PLCC68

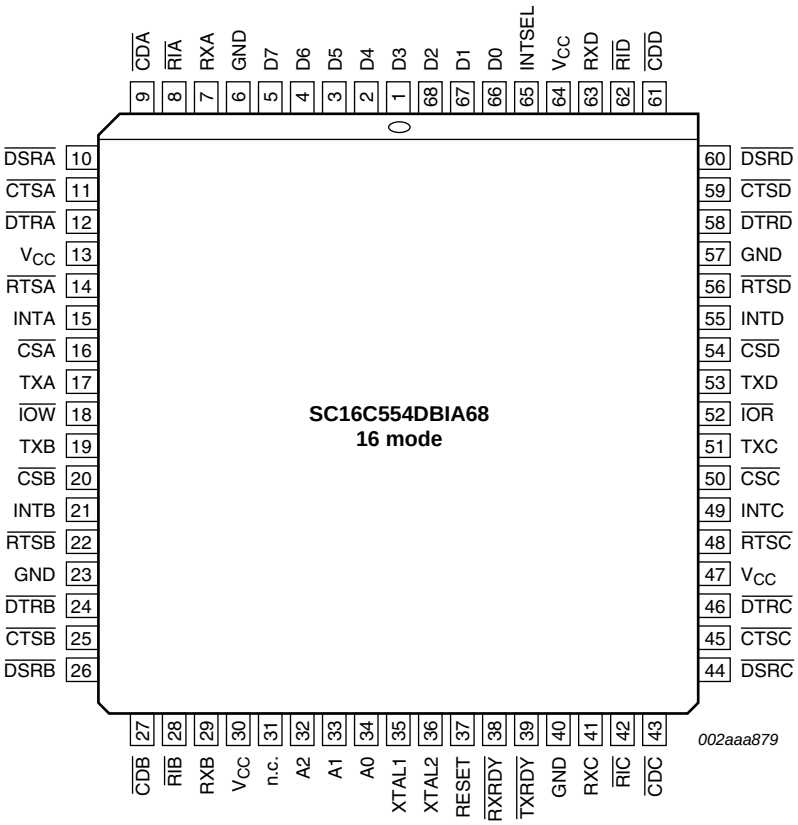


Fig 3. Pin configuration for PLCC68 (16 mode)

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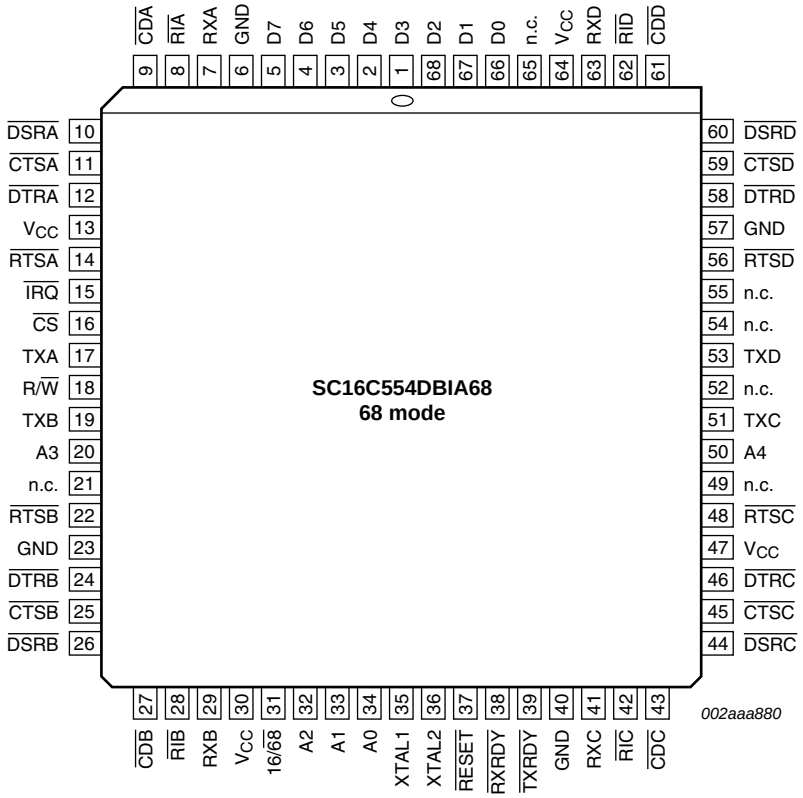


Fig 4. Pin configuration for PLCC68 (68 mode)

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5.1.2 LQFP64

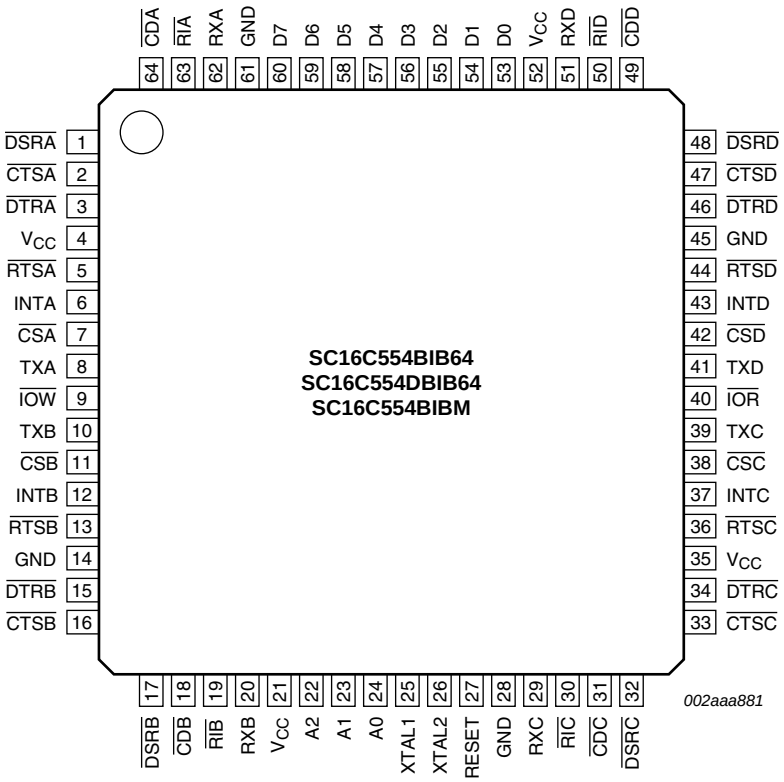


Fig 5. Pin configuration for LQFP64

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5.1.3 LQFP80

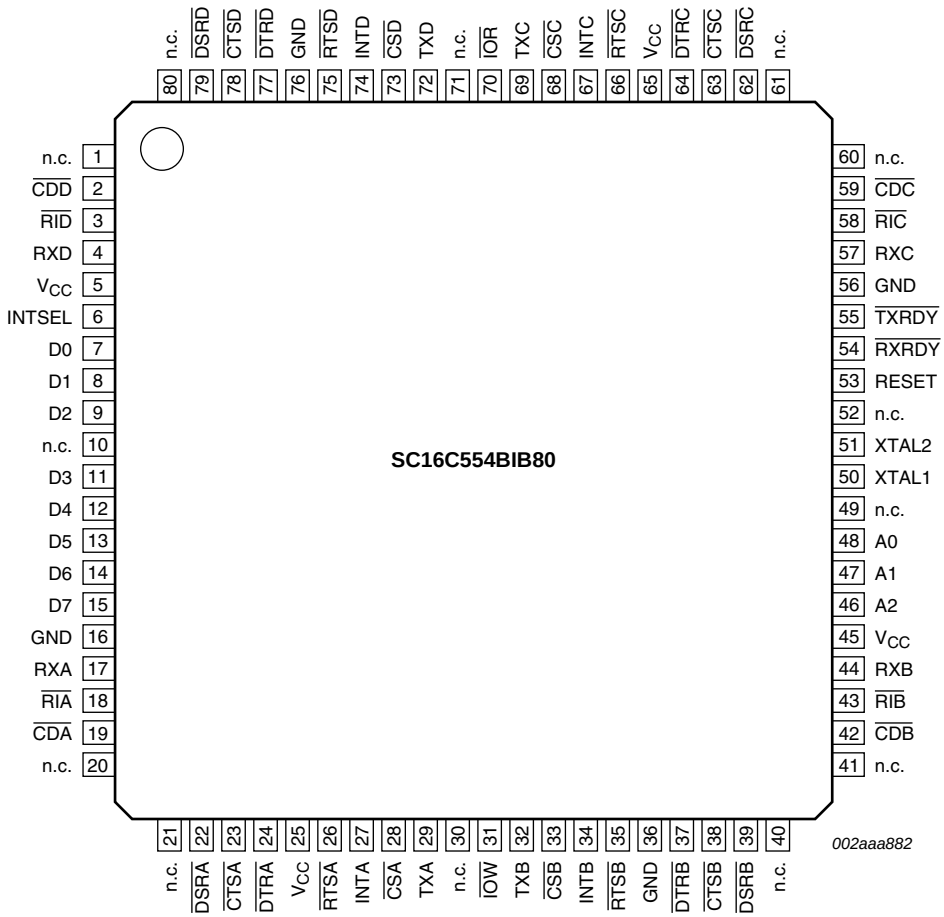


Fig 6. Pin configuration for LQFP80

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5.1.4 HVQFN48

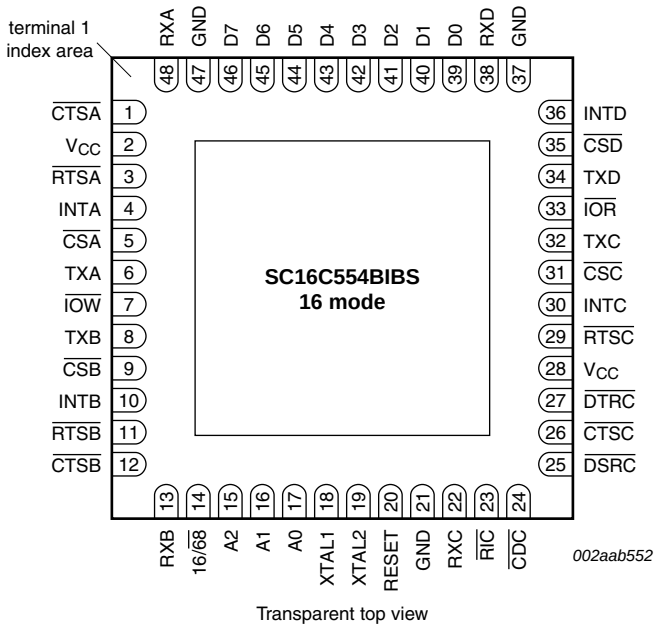


Fig 7. Pin configuration for HVQFN (16 mode)

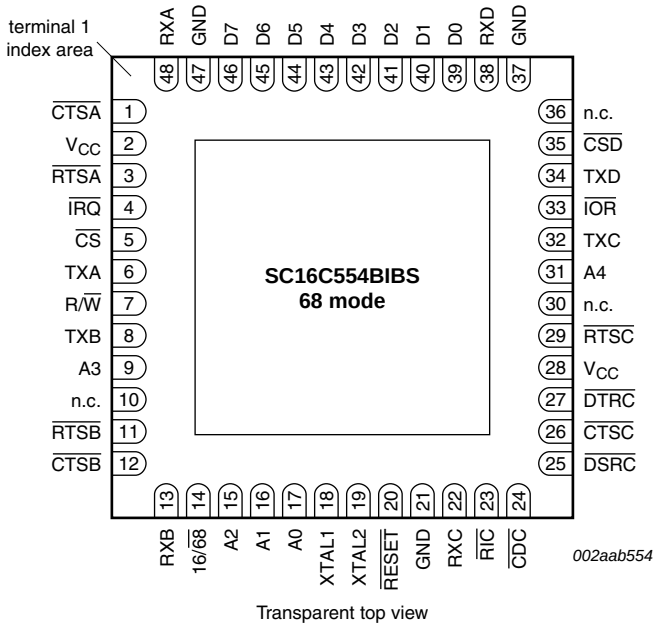


Fig 8. Pin configuration for HVQFN (68 mode)

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5.2 Pin description

Table 2. Pin description

Symbol	Pin				Type	Description
	PLCC68	LQFP64	LQFP80	HVQFN48		
16/$\overline{68}$	31	-	-	14	I	**16/68 Interface type select (input with internal pull-up).** This input provides the 16 (Intel) or 68 (Motorola) bus interface type select. The functions of $\overline{IOR}$, $\overline{IOW}$, INTA to INTD, and $\overline{CSA}$ to $\overline{CSD}$ are re-assigned with the logic state of this pin. When this pin is a logic 1, the 16 mode interface (16C554) is selected. When this pin is a logic 0, the 68 mode interface (68C554) is selected. When this pin is a logic 0, $\overline{IOW}$ is re-assigned to R/$\overline{W}$, RESET is re-assigned to $\overline{RESET}$, $\overline{IOR}$ is not used, and INTA to INTD are connected in a wire-OR configuration. The wire-OR outputs are connected internally to the open-drain IRQ signal output. This pin is not available on 64-pin packages which operate in the 16 mode only.
A0	34	24	48	17	I	**Address 0 select bit.** Internal registers address selection in 16 and 68 modes.
A1	33	23	47	16	I	**Address 1 select bit.** Internal registers address selection in 16 and 68 modes.
A2	32	22	46	15	I	**Address 2 select bit.** Internal registers address selection in 16 and 68 modes.
A3	20	-	-	9	I	**Address 3 to Address 4 select bits.** When the 68 mode is selected, these pins are used to address or select individual UARTs (providing $\overline{CS}$ is a logic 0). In the 16 mode, these pins are re-assigned as chip selects, see $\overline{CSB}$ and $\overline{CSC}$.
A4	50	-	-	31	I	
$\overline{CDA}$	9	64	19	-	I	**Carrier Detect (active LOW).** These inputs are associated with individual UART channels A through D. A logic 0 on this pin indicates that a carrier has been detected by the modem for that channel.
$\overline{CDB}$	27	18	42	-	I	
$\overline{CDC}$	43	31	59	24	I	
$\overline{CDD}$	61	49	2	-	I	
$\overline{CS}$	16	-	-	5	I	**Chip Select (active LOW).** In the 68 mode, this pin functions as a multiple channel chip enable. In this case, all four UARTs (A to D) are enabled when the $\overline{CS}$ pin is a logic 0. An individual UART channel is selected by the data contents of address bits A3 to A4. when the 16 mode is selected (68-pin devices), this pin functions as $\overline{CSA}$ (see definition under $\overline{CSA}$, $\overline{CSB}$).
$\overline{CSA}$	16	7	28	5	I	**Chip Select A, B, C, D (active LOW).** This function is associated with the 16 mode only, and for individual channels 'A' through 'D'. When in 16 mode, these pins enable data transfers between the user CPU and the SC16C554B/554DB for the channel(s) addressed. Individual UART sections (A, B, C, D) are addressed by providing a logic 0 on the respective $\overline{CSA}$ to $\overline{CSD}$ pin. When the 68 mode is selected, the functions of these pins are re-assigned. 68 mode functions are described under their respective name/pin headings.
$\overline{CSB}$	20	11	33	9	I	
$\overline{CSC}$	50	38	68	31	I	
$\overline{CSD}$	54	42	73	35	I	

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Table 2. Pin description *...continued*

Symbol	Pin				Type	Description
	PLCC68	LQFP64	LQFP80	HVQFN48		
$\overline{CTSA}$	11	2	23	1	I	**Clear to Send (active LOW).** These inputs are associated with individual UART channels A to D. A logic 0 on the $\overline{CTSn}$ pin indicates the modem or data set is ready to accept transmit data from the SC16C554B/554DB. Status can be tested by reading MSR[4]. This pin only affects the transmit or receive operations when auto-$\overline{CTS}$ function is enabled via MCR[5] for hardware flow control operation.
$\overline{CTSB}$	25	16	38	12	I	
$\overline{CTSC}$	45	33	63	26	I	
$\overline{CTSD}$	59	47	78	-	I	
D0	66	53	7	39	I/O	**Data bus (bidirectional).** These pins are the 8-bit, 3-state data bus for transferring information to or from the controlling CPU. D0 is the least significant bit and the first data bit in a transmit or receive serial data stream.
D1	67	54	8	40	I/O	
D2	68	55	9	41	I/O	
D3	1	56	11	42	I/O	
D4	2	57	12	43	I/O	
D5	3	58	13	44	I/O	
D6	4	59	14	45	I/O	
D7	5	60	15	46	I/O	
$\overline{DSRA}$	10	1	22	-	I	**Data Set Ready (active LOW).** These inputs are associated with individual UART channels, A through D. A logic 0 on this pin indicates the modem or data set is powered-on and is ready for data exchange with the UART. This pin has no effect on the UART's transmit or receive operation.
$\overline{DSRB}$	26	17	39	-	I	
$\overline{DSRC}$	44	32	62	25	I	
$\overline{DSRD}$	60	48	79	-	I	
$\overline{DTRA}$	12	3	24	-	O	**Data Terminal Ready (active LOW).** These outputs are associated with individual UART channels, A through D. A logic 0 on this pin indicates that the SC16C554B/554DB is powered-on and ready. This pin can be controlled via the Modem Control Register. Writing a logic 1 to MCR[0] will set the $\overline{DTRn}$ output to logic 0, enabling the modem. This pin will be a logic 1 after writing a logic 0 to MCR[0], or after a reset. This pin has no effect on the UART's transmit or receive operation.
$\overline{DTRB}$	24	15	37	-	O	
$\overline{DTRC}$	46	34	64	27	O	
$\overline{DTRD}$	58	46	77	-	O	
GND	6, 23, 40, 57	14, 28, 45, 61	16, 36, 56, 76	21, 37, 47[1]	I	**Signal and power ground.**
INTA	15	6	27	4	O	**Interrupt A, B, C, D (active HIGH).** This function is associated with the 16 mode only. These pins provide individual channel interrupts INTA to INTD. INTA to INTD are enabled when MCR[3] is set to a logic 1, interrupts are enabled in the Interrupt Enable Register (IER), and when an interrupt condition exists. Interrupt conditions include: receiver errors, available receiver buffer data, transmit buffer empty, or when a modem status flag is detected. When the 68 mode is selected, the functions of these pins are re-assigned. 68 mode functions are described under their respective name/pin headings.
INTB	21	12	34	10	O	
INTC	49	37	67	30	O	
INTD	55	43	74	36	O	

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Table 2. Pin description *...continued*

Symbol	Pin				Type	Description
	PLCC68	LQFP64	LQFP80	HVQFN48		
INTSEL	65	-	6	-	I	**Interrupt Select (active HIGH, with internal pull-down).** This function is associated with the 16 mode only. When the 16 mode is selected, this pin can be used in conjunction with MCR[3] to enable or disable the 3-state interrupts, INTA to INTD, or override MCR[3] and force continuous interrupts. Interrupt outputs are enabled continuously by making this pin a logic 1. Making this pin a logic 0 allows MCR[3] to control the 3-state interrupt output. In this mode, MCR[3] is set to a logic 1 to enable the 3-state outputs. This pin is disabled in the 68 mode. Due to pin limitations on the 64-pin packages, this pin is not available. To cover this limitation, the SC16C554DBIB64 version operates in the continuous interrupt enable mode by bonding this pin to V_{CC} internally. The SC16C554BIB64 operates with MCR[3] control by bonding this pin to GND. The INTSEL pin is not available on the HVQFN48 package.
$\overline{IOR}$	52	40	70	33	I	**Input/Output Read strobe (active LOW).** This function is associated with the 16 mode only. A logic 0 transition on this pin will load the contents of an internal register defined by address bits A0 to A2 onto the SC16C554B/554DB data bus (D0 to D7) for access by external CPU. This pin is disabled in the 68 mode.
$\overline{IOW}$	18	9	31	7	I	**Input/Output Write strobe (active LOW).** This function is associated with the 16 mode only. A logic 0 transition on this pin will transfer the contents of the data bus (D0 to D7) from the external CPU to an internal register that is defined by address bits A0 to A2. When the 68 mode is selected, this pin functions as R/$\overline{W}$ (see definition under R/$\overline{W}$).
$\overline{IRQ}$	15	-	-	4	O	**Interrupt Request or Interrupt 'A'.** This function is associated with the 68 mode only. In the 68 mode, interrupts from UART channels A to D are wire-ORed internally to function as a single IRQ interrupt. This pin transitions to a logic 0 (if enabled by the Interrupt Enable Register) whenever a UART channel(s) requires service. Individual channel interrupt status can be determined by addressing each channel through its associated internal register, using $\overline{CS}$ and A3 to A4. In the 68 mode, and external pull-up resistor must be connected between this pin and V_{CC}. The function of this pin changes to INTA when operating in the 16 mode (see definition under INTA).
n.c.	21, 49, 52, 54, 55, 65	-	1, 10, 20, 21, 30, 40, 41, 49, 52, 60, 61, 71, 80	-	-	not connected

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Table 2. Pin description *...continued*

Symbol	Pin				Type	Description
	PLCC68	LQFP64	LQFP80	HVQFN48		
$\overline{\text{RESET}}$ (RESET)	37	27	53	20	I	**Reset.** In the 16 mode, a logic 1 on this pin will reset the internal registers and all the outputs. The UART transmitter output and the receiver input will be disabled during reset time. (See Section 7.10 "SC16C554B/554DB external reset conditions" for initialization details.) When 16/$\overline{68}$ is a logic 0 (68 mode), this pin functions similarly, bus as an inverted reset interface signal, $\overline{\text{RESET}}$.
$\overline{\text{RIA}}$	8	63	18	-	I	**Ring Indicator (active LOW).** These inputs are associated with individual UART channels, A to D. A logic 0 on this pin indicates the modem has received a ringing signal from the telephone line. A logic 1 transition on this input pin will generate an interrupt.
RIB	28	19	43	-	I	
RIC	42	30	58	23	I	
RID	62	50	3	-	I	
$\overline{\text{RTSA}}$	14	5	26	3	O	**Request to Send (active LOW).** These outputs are associated with individual UART channels, A to D. A logic 0 on the $\overline{\text{RTS}}$n pin indicates the transmitter has data ready and waiting to send. Writing a logic 1 in the Modem Control Register MCR[1] will set this pin to a logic 0, indicating data is available. After a reset this pin will be set to a logic 1. This pin only affects the transmit and receive operations when auto-$\overline{\text{RTS}}$ function is enabled via MCR[5] for hardware flow control operation.
$\overline{\text{RTSB}}$	22	13	35	11	O	
$\overline{\text{RTSC}}$	48	36	66	29	O	
$\overline{\text{RTSD}}$	56	44	75	-	O	
R/$\overline{\text{W}}$	18	-	-	7	I	**Read/Write strobe.** This function is associated with the 68 mode only. This pin provides the combined functions for Read or Write strobes. Logic 1 = Read from UART register selected by $\overline{\text{CS}}$ and A0 to A4. Logic 0 = Write to UART register selected by $\overline{\text{CS}}$ and A0 to A4.
RXA	7	62	17	48	I	**Receive data input RXA to RXD.** These inputs are associated with individual serial channel data to the SC16C554B/554DB. The RXn signal will be a logic 1 during reset, idle (no data), or when the transmitter is disabled. During the local Loopback mode, the RXn input pin is disabled and TX data is connected to the UART RX input internally.
RXB	29	20	44	13	I	
RXC	41	29	57	22	I	
RXD	63	51	4	38	I	
$\overline{\text{RXRDY}}$	38	-	54	-	O	**Receive Ready (active LOW).** $\overline{\text{RXRDY}}$ contains the wire-ORed status of all four receive channel FIFOs, RXRDYA to RXRDYD. A logic 0 indicates receive data ready status, that is, the RHR is full, or the FIFO has one or more RX characters available for unloading. This pin goes to a logic 1 when the FIFO/RHR is empty, or when there are no more characters available in either the FIFO or RHR. Individual channel RX status is read by examining individual internal registers via $\overline{\text{CS}}$ and A0 to A4 pin functions. The $\overline{\text{RXRDY}}$ pin is not available on the HVQFN48 package.

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Table 2. Pin description *...continued*

Symbol	Pin				Type	Description
	PLCC68	LQFP64	LQFP80	HVQFN48		
TXA	17	8	29	6	O	**Transmit data A, B, C, D.** These outputs are associated with individual serial transmit channel data from the SC16C554B/554DB. The TX signal will be a logic 1 during reset, idle (no data), or when the transmitter is disabled. During the local Loopback mode, the TXn output pin is disabled and TX data is internally connected to the UART RX input.
TXB	19	10	32	8	O	
TXC	51	39	69	32	O	
TXD	53	41	72	34	O	
$\overline{\text{TXRDY}}$	39	-	55	-	O	**Transmit Ready (active LOW).** $\overline{\text{TXRDY}}$ contains the wire-ORed status of all four transmit channel FIFOs, TXRDYA to TXRDYD. A logic 0 indicates a buffer ready status, that is, at least one location is empty and available in one of the TX channels (A to D). This pin goes to a logic 1 when all four channels have no more empty locations in the TX FIFO or THR. Individual channel TX status can be read by examining individual internal registers via $\overline{\text{CS}}$ and A0 to A4 pin functions. The $\overline{\text{TXRDY}}$ pin is not available on the HVQFN48 package.
V_{CC}	13, 30, 47, 64	4, 21, 35, 52	5, 25, 45, 65	2, 28	I	**Power supply inputs.**
XTAL1	35	25	50	18	I	**Crystal or external clock input.** Functions as a crystal input or as an external clock input. A crystal can be connected between this pin and XTAL2 to form an internal oscillator circuit (see Figure 13). Alternatively, an external clock can be connected to this pin to provide custom data rates. (See Section 6.6 "Programmable baud rate generator".)
XTAL2	36	26	51	19	O	**Output of the crystal oscillator or buffered clock.** (See also XTAL1.) Crystal oscillator output or buffered clock output.

[1] HVQFN48 package die supply ground is connected to both GND pins and exposed center pad. GND pins must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board and for proper heat conduction through the board, thermal vias need to be incorporated in the PCB in the thermal pad region.

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6. Functional description

The SC16C554B/554DB provides serial asynchronous receive data synchronization, parallel-to-serial and serial-to-parallel data conversions for both the transmitter and receiver sections. These functions are necessary for converting the serial data stream into parallel data that is required with digital data systems. Synchronization for the serial data stream is accomplished by adding start and stop bits to the transmit data to form a data character. Data integrity is insured by attaching a parity bit to the data character. The parity bit is checked by the receiver for any transmission bit errors. The electronic circuitry to provide all these functions is fairly complex, especially when manufactured on a single integrated silicon chip. The SC16C554B/554DB represents such an integration with greatly enhanced features. The SC16C554B/554DB is fabricated with an advanced CMOS process to achieve low drain power and high speed requirements.

The SC16C554B/554DB is an upward solution that provides 16 bytes of transmit and receive FIFO memory, instead of none in the 16C454. The SC16C554B/554DB is designed to work with high speed modems and shared network environments that require fast data processing time. Increased performance is realized in the SC16C554B/554DB by the larger transmit and receive FIFOs. This allows the external processor to handle more networking tasks within a given time. In addition, the four selectable levels of FIFO trigger interrupt is uniquely provided for maximum data throughput performance, especially when operating in a multi-channel environment. The combination of the above greatly reduces the bandwidth requirement of the external controlling CPU, increases performance, and reduces power consumption.

The SC16C554B/554DBAI68 combines the package interface modes of the 16C454/554 and 68C454/554 series on a single integrated chip. The 16 mode interface is designed to operate with the Intel-type of microprocessor bus, while the 68 mode is intended to operate with Motorola and other popular microprocessors. Following a reset, the SC16C554B/554DBAI68 is downward compatible with the 16C454/554 or the 68C454/554, dependent on the state of the interface mode selection pin, 16/$\overline{68}$.

The SC16C554B/554DB is capable of operation to 1.5 Mbit/s with a 24 MHz crystal and up to 5 Mbit/s with an external clock input (at 3.3 V and 5 V; at 2.5 V the maximum speed is 3 Mbit/s).

The rich feature set of the SC16C554B/554DB is available through internal registers. Selectable receive FIFO trigger levels, selectable transmit and receive baud rates, and modem interface controls are all standard features. In the 16 mode, INTSEL and MCR[3] can be configured to provide a software controlled or continuous interrupt capability. Due to pin limitations of the 64-pin package, this feature is offered by two different LQFP64 packages. The SC16C554DB operates in the continuous interrupt enable mode by bonding INTSEL to V_{CC} internally. The SC16C554B operates in conjunction with MCR[3] by bonding INTSEL to GND internally.

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6.1 Interface options

Two user interface modes are selectable for the PLCC68 package. These interface modes are designated as the ‘16 mode’ and the ‘68 mode’. This nomenclature corresponds to the early 16C454/554 and 68C454/554 package interfaces respectively.

6.1.1 The 16 mode interface

The 16 mode configures the package interface pins for connection as a standard 16 series (Intel) device and operates similar to the standard CPU interface available on the 16C454/554. In the 16 mode (pin 16/$\overline{68}$ = logic 1), each UART is selected with individual chip select ($\overline{CSn}$) pins, as shown in Table 3.

Table 3. Serial port channel selection, 16 mode interface

$\overline{CSA}$	$\overline{CSB}$	$\overline{CSC}$	$\overline{CSD}$	UART channel
1	1	1	1	none
0	1	1	1	A
1	0	1	1	B
1	1	0	1	C
1	1	1	0	D

6.1.2 The 68 mode interface

The 68 mode configures the package interface pins for connection with Motorola, and other popular microprocessor bus types. The interface operates similar to the 68C454/554. In this mode, the SC16C554B/554DB decodes two additional addresses, A3 to A4, to select one of the four UART ports. The A3 to A4 address decode function is used only when in the 68 mode (16/$\overline{68}$ = logic 0), and is shown in Table 4.

Table 4. Serial port channel selection, 68 mode interface

$\overline{CS}$	A4	A3	UART channel
1	n/a	n/a	none
0	0	0	A
0	0	1	B
0	1	0	C
0	1	1	D

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6.2 Internal registers

The SC16C554B/554DB provides 12 internal registers for monitoring and control. These registers are shown in Table 5. These registers function as data holding registers (THR/RHR), interrupt status and control registers (IER/ISR), a FIFO Control Register (FCR), line status and control registers (LCR/LSR), modem status and control registers (MCR/MSR), programmable data rate (clock) control registers (DLL/DLM), and a user accessible Scratchpad Register (SPR). Register functions are more fully described in the following paragraphs.

Table 5. Internal registers decoding

A2	A1	A0	Read mode	Write mode
General register set (THR/RHR, IER/ISR, MCR/MSR, FCR, LCR/LSR, SPR)[1]				
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1	Interrupt Enable Register	Interrupt Enable Register
0	1	0	Interrupt Status Register	FIFO Control Register
0	1	1	Line Control Register	Line Control Register
1	0	0	Modem Control Register	Modem Control Register
1	0	1	Line Status Register	n/a
1	1	0	Modem Status Register	n/a
1	1	1	Scratchpad Register	Scratchpad Register
Baud rate register set (DLL/DLM)[2]				
0	0	0	LSB of Divisor Latch	LSB of Divisor Latch
0	0	1	MSB of Divisor Latch	MSB of Divisor Latch

[1] These registers are accessible only when LCR[7] is a logic 0.

[2] These registers are accessible only when LCR[7] is a logic 1.

6.3 FIFO operation

The 16 byte transmit and receive data FIFOs are enabled by the FIFO Control Register (FCR) bit 0. With SC16C554B devices, the user can set the receive trigger level, but not the transmit trigger level. The receiver FIFO section includes a time-out function to ensure data is delivered to the external CPU. An interrupt is generated whenever the Receive Holding Register (RHR) has not been read following the loading of a character or the receive trigger level has not been reached.

Table 6. Flow control mechanism

Selected trigger level (characters)	INTn pin activation	Negate $\overline{RTS}$	Assert $\overline{RTS}$
1	1	4	1
4	4	8	4
8	8	12	8
14	14	14	10

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6.4 Autoflow control (see Figure 9)

Autoflow control is comprised of auto-$\overline{\text{CTS}}$ and auto-$\overline{\text{RTS}}$. With auto-$\overline{\text{CTS}}$, the $\overline{\text{CTS}}$ input must be active before the transmitter FIFO can emit data. With auto-$\overline{\text{RTS}}$, $\overline{\text{RTS}}$ becomes active when the receiver needs more data and notifies the sending serial device. When $\overline{\text{RTS}}$ is connected to $\overline{\text{CTS}}$, data transmission does not occur unless the receiver FIFO has space for the data; thus, overrun errors are eliminated using UART 1 and UART 2 from a SC16C554B/554DB with the autoflow control enabled. If not, overrun errors occur when the transmit data rate exceeds the receiver FIFO read latency.

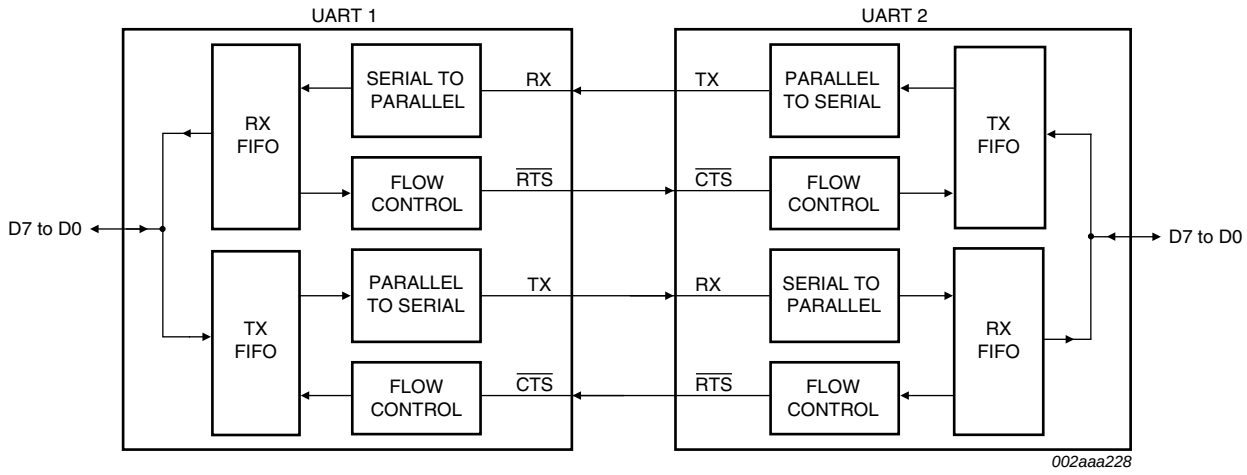


Fig 9. Autoflow control (auto-$\overline{\text{RTS}}$ and auto-$\overline{\text{CTS}}$) example

6.4.1 Auto-$\overline{\text{RTS}}$ (see Figure 9)

Auto-$\overline{\text{RTS}}$ data flow control originates in the receiver timing and control block (see block diagrams in Figure 1 and Figure 2) and is linked to the programmed receiver FIFO trigger level. When the receiver FIFO level reaches a trigger level of 1, 4, or 8 (see Figure 11), $\overline{\text{RTS}}$ is de-asserted. With trigger levels of 1, 4, and 8, the sending UART may send an additional byte after the trigger level is reached (assuming the sending UART has another byte to send) because it may not recognize the de-assertion of $\overline{\text{RTS}}$ until after it has begun sending the additional byte. $\overline{\text{RTS}}$ is automatically reasserted once the RX FIFO is emptied by reading the receiver buffer register. When the trigger level is 14 (see Figure 12), $\overline{\text{RTS}}$ is de-asserted after the first data bit of the 16th character is present on the RX line. $\overline{\text{RTS}}$ is reasserted when the RX FIFO has at least one available byte space.

Remark: Auto-$\overline{\text{RTS}}$ is not supported in channel D of the HVQFN48 package, therefore MCR[5] of channel D should not be written.

6.4.2 Auto-$\overline{\text{CTS}}$ (see Figure 9)

The transmitter circuitry checks $\overline{\text{CTS}}$ before sending the next data byte. When $\overline{\text{CTS}}$ is active, it sends the next byte. To stop the transmitter from sending the following byte, $\overline{\text{CTS}}$ must be released before the middle of the last stop bit that is currently being sent (see Figure 10). The auto-$\overline{\text{CTS}}$ function reduces interrupts to the host system. When flow control is enabled, $\overline{\text{CTS}}$ level changes do not trigger host interrupts because the device automatically controls its own transmitter. Without auto-$\overline{\text{CTS}}$, the transmitter sends any data present in the transmit FIFO and a receiver overrun error may result.

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Remark: Auto-$\overline{\text{CTS}}$ is not supported in channel D of the HVQFN48 package, therefore MCR[5] of channel D should not be written.

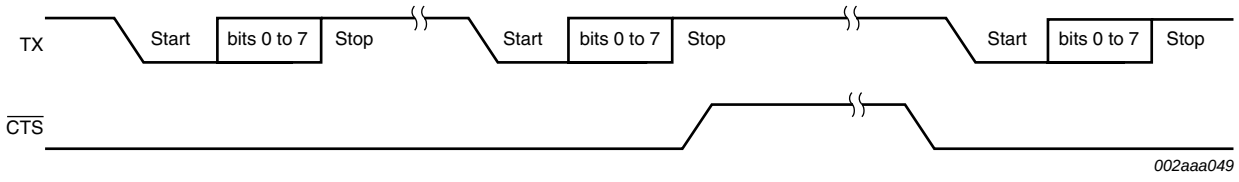
6.4.3 Enabling autoflow control and auto-$\overline{\text{CTS}}$

Autoflow control is enabled by setting MCR[5] and MCR[1].

Table 7. Enabling autoflow control and auto-$\overline{\text{CTS}}$

MCR[5]	MCR[1]	Selection
1	1	auto $\overline{\text{RTS}}$ and $\overline{\text{CTS}}$
1	0	auto $\overline{\text{CTS}}$
0	X	disable

6.4.4 Auto-$\overline{\text{CTS}}$ and auto-$\overline{\text{RTS}}$ functional timing



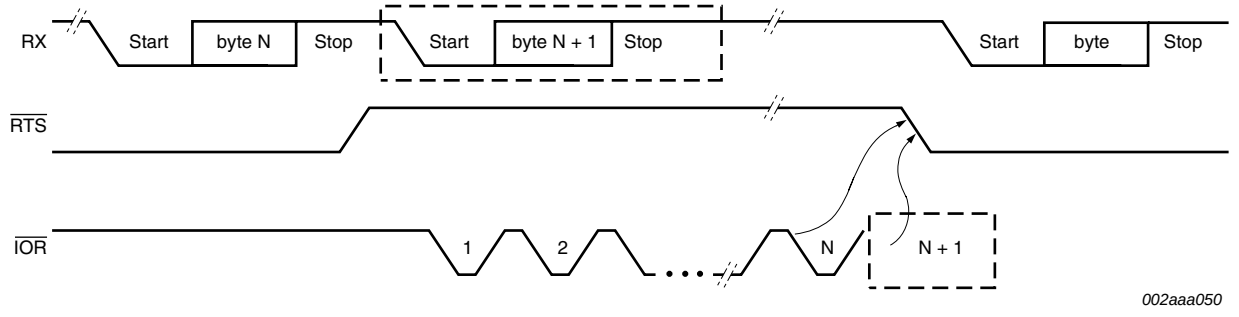
(1) When $\overline{\text{CTS}}$ is LOW, the transmitter keeps sending serial data out.

(2) If $\overline{\text{CTS}}$ goes HIGH before the middle of the last stop bit of the current byte, the transmitter finishes sending the current byte, but is does not send the next byte.

(3) When $\overline{\text{CTS}}$ goes from HIGH to LOW, the transmitter begins sending data again.

Fig 10. $\overline{\text{CTS}}$ functional timing waveforms

The receiver FIFO trigger level can be set to 1 byte, 4 bytes, 8 bytes, or 14 bytes. These are described in Figure 11 and Figure 12.



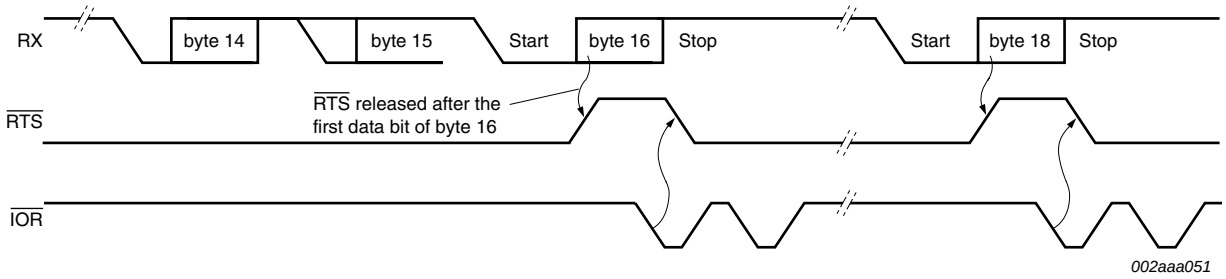
(1) N = RCV FIFO trigger level (1 byte, 4 bytes, or 8 bytes).

(2) The two blocks in dashed lines cover the case where an additional byte is sent as described in Section 6.4.1.

Fig 11. $\overline{\text{RTS}}$ functional timing waveforms, RCV FIFO trigger level = 1 byte, 4 bytes, or 8 bytes

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(1) $\overline{RTS}$ is de-asserted when the receiver receives the first data bit of the sixteenth byte. The receive FIFO is full after finishing the sixteenth byte.

(2) $\overline{RTS}$ is asserted again when there is at least one byte of space available and no incoming byte is in processing, or there is more than one byte of space available.

(3) When the receive FIFO is full, the first receive buffer register read re-asserts $\overline{RTS}$.

Fig 12. $\overline{RTS}$ functional timing waveforms, RCV FIFO trigger level = 14 bytes

6.5 Hardware/software and time-out interrupts

Following a reset, if the transmitter interrupt is enabled, the SC16C554B/554DB will issue an interrupt to indicate that the Transmit Holding Register is empty. This interrupt must be serviced prior to continuing operations. The LSR register provides the current singular highest priority interrupt only. Only after servicing the higher pending interrupt will the lower priority interrupt(s) be reflected in the status register. Servicing the interrupt without investigating further interrupt conditions can result in data errors.

When two interrupt conditions have the same priority, it is important to service these interrupts correctly. Receive Data Ready and Receive Time-Out have the same interrupt priority (when enabled by IER[0]). The receiver issues an interrupt after the number of characters have reached the programmed trigger level. In this case, the SC16C554B/554DB FIFO may hold more characters than the programmed trigger level. Following the removal of a data byte, the user should re-check LSR[0] for additional characters. A Receive Time-Out will not occur if the receive FIFO is empty. The time-out counter is reset at the center of each stop bit received or each time the Receive Holding Register (RHR) is read. The actual time-out value is 4 character time.

In the 16 mode for the PLCC68 package, the system/board designer can optionally provide software controlled 3-state interrupt operation. This is accomplished by INTSEL and MCR[3]. When INTSEL interface pin is left open or made a logic 0, MCR[3] controls the 3-state interrupt outputs, INTA to INTD. When INTSEL is a logic 1, MCR[3] has no effect on the INTA to INTD outputs, and the package operates with interrupt outputs enabled continuously.

6.6 Programmable baud rate generator

The SC16C554B/554DB supports high speed modem technologies that have increased input data rates by employing data compression schemes. For example, a 33.6 kbit/s modem that employs data compression may require a 115.2 kbit/s input data rate. A 128.0 kbit/s ISDN modem that supports data compression may need an input data rate of 460.8 kbit/s.

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A single baud rate generator is provided for the transmitter and receiver, allowing independent TX/RX channel control. The programmable Baud Rate Generator is capable of accepting an input clock up to 80 MHz (for 3.3 V and 5 V operation), as required for supporting a 5 Mbit/s data rate. The SC16C554B/554DB can be configured for internal or external clock operation. For internal clock oscillator operation, an industry standard microprocessor crystal (parallel resonant/22 pF to 33 pF load) is connected externally between the XTAL1 and XTAL2 pins (see Figure 13). Alternatively, an external clock can be connected to the XTAL1 pin to clock the internal baud rate generator for standard or custom rates (see Table 8).

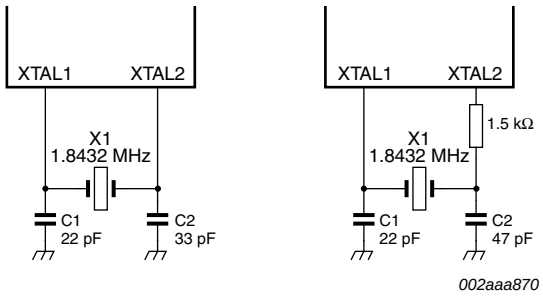


Fig 13. Crystal oscillator connection

Programming the Baud Rate Generator registers DLM (MSB) and DLL (LSB) provides a user capability for selecting the desired final baud rate.

Table 8. Baud rate generator programming table using a 7.3728 MHz clock

Output baud rate (bit/s)	User 16× clock divisor		DLM program value (hex)	DLL program value (hex)
	Decimal	Hexadecimal		
200	2304	900	09	00
1200	384	180	01	80
2400	192	C0	00	C0
4800	96	60	00	60
9600	48	30	00	30
19.2 k	24	18	00	18
38.4 k	12	0C	00	0C
76.8 k	6	06	00	06
153.6 k	3	03	00	03
230.4 k	2	02	00	02
460.8 k	1	01	00	01

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6.7 DMA operation

The SC16C554B/554DB FIFO trigger level provides additional flexibility to the user for block mode operation. LSR[6:5] provide an indication when the transmitter is empty or has an empty location(s). The user can optionally operate the transmit and receive FIFOs in the DMA mode (FCR[3]). When the transmit and receive FIFOs are enabled and the DMA mode is de-activated (DMA Mode 0), the SC16C554B/554DB activates the interrupt output pin for each data transmit or receive operation. When DMA mode is activated (DMA Mode 1), the user takes the advantage of block mode operation by loading or unloading the FIFO in a block sequence determined by the preset trigger level. In this mode, the SC16C554B/554DB sets the interrupt output pin when the characters in the receive FIFOs are above the receive trigger level.

Remark: DMA operation is not supported in the HVQFN48 package.

6.8 Loopback mode

The internal loopback capability allows on-board diagnostics. In the Loopback mode, the normal modem interface pins are disconnected and reconfigured for loopback internally. MCR[3:0] register bits are used for controlling loopback diagnostic testing. In the Loopback mode, $\overline{OP2}$ and $\overline{OP1}$ in the MCR register (bits 3:2) control the modem $\overline{RI}$ and $\overline{CD}$ inputs, respectively. MCR signals $\overline{RTS}$ and $\overline{DTR}$ (bits 1:0) are used to control the modem $\overline{CTS}$ and $\overline{DSR}$ inputs, respectively. The transmitter output (TX) and the receiver input (RX) are disconnected from their associated interface pins, and instead are connected together internally (see Figure 14). The $\overline{CTS}$, $\overline{DSR}$, $\overline{CD}$, and $\overline{RI}$ are disconnected from their normal modem control input pins, and instead are connected internally to $\overline{RTS}$, $\overline{DTR}$, $\overline{OP2}$ and $\overline{OP1}$. Loopback test data is entered into the Transmit Holding Register via the user data bus interface, D0 to D7. The transmit UART serializes the data and passes the serial data to the receive UART via the internal loopback connection. The receive UART converts the serial data back into parallel data that is then made available at the user data interface D0 to D7. The user optionally compares the received data to the initial transmitted data for verifying error-free operation of the UART TX/RX circuits.

In this mode, the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational. However, the interrupts can only be read using lower four bits of the Modem Status Register (MSR[3:0]) instead of the four Modem Status Register bits 7:4. The interrupts are still controlled by the IER.

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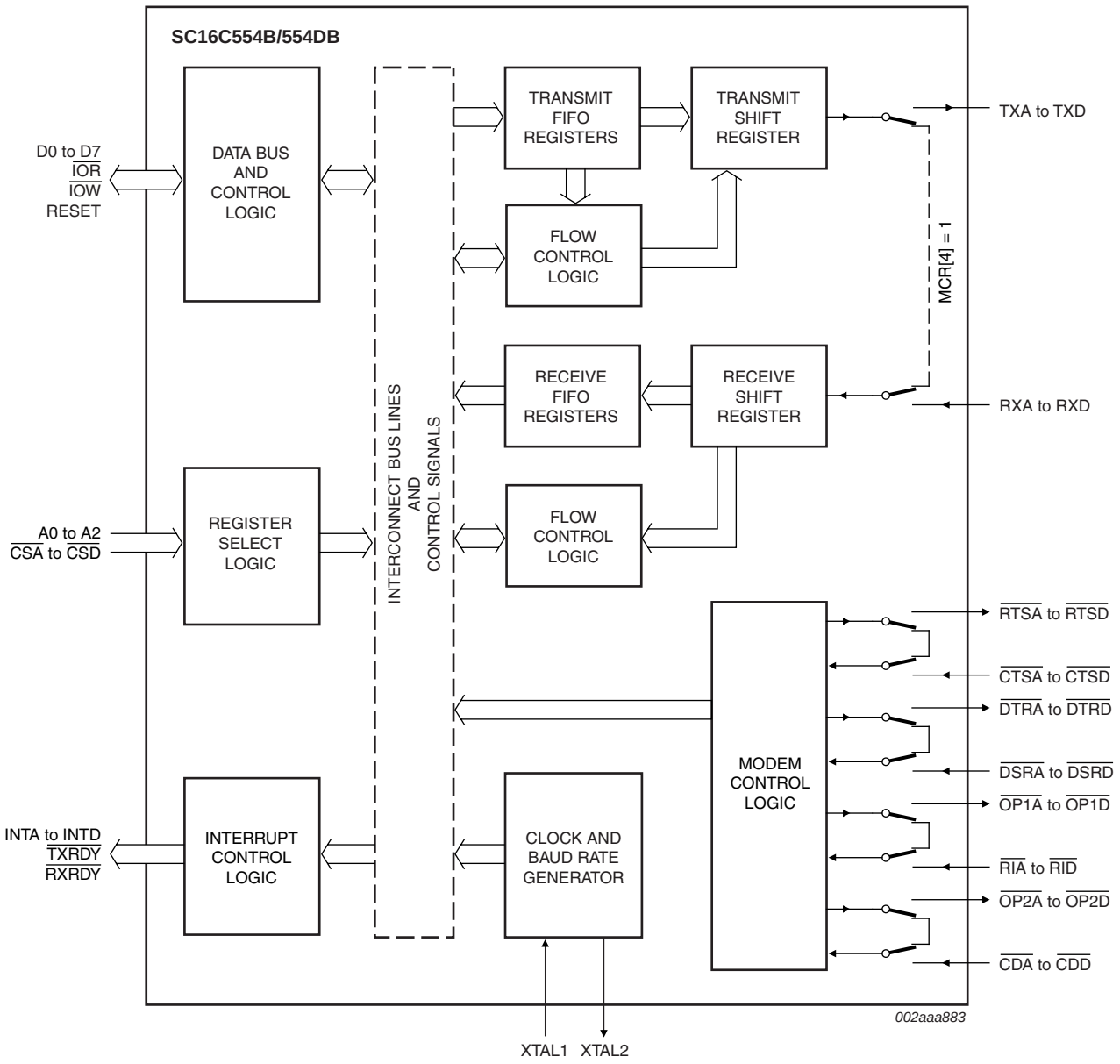


Fig 14. Internal Loopback mode diagram (16 mode)

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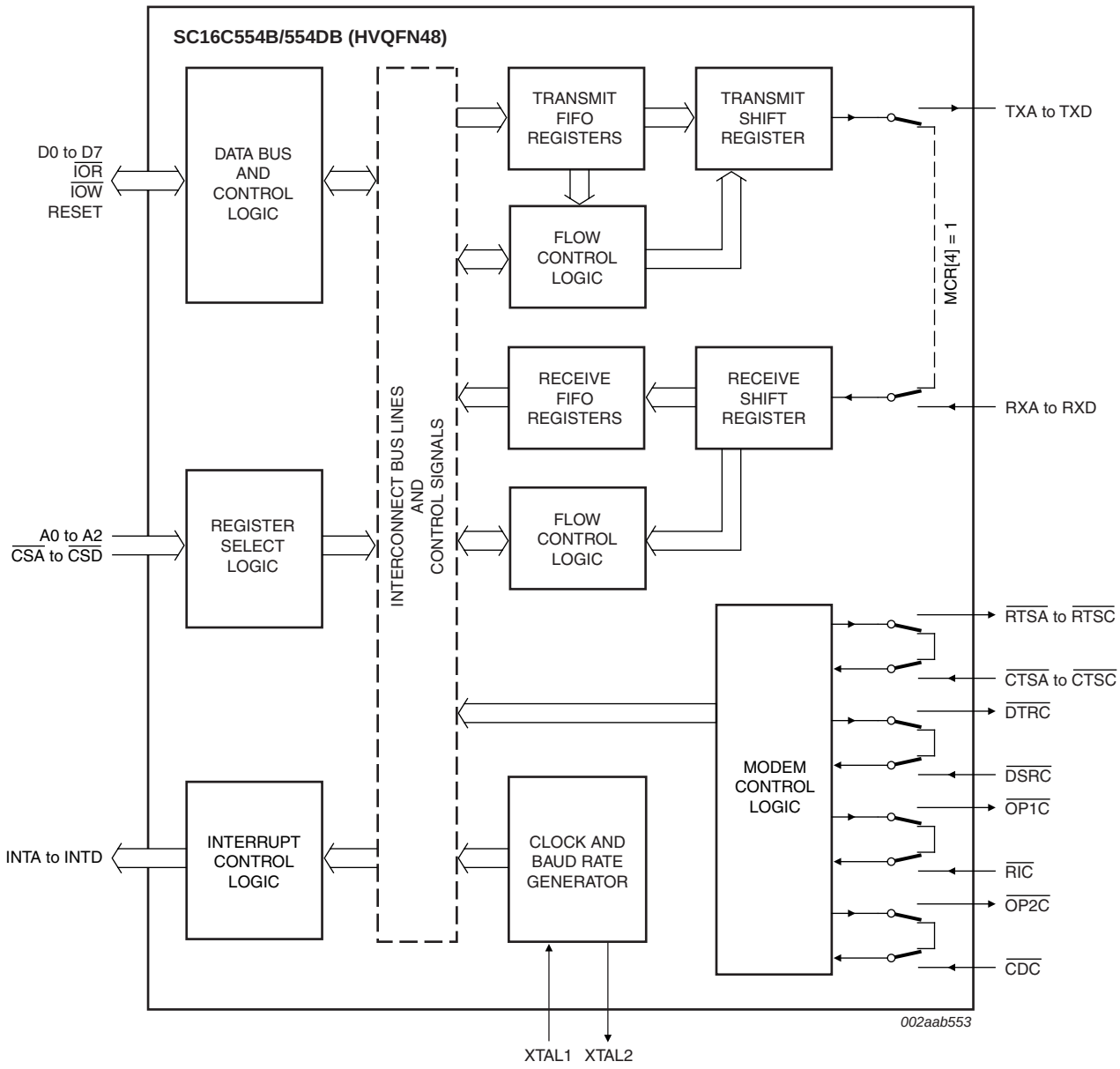


Fig 15. Internal Loopback mode diagram (16 mode) for HVQFN48 package

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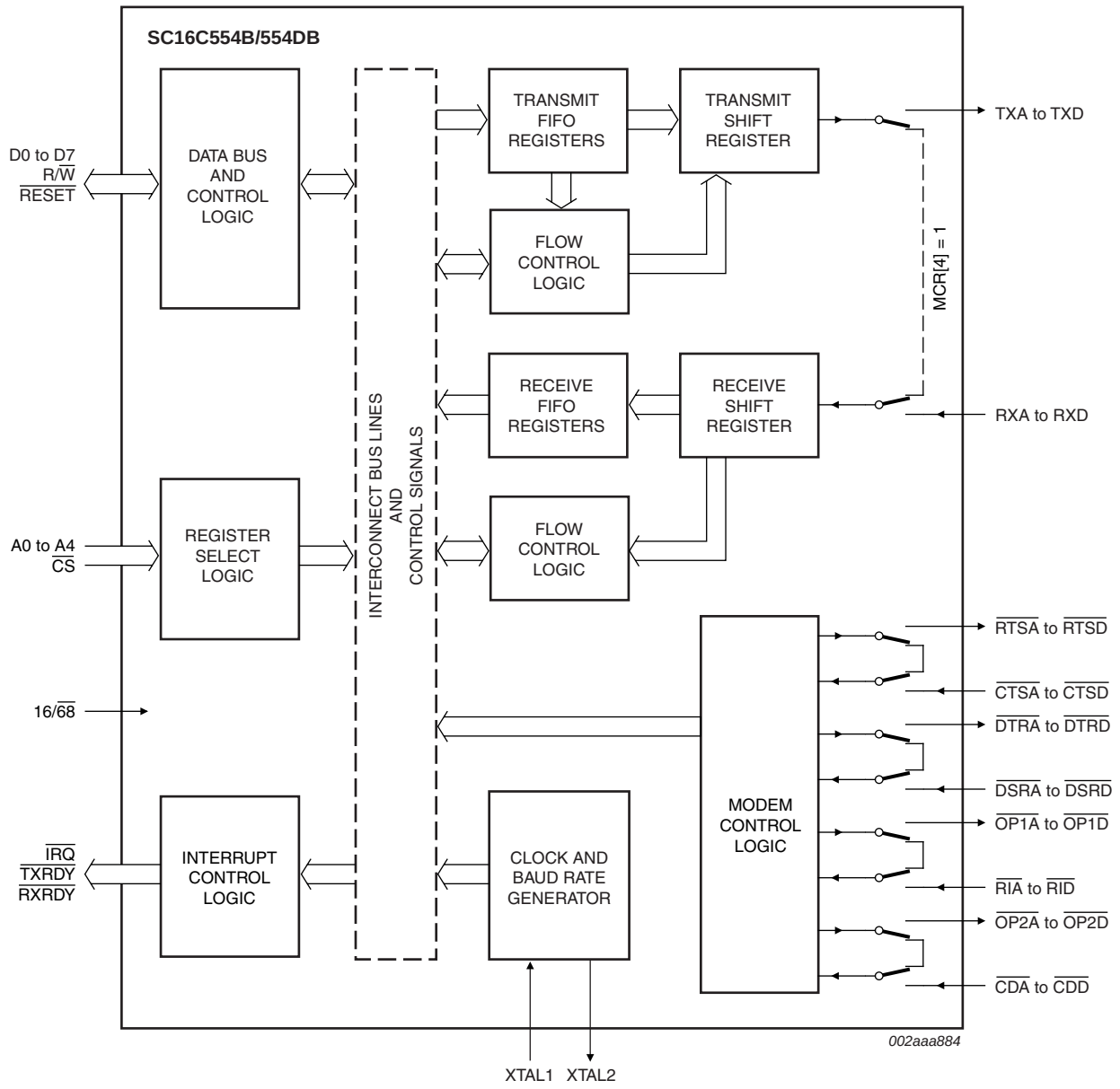


Fig 16. Internal Loopback mode diagram (68 mode)

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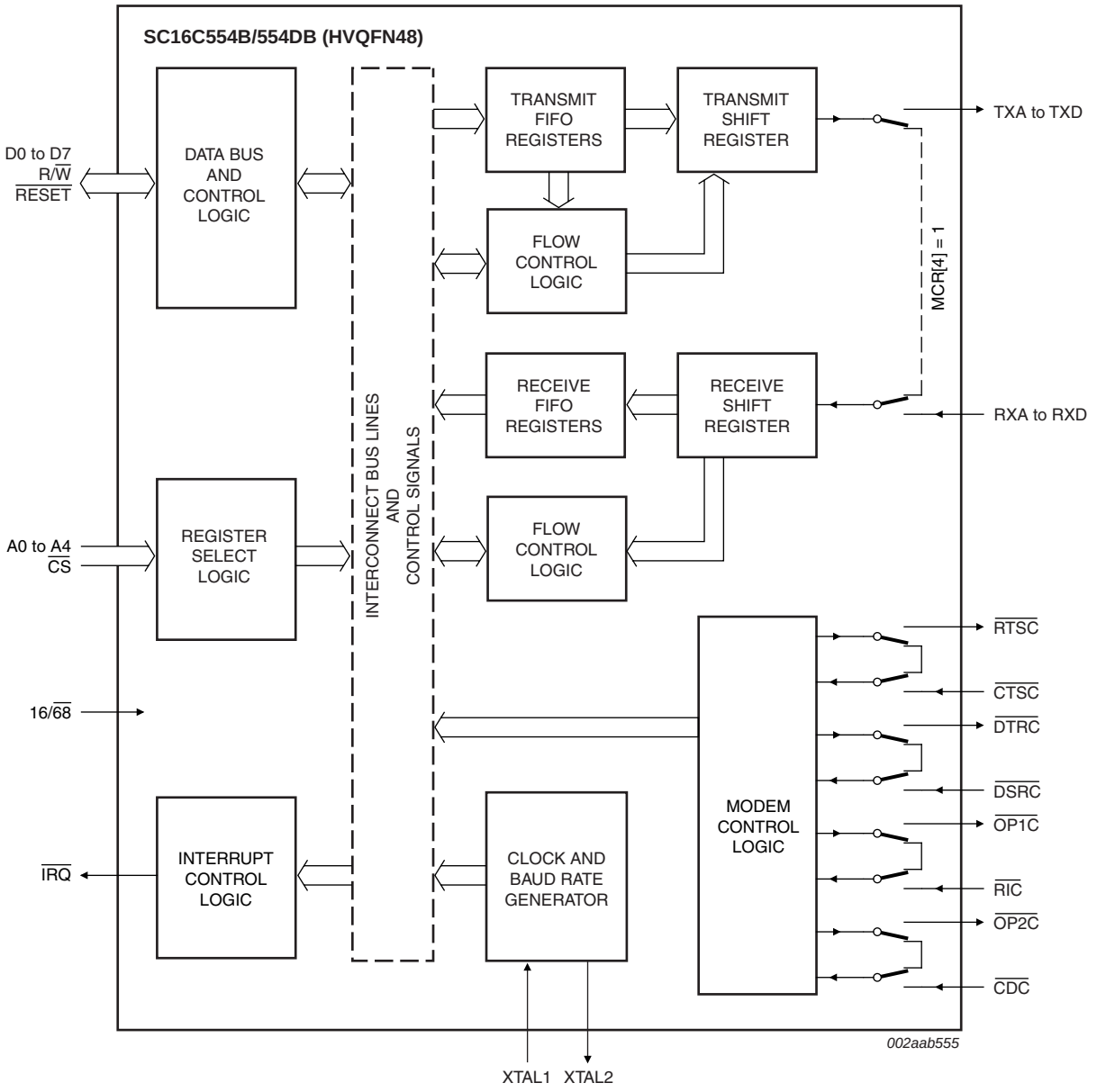


Fig 17. Internal Loopback mode diagram (68 mode) for HVQFN48 package

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7. Register descriptions

Table 9 details the assigned bit functions for the SC16C554B/554DB internal registers. The assigned bit functions are more fully defined in Section 7.1 through Section 7.10.

Table 9. SC16C554B/554DB internal registers

A2	A1	A0	Register	Default[1]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
General Register set[2]												
0	0	0	RHR	XX	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	0	0	THR	XX	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	0	1	IER	00	0	0	0	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0	1	0	FCR	00	RCVR trigger (MSB)	RCVR trigger (LSB)	reserved	reserved	DMA mode select[3]	XMIT FIFO reset	RCVR FIFO reset	FIFO enable
0	1	0	ISR	01	FIFOs enabled	FIFOs enabled	0	0	INT priority bit 2	INT priority bit 1	INT priority bit 0	INT status
0	1	1	LCR	00	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit 1	word length bit 0
1	0	0	MCR	00	0	0	autoflow control enable[4]	loop back	$\overline{OP2}$, INTn enable	$\overline{OP1}$	$\overline{RTS}$	$\overline{DTR}$
1	0	1	LSR	60	FIFO data error	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1	1	0	MSR	X0	CD	RI	DSR	CTS	$\Delta\overline{CD}$	$\Delta\overline{RI}$	$\Delta\overline{DSR}$	$\Delta\overline{CTS}$
1	1	1	SPR	FF	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Special Register set[5]												
0	0	0	DLL	XX	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	0	1	DLM	XX	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8

[1] The value shown represents the register's initialized hexadecimal value; X = not applicable.

[2] These registers are accessible only when LCR[7] = 0.

[3] This function is not supported in the HVQFN48 package.

[4] Autoflow control is not supported by channel D of the HVQFN48 package, and this bit should not be written on channel D.

[5] The Special Register set is accessible only when LCR[7] is set to a logic 1.

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7.1 Transmit Holding Register (THR) and Receive Holding Register (RHR)

The serial transmitter section consists of an 8-bit Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the THR is provided in the Line Status Register (LSR). Writing to the THR transfers the contents of the data bus (D7 to D0) to the THR, providing that the THR or TSR is empty. The THR empty flag in the LSR register will be set to a logic 1 when the transmitter is empty or when data is transferred to the TSR. Note that a write operation can be performed when the THR empty flag is set (logic 0 = FIFO full; logic 1 = at least one FIFO location available).

The serial receive section also contains an 8-bit Receive Holding Register (RHR). Receive data is removed from the SC16C554B/554DB and receive FIFO by reading the RHR register. The receive section provides a mechanism to prevent false starts. On the falling edge of a start or false start bit, an internal receiver counter starts counting clocks at the 16× clock rate. After $7\frac{1}{2}$ clocks, the start bit time should be shifted to the center of the start bit. At this time the start bit is sampled, and if it is still a logic 0 it is validated. Evaluating the start bit in this manner prevents the receiver from assembling a false character. Receiver status codes will be posted in the LSR.

7.2 Interrupt Enable Register (IER)

The Interrupt Enable Register (IER) masks the interrupts from receiver ready, transmitter empty, line status and modem status registers. These interrupts would normally be seen on the INTA to INTD output pins in the 16 mode, or on wire-OR IRQ output pin in the 68 mode.

Table 10. Interrupt Enable Register bits description

Bit	Symbol	Description
7:4	IER[7:4]	Reserved; set to ‘0’.
3	IER[3]	Modem status interrupt. logic 0 = disable the modem status register interrupt (normal default condition) logic 1 = enable the modem status register interrupt
2	IER[2]	Receive line status interrupt. logic 0 = disable the receiver line status interrupt (normal default condition) logic 1 = enable the receiver line status interrupt
1	IER[1]	Transmit Holding Register interrupt. This interrupt will be issued whenever the THR is empty, and is associated with LSR[1]. logic 0 = disable the transmitter empty interrupt (normal default condition) logic 1 = enable the transmitter empty interrupt
0	IER[0]	Receive Holding Register interrupt. This interrupt will be issued when the FIFO has reached the programmed trigger level, or is cleared when the FIFO drops below the trigger level in the FIFO mode of operation. logic 0 = disable the receiver ready interrupt (normal default condition) logic 1 = enable the receiver ready interrupt

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7.2.1 IER versus Receive FIFO interrupt mode operation

When the receive FIFO (FCR[0] = logic 1), and receive interrupts (IER[0] = logic 1) are enabled, the receive interrupts and register status will reflect the following:

- The receive data available interrupts are issued to the external CPU when the FIFO has reached the programmed trigger level. It will be cleared when the FIFO drops below the programmed trigger level.
- FIFO status will also be reflected in the user accessible ISR register when the FIFO trigger level is reached. Both the ISR register status bit and the interrupt will be cleared when the FIFO drops below the trigger level.
- The data ready bit (LSR[0]) is set as soon as a character is transferred from the shift register to the receive FIFO. It is reset when the FIFO is empty.

7.2.2 IER versus Receive/Transmit FIFO polled mode operation

When FCR[0] = logic 1, resetting IER[3:0] enables the SC16C554B/554DB in the FIFO polled mode of operation. Since the receiver and transmitter have separate bits in the LSR, either or both can be used in the polled mode by selecting respective transmit or receive control bit(s).

- LSR[0] will be a logic 1 as long as there is one byte in the receive FIFO.
- LSR[4:1] will provide the type of errors encountered, if any.
- LSR[5] will indicate when the transmit FIFO is empty.
- LSR[6] will indicate when both the transmit FIFO and Transmit Shift Register are empty.
- LSR[7] will indicate any FIFO data errors.

7.3 FIFO Control Register (FCR)

This register is used to enable the FIFOs, clear the FIFOs, set the receive FIFO trigger levels, and select the DMA mode.

7.3.1 DMA mode

7.3.1.1 Mode 0 (FCR bit 3 = 0)

Set and enable the interrupt for each single transmit or receive operation, and is similar to the 16C454 mode. Transmit Ready ($\overline{\text{TXRDY}}$) will go to a logic 0 whenever an empty transmit space is available in the Transmit Holding Register (THR). Receive Ready ($\overline{\text{RXRDY}}$) will go to a logic 0 whenever the Receive Holding Register (RHR) is loaded with a character.

7.3.1.2 Mode 1 (FCR bit 3 = 1)

Set and enable the interrupt in a block mode operation. The transmit interrupt is set when there are one or more FIFO locations empty. The receive interrupt is set when the receive FIFO fills to the programmed trigger level. However, the FIFO continues to fill regardless of the programmed level until the FIFO is full. $\overline{\text{RXRDY}}$ remains a logic 0 as long as the FIFO fill level is above the programmed trigger level.

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7.3.2 FIFO mode

Table 11. FIFO Control Register bits description

Bit	Symbol	Description
7:6	FCR[7:6]	RCVR trigger. These bits are used to set the trigger level for the receive FIFO interrupt. An interrupt is generated when the number of characters in the FIFO equals the programmed trigger level. However, the FIFO will continue to be loaded until it is full. Refer to Table 12.
5:4	FCR[5:4]	not used; initialized to logic 0
3	FCR[3]	DMA mode select. logic 0 = set DMA mode '0' (normal default condition) logic 1 = set DMA mode '1' **Transmit operation in mode '0':** When the SC16C554B/554DB is in the 16C450 mode (FIFOs disabled; FCR[0] = logic 0) or in the FIFO mode (FIFOs enabled; FCR[0] = logic 1; FCR[3] = logic 0), and when there are no characters in the transmit FIFO or Transmit Holding Register, the $\overline{\text{TXRDY}}$ pin will be a logic 0. Once active, the $\overline{\text{TXRDY}}$ pin will go to a logic 1 after the first character is loaded into the Transmit Holding Register. **Receive operation in mode '0':** When the SC16C554B/554DB is in mode '0' (FCR[0] = logic 0), or in the FIFO mode (FCR[0] = logic 1; FCR[3] = logic 0) and there is at least one character in the receive FIFO, the $\overline{\text{RXRDY}}$ pin will be a logic 0. Once active, the $\overline{\text{RXRDY}}$ pin will go to a logic 1 when there are no more characters in the receiver. **Transmit operation in mode '1':** When the SC16C554B/554DB is in FIFO mode (FCR[0] = logic 1; FCR[3] = logic 1), the $\overline{\text{TXRDY}}$ pin will be a logic 1 when the transmit FIFO is completely full. It will be a logic 0 if one or more FIFO locations are empty. **Receive operation in mode '1':** When the SC16C554B/554DB is in FIFO mode (FCR[0] = logic 1; FCR[3] = logic 1) and the trigger level has been reached, or a Receive Time-out has occurred, the $\overline{\text{RXRDY}}$ pin will go to a logic 0. Once activated, it will go to a logic 1 after there are no more characters in the FIFO.
2	FCR[2]	XMIT FIFO reset. logic 0 = no FIFO transmit reset (normal default condition) logic 1 = clears the contents of the transmit FIFO and resets the FIFO counter logic (the Transmit Shift Register is not cleared or altered). This bit will return to a logic 0 after clearing the FIFO.
1	FCR[1]	RCVR FIFO reset. logic 0 = no FIFO receive reset (normal default condition) logic 1 = clears the contents of the receive FIFO and resets the FIFO counter logic (the Receive Shift Register is not cleared or altered). This bit will return to a logic 0 after clearing the FIFO.
0	FCR[0]	FIFO enable. logic 0 = disable the transmit and receive FIFO (normal default condition) logic 1 = enable the transmit and receive FIFO. **This bit must be a 1 when other FCR bits are written to, or they will not be programmed.**

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Table 12. RCVR trigger levels

FCR[7]	FCR[6]	RX FIFO trigger level
0	0	1
0	1	4
1	0	8
1	1	14

7.4 Interrupt Status Register (ISR)

The SC16C554B/554DB provides four levels of prioritized interrupts to minimize external software interaction. The Interrupt Status Register (ISR) provides the user with four interrupt status bits. Performing a read cycle on the ISR will provide the user with the highest pending interrupt level to be serviced. No other interrupts are acknowledged until the pending interrupt is serviced. Whenever the Interrupt Status Register is read, the interrupt status is cleared. However, it should be noted that only the current pending interrupt is cleared by the read. A lower level interrupt may be seen after re-reading the interrupt status bits. Table 13 “Interrupt source” shows the data values (bits 0 to 5) for the four prioritized interrupt levels and the interrupt sources associated with each of these interrupt levels.

Table 13. Interrupt source

Priority level	ISR[5]	ISR[4]	ISR[3]	ISR[2]	ISR[1]	ISR[0]	Source of the interrupt
1	0	0	0	1	1	0	LSR (Receiver Line Status Register)
2	0	0	0	1	0	0	RXRDY (Receive Data Ready)
2	0	0	1	1	0	0	RXRDY (Receive Data time-out)
3	0	0	0	0	1	0	TXRDY (Transmitter Holding Register Empty)
4	0	0	0	0	0	0	MSR (Modem Status Register)

Table 14. Interrupt Status Register bits description

Bit	Symbol	Description
7:6	ISR[7:6]	FIFOs enabled. These bits are set to a logic 0 when the FIFO is not being used. They are set to a logic 1 when the FIFOs are enabled. logic 0 or cleared = default condition
5:4	ISR[5:4]	Reserved; set to 0.
3:1	ISR[3:1]	INT priority bits 2 to 0. These bits indicate the source for a pending interrupt at interrupt priority levels 1, 2, and 3 (see Table 13). logic 0 or cleared = default condition
0	ISR[0]	INT status. logic 0 = an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine logic 1 = no interrupt pending (normal default condition)

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7.5 Line Control Register (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The word length, the number of stop bits, and the parity are selected by writing the appropriate bits in this register.

Table 15. Line Control Register bits description

Bit	Symbol	Description
7	LCR[7]	Divisor latch enable. The internal baud rate counter latch and Enhance Feature mode enable. logic 0 = divisor latch disabled (normal default condition) logic 1 = divisor latch enabled
6	LCR[6]	Set break. When enabled, the Break control bit causes a break condition to be transmitted (the TX output is forced to a logic 0 state). This condition exists until disabled by setting LCR[6] to a logic 0. logic 0 = no TX break condition (normal default condition) logic 1 = forces the transmitter output (TX) to a logic 0 for alerting the remote receiver to a line break condition
5	LCR[5]	Set parity. If the parity bit is enabled, LCR[5] selects the forced parity format. Programs the parity conditions (see Table 16). logic 0 = parity is not forced (normal default condition) LCR[5] = logic 1 and LCR[4] = logic 0: parity bit is forced to a logic 1 for the transmit and receive data LCR[5] = logic 1 and LCR[4] = logic 1: parity bit is forced to a logic 0 for the transmit and receive data
4	LCR[4]	Even parity. If the parity bit is enabled with LCR[3] set to a logic 1, LCR[4] selects the even or odd parity format. logic 0 = odd parity is generated by forcing an odd number of logic 1s in the transmitted data. The receiver must be programmed to check the same format (normal default condition). logic 1 = even parity is generated by forcing an even number of logic 1s in the transmitted data. The receiver must be programmed to check the same format.
3	LCR[3]	Parity enable. Parity or no parity can be selected via this bit. logic 0 = no parity (normal default condition) logic 1 = a parity bit is generated during the transmission, receiver checks the data and parity for transmission errors
2	LCR[2]	Stop bits. The length of stop bit is specified by this bit in conjunction with the programmed word length (see Table 17). logic 0 or cleared = default condition
1:0	LCR[1:0]	Word length bits 1, 0. These two bits specify the word length to be transmitted or received (see Table 18). logic 0 or cleared = default condition

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Table 16. LCR[5] parity selection

LCR[5]	LCR[4]	LCR[3]	Parity selection
X	X	0	no parity
0	0	1	odd parity
0	1	1	even parity
1	0	1	forced parity ‘1’
1	1	1	forced parity ‘0’

Table 17. LCR[2] stop bit length

LCR[2]	Word length (bits)	Stop bit length (bit times)
0	5, 6, 7, 8	1
1	5	$1\frac{1}{2}$
1	6, 7, 8	2

Table 18. LCR[1:0] word length

LCR[1]	LCR[0]	Word length (bits)
0	0	5
0	1	6
1	0	7
1	1	8

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7.6 Modem Control Register (MCR)

This register controls the interface with the modem or a peripheral device.

Table 19. Modem Control Register bits description

Bit	Symbol	Description
7:6	MCR[7:6]	Reserved; set to '0'.
5	MCR[5]	Autoflow control enable.
4	MCR[4]	Loopback. Enable the local Loopback mode (diagnostics). In this mode the transmitter output (TXn) and the receiver input (RXn), $\overline{CTS}$, $\overline{DSR}$, $\overline{CD}$, and $\overline{RI}$ are disconnected from the SC16C554B/554DB I/O pins. Internally the modem data and control pins are connected into a loopback data configuration (see Figure 14). In this mode, the receiver and transmitter interrupts remain fully operational. The Modem Control Interrupts are also operational, but the interrupts' sources are switched to the lower four bits of the Modem Control. Interrupts continue to be controlled by the IER register. logic 0 = disable Loopback mode (normal default condition) logic 1 = enable local Loopback mode (diagnostics)
3	MCR[3]	$\overline{OP2}$, INTn enable. Used to control the modem $\overline{CD}$ signal in the Loopback mode. logic 0 = forces INTA to INTD outputs to the 3-state mode during the 16 mode (normal default condition). In the Loopback mode, sets $\overline{OP2}$ ($\overline{CD}$) internally to a logic 1. logic 1 = forces the INTA to INTD outputs to the active mode during the 16 mode. In the Loopback mode, sets $\overline{OP2}$ ($\overline{CD}$) internally to a logic 0.
2	MCR[2]	$\overline{OP1}$. This bit is used in the Loopback mode only. In the Loopback mode, this bit is used to write the state of the modem $\overline{RI}$ interface signal via $\overline{OP1}$.
1	MCR[1]	$\overline{RTS}$ logic 0 = force $\overline{RTS}$ output to a logic 1 (normal default condition) logic 1 = force $\overline{RTS}$ output to a logic 0 Automatic $\overline{RTS}$ may be used for hardware flow control by enabling MCR[5].
0	MCR[0]	$\overline{DTR}$ logic 0 = force $\overline{DTR}$ output to a logic 1 (normal default condition) logic 1 = force $\overline{DTR}$ output to a logic 0

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7.7 Line Status Register (LSR)

This register provides the status of data transfers between the SC16C554B/554DB and the CPU.

Table 20. Line Status Register bits description

Bit	Symbol	Description
7	LSR[7]	FIFO data error. logic 0 = no error (normal default condition) logic 1 = at least one parity error, framing error or break indication is in the current FIFO data. This bit is cleared when LSR register is read.
6	LSR[6]	THR and TSR empty. This bit is the Transmit Empty indicator. This bit is set to a logic 1 whenever the Transmit Holding Register and the Transmit Shift Register are both empty. It is reset to logic 0 whenever either the THR or TSR contains a data character. In the FIFO mode, this bit is set to logic 1 whenever the transmit FIFO and Transmit Shift Register are both empty.
5	LSR[5]	THR empty. This bit is the Transmit Holding Register Empty indicator. This bit indicates that the UART is ready to accept a new character for transmission. In addition, this bit causes the UART to issue an interrupt to CPU when the THR interrupt enable is set. The THR bit is set to a logic 1 when a character is transferred from the Transmit Holding Register into the Transmitter Shift Register. The bit is reset to a logic 0 concurrently with the loading of the transmitter holding register by the CPU. In the FIFO mode, this bit is set when the transmit FIFO is empty; it is cleared when at least 1 byte is written to the transmit FIFO.
4	LSR[4]	Break interrupt. logic 0 = no break condition (normal default condition) logic 1 = the receiver received a break signal (RX was a logic 0 for one character frame time). In the FIFO mode, only one break character is loaded into the FIFO.
3	LSR[3]	Framing error. logic 0 = no framing error (normal default condition) logic 1 = framing error. The receive character did not have a valid stop bit(s). In the FIFO mode, this error is associated with the character at the top of the FIFO.
2	LSR[2]	Parity error. logic 0 = no parity error (normal default condition) logic 1 = parity error. The receive character does not have correct parity information and is suspect. In the FIFO mode, this error is associated with the character at the top of the FIFO.
1	LSR[1]	Overrun error. logic 0 = no overrun error (normal default condition) logic 1 = overrun error. A data overrun error occurred in the Receive Shift Register. This happens when additional data arrives while the FIFO is full. In this case, the previous data in the shift register is overwritten. Note that under this condition, the data byte in the Receive Shift Register is not transferred into the FIFO, therefore the data in the FIFO is not corrupted by the error.
0	LSR[0]	Receive data ready. logic 0 = no data in Receive Holding Register or FIFO (normal default condition) logic 1 = data has been received and is saved in the Receive Holding Register or FIFO

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7.8 Modem Status Register (MSR)

This register provides the current state of the control interface signals from the modem, or other peripheral device to which the SC16C554B/554DB is connected. Four bits of this register are used to indicate the changed information. These bits are set to a logic 1 whenever a control input from the modem changes state. These bits are set to a logic 0 whenever the CPU reads this register.

Table 21. Modem Status Register bits description

Bit	Symbol	Description
7	MSR[7]	CD (active HIGH, logic 1). Normally this bit is the complement of the $\overline{CD}$ input. In the Loopback mode this bit is equivalent to the $\overline{OP2}$ bit in the MCR register.
6	MSR[6]	RI (active HIGH, logic 1). Normally this bit is the complement of the $\overline{RI}$ input. In the Loopback mode this bit is equivalent to the $\overline{OP1}$ bit in the MCR register.
5	MSR[5]	DSR (active HIGH, logic 1). Normally this bit is the complement of the $\overline{DSR}$ input. In Loopback mode this bit is equivalent to the DTR bit in the MCR register.
4	MSR[4]	CTS (active HIGH, logic 1). $\overline{CTS}$ functions as hardware flow control signal input if it is enabled via MCR[5]. Flow control (when enabled) allows starting and stopping the transmissions based on the external modem $\overline{CTS}$ signal. A logic 1 at the $\overline{CTS}$ pin will stop SC16C554B/554DB transmissions as soon as current character has finished transmission. Normally MSR[4] is the complement of the $\overline{CTS}$ input. However, in the Loopback mode, this bit is equivalent to the RTS bit in the MCR register.
3	MSR[3]	$\Delta\overline{CD}$ [1] Logic 0 = No $\overline{CD}$ change (normal default condition). Logic 1 = The $\overline{CD}$ input to the SC16C554B/554DB has changed state since the last time it was read. A modem Status Interrupt will be generated.
2	MSR[2]	$\Delta\overline{RI}$ [1] Logic 0 = No $\overline{RI}$ change (normal default condition). Logic 1 = The $\overline{RI}$ input to the SC16C554B/554DB has changed from a logic 0 to a logic 1. A modem Status Interrupt will be generated.
1	MSR[1]	$\Delta\overline{DSR}$ [1] Logic 0 = No $\overline{DSR}$ change (normal default condition). Logic 1 = The $\overline{DSR}$ input to the SC16C554B/554DB has changed state since the last time it was read. A modem Status Interrupt will be generated.
0	MSR[0]	$\Delta\overline{CTS}$ [1] Logic 0 = No $\overline{CTS}$ change (normal default condition). Logic 1 = The $\overline{CTS}$ input to the SC16C554B/554DB has changed state since the last time it was read. A modem Status Interrupt will be generated.

[1] Whenever any MSR[3:0] is set to logic 1, a Modem Status Interrupt will be generated.

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7.9 Scratchpad Register (SPR)

The SC16C554B/554DB provides a temporary data register to store 8 bits of user information.

7.10 SC16C554B/554DB external reset conditions

Table 22. Reset state for registers

Register	Reset state
IER	IER[7:0] = 0
ISR	ISR[7:1] = 0; ISR[0] = 1
LCR	LCR[7:0] = 0
MCR	MCR[7:0] = 0
LSR	LSR[7] = 0; LSR[6:5] = 1; LSR[4:0] = 0
MSR	MSR[7:4] = input signals; MSR[3:0] = 0
FCR	FCR[7:0] = 0

Table 23. Reset state for outputs

Output	Reset state
TXA, TXB, TXC, TXD	HIGH
$\overline{\text{RTSA}}$, $\overline{\text{RTSB}}$, $\overline{\text{RTSC}}$, $\overline{\text{RTSD}}$	HIGH
$\overline{\text{DTRA}}$, $\overline{\text{DTRB}}$, $\overline{\text{DTRC}}$, $\overline{\text{DTRD}}$	HIGH
$\overline{\text{RXRDY}}$	HIGH
$\overline{\text{TXRDY}}$	LOW

8. Limiting values

Table 24. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-	7	V
V_n	voltage on any other pin	at D7 to D0	GND – 0.3	V_{CC} + 0.3	V
		at any input only pin	GND – 0.3	5.3	V
T_{amb}	ambient temperature		–40	+85	°C
T_{stg}	storage temperature		–65	+150	°C
P_{tot}/pack	total power dissipation per package		-	500	mW

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9. Static characteristics

Table 25. Static characteristics

T_{amb} = −40 °C to +85 °C; tolerance of V_{CC} = ±10 %, unless otherwise specified.

Symbol	Parameter	Conditions		V_{CC} = 2.5 V		V_{CC} = 3.3 V		V_{CC} = 5.0 V		Unit
				Min	Max	Min	Max	Min	Max	
$V_{IL(clk)}$	clock LOW-level input voltage			−0.3	+0.45	−0.3	+0.6	−0.5	+0.6	V
$V_{IH(clk)}$	clock HIGH-level input voltage			1.8	V_{CC}	2.4	V_{CC}	3.0	V_{CC}	V
V_{IL}	LOW-level input voltage	except XTAL1 clock		−0.3	+0.65	−0.3	+0.8	−0.5	+0.8	V
V_{IH}	HIGH-level input voltage	except XTAL1 clock		1.6	-	2.0	-	2.2	-	V
V_{OL}	LOW-level output voltage	on all outputs	[1]							
		I_{OL} = 5 mA (data bus)		-	-	-	-	-	0.4	V
		I_{OL} = 4 mA (other outputs)		-	-	-	0.4	-	-	V
		I_{OL} = 2 mA (data bus)		-	0.4	-	-	-	-	V
		I_{OL} = 1.6 mA (other outputs)		-	0.4	-	-	-	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = −5 mA (data bus)		-	-	-	-	2.4	-	V
		I_{OH} = −1 mA (other outputs)		-	-	2.0	-	-	-	V
		I_{OH} = −800 µA (data bus)		1.85	-	-	-	-	-	V
		I_{OH} = −400 µA (other outputs)		1.85	-	-	-	-	-	V
I_{LIL}	LOW-level input leakage current			-	±10	-	±10	-	±10	µA
$I_{L(clk)}$	clock leakage current			-	±30	-	±30	-	±30	µA
I_{CC}	supply current	f = 5 MHz		-	4.5	-	6	-	6	mA
C_i	input capacitance			-	5	-	5	-	5	pF
$R_{pu(int)}$	internal pull-up resistance		[2]	500	-	500	-	500	-	kΩ

[1] Except XTAL2, V_{OL} = 1 V typical.

[2] Refer to Table 2 “Pin description” for a listing of pins having internal pull-up resistors.

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10. Dynamic characteristics

Table 26. Dynamic characteristics

T_{amb} = −40 °C to +85 °C; tolerance of V_{CC} ±10 %, unless otherwise specified.

Symbol	Parameter	Conditions		V_{CC} = 2.5 V		V_{CC} = 3.3 V		V_{CC} = 5.0 V		Unit
				Min	Max	Min	Max	Min	Max	
t_{WH}	pulse width HIGH			10	-	6	-	6	-	ns
t_{WL}	pulse width LOW			10	-	6	-	6	-	ns
f_{XTAL}	oscillator/clock frequency		[1][2]	-	48	-	80		80	MHz
t_{6s}	address set-up time			0	-	0	-	0	-	ns
t_{6h}	address hold time			0	-	0	-	0	-	ns
t_{7d}	$\overline{IOR}$ delay from chip select			10	-	10	-	10	-	ns
t_{7w}	$\overline{IOR}$ strobe width	25 pF load		77	-	26	-	23	-	ns
t_{7h}	chip select hold time from $\overline{IOR}$			0	-	0	-	0	-	ns
t_{9d}	read cycle delay	25 pF load		20	-	20	-	20	-	ns
t_{12d}	delay from $\overline{IOR}$ to data	25 pF load		-	77	-	26	-	23	ns
t_{12h}	data disable time	25 pF load		-	15	-	15	-	15	ns
t_{13d}	$\overline{IOW}$ delay from chip select			10	-	10	-	10	-	ns
t_{13w}	$\overline{IOW}$ strobe width			20	-	20	-	15	-	ns
t_{13h}	chip select hold time from $\overline{IOW}$			0	-	0	-	0	-	ns
t_{15d}	write cycle delay			25	-	25	-	20	-	ns
t_{16s}	data set-up time			20	-	20	-	15	-	ns
t_{16h}	data hold time			15	-	5	-	5	-	ns
t_{17d}	delay from $\overline{IOW}$ to output	25 pF load		-	100	-	33	-	29	ns
t_{18d}	delay to set interrupt from modem input	25 pF load		-	100	-	24	-	23	ns
t_{19d}	delay to reset interrupt from $\overline{IOR}$	25 pF load		-	100	-	24	-	23	ns
t_{20d}	delay from stop to set interrupt			-	$1T_{RCLK}$ [3]	-	$1T_{RCLK}$ [3]	-	$1T_{RCLK}$ [3]	ns
t_{21d}	delay from $\overline{IOR}$ to reset interrupt	25 pF load		-	100	-	29	-	28	ns
t_{22d}	delay from start to set interrupt			-	100	-	45	-	40	ns
t_{23d}	delay from $\overline{IOW}$ to transmit start			$8T_{RCLK}$ [3]	$24T_{RCLK}$ [3]	$8T_{RCLK}$ [3]	$24T_{RCLK}$ [3]	$8T_{RCLK}$ [3]	$24T_{RCLK}$ [3]	ns
t_{24d}	delay from $\overline{IOW}$ to reset interrupt			-	100	-	45	-	40	ns
t_{25d}	delay from stop to set $\overline{RXRDY}$			-	$1T_{RCLK}$ [3]	-	$1T_{RCLK}$ [3]	-	$1T_{RCLK}$ [3]	ns
t_{26d}	delay from $\overline{IOR}$ to reset $\overline{RXRDY}$			-	100	-	45	-	40	ns

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Table 26. Dynamic characteristics *...continued*

T_{amb} = −40 °C to +85 °C; tolerance of V_{CC} ± 10 %, unless otherwise specified.

Symbol	Parameter	Conditions		V_{CC} = 2.5 V		V_{CC} = 3.3 V		V_{CC} = 5.0 V		Unit
				Min	Max	Min	Max	Min	Max	
t_{27d}	delay from $\overline{IOW}$ to set $\overline{TXRDY}$			-	100	-	45	-	40	ns
t_{28d}	delay from start to reset $\overline{TXRDY}$			-	$8T_{RCLK}$ [3]	-	$8T_{RCLK}$ [3]	-	$8T_{RCLK}$ [3]	ns
t_{30s}	address set-up time			10	-	10	-	10	-	ns
t_{30w}	chip select strobe width	25 pF load	[1]	90	-	26	-	23	-	ns
t_{30h}	address hold time			15	-	15	-	15	-	ns
t_{30d}	read cycle delay	25 pF load		20	-	20	-	20	-	ns
t_{31d}	delay from $\overline{CS}$ to data	25 pF load		-	90	-	26	-	23	ns
t_{31h}	data disable time	25 pF load		-	15	-	15	-	15	ns
t_{32s}	write strobe set-up time			10	-	10	-	10	-	ns
t_{32h}	write strobe hold time			10	-	10	-	10	-	ns
t_{32d}	write cycle delay			25	-	25	-	20	-	ns
t_{33s}	data set-up time			20	-	15	-	15	-	ns
t_{33h}	data hold time			15	-	5	-	5	-	ns
t_{RESET}	RESET pulse width		[4]	200	-	40	-	40	-	ns
N	baud rate divisor			1	$(2^{16} - 1)$	1	$(2^{16} - 1)$	1	$(2^{16} - 1)$	

[1] Applies to external clock, crystal oscillator max 24 MHz.

[2] Maximum frequency = $\frac{1}{t_{w(clk)}}$

[3] RCLK is an internal signal derived from Divisor Latch LSB (DLL) and Divisor Latch MSB (DLM) divisor latches.

[4] Reset pulse must happen when these signals are inactive: $\overline{CSA}$, $\overline{CSB}$, $\overline{CSC}$, $\overline{CSD}$, $\overline{IOW}$, $\overline{IOR}$.

10.1 Timing diagrams

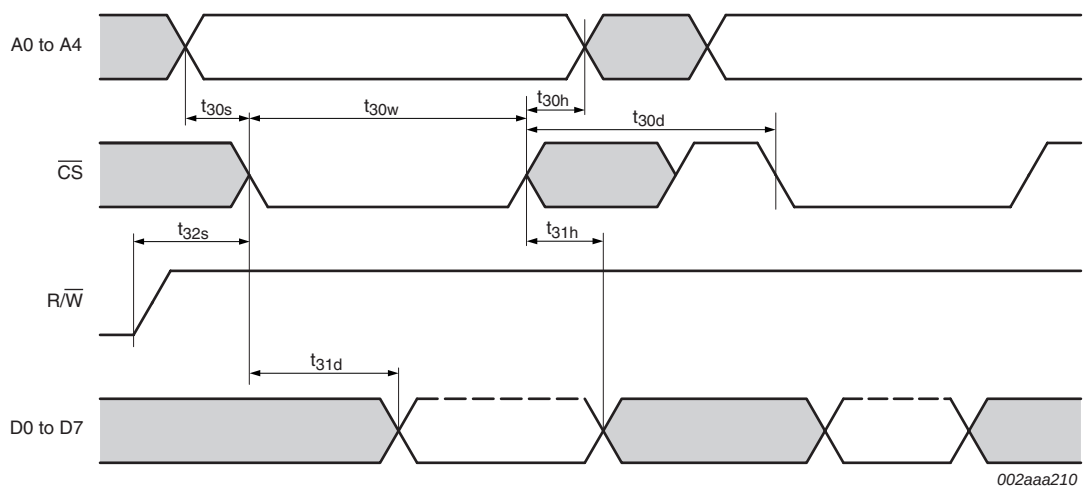


Fig 18. General read timing in 68 mode

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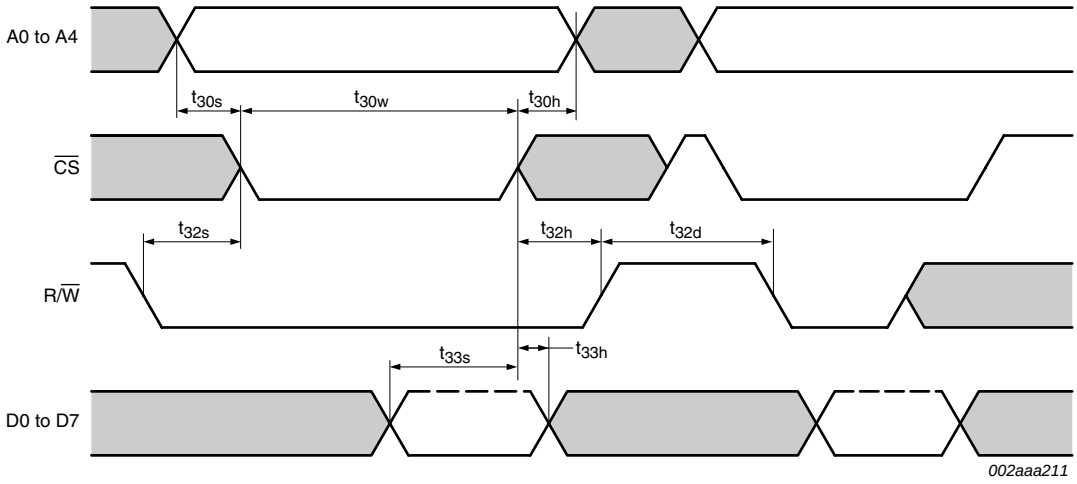


Fig 19. General write timing in 68 mode

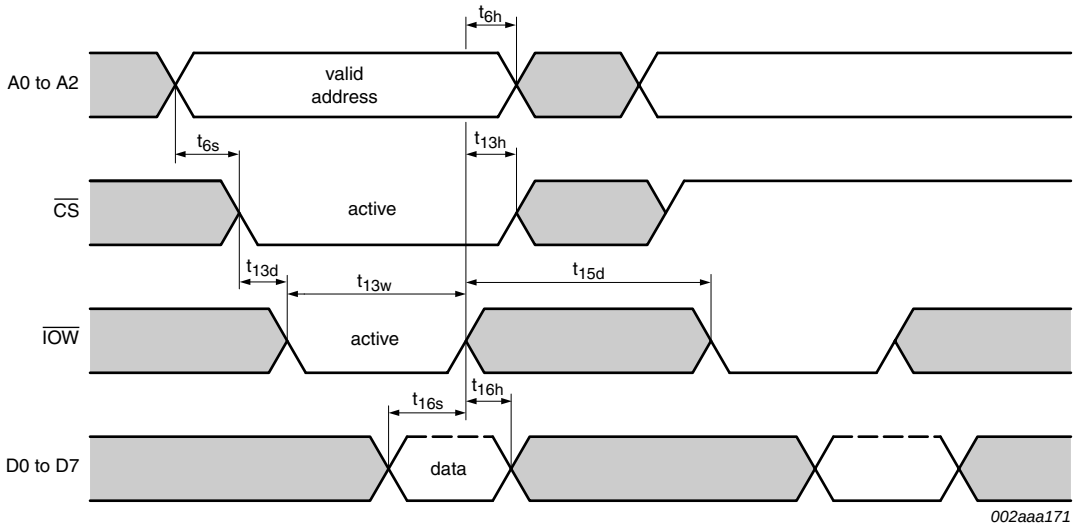


Fig 20. General write timing in 16 mode

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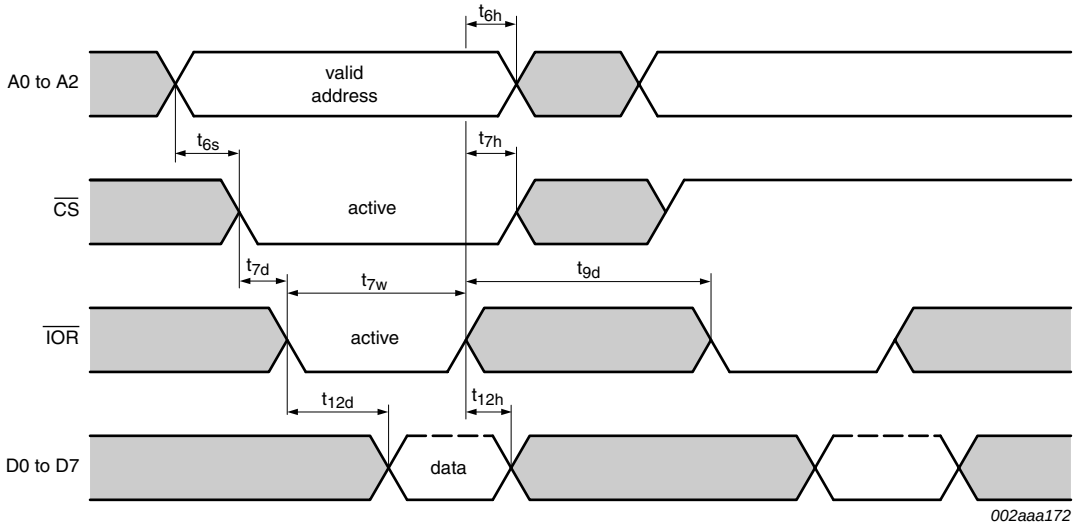


Fig 21. General read timing in 16 mode

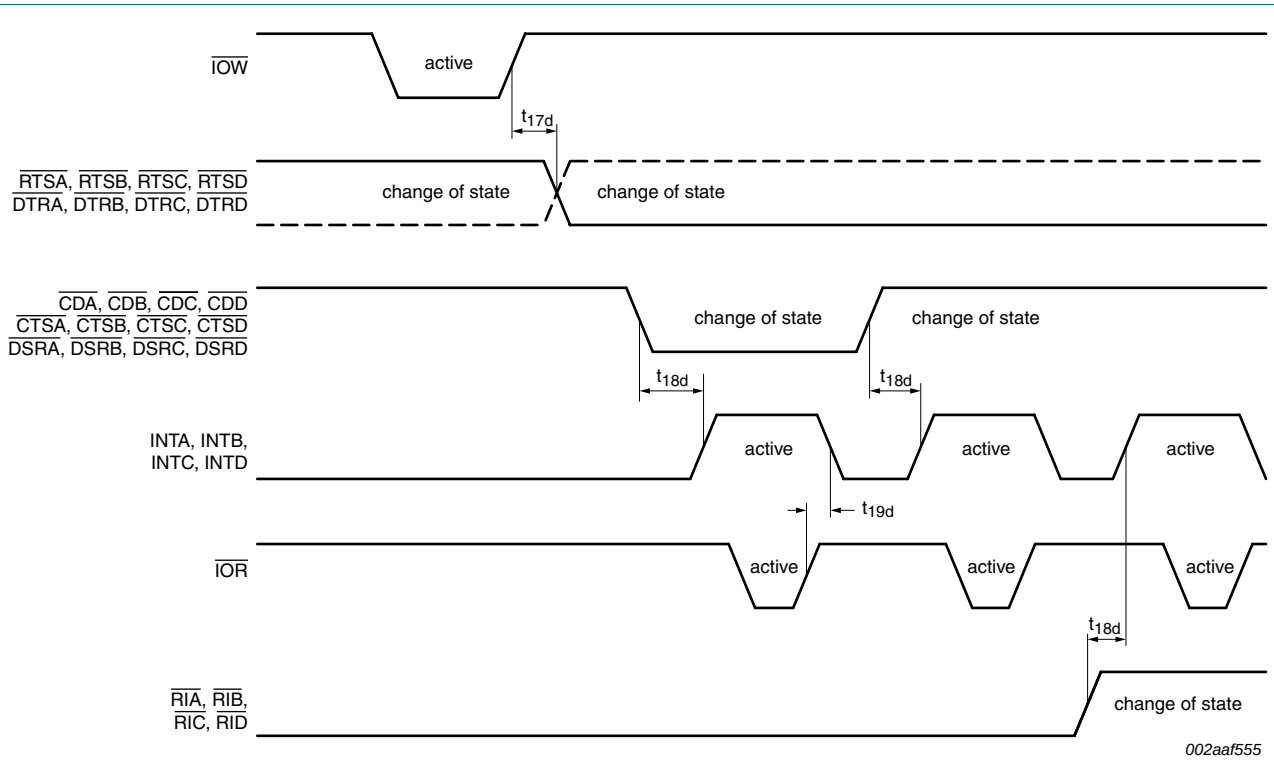
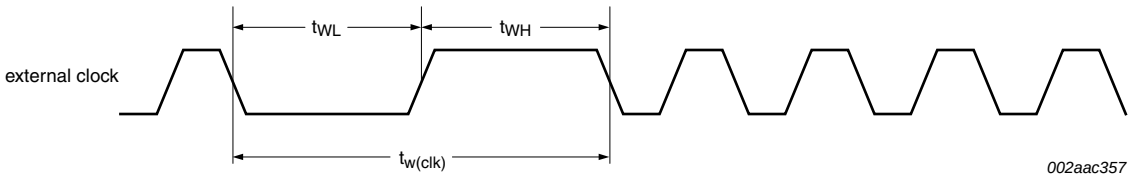


Fig 22. Modem input/output timing

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$$f_{XTAL} = \frac{1}{t_{w(clk)}}$$

Fig 23. External clock timing

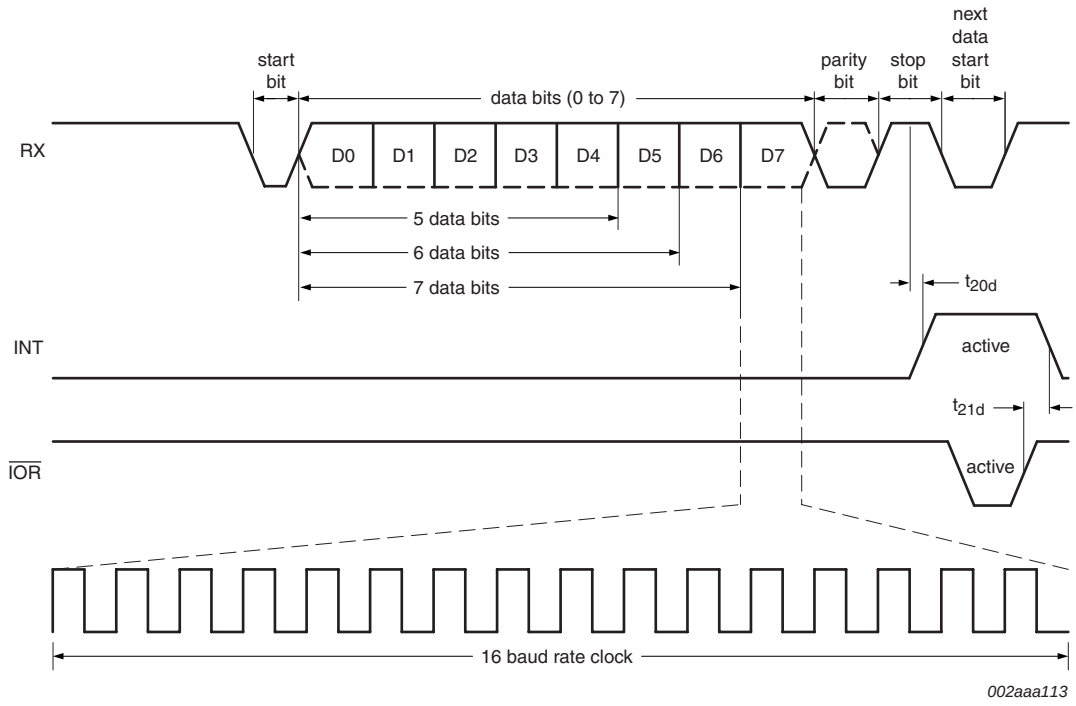


Fig 24. Receive timing

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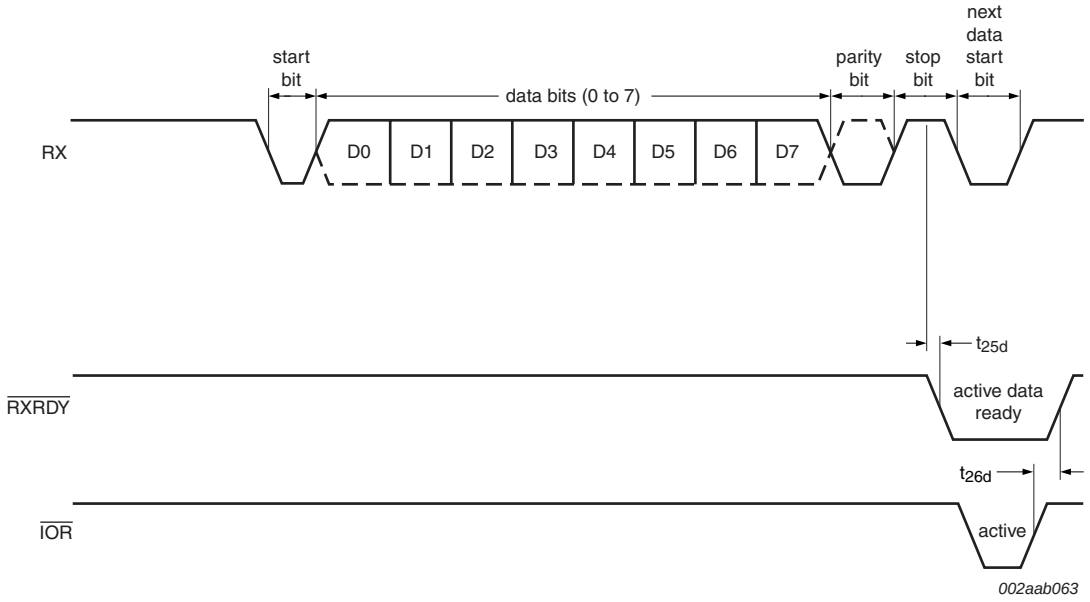


Fig 25. Receive ready timing in non-FIFO mode

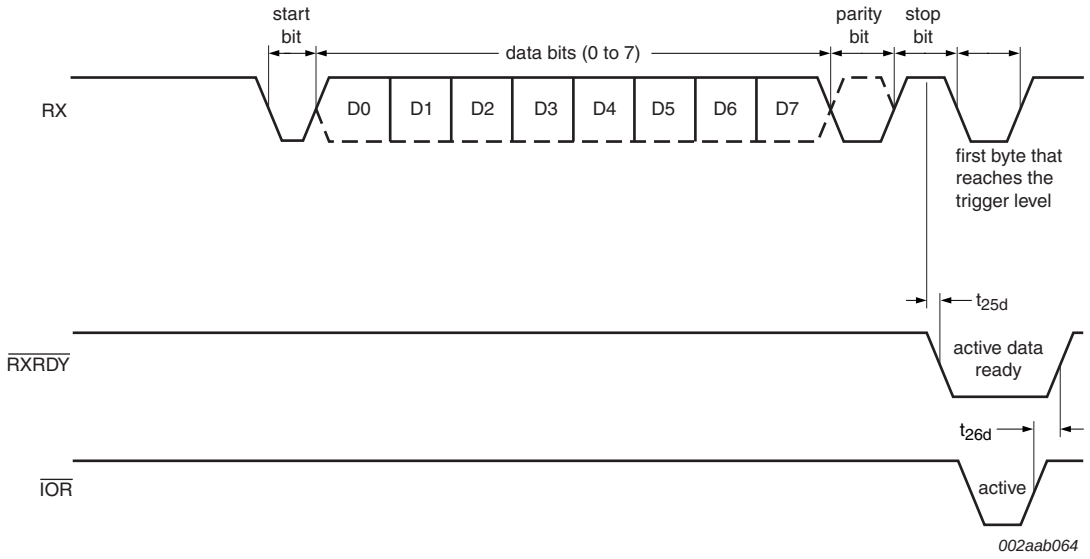


Fig 26. Receive ready timing in FIFO mode

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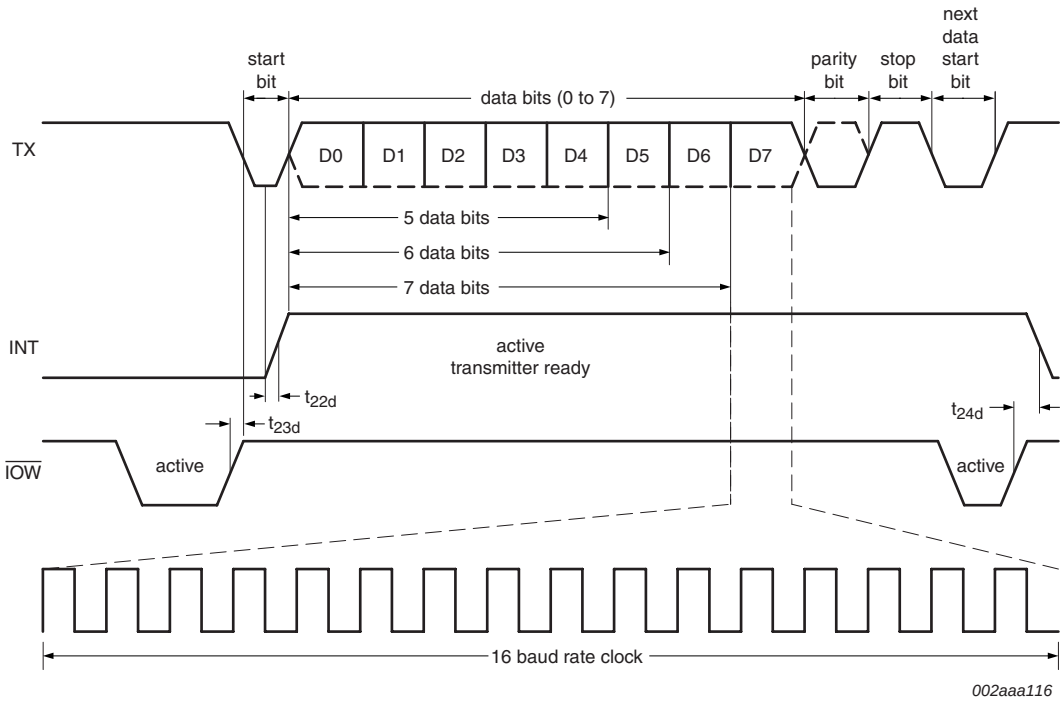


Fig 27. Transmit timing

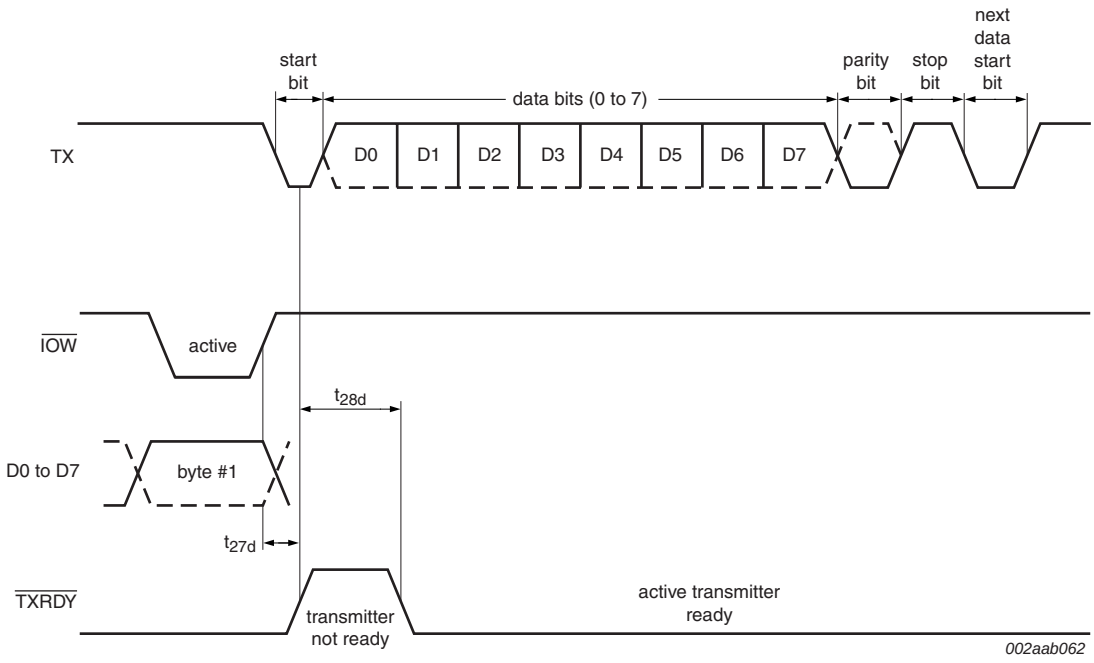


Fig 28. Transmit ready timing in non-FIFO mode

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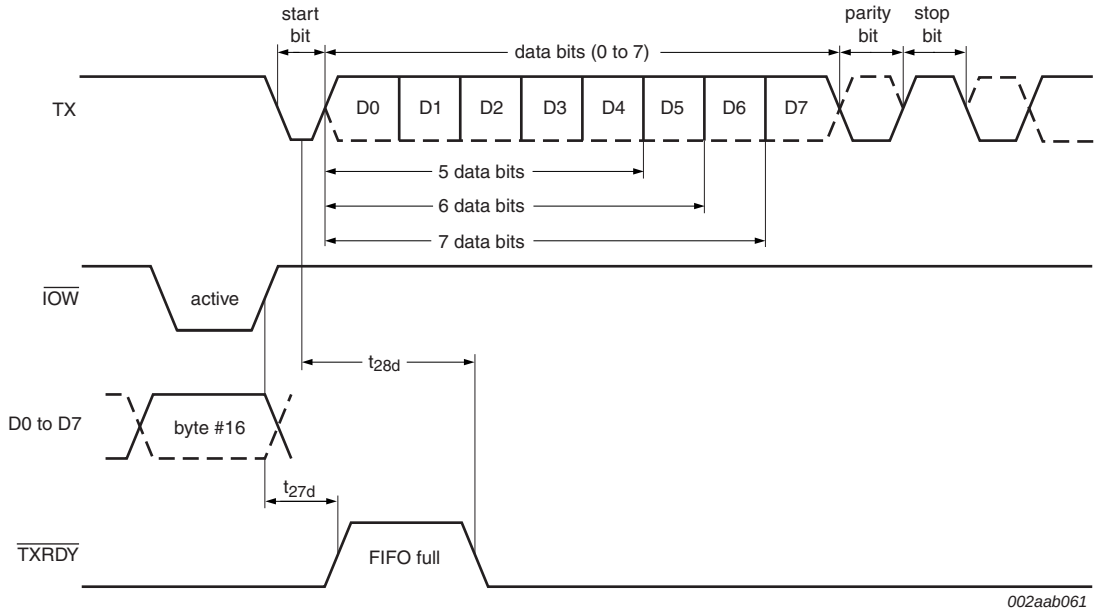


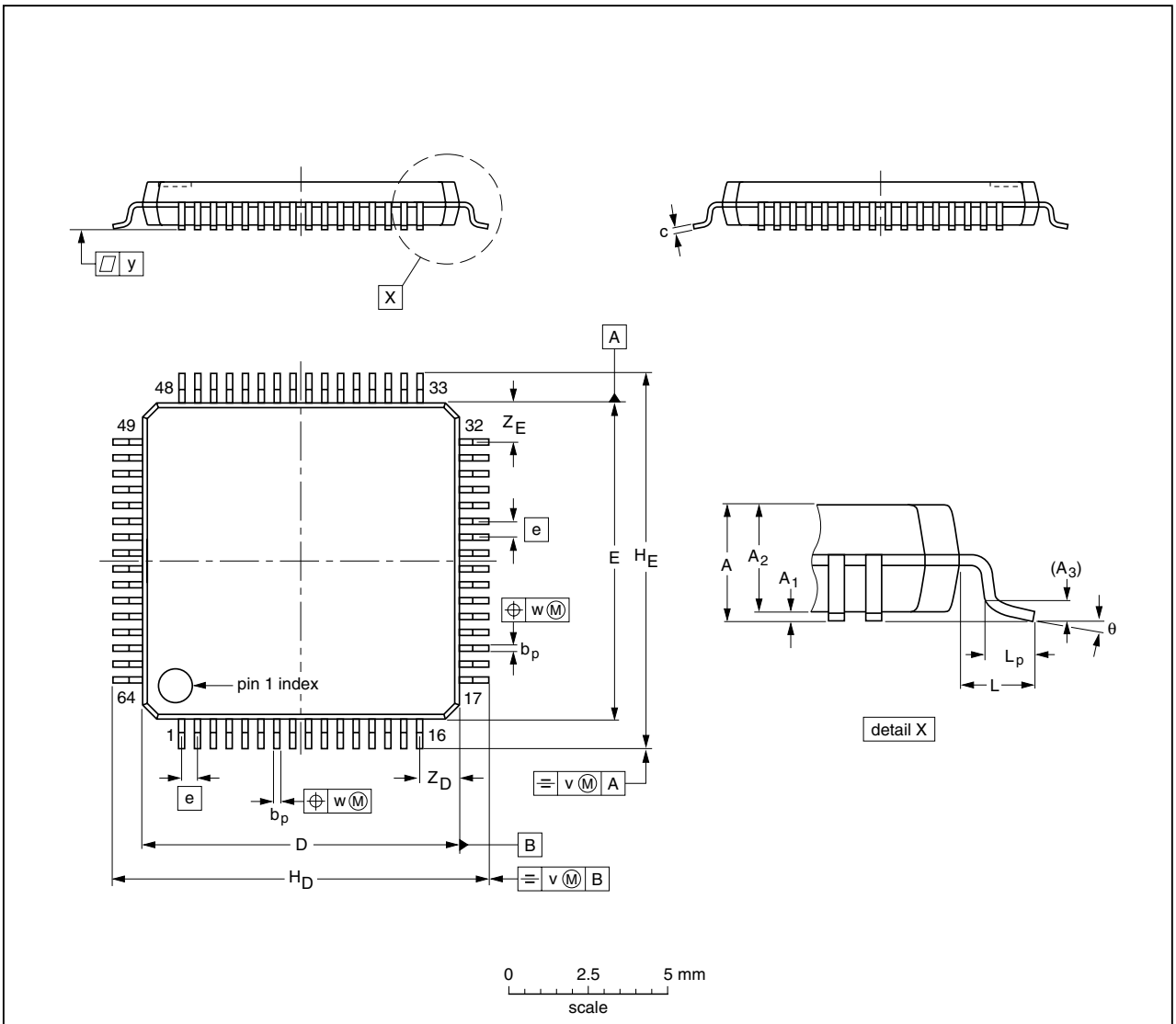
Fig 29. Transmit ready timing in FIFO mode (DMA mode '1')

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11. Package outline

LQFP64: plastic low profile quad flat package; 64 leads; body 10 x 10 x 1.4 mm **SOT314-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	10.1 9.9	10.1 9.9	0.5	12.15 11.85	12.15 11.85	1	0.75 0.45	0.2	0.12	0.1	1.45 1.05	1.45 1.05	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

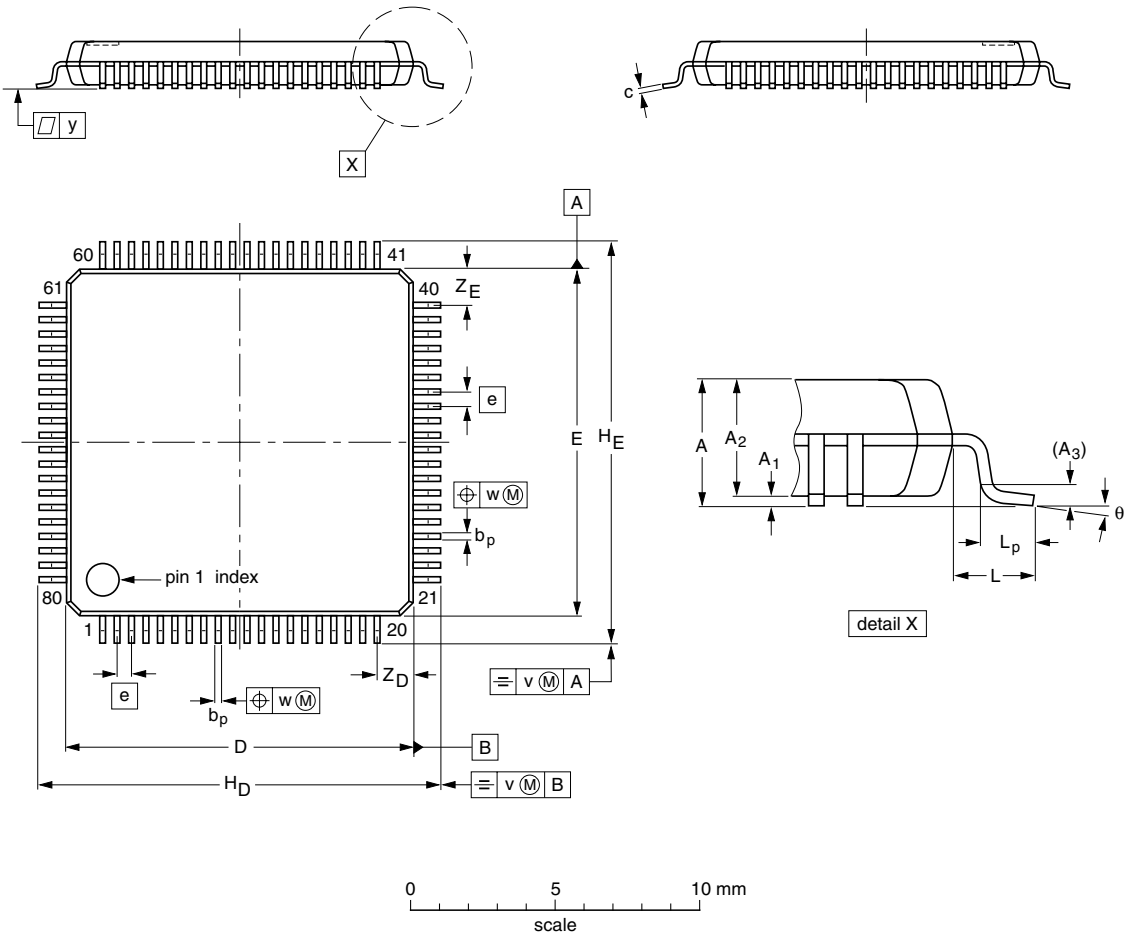
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT314-2	136E10	MS-026				~~00-01-19~~ 03-02-25

Fig 30. Package outline SOT314-2 (LQFP64)

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LQFP80: plastic low profile quad flat package; 80 leads; body 12 x 12 x 1.4 mm **SOT315-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.16 0.04	1.5 1.3	0.25	0.27 0.13	0.18 0.12	12.1 11.9	12.1 11.9	0.5	14.15 13.85	14.15 13.85	1	0.75 0.30	0.2	0.15	0.1	1.45 1.05	1.45 1.05	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

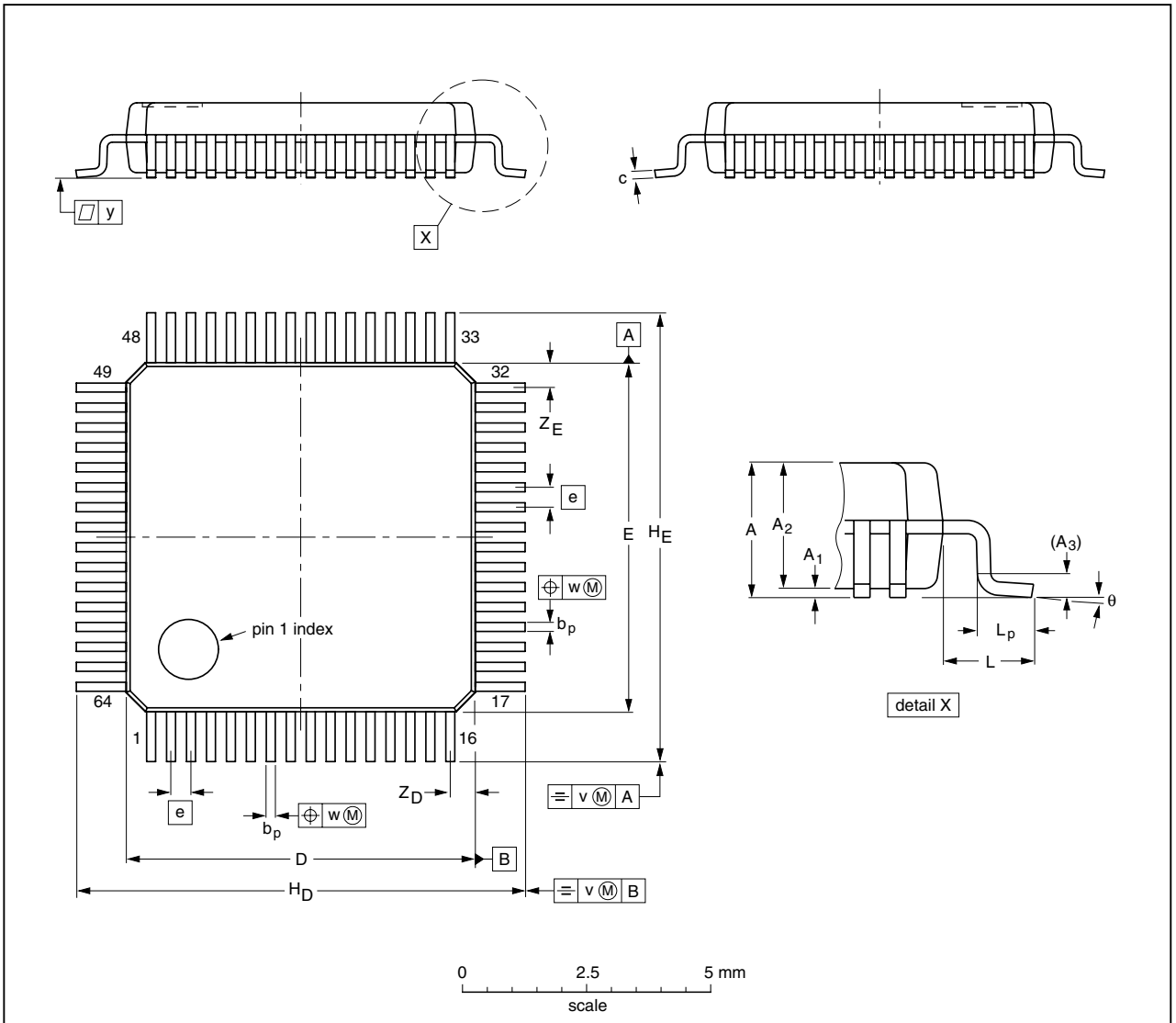
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT315-1	136E15	MS-026				~~00-01-19~~ 03-02-25

Fig 31. Package outline SOT315-1 (LQFP80)

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LQFP64: plastic low profile quad flat package; 64 leads; body 7 x 7 x 1.4 mm **SOT414-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.23 0.13	0.20 0.09	7.1 6.9	7.1 6.9	0.4	9.15 8.85	9.15 8.85	1	0.75 0.45	0.2	0.08	0.08	0.64 0.36	0.64 0.36	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

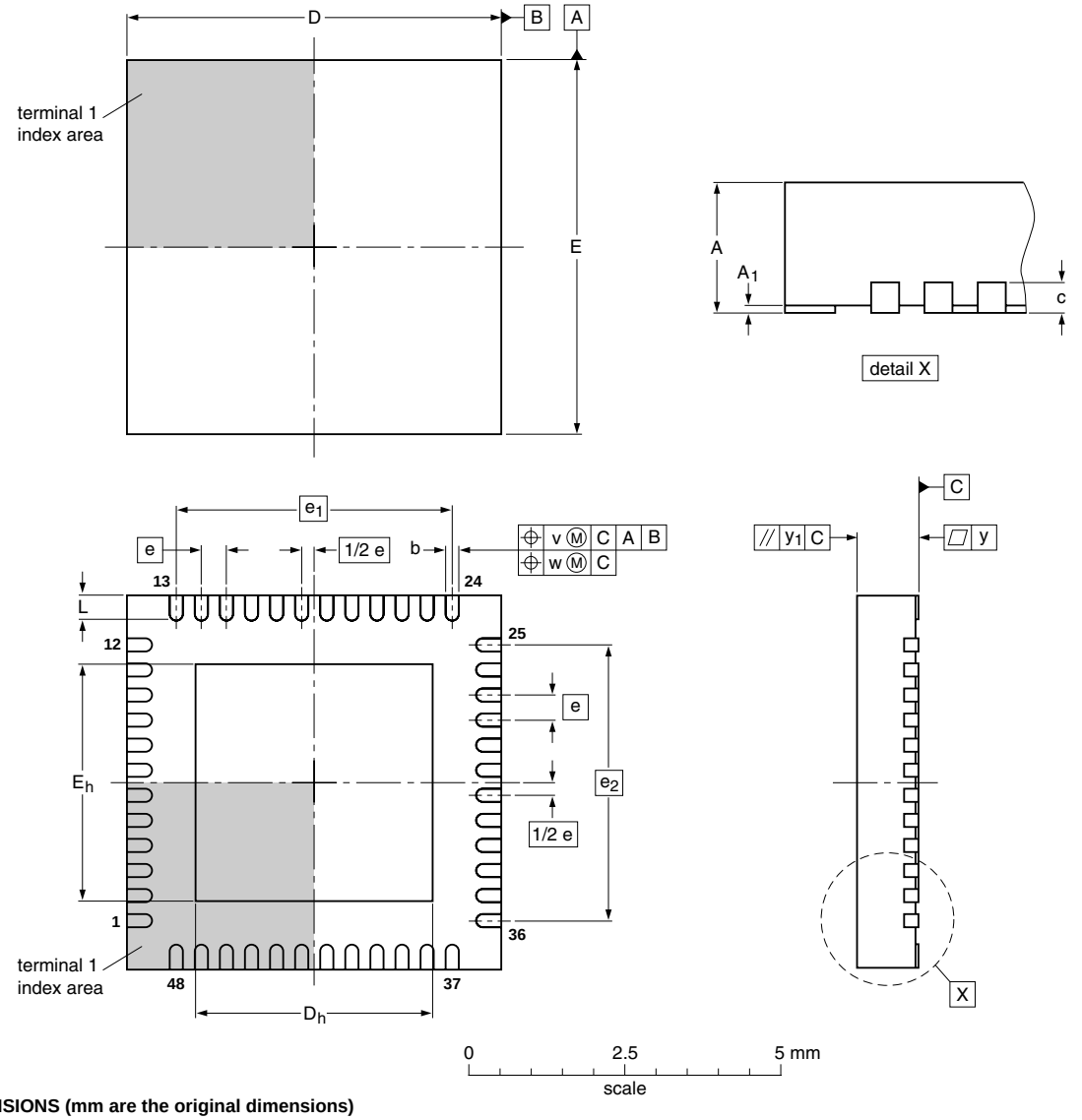
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT414-1	136E06	MS-026				~~00-01-19~~ 03-02-20

Fig 32. Package outline SOT414-1 (LQFP64)

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HVQFN48: plastic thermal enhanced very thin quad flat package; no leads; 48 terminals; body 6 x 6 x 0.85 mm **SOT778-3**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.25 0.15	0.2	6.1 5.9	3.95 3.65	6.1 5.9	3.95 3.65	0.4	4.4	4.4	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included

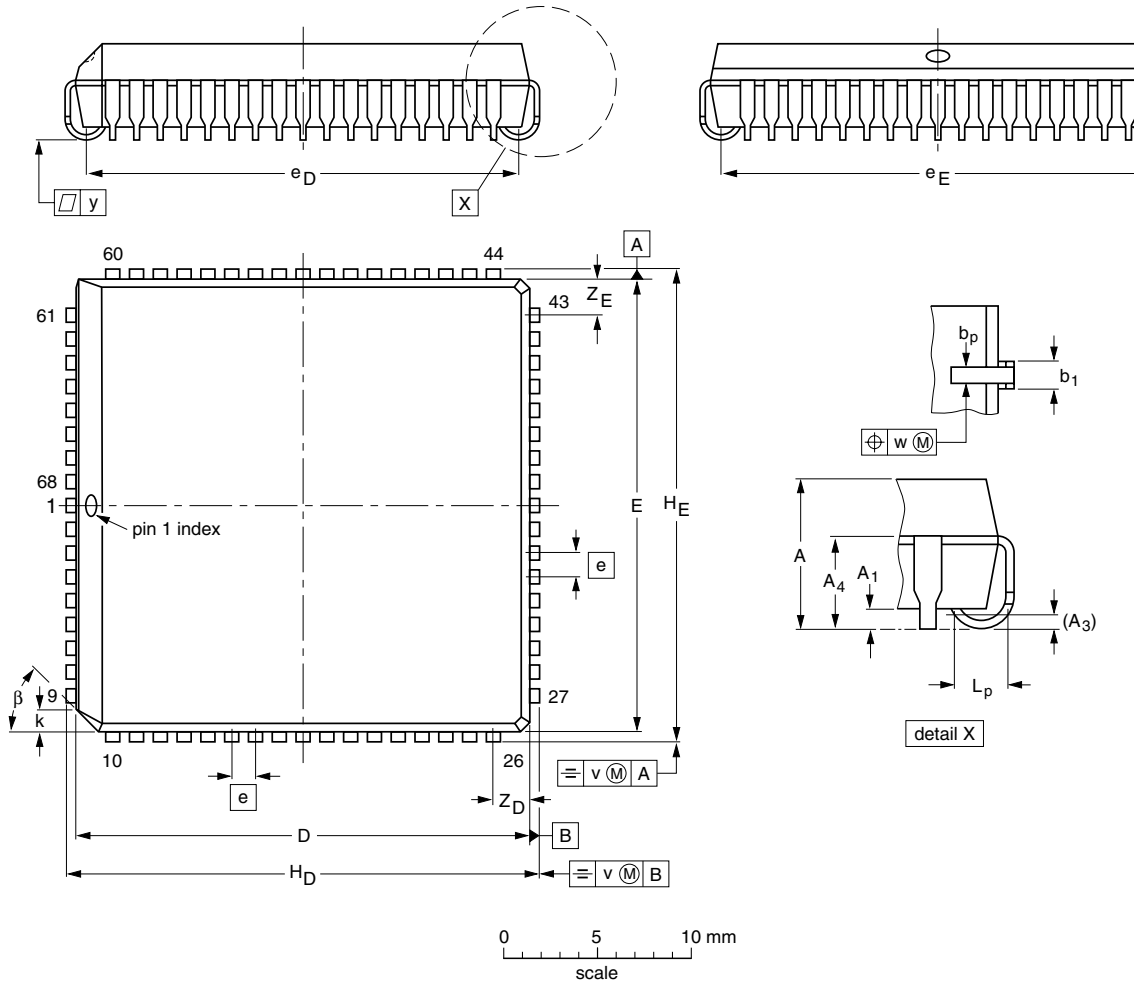
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT778-3	- - -	- - -	- - -			~~04-06-16~~ 04-06-23

Fig 33. Package outline SOT778-3 (HVQFN48)

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PLCC68: plastic leaded chip carrier; 68 leads **SOT188-2**



DIMENSIONS (mm dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.3	0.53 0.33	0.81 0.66	24.33 24.13	24.33 24.13	1.27	23.62 22.61	23.62 22.61	25.27 25.02	25.27 25.02	1.22 1.07	1.44 1.02	0.18	0.18	0.1	2.16	2.16	45°
inches	0.180 0.165	0.02	0.01	0.13	0.021 0.013	0.032 0.026	0.958 0.950	0.958 0.950	0.05	0.93 0.89	0.93 0.89	0.995 0.985	0.995 0.985	0.048 0.042	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT188-2	112E10	MS-018	EDR-7319			~~99-12-27~~ 01-11-14

Fig 34. Package outline SOT188-2 (PLCC68)

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12. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

12.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

12.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

12.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

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12.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 35) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 27 and 28

Table 27. SnPb eutectic process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 28. Lead-free process (from J-STD-020C)

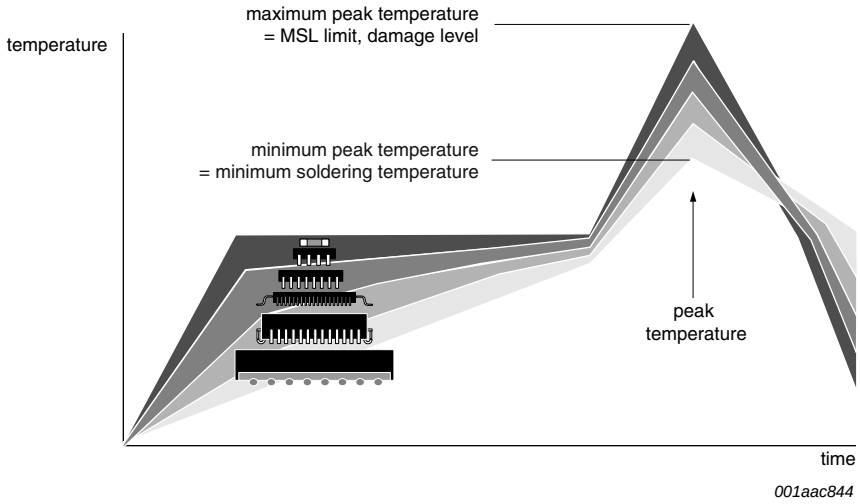
Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 35.

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MSL: Moisture Sensitivity Level

Fig 35. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

13. Abbreviations

Table 29. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
CPU	Central Processing Unit
DMA	Direct Memory Access
FIFO	First In, First Out
I/O	Input/Output
ISDN	Integrated Service Digital Network
LSB	Least Significant Bit
MSB	Most Significant Bit
PCB	Printed-Circuit Board
QUART	4-channel (Quad) Universal Asynchronous Receiver and Transmitter
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver and Transmitter

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14. Revision history

Table 30. Revision history

Document ID	Release date	Data sheet status	Supersedes
SC16C554B_554DB v.4	20100608	Product data sheet	SC16C554B_554DB_3
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Section 2 “Features and benefits”: 7th bullet item changed from “5 V tolerant inputs” to “5 V tolerant on input pins only”; added Footnote 1. • Figure 9 “Autoflow control (auto-RTS and auto-CTS) example” updated • Table 24 “Limiting values”: – parameter description for symbol V_n changed from “voltage at any pin” to “voltage on any other pin”; added separate conditions for “at D7 to D0” and “at any input only pin” – symbol for ‘total power dissipation per package” changed from “$P_{tot(pack)}$” to “P_{tot}/pack” • Table 25 “Static characteristics”: – symbol “$V_{IL(CK)}$” changed to “$V_{IL(clk)}$” – symbol “$V_{IH(CK)}$” changed to “$V_{IH(clk)}$” – parameter description for V_{OL}: moved “on all outputs” to Conditions column – symbol/parameter “I_{CL}, clock leakage” changed to “$I_{L(clk)}$, clock leakage current” – deleted (empty) Typ columns • Table 26 “Dynamic characteristics”: – symbol “t_{1w}, t_{2w}, clock pulse duration” is split to two symbols/parameters: “t_{WH}, pulse width HIGH” and “t_{WL}, pulse width LOW” – Table note [2]: fraction’s denominator changed from “t_{3w}” to “$t_{w(clk)}$” – added Table note [4] and its reference at t_{RESET} • Figure 23 “External clock timing”: – symbol changed from “t_{2w}” to “t_{WL}” – symbol changed from “t_{1w}” to “t_{WH}” – symbol changed from “t_{3w}” to “$t_{w(clk)}$” • updated soldering information		
SC16C554B_554DB_3	20050901	Product data sheet	SC16C554B_554DB_2
SC16C554B_554DB_2 (9397 750 14966)	20050613	Product data sheet	SC16C554B_554DB_1
SC16C554B_554DB_1 (9397 750 13133)	20050209	Product data sheet	-

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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Date of release: 8 June 2010
Document identifier: SC16C554B_554DB

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