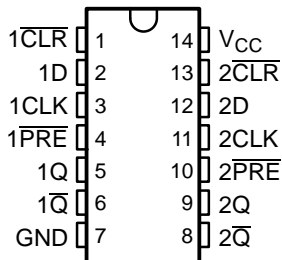


FEATURES

- Operate From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 5.2 ns at 3.3 V
- Typical V_{OLP} (Output Ground Bounce) <math><0.8\text{ V}</math> at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) $>2\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

SN54LVC74A . . . J OR W PACKAGE
SN74LVC74A . . . D, DB, NS, OR PW PACKAGE
(TOP VIEW)



SN74LVC74A . . . RGY PACKAGE
(TOP VIEW)



SN54LVC74A . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection

DESCRIPTION/ORDERING INFORMATION

The SN54LVC74A dual positive-edge-triggered D-type flip-flop is designed for 2.7-V to 3.6-V V_{CC} operation, and the SN74LVC74A dual positive-edge-triggered D-type flip-flop is designed for 1.65-V to 3.6-V V_{CC} operation.

ORDERING INFORMATION

| T_A | PACKAGE ⁽¹⁾ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|------------------------|---------------|-----------------------|------------------|
| –40°C to 85°C | QFN – RGY | Reel of 1000 | SN74LVC74ARGYR | LC74A |
| | | Tube of 50 | SN74LVC74AD | LVC74A |
| | SOIC – D | Reel of 2500 | SN74LVC74ADR | |
| | | Reel of 250 | SN74LVC74ADT | |
| | SOP – NS | Reel of 2000 | SN74LVC74ANSR | LCV74A |
| | SSOP – DB | Reel of 2000 | SN74LVC74ADBR | LC74A |
| | TSSOP – PW | Tube of 90 | SN74LVC74APW | LC74A |
| Reel of 2000 | | SN74LVC74APWR | | |
| Reel of 250 | | SN74LVC74APWT | | |
| –55°C to 125°C | CDIP – J | Tube of 25 | SNJ54LVC74AJ | SNJ54LVC74AJ |
| | CFP – W | Tube of 150 | SNJ54LVC74AW | SNJ54LVC74AW |
| | LCCC – FK | Tube of 55 | SNJ54LVC74AFK | SNJ54LVC74AFK |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SN54LVC74A, SN74LVC74A
DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS
WITH CLEAR AND PRESET

SCAS287S—JANUARY 1993—REVISED MAY 2005

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

A low level at the preset ($\overline{\text{PRE}}$) or clear ($\overline{\text{CLR}}$) inputs sets or resets the outputs, regardless of the levels of the other inputs. When $\overline{\text{PRE}}$ and $\overline{\text{CLR}}$ are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

The data I/Os and control inputs are overvoltage tolerant. This feature allows the use of these devices for down-translation in a mixed-voltage environment.

FUNCTION TABLE

| INPUTS | | | | OUTPUTS | |
|--------|-------------------------|-----|---|------------------|-------------------------|
| PRE | $\overline{\text{CLR}}$ | CLK | D | Q | $\overline{\text{Q}}$ |
| L | H | X | X | H | L |
| H | L | X | X | L | H |
| L | L | X | X | H ⁽¹⁾ | H ⁽¹⁾ |
| H | H | ↑ | H | H | L |
| H | H | ↑ | L | L | H |
| H | H | L | X | Q ₀ | $\overline{\text{Q}}_0$ |

(1) This configuration is nonstable; that is, it does not persist when $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ returns to its inactive (high) level.

LOGIC DIAGRAM, EACH FLIP-FLOP
(POSITIVE LOGIC)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|------------------|---|----------------------------|-----------------------|---------|
| V _{CC} | Supply voltage range | –0.5 | 6.5 | V |
| V _I | Input voltage range ⁽²⁾ | –0.5 | 6.5 | V |
| V _O | Output voltage range ⁽²⁾⁽³⁾ | –0.5 | V _{CC} + 0.5 | V |
| I _{IK} | Input clamp current | V _I < 0 | | –50 mA |
| I _{OK} | Output clamp current | V _O < 0 | | –50 mA |
| I _O | Continuous output current | | | ±50 mA |
| | Continuous current through V _{CC} or GND | | | ±100 mA |
| θ _{JA} | Package thermal impedance | D package ⁽⁴⁾ | | 86 °C/W |
| | | DB package ⁽⁴⁾ | | 96 |
| | | NS package ⁽⁴⁾ | | 76 |
| | | PW package ⁽⁴⁾ | | 113 |
| | | RGY package ⁽⁵⁾ | | 47 |
| T _{stg} | Storage temperature range | –65 | 150 | °C |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the recommended operating conditions table.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.
- (5) The package thermal impedance is calculated in accordance with JESD 51-5.

Recommended Operating Conditions⁽¹⁾

| | | SN54LVC74A | | SN74LVC74A | | UNIT |
|-----------------|------------------------------------|------------------------------------|-----------------|------------------------|-----------------|------|
| | | MIN | MAX | MIN | MAX | |
| V _{CC} | Supply voltage | Operating | | 2 | 3.6 | V |
| | | Data retention only | | 1.5 | | |
| V _{IH} | High-level input voltage | V _{CC} = 1.65 V to 1.95 V | | 0.65 × V _{CC} | | V |
| | | V _{CC} = 2.3 V to 2.7 V | | 1.7 | | |
| | | V _{CC} = 2.7 V to 3.6 V | | 2 | 2 | |
| V _{IL} | Low-level input voltage | V _{CC} = 1.65 V to 1.95 V | | 0.35 × V _{CC} | | V |
| | | V _{CC} = 2.3 V to 2.7 V | | 0.7 | | |
| | | V _{CC} = 2.7 V to 3.6 V | | 0.8 | 0.8 | |
| V _I | Input voltage | 0 | 5.5 | 0 | 5.5 | V |
| V _O | Output voltage | 0 | V _{CC} | 0 | V _{CC} | V |
| I _{OH} | High-level output current | V _{CC} = 1.65 V | | –4 | | mA |
| | | V _{CC} = 2.3 V | | –8 | | |
| | | V _{CC} = 2.7 V | | –12 | –12 | |
| | | V _{CC} = 3 V | | –24 | –24 | |
| I _{OL} | Low-level output current | V _{CC} = 1.65 V | | 4 | | mA |
| | | V _{CC} = 2.3 V | | 8 | | |
| | | V _{CC} = 2.7 V | | 12 | 12 | |
| | | V _{CC} = 3 V | | 24 | 24 | |
| Δt/Δv | Input transition rise or fall rate | 10 | | 10 | 10 | ns/V |
| T _A | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN54LVC74A, SN74LVC74A DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLEAR AND PRESET

SCAS287S—JANUARY 1993—REVISED MAY 2005

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | SN54LVC74A | | | SN74LVC74A | | | UNIT |
|--------------------------|---|-----------------|-----------------------|--------------------|------|-----------------------|--------------------|-----|------|
| | | | MIN | TYP ⁽¹⁾ | MAX | MIN | TYP ⁽¹⁾ | MAX | |
| V _{OH} | I _{OH} = -100 μA | 1.65 V to 3.6 V | | | | V _{CC} - 0.2 | | | V |
| | | 2.7 V to 3.6 V | V _{CC} - 0.2 | | | | | | |
| | I _{OH} = -4 mA | 1.65 V | | | 1.2 | | | | |
| | I _{OH} = -8 mA | 2.3 V | | | 1.7 | | | | |
| | I _{OH} = -12 mA | 2.7 V | | 2.2 | | 2.2 | | | |
| | | 3 V | | 2.4 | | 2.4 | | | |
| I _{OH} = -24 mA | 3 V | | 2.2 | | 2.2 | | | | |
| V _{OL} | I _{OL} = 100 μA | 1.65 V to 3.6 V | | | | 0.2 | | | V |
| | | 2.7 V to 3.6 V | | | 0.2 | | | | |
| | I _{OL} = 4 mA | 1.65 V | | | 0.45 | | | | |
| | I _{OL} = 8 mA | 2.3 V | | | 0.7 | | | | |
| | I _{OL} = 12 mA | 2.7 V | | | 0.4 | 0.4 | | | |
| | | 3 V | | | 0.55 | 0.55 | | | |
| I _I | V _I = 5.5 V or GND | 3.6 V | | | ±5 | | ±5 | μA | |
| I _{CC} | V _I = V _{CC} or GND, I _O = 0 | 3.6 V | | | 10 | | 10 | μA | |
| ΔI _{CC} | One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND | 2.7 V to 3.6 V | | | 500 | | 500 | μA | |
| C _i | V _I = V _{CC} or GND | 3.3 V | | | 5 | | 5 | pF | |

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

| | | SN54LVC74A | | | | UNIT |
|--------------------|----------------------------|-------------------------|-----|---------------------------------|-----|------|
| | | V _{CC} = 2.7 V | | V _{CC} = 3.3 V ± 0.3 V | | |
| | | MIN | MAX | MIN | MAX | |
| f _{clock} | Clock frequency | | 83 | | 100 | MHz |
| t _w | Pulse duration | PRE or CLR low | | 3.3 | 3.3 | ns |
| | | CLK high or low | | 3.3 | 3.3 | |
| t _{su} | Setup time before CLK↑ | Data | | 3.4 | 3 | ns |
| | | PRE or CLR inactive | | 2.2 | 2 | |
| t _h | Hold time, data after CLK↑ | | 1 | | 1 | ns |

Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

| | | SN74LVC74A | | | | | | | | UNIT |
|--------------------|--------------------------------------|---|-----|---|-----|-------------------------|-----|---|-----|------|
| | | $V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$ | | $V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$ | | $V_{CC} = 2.7\text{ V}$ | | $V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$ | | |
| | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| f_{clock} | Clock frequency | 83 | | 83 | | 83 | | 150 | | MHz |
| t_w | Pulse duration | $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ low | | 4.1 | | 3.3 | | 3.3 | | ns |
| | | CLK high or low | | 4.1 | | 3.3 | | 3.3 | | |
| t_{su} | Setup time before CLK \uparrow | Data | | 3.6 | | 2.3 | | 3.4 | | ns |
| | | $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive | | 2.7 | | 1.9 | | 2.2 | | |
| t_h | Hold time, data after CLK \uparrow | 1 | | 1 | | 1 | | 0 | | ns |

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54LVC74A | | | | UNIT |
|------------------|--|---------------------|-------------------------|-----|---|-----|------|
| | | | $V_{CC} = 2.7\text{ V}$ | | $V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$ | | |
| | | | MIN | MAX | MIN | MAX | |
| f_{max} | | | 83 | | 100 | | MHz |
| t_{pd} | CLK | Q or \overline{Q} | 6 | | 1 5.2 | | ns |
| | $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ | | 6.4 | | 1 5.4 | | |

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN74LVC74A | | | | | | | | UNIT |
|--------------------|--|---------------------|--|-----|---|-----|-------------------------|-----|---|-----|------|
| | | | $V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$ | | $V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$ | | $V_{CC} = 2.7\text{ V}$ | | $V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$ | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| f_{max} | | | 83 | | 83 | | 83 | | 150 | | MHz |
| t_{pd} | CLK | Q or \overline{Q} | 1 7.1 | | 1 4.4 | | 1 6 | | 1 5.2 | | ns |
| | $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ | | 1 6.9 | | 1 4.6 | | 1 6.4 | | 1 5.4 | | |
| $t_{\text{sk(o)}}$ | | | | | | | | | 1 | | ns |

Operating Characteristics

$T_A = 25^\circ\text{C}$

| PARAMETER | TEST CONDITIONS | $V_{CC} = 1.8\text{ V}$ | $V_{CC} = 2.5\text{ V}$ | $V_{CC} = 3.3\text{ V}$ | UNIT | |
|-----------------|---|-------------------------|-------------------------|-------------------------|------|----|
| | | TYP | TYP | TYP | | |
| C_{pd} | Power dissipation capacitance per flip-flop | f = 10 MHz | 24 | 24 | 26 | pF |

PARAMETER MEASUREMENT INFORMATION



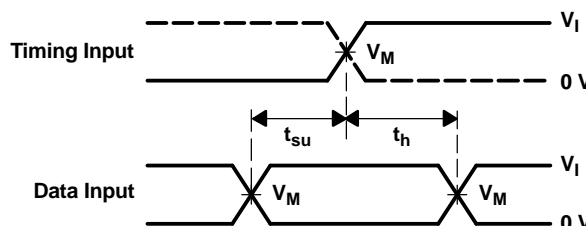
LOAD CIRCUIT

| TEST | S1 |
|-------------------|------------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | V_{LOAD} |
| t_{PHZ}/t_{PZH} | GND |

| V_{CC} | INPUTS | | V_M | V_{LOAD} | C_L | R_L | V_{Δ} |
|----------------------------------|----------|----------------------|------------|-------------------|-------|--------------|--------------|
| | V_I | t_r/t_f | | | | | |
| $1.8\text{ V} \pm 0.15\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 k Ω | 0.15 V |
| $2.5\text{ V} \pm 0.2\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 Ω | 0.15 V |
| 2.7 V | 2.7 V | $\leq 2.5\text{ ns}$ | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |
| $3.3\text{ V} \pm 0.3\text{ V}$ | 2.7 V | $\leq 2.5\text{ ns}$ | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |



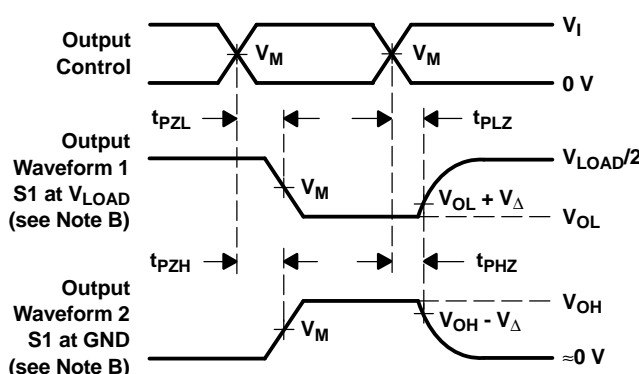
VOLTAGE WAVEFORMS
 PULSE DURATION



VOLTAGE WAVEFORMS
 SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
 PROPAGATION DELAY TIMES
 INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
 ENABLE AND DISABLE TIMES
 LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50\ \Omega$.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| 5962-9761601Q2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type |
| 5962-9761601QCA | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type |
| 5962-9761601QDA | ACTIVE | CFP | W | 14 | 1 | TBD | A42 | N / A for Pkg Type |
| 5962-9761601V2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type |
| 5962-9761601VCA | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type |
| 5962-9761601VDA | ACTIVE | CFP | W | 14 | 1 | TBD | A42 | N / A for Pkg Type |
| SN74LVC74AD | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC74ADBLE | OBSOLETE | SSOP | DB | 14 | | TBD | Call TI | Call TI |
| SN74LVC74ADBR | ACTIVE | SSOP | DB | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC74ADBRG4 | ACTIVE | SSOP | DB | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC74ADE4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC74ADG4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC74ADR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC74ADRE4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC74ADRG4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC74ADT | ACTIVE | SOIC | D | 14 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC74ADTE4 | ACTIVE | SOIC | D | 14 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC74ADTG4 | ACTIVE | SOIC | D | 14 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC74ANSR | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC74ANSRG4 | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC74APW | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC74APWE4 | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC74APWG4 | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC74APWLE | OBSOLETE | TSSOP | PW | 14 | | TBD | Call TI | Call TI |
| SN74LVC74APWR | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC74APWRE4 | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC74APWRG3 | PREVIEW | TSSOP | PW | 14 | 2000 | TBD | Call TI | Call TI |
| SN74LVC74APWRG4 | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC74APWT | ACTIVE | TSSOP | PW | 14 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| | | | | | | no Sb/Br) | | |
| SN74LVC74APWTE4 | ACTIVE | TSSOP | PW | 14 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC74APWTG4 | ACTIVE | TSSOP | PW | 14 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC74ARGYR | ACTIVE | VQFN | RGY | 14 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| SN74LVC74ARGYRG4 | ACTIVE | VQFN | RGY | 14 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| SNJ54LVC74AFK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type |
| SNJ54LVC74AJ | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type |
| SNJ54LVC74AW | ACTIVE | CFP | W | 14 | 1 | TBD | A42 | N / A for Pkg Type |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN54LVC74A, SN54LVC74A-SP, SN74LVC74A :

- Automotive: [SN74LVC74A-Q1](#)
- Enhanced Product: [SN74LVC74A-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LVC74ADBR | SSOP | DB | 14 | 2000 | 330.0 | 16.4 | 8.2 | 6.6 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LVC74ADR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LVC74ANSR | SO | NS | 14 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LVC74APWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LVC74ARGYR | VQFN | RGY | 14 | 3000 | 330.0 | 12.4 | 3.75 | 3.75 | 1.15 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVC74ADBR | SSOP | DB | 14 | 2000 | 346.0 | 346.0 | 33.0 |
| SN74LVC74ADR | SOIC | D | 14 | 2500 | 346.0 | 346.0 | 33.0 |
| SN74LVC74ANSR | SO | NS | 14 | 2000 | 346.0 | 346.0 | 33.0 |
| SN74LVC74APWR | TSSOP | PW | 14 | 2000 | 346.0 | 346.0 | 29.0 |
| SN74LVC74ARGYR | VQFN | RGY | 14 | 3000 | 346.0 | 346.0 | 29.0 |

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



4040180-2/D 07/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

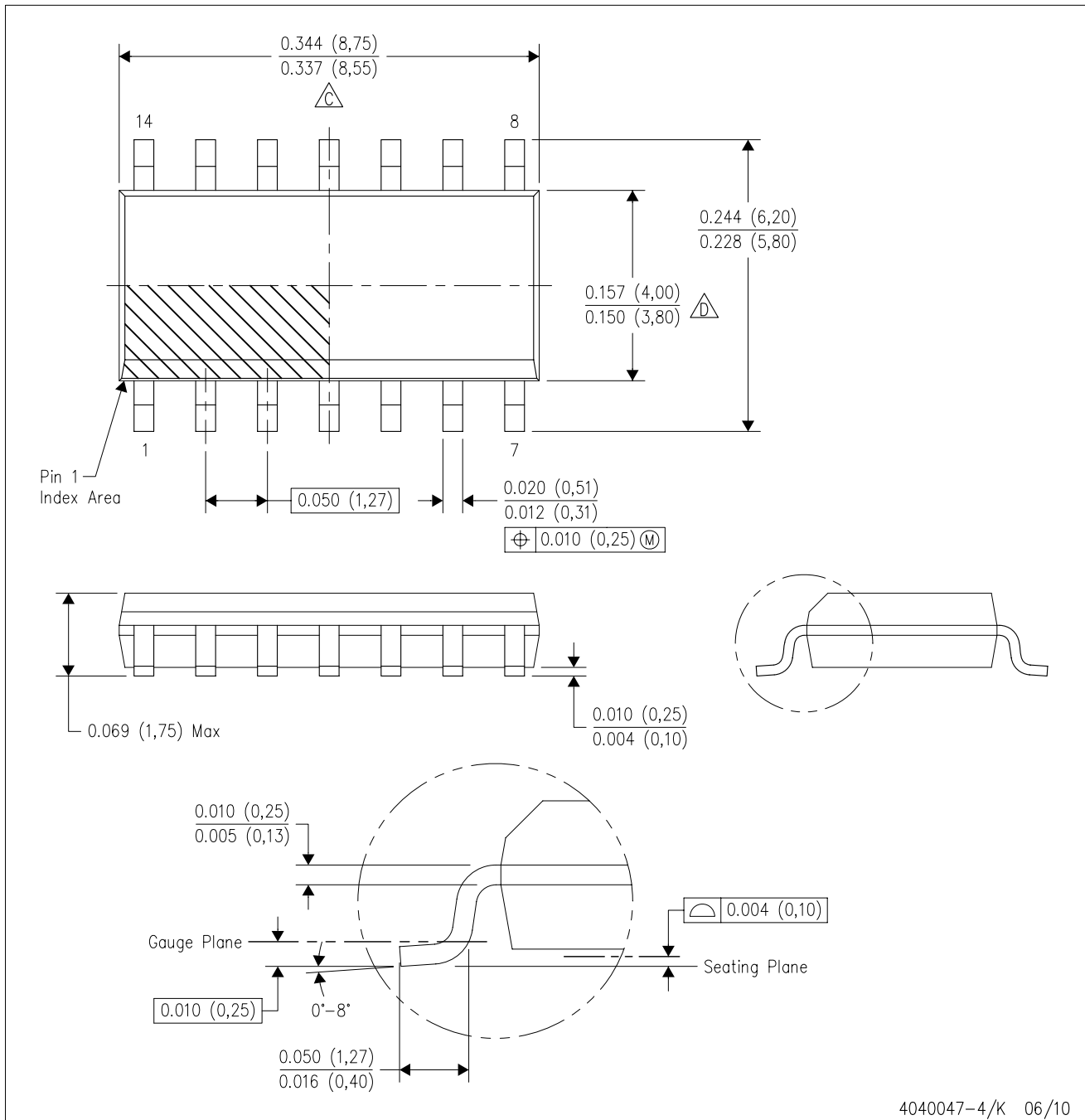
28 TERMINAL SHOWN





- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

D (R-PDSO-G14)

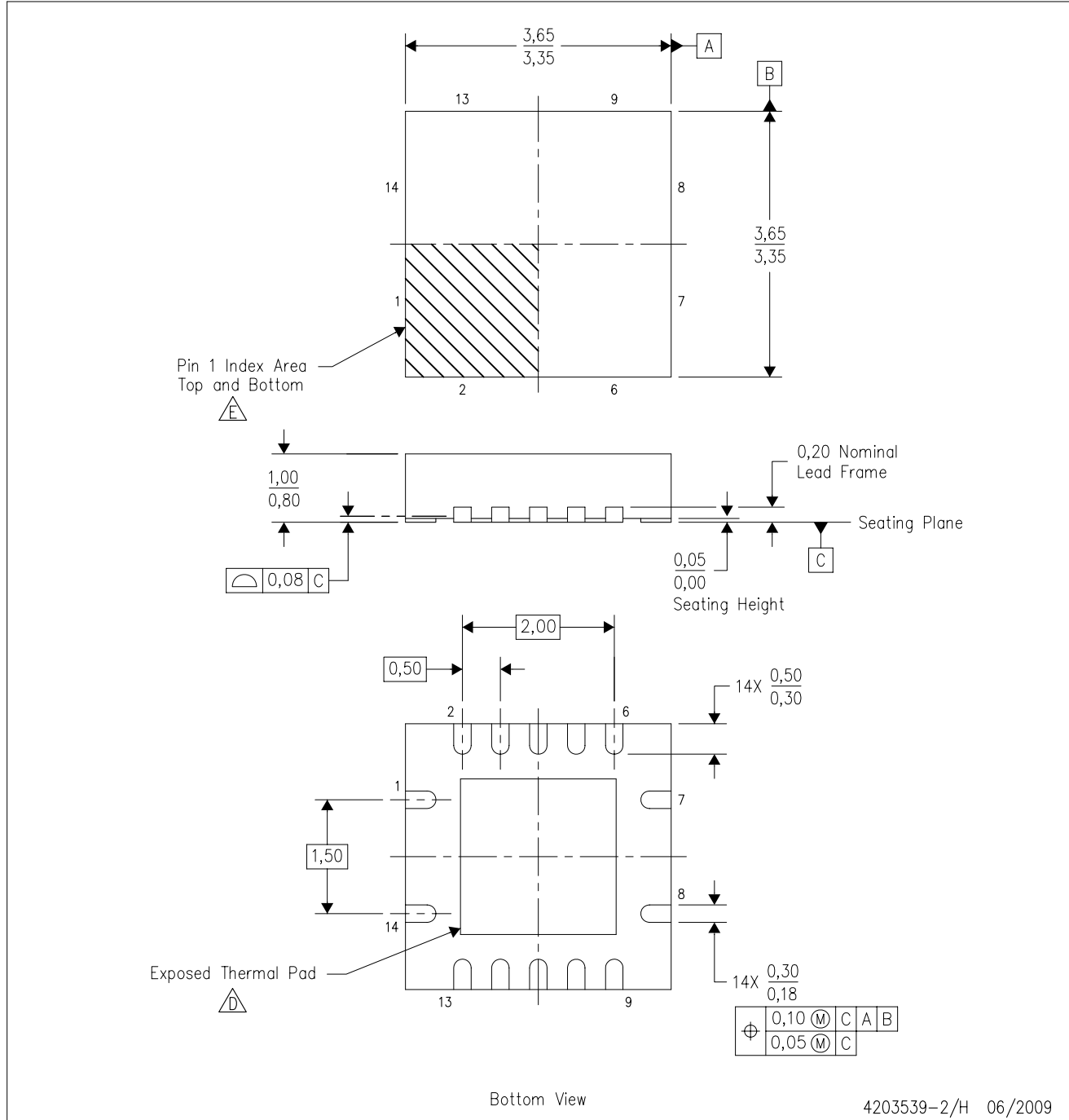
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 -  Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AB.

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



4203539-2/H 06/2009

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) package configuration.
 - D The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
 - E Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
 - F. Package complies to JEDEC MO-241 variation BA.

MECHANICAL DATA

NS (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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