

## Features

- 16-Mbit nonvolatile static random access memory (nvSRAM)
  - 30-ns and 45-ns access times
  - Logically organized as 1024 K × 16
  - Hands-off automatic STORE on power-down with only a small capacitor
  - STORE to QuantumTrap nonvolatile elements is initiated by software, device pin, or AutoStore on power-down
  - RECALL to SRAM initiated by software or power-up
- High reliability
  - Infinite read, write, and RECALL cycles
  - 1 million STORE cycles to QuantumTrap
  - Data retention: 20 years
- Sleep mode operation
- Low power consumption
  - Active current of 75 mA at 45 ns
  - Standby mode current of 650  $\mu$ A
  - Sleep mode current of 10  $\mu$ A
- Operating voltage
  - Core  $V_{CC}$  = 2.7 V to 3.6 V; I/O  $V_{CCQ}$  = 1.65 V to 1.95 V

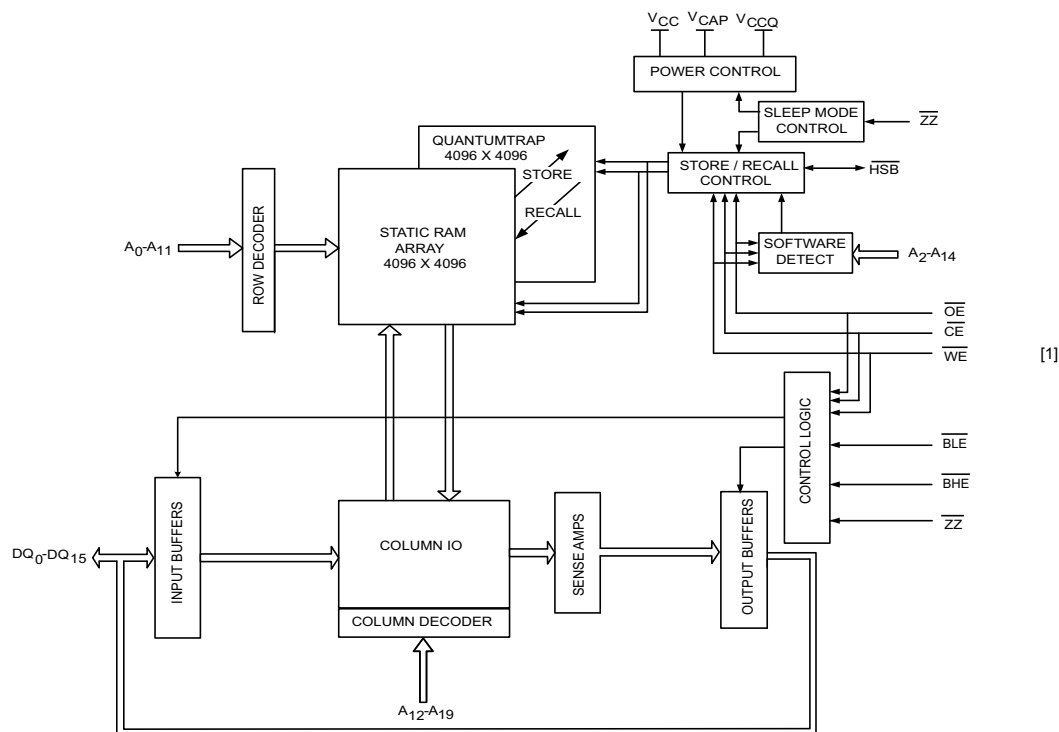
- Industrial temperature: -40 °C to +85 °C
- 165-ball fine-pitch ball grid array (FBGA) package
- Restriction of hazardous substances (RoHS) compliant

## Functional Description

The Cypress CY14V116N is a fast SRAM, with a nonvolatile element in each memory cell. The memory is organized as 1024 K words of 16 bits each. The embedded nonvolatile elements incorporate QuantumTrap technology, producing the world's most reliable nonvolatile memory. The SRAM can be read and written an infinite number of times. The nonvolatile data residing in the nonvolatile elements do not change when data is written to the SRAM. Data transfers from the SRAM to the nonvolatile elements (the STORE operation) takes place automatically at power-down. On power-up, data is restored to the SRAM (the RECALL operation) from the nonvolatile memory. Both the STORE and RECALL operations are also available under software control.

For a complete list of related documentation, click [here](#).

## Logic Block Diagram



### Note

1. In this datasheet,  $\overline{CE}$  refers to the internal logical combination of  $\overline{CE}_1$  and  $CE_2$ , such that when  $\overline{CE}_1$  is LOW and  $CE_2$  is HIGH,  $\overline{CE}$  is LOW. For all other cases  $\overline{CE}$  is HIGH.

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## Pinout

**Figure 1. Pin Diagram: 165-Ball FBGA (×16)**

	1	2	3	4	5	6	7	8	9	10	11
<b>A</b>	NC	A <sub>6</sub>	A <sub>8</sub>	$\overline{WE}$	$\overline{BLE}$	$\overline{CE_1}$	NC	$\overline{OE}$	A <sub>5</sub>	A <sub>3</sub>	NC
<b>B</b>	NC	DQ <sub>0</sub>	DQ <sub>1</sub>	A <sub>4</sub>	$\overline{BHE}$	CE <sub>2</sub>	NC	A <sub>2</sub>	NC	NC	NC
<b>C</b>	$\overline{ZZ}$	NC	NC	V <sub>SS</sub>	A <sub>0</sub>	A <sub>7</sub>	A <sub>1</sub>	V <sub>SS</sub>	NC	DQ <sub>15</sub>	DQ <sub>14</sub>
<b>D</b>	NC	DQ <sub>2</sub>	NC	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	NC	NC	NC
<b>E</b>	NC	V <sub>CAP</sub>	NC	V <sub>CCQ</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>CCQ</sub>	NC	DQ <sub>13</sub>	NC
<b>F</b>	NC	DQ <sub>3</sub>	NC	V <sub>CCQ</sub>	V <sub>CC</sub>	V <sub>SS</sub>	V <sub>CC</sub>	V <sub>CCQ</sub>	NC	NC	DQ <sub>12</sub>
<b>G</b>	$\overline{HSB}$	NC	NC	V <sub>CCQ</sub>	V <sub>CC</sub>	V <sub>SS</sub>	V <sub>CC</sub>	V <sub>CCQ</sub>	NC	NC	NC
<b>H</b>	NC	NC	V <sub>CCQ</sub>	V <sub>CCQ</sub>	V <sub>CC</sub>	V <sub>SS</sub>	V <sub>CC</sub>	V <sub>CCQ</sub>	V <sub>CCQ</sub>	NC	NC
<b>J</b>	NC	NC	NC	V <sub>CCQ</sub>	V <sub>CC</sub>	V <sub>SS</sub>	V <sub>CC</sub>	V <sub>CCQ</sub>	NC	DQ <sub>8</sub>	NC
<b>K</b>	NC	NC	DQ <sub>4</sub>	V <sub>CCQ</sub>	V <sub>CC</sub>	V <sub>SS</sub>	V <sub>CC</sub>	V <sub>CCQ</sub>	NC	NC	NC
<b>L</b>	NC	DQ <sub>5</sub>	NC	V <sub>CCQ</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>CCQ</sub>	NC	NC	DQ <sub>9</sub>
<b>M</b>	NC	NC	NC	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	NC	DQ <sub>10</sub>	NC
<b>N</b>	NC	DQ <sub>6</sub>	DQ <sub>7</sub>	V <sub>SS</sub>	A <sub>11</sub>	A <sub>10</sub>	A <sub>9</sub>	V <sub>SS</sub>	NC	NC	NC
<b>P</b>	NC	NC	NC	A <sub>13</sub>	A <sub>19</sub>	NC	A <sub>18</sub>	A <sub>12</sub>	NC	DQ <sub>11</sub>	NC
<b>R</b>	NC	NC	A <sub>15</sub>	NC	A <sub>17</sub>	NC	A <sub>16</sub>	NC <sup>[2]</sup>	A <sub>14</sub>	NC	NC

**Note**

2. Address expansion for 32-Mbit. NC pin not connected to die.

**Table 1. Pin Definitions**

Pin Name	I/O Type	Description
A <sub>0</sub> – A <sub>19</sub>	Input	<b>Address inputs.</b> Used to select one of the 1,048,576 words of the nvSRAM.
DQ <sub>0</sub> – DQ <sub>15</sub>	Input/Output	<b>Bidirectional data I/O lines.</b> Used as input or output lines depending on operation.
$\overline{WE}$	Input	<b>Write Enable input, Active LOW.</b> When selected LOW, data on the I/O pins is written to the specific address location.
$\overline{CE}_1, CE_2$	Input	<b>Chip Enable input.</b> The device is selected and a memory access begins on the falling edge of $\overline{CE}_1$ (while $CE_2$ is HIGH) or the rising edge of $CE_2$ (while $\overline{CE}_1$ is LOW).
$\overline{OE}$	Input	<b>Output Enable, Active LOW.</b> The active LOW $\overline{OE}$ input enables the data output buffers during read cycles. Deasserting $\overline{OE}$ HIGH causes the I/O pins to tristate.
$\overline{BLE}$	Input	<b>Byte Enable, Active LOW.</b> When selected LOW, enables DQ <sub>7</sub> –DQ <sub>0</sub> .
$\overline{BHE}$	Input	<b>Byte Enable, Active LOW.</b> When selected LOW, enables DQ <sub>15</sub> –DQ <sub>8</sub> .
$\overline{ZZ}$	Input	<b>Sleep Mode Enable.</b> When the $\overline{ZZ}$ pin is pulled LOW, the device enters a low-power Sleep mode and consumes the lowest power. Because this input is logically AND'ed with $\overline{CE}$ , $\overline{ZZ}$ must be HIGH for normal operation.
V <sub>CC</sub>	Power supply	<b>Power.</b> Power supply inputs to the core of the device.
V <sub>CCQ</sub>	Power supply	<b>I/O Power.</b> Power supply inputs for the inputs and outputs of the device.
V <sub>SS</sub>	Power Supply	<b>Ground for the device.</b> Must be connected to ground of the system.
$\overline{HSB}$	Input/Output	<b>Hardware STORE Busy (<math>\overline{HSB}</math>).</b> When LOW, this output indicates that a Hardware STORE is in progress. When pulled LOW external to the <u>chip</u> , it initiates a nonvolatile STORE operation. After each Hardware and Software STORE operation, $\overline{HSB}$ is driven HIGH for a short time (t <sub>HHHD</sub> ) with standard output high current and then a weak internal pull-up resistor keeps this pin HIGH (external pull-up resistor connection optional).
V <sub>CAP</sub>	Power Supply	<b>AutoStore capacitor.</b> Supplies power to the nvSRAM during power loss to store data from SRAM to nonvolatile elements.
NC	NC	<b>No Connect.</b> Die pads are not connected to the package pin.

## Device Operation

The CY14V116N nvSRAM is made up of two functional components paired in the same physical cell. These are an SRAM memory cell and a nonvolatile QuantumTrap cell. The SRAM memory cell operates as a standard fast static RAM. Data in the SRAM is transferred to the nonvolatile cell (the STORE operation) automatically at power-down, or from the nonvolatile cell to the SRAM (the RECALL operation) on power-up. Both the STORE and RECALL operations are also available under software control. Using this unique architecture, all cells are stored and recalled in parallel. During the STORE and RECALL operations, SRAM read and write operations are inhibited. The CY14V116N supports infinite reads and writes to the SRAM. In addition, it provides infinite RECALL operations from the nonvolatile cells and up to 1 million STORE operations. See the [Truth Table For SRAM Operations](#) on page 20 for a complete description of read and write modes.

## SRAM Read

The CY14V116N performs a read cycle whenever  $\overline{CE}$  and  $\overline{OE}$  are LOW, and  $\overline{WE}$ ,  $\overline{ZZ}$ , and HSB are HIGH. The address specified on pins  $A_0$ – $A_{19}$  determines which of the 1,048,576 words of 16 bits each are accessed. Byte enables ( $\overline{BHE}$ ,  $\overline{BLE}$ ) determine which bytes are enabled to the output. When the read is initiated by an address transition, the outputs are valid after a delay of  $t_{AA}$  (read cycle 1). If the read is initiated by  $\overline{CE}$  or  $\overline{OE}$ , the outputs are valid at  $t_{ACE}$  or at  $t_{DOE}$ , whichever is later (read cycle 2). The data output repeatedly responds to address changes within the  $t_{AA}$  access time without the need for transitions on any control input pins. This remains valid until another address change or until  $\overline{CE}$  or  $\overline{OE}$  is brought HIGH, or  $\overline{WE}$  or HSB is brought LOW.

## SRAM Write

A write cycle is performed when  $\overline{CE}$  and  $\overline{WE}$  are LOW and HSB is HIGH. The address inputs must be stable before entering the write cycle and must remain stable until  $\overline{CE}$  or  $\overline{WE}$  goes HIGH at the end of the cycle. The data on the common I/O pins  $DQ_0$ – $DQ_{15}$  is written into the memory if it is valid  $t_{SD}$  before the end of a  $\overline{WE}$ -controlled write or before the end of a  $\overline{CE}$ -controlled write. The Byte Enable inputs ( $\overline{BHE}$ ,  $\overline{BLE}$ ) determine which bytes are written. Keep  $\overline{OE}$  HIGH during the entire write cycle to avoid data bus contention on common I/O lines. If  $\overline{OE}$  is left LOW, the internal circuitry turns off the output buffers  $t_{HZWE}$  after  $\overline{WE}$  goes LOW.

## AutoStore Operation (Power-Down)

The CY14V116N stores data to the nonvolatile QuantumTrap cells using one of the three storage operations. These three operations are: Hardware STORE, activated by the HSB; Software STORE, activated by an address sequence; AutoStore, on device power-down. The AutoStore operation is a unique feature of nvSRAM and is enabled by default on the CY14V116N device.

During normal operation, the device draws current from  $V_{CC}$  to charge a capacitor connected to the  $V_{CAP}$  pin. This stored charge is used by the chip to perform a STORE operation during power-down. If the voltage on the  $V_{CC}$  pin drops below  $V_{SWITCH}$ , the part automatically disconnects the  $V_{CAP}$  pin from  $V_{CC}$  and a STORE operation is initiated with power provided by the  $V_{CAP}$  capacitor.

**Note** If the capacitor is not connected to the  $V_{CAP}$  pin, AutoStore must be disabled using the soft sequence specified in the section [Preventing AutoStore](#) on page 9. If AutoStore is enabled without a capacitor on the  $V_{CAP}$  pin, the device attempts an AutoStore operation without sufficient charge to complete the STORE. This corrupts the data stored in the nvSRAM.

**Figure 2. AutoStore Mode**

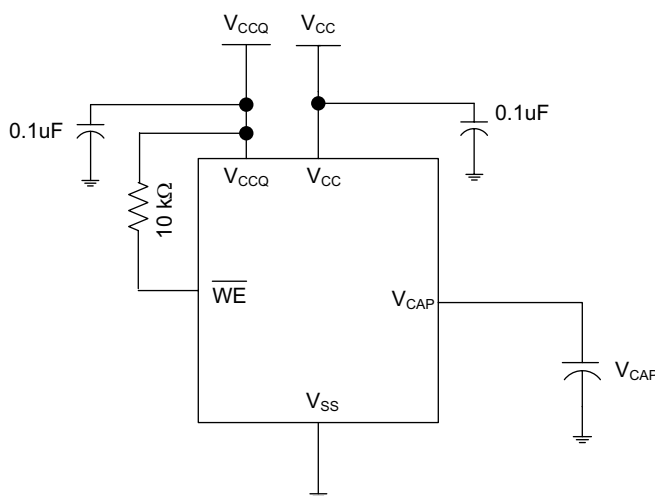


Figure 2 shows the proper connection of the storage capacitor ( $V_{CAP}$ ) for automatic STORE operation. Refer to [DC Electrical Characteristics](#) on page 10 for the size of the  $V_{CAP}$ . The voltage on the  $V_{CAP}$  pin is driven to  $V_{V_{CAP}}$  by a regulator on the chip. A pull-up resistor should be placed on  $\overline{WE}$  to hold it inactive during power-up. This pull-up resistor is only effective if the  $\overline{WE}$  signal is in tristate during power-up. When the nvSRAM comes out of power-up-RECALL, the host microcontroller must be active or the  $\overline{WE}$  held inactive until the host microcontroller comes out of reset.

To reduce unnecessary nonvolatile STOREs, AutoStore and Hardware STORE operations are ignored unless at least one write operation has taken place (which sets a write latch) since the most recent STORE or RECALL cycle. Software initiated STORE cycles are performed regardless of whether a write operation has taken place.

## Hardware STORE (HSB) Operation

The CY14V116N provides the  $\overline{\text{HSB}}$  pin to control and acknowledge the STORE operations. The  $\overline{\text{HSB}}$  pin is used to request a Hardware STORE cycle. When the  $\overline{\text{HSB}}$  pin is driven LOW, the device conditionally initiates a STORE operation after  $t_{\text{DELAY}}$ . A STORE cycle begins only if a write to the SRAM has taken place since the last STORE or RECALL cycle. The  $\overline{\text{HSB}}$  pin also acts as an open drain driver (an internal 100-k $\Omega$  weak pull-up resistor) that is internally driven LOW to indicate a busy condition when the STORE (initiated by any means) is in progress.

**Note** After each Hardware and Software STORE operation,  $\overline{\text{HSB}}$  is driven HIGH for a short time ( $t_{\text{HHHD}}$ ) with standard output high current and then remains HIGH by an internal 100-k $\Omega$  pull-up resistor.

SRAM write operations that are in progress when  $\overline{\text{HSB}}$  is driven LOW by any means are given time ( $t_{\text{DELAY}}$ ) to complete before the STORE operation is initiated. However, any SRAM write cycles requested after  $\overline{\text{HSB}}$  goes LOW are inhibited until  $\overline{\text{HSB}}$  returns HIGH. If the write latch is not set,  $\overline{\text{HSB}}$  is not driven LOW by the device. However, any of the SRAM read and write cycles are inhibited until  $\overline{\text{HSB}}$  is returned HIGH by the host microcontroller or another external source.

During any STORE operation, regardless of how it is initiated, the device continues to drive the  $\overline{\text{HSB}}$  pin LOW, releasing it only when the STORE is complete. Upon completion of the STORE operation, the nvSRAM memory access is inhibited for  $t_{\text{LZHSB}}$  time after the  $\overline{\text{HSB}}$  pin returns HIGH. Leave the  $\overline{\text{HSB}}$  disconnected if it is not used.

## Hardware RECALL (Power-Up)

During power-up or after any low-power condition ( $V_{\text{CC}} < V_{\text{SWITCH}}$ ), an internal RECALL request is latched. When  $V_{\text{CC}}$  again exceeds the  $V_{\text{SWITCH}}$  on power-up, a RECALL cycle is automatically initiated and takes  $t_{\text{HRECALL}}$  to complete. During this time, the  $\overline{\text{HSB}}$  pin is driven LOW by the  $\overline{\text{HSB}}$  driver and all reads and writes to nvSRAM are inhibited.

## Software STORE

Data is transferred from the SRAM to the nonvolatile memory by a software address sequence. A Software STORE cycle is initiated by executing sequential  $\overline{\text{CE}}$  or  $\overline{\text{OE}}$  controlled read cycles from six specific address locations in exact order. During the STORE cycle, the previous nonvolatile data is first erased, followed by a store into the nonvolatile elements. After a STORE cycle is initiated, further reads and writes are disabled until the cycle is completed.

Because a sequence of reads from specific addresses is used for STORE initiation, it is important that no other read or write accesses intervene in the sequence. Otherwise, the sequence is aborted and no STORE or RECALL takes place.

To initiate the Software STORE cycle, the following read sequence must be performed:

1. Read address 0x4E38 Valid Read
2. Read address 0xB1C7 Valid Read
3. Read address 0x83E0 Valid Read
4. Read address 0x7C1F Valid Read
5. Read address 0x703F Valid Read
6. Read address 0x8FC0 Initiate STORE cycle

The software sequence may be clocked with  $\overline{\text{CE}}$ -controlled reads or  $\overline{\text{OE}}$ -controlled reads, with  $\overline{\text{WE}}$  kept HIGH for all the six read sequences. After the sixth address in the sequence is entered, the STORE cycle commences and the chip is disabled.  $\overline{\text{HSB}}$  is driven LOW. After the  $t_{\text{STORE}}$  cycle time is fulfilled, the SRAM is activated again for the read and write operation.

## Software RECALL

Data is transferred from the nonvolatile memory to the SRAM by a software address sequence. A software RECALL cycle is initiated with a sequence of read operations in a manner similar to the Software STORE initiation. To initiate the RECALL cycle, perform the following sequence of  $\overline{\text{CE}}$  or  $\overline{\text{OE}}$  controlled read operations:

1. Read address 0x4E38 Valid Read
2. Read address 0xB1C7 Valid Read
3. Read address 0x83E0 Valid Read
4. Read address 0x7C1F Valid Read
5. Read address 0x703F Valid Read
6. Read address 0x4C63 Initiate RECALL cycle

Internally, RECALL is a two-step procedure. First, the SRAM data is cleared; then, the nonvolatile information is transferred into the SRAM cells. After the  $t_{\text{RECALL}}$  cycle time, the SRAM is again ready for read and write operations. The RECALL operation does not alter the data in the nonvolatile elements.

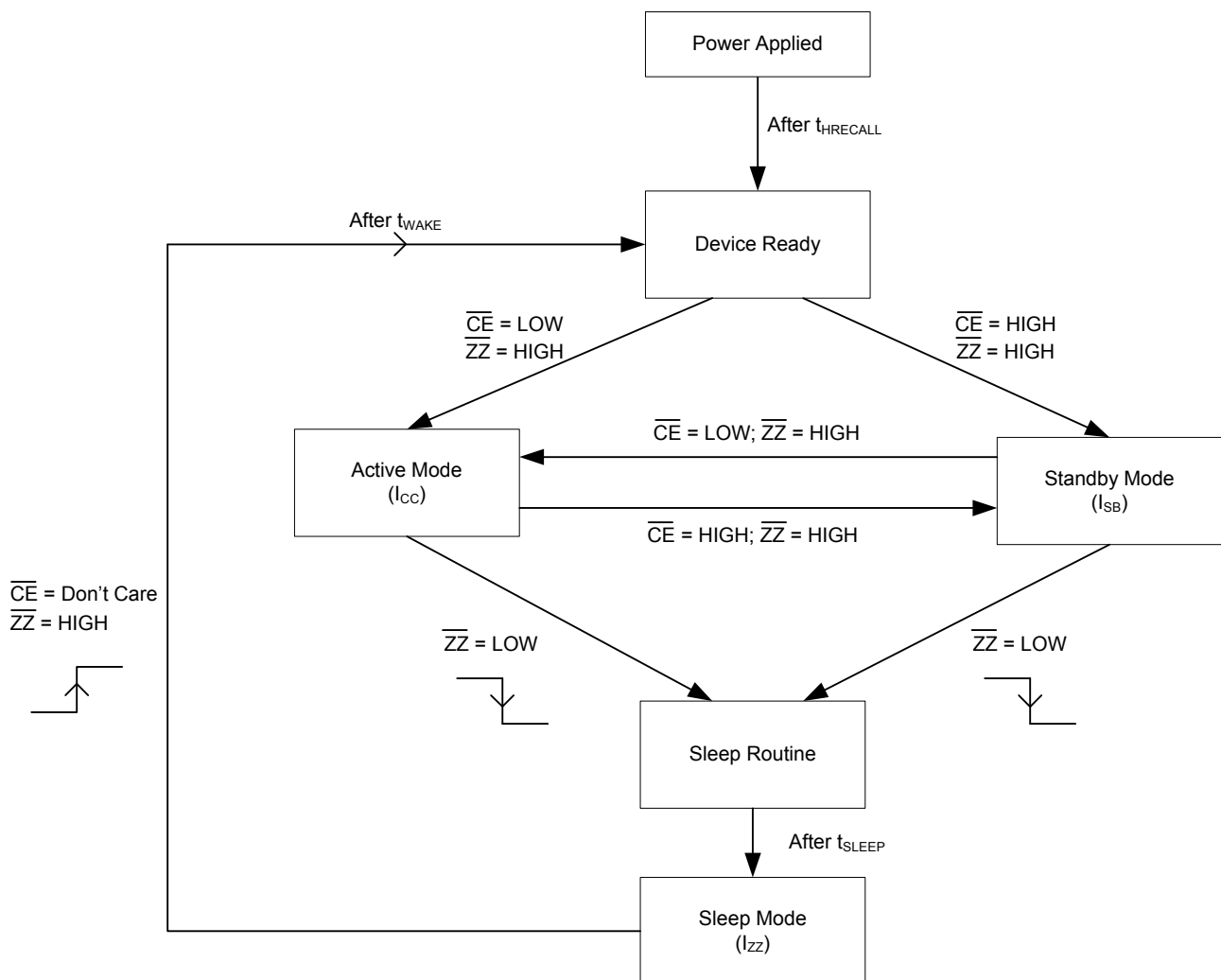
## Sleep Mode

In Sleep mode, the device consumes the lowest power supply current ( $I_{ZZ}$ ). The device enters a low-power Sleep mode after asserting the  $\overline{ZZ}$  pin LOW. After the Sleep mode is registered, the nvSRAM does a STORE operation to secure the data to the nonvolatile memory and then enters the low-power mode. The device starts consuming  $I_{ZZ}$  current after  $t_{SLEEP}$  time from the instance when the Sleep mode is initiated. When the  $\overline{ZZ}$  pin is LOW, all input pins are ignored except the  $\overline{ZZ}$  pin. The nvSRAM is not accessible for normal operations while it is in Sleep mode.

When the  $\overline{ZZ}$  pin is de-asserted (HIGH), there is a delay  $t_{WAKE}$  before you can access the device. If Sleep mode is not used, the  $\overline{ZZ}$  pin should be tied to  $V_{CCQ}$ .

**Note** When nvSRAM enters the Sleep mode, it initiates a nonvolatile STORE cycle, which results in losing one endurance cycle for every Sleep mode entry unless the data was not written to the nvSRAM since the last nonvolatile STORE/RECALL operation.

**Figure 3. Sleep Mode ( $\overline{ZZ}$ ) Flow Diagram**



**Table 2. Mode Selection**

$\overline{CE}^{[3]}$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}, \overline{BLE}$	$A_{15} - A_0^{[4]}$	Mode	I/O	Power
H	X	X	X	X	Not selected	Output High Z	Standby
L	H	L	L	X	Read SRAM	Output Data	Active
L	L	X	L	X	Write SRAM	Input Data	Active
L	H	L	X	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x8B45	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM AutoStore Disable	Output Data Output Data Output Data Output Data Output Data Output Data	Active <sup>[5]</sup>
L	H	L	X	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x4B46	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM AutoStore Enable	Output Data Output Data Output Data Output Data Output Data Output Data	Active <sup>[5]</sup>
L	H	L	X	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x8FC0	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile STORE	Output Data Output Data Output Data Output Data Output Data Output High Z	Active $I_{CC2}^{[5]}$
L	H	L	X	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x4C63	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile RECALL	Output Data Output Data Output Data Output Data Output Data Output High Z	Active <sup>[5]</sup>

**Notes**

3. In this datasheet,  $\overline{CE}$  refers to the internal logical combination of  $\overline{CE}_1$  and  $CE_2$  such that when  $\overline{CE}_1$  is LOW and  $CE_2$  is HIGH,  $\overline{CE}$  is LOW. Intermediate voltage levels are not permitted on any of the chip enable pins.
4. While there are 20 address lines on the CY14V116N, only 13 address lines ( $A_{14}-A_2$ ) are used to control software modes. The remaining address lines are don't care.
5. The six consecutive address locations must be in the order listed.  $\overline{WE}$  must be HIGH during all six cycles to enable a nonvolatile operation.



## Preventing AutoStore

The AutoStore function is disabled by initiating an AutoStore disable sequence. A sequence of read operations is performed in a manner similar to the Software STORE initiation. To initiate the AutoStore disable sequence, the following sequence of  $\overline{CE}$  or  $\overline{OE}$  controlled read operations must be performed:

1. Read address 0x4E38 Valid Read
2. Read address 0xB1C7 Valid Read
3. Read address 0x83E0 Valid Read
4. Read address 0x7C1F Valid Read
5. Read address 0x703F Valid Read
6. Read address 0x8B45 AutoStore Disable

AutoStore is re-enabled by initiating an AutoStore enable sequence. A sequence of read operations is performed in a manner similar to the software RECALL initiation. To initiate the AutoStore enable sequence, the following sequence of  $\overline{CE}$  or  $\overline{OE}$  controlled read operations must be performed:

1. Read address 0x4E38 Valid Read
2. Read address 0xB1C7 Valid Read
3. Read address 0x83E0 Valid Read
4. Read address 0x7C1F Valid Read
5. Read address 0x703F Valid Read
6. Read address 0x4B46 AutoStore Enable

If the AutoStore function is disabled or re-enabled, a manual software STORE operation must be performed to save the AutoStore state through subsequent power-down cycles. The part comes from the factory with AutoStore enabled and 0x00 written in all cells.

## Data Protection

The CY14V116N protects data from corruption during low-voltage conditions by inhibiting all externally initiated STORE and write operations. The low-voltage condition is detected when  $V_{CC}$  is less than  $V_{SWITCH}$ . If the CY14V116N is in a Write mode at power-up (both  $\overline{CE}$  and  $\overline{WE}$  are LOW), after a RECALL or STORE, the write is inhibited until the SRAM is enabled after  $t_{LZHSB}$  (HSB to output active). When  $V_{CC} < V_{IODIS}$ , I/Os are disabled (no STORE takes place). This protects against inadvertent writes during power-up or brown out conditions.

## Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... -65 °C to +150 °C

Maximum accumulated storage time

At 150 °C ambient temperature ..... 1000 h

At 85 °C ambient temperature ..... 20 Years

Maximum junction temperature ..... 150 °C

Supply voltage on  $V_{CC}$  relative to  $V_{SS}$  ..... -0.5 V to +4.1 V

Supply voltage on  $V_{CCQ}$  relative to  $V_{SS}$  .... -0.5 V to +2.45 V

Voltage applied to outputs

in high-Z state ..... -0.5 V to  $V_{CCQ} + 0.5$  V

Input voltage ..... -0.5 V to  $V_{CCQ} + 0.5$  V

Transient voltage (<20 ns) on

any pin to ground potential ..... -2.0 V to  $V_{CCQ} + 2.0$  V

Package power dissipation

capability ( $T_A = 25$  °C) ..... 1.0 W

Surface mount lead soldering

temperature (3 Seconds) ..... +260 °C

DC output current (1 output at a time, 1s duration) ..... 20 mA

Static discharge voltage ..... > 2001 V  
(per MIL-STD-883, Method 3015)

Latch-up current ..... > 140 mA

## Operating Range

Range	Ambient Temperature ( $T_A$ )	$V_{CC}$	$V_{CCQ}$
Industrial	-40 °C to +85 °C	2.7 V to 3.6 V	1.65 V to 1.95 V

## DC Electrical Characteristics

Over the [Operating Range](#)

Parameter	Description	Test Conditions	Min	Typ <sup>[6]</sup>	Max	Unit
$V_{CC}$	Core power supply		2.7	3.0	3.6	V
$V_{CCQ}$	I/O power supply		1.65	1.80	1.95	V
$I_{CC1}$	Average $V_{CC}$ current	Values obtained without output loads ( $I_{OUT} = 0$ mA)	-	-	95	mA
		$t_{RC} = 30$ ns				
		$t_{RC} = 45$ ns	-	-	75	mA
$I_{CCQ1}$	Average $V_{CCQ}$ current	Values obtained without output loads ( $I_{OUT} = 0$ mA)	-	-	30	mA
		$t_{RC} = 30$ ns				
		$t_{RC} = 45$ ns	-	-	25	mA
$I_{CC2}$	Average $V_{CC}$ current during STORE	All inputs don't care, $V_{CC} = V_{CC}(\text{max})$ . Average current for duration $t_{STORE}$	-	-	10	mA
$I_{CC3}$	Average $V_{CC}$ current at $t_{RC} = 200$ ns, $V_{CC}(\text{typ})$ , 25 °C	All inputs cycling at CMOS levels. Values obtained without output loads ( $I_{OUT} = 0$ mA).	-	50	-	mA
$I_{CCQ3}$	Average $V_{CC}$ current at $t_{RC} = 200$ ns, $V_{CCQ}(\text{typ})$ , 25 °C	All inputs cycling at CMOS levels. Values obtained without output loads ( $I_{OUT} = 0$ mA).	-	15	-	mA
$I_{CC4}$ <sup>[7]</sup>	Average $V_{CAP}$ current during AutoStore cycle	All inputs don't care. Average current for duration $t_{STORE}$	-	-	6	mA
$I_{SB}$	$V_{CC}$ standby current	$\overline{CE} \geq (V_{CCQ} - 0.2 \text{ V})$ . $V_{IN} \leq 0.2 \text{ V}$ or $\geq (V_{CCQ} - 0.2 \text{ V})$ . Standby current level after nonvolatile cycle is complete. Inputs are static. $f = 0$ MHz.	$t_{RC} = 30$ ns	-	-	650 $\mu\text{A}$
			$t_{RC} = 45$ ns	-	-	500 $\mu\text{A}$
$I_{ZZ}$	Sleep mode current	All inputs are static at CMOS level	-	-	10	$\mu\text{A}$

### Notes

6. Typical values are at 25 °C,  $V_{CC} = V_{CC}(\text{typ})$  and  $V_{CCQ} = V_{CCQ}(\text{typ})$ . Not 100% tested.

7. This parameter is only guaranteed by design and is not tested.

## DC Electrical Characteristics (continued)

Over the [Operating Range](#)

Parameter	Description	Test Conditions	Min	Typ <sup>[6]</sup>	Max	Unit
$I_{IX}^{[8]}$	Input leakage current (except HSB)	$V_{CC} = V_{CC}(\text{max}), V_{SS} \leq V_{IN} \leq V_{CC}$	-1	-	+1	$\mu\text{A}$
	Input leakage current (for HSB)	$V_{CC} = V_{CC}(\text{max}), V_{SS} \leq V_{IN} \leq V_{CC}$	-100	-	+1	$\mu\text{A}$
$I_{OZ}$	Off state output leakage current	$V_{CC} = V_{CC}(\text{max}), V_{SS} \leq V_{OUT} \leq V_{CC}, \overline{CE}$ or $\overline{OE} \geq V_{IH}$ or $\overline{BLE}/\overline{BHE} \geq V_{IH}$ or $\overline{WE} \leq V_{IL}$	-1	-	+1	$\mu\text{A}$
$V_{IH}$	Input HIGH voltage		$0.7 \times V_{CCQ}$	-	$V_{CCQ} + 0.3$	V
$V_{IL}$	Input LOW voltage		$V_{SS} - 0.3$	-	$0.3 \times V_{CCQ}$	V
$V_{OH}$	Output HIGH voltage	$I_{OUT} = -1 \text{ mA}$	$V_{CCQ} - 0.45$	-	-	V
$V_{OL}$	Output LOW voltage	$I_{OUT} = 2 \text{ mA}$	-	-	0.45	V
$V_{CAP}^{[9]}$	Storage capacitor	Between $V_{CAP}$ pin and $V_{SS}$	19.8	22.0	82.0	$\mu\text{F}$
$V_{V_{CAP}}^{[10, 11]}$	Maximum voltage driven on $V_{CAP}$ pin by the device	$V_{CC} = V_{CC}(\text{max})$	-	-	5.0	V

## Data Retention and Endurance

Over the [Operating Range](#)

Parameter	Description	Min	Unit
$\text{DATA}_R$	Data retention	20	Years
$\text{NV}_C$	Nonvolatile STORE operations	1,000,000	Cycles

## Capacitance

In the following table, the capacitance parameters are listed.<sup>[11]</sup>

Parameter	Description	Test Conditions	Max	Unit
$C_{IN}$	Input capacitance	$T_A = 25^\circ\text{C}, f = 1 \text{ MHz},$ $V_{CC} = V_{CC}(\text{typ}), V_{CCQ} = V_{CCQ}(\text{typ})$	10	pF
$C_{IO}$	Input/Output capacitance		10	pF
$C_{OUT}$	Output capacitance		10	pF

## Thermal Resistance

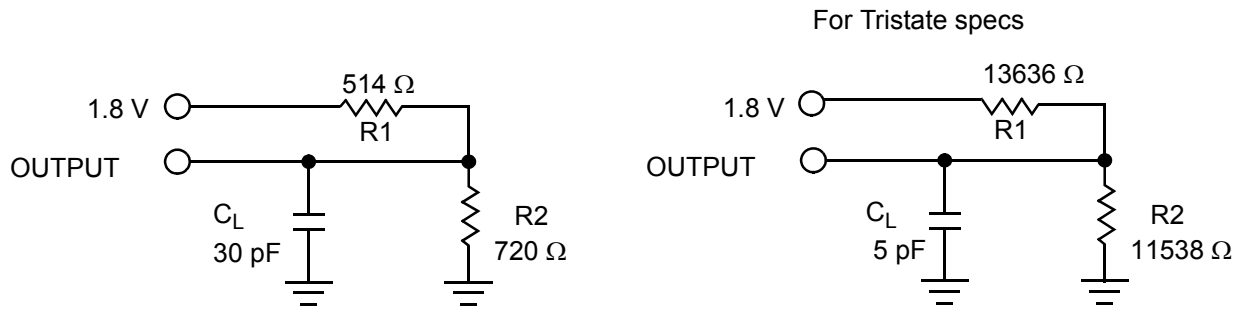
In the following table, the thermal resistance parameters are listed.<sup>[11]</sup>

Parameter	Description	Test Conditions	165-FBGA	Unit
$\Theta_{JA}$	Thermal resistance (Junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	15.6	$^\circ\text{C/W}$
$\Theta_{JC}$	Thermal resistance (Junction to case)		2.9	$^\circ\text{C/W}$

### Notes

- The HSB pin has  $I_{OUT} = -4 \mu\text{A}$  for  $V_{OH}$  of 1.07 V when both active HIGH and LOW drivers are disabled. When they are enabled standard  $V_{OH}$  and  $V_{OL}$  are valid. This parameter is characterized but not tested.
- Min  $V_{CAP}$  value guarantees that there is a sufficient charge available to complete a successful AutoStore operation. Max  $V_{CAP}$  value guarantees that the capacitor on  $V_{CAP}$  is charged to a minimum voltage during a Power-Up RECALL cycle so that an immediate power-down cycle can complete a successful AutoStore. Therefore, it is always recommended to use a capacitor within the specified min and max limits.
- Maximum voltage on  $V_{CAP}$  pin ( $V_{V_{CAP}}$ ) is provided for guidance when choosing the  $V_{CAP}$  capacitor. The voltage rating of the  $V_{CAP}$  capacitor across the operating temperature range should be higher than the  $V_{V_{CAP}}$  voltage.
- These parameters are only guaranteed by design and are not tested.

**Figure 4. AC Test Loads and Waveforms**



### AC Test Conditions

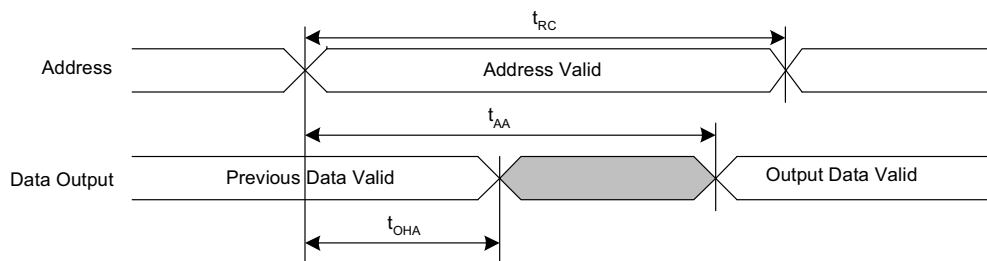
Input pulse levels.....0 V to 1.8 V  
 Input rise and fall times (10% - 90%).....  $\leq 3 \text{ ns}$   
 Input and output timing reference levels..... 0.9 V

## AC Switching Characteristics

Over the [Operating Range](#)<sup>[12]</sup>

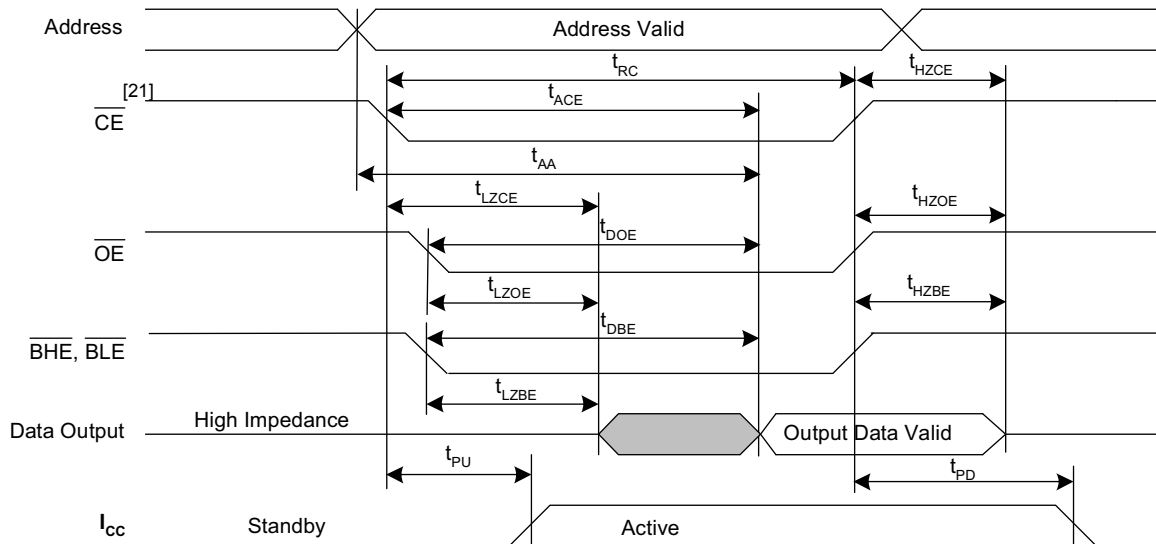
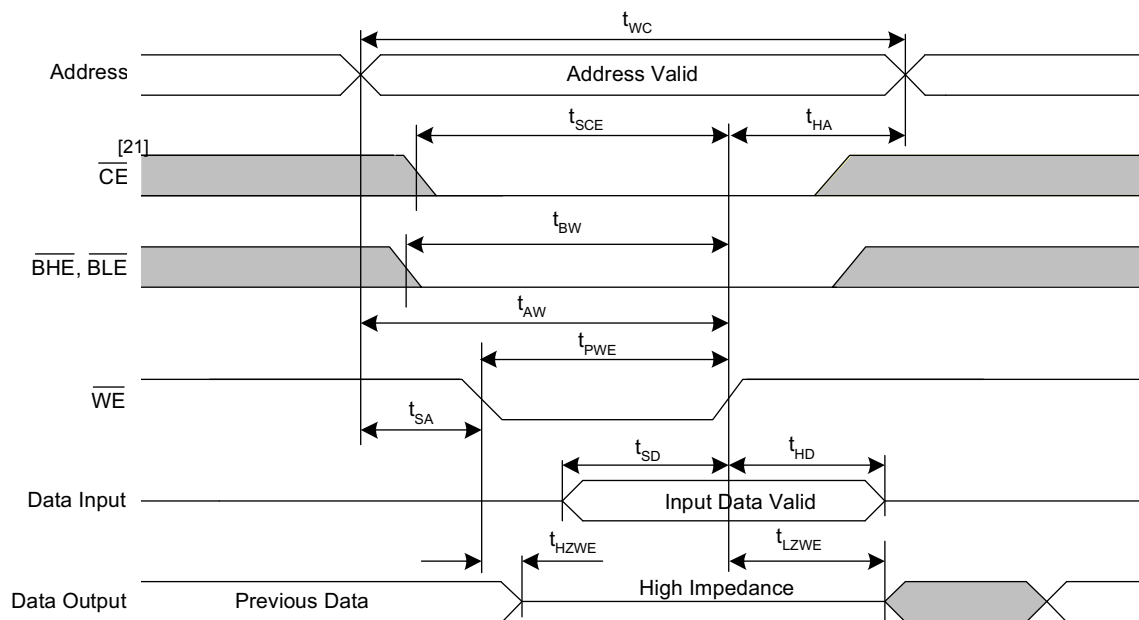
Parameters		Description	30 ns		45 ns		Unit
Cypress Parameter	Alt Parameter		Min	Max	Min	Max	
SRAM Read Cycle							
t <sub>ACE</sub>	t <sub>ACS</sub>	Chip enable access time	–	30	–	45	ns
t <sub>RC</sub> <sup>[14]</sup>	t <sub>RC</sub>	Read cycle time	30	–	45	–	ns
t <sub>AA</sub> <sup>[15]</sup>	t <sub>AA</sub>	Address access time	–	30	–	45	ns
t <sub>DOE</sub>	t <sub>OE</sub>	Output enable to data valid	–	14	–	20	ns
t <sub>OHA</sub> <sup>[15]</sup>	t <sub>OH</sub>	Output hold after address change	3	–	3	–	ns
t <sub>LZCE</sub> <sup>[16]</sup>	t <sub>LZ</sub>	Chip enable to output active	3	–	3	–	ns
t <sub>HZCE</sub> <sup>[13, 16]</sup>	t <sub>HZ</sub>	Chip disable to output inactive	–	12	–	15	ns
t <sub>LZOE</sub> <sup>[16]</sup>	t <sub>OLZ</sub>	Output enable to output active	0	–	0	–	ns
t <sub>HZOE</sub> <sup>[13, 16]</sup>	t <sub>OHZ</sub>	Output disable to output inactive	–	12	–	15	ns
t <sub>PU</sub> <sup>[16]</sup>	t <sub>PA</sub>	Chip enable to power active	0	–	0	–	ns
t <sub>PD</sub> <sup>[16]</sup>	t <sub>PS</sub>	Chip disable to power standby	–	30	–	45	ns
t <sub>DBE</sub>	-	Byte enable to data valid	–	14	–	20	ns
t <sub>LZBE</sub> <sup>[16]</sup>	-	Byte enable to output active	0	–	0	–	ns
t <sub>HZBE</sub> <sup>[13, 16]</sup>	-	Byte disable to output inactive	–	12	–	15	ns
SRAM Write Cycle							
t <sub>WC</sub>	t <sub>WC</sub>	Write cycle time	30	–	45	–	ns
t <sub>PWE</sub>	t <sub>WP</sub>	Write pulse width	24	–	30	–	ns
t <sub>SCE</sub>	t <sub>CW</sub>	Chip enable to end of write	24	–	30	–	ns
t <sub>SD</sub>	t <sub>DW</sub>	Data setup to end of write	14	–	15	–	ns
t <sub>HD</sub>	t <sub>DH</sub>	Data hold after end of write	0	–	0	–	ns
t <sub>AW</sub>	t <sub>AW</sub>	Address setup to end of write	24	–	30	–	ns
t <sub>SA</sub>	t <sub>AS</sub>	Address setup to start of write	0	–	0	–	ns
t <sub>HA</sub>	t <sub>WR</sub>	Address hold after end of write	0	–	0	–	ns
t <sub>HZWE</sub> <sup>[13, 16, 17]</sup>	t <sub>WZ</sub>	Write enable to output disable	–	12	–	15	ns
t <sub>LZWE</sub> <sup>[16]</sup>	t <sub>OW</sub>	Output active after end of write	3	–	3	–	ns
t <sub>BW</sub>	-	Byte enable to end of write	24	–	30	–	ns

**Figure 5. SRAM Read Cycle 1: Address Controlled**<sup>[14, 15, 18]</sup>



### Notes

12. Test conditions assume a signal transition time of 3 ns or less, timing reference levels of  $V_{CCQ}/2$ , input pulse levels of 0 to  $V_{CCQ}$  (typ), and output loading of the specified  $I_{OL}/I_{OH}$  and 30-pF load capacitance, as shown in [Figure 4](#) on page 12.
13.  $t_{HZCE}$ ,  $t_{HZOE}$ ,  $t_{HZBE}$ , and  $t_{HZWE}$  are specified with a load capacitance of 5 pF. Transition is measured  $\pm 200$  mV from the steady state output voltage.
14.  $\overline{WE}$  must be HIGH during SRAM read cycles.
15. Device is continuously selected with  $\overline{CE}$ ,  $\overline{OE}$  and  $\overline{BLE}$ ,  $\overline{BHE}$  LOW.
16. These parameters are only guaranteed by design and are not tested.
17. If  $\overline{WE}$  is LOW when  $\overline{CE}$  goes LOW, the outputs remain in the high impedance state.
18. HSB must remain HIGH during Read and Write cycles.

**Figure 6. SRAM Read Cycle 2:  $\overline{CE}$  and  $\overline{OE}$  Controlled<sup>[19, 20]</sup>**

**Figure 7. SRAM Write Cycle 1:  $\overline{WE}$  Controlled<sup>[22, 20, 23]</sup>**

**Notes**

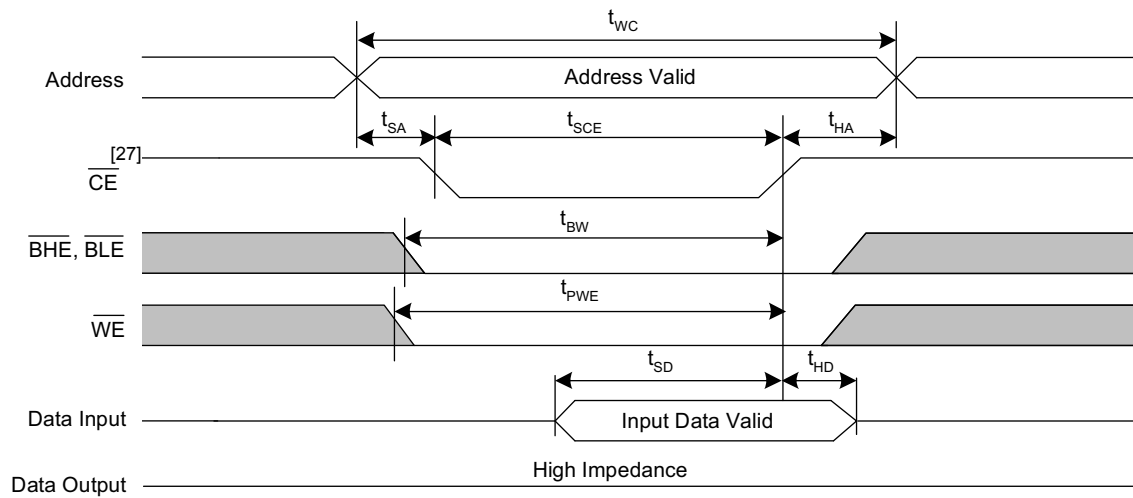
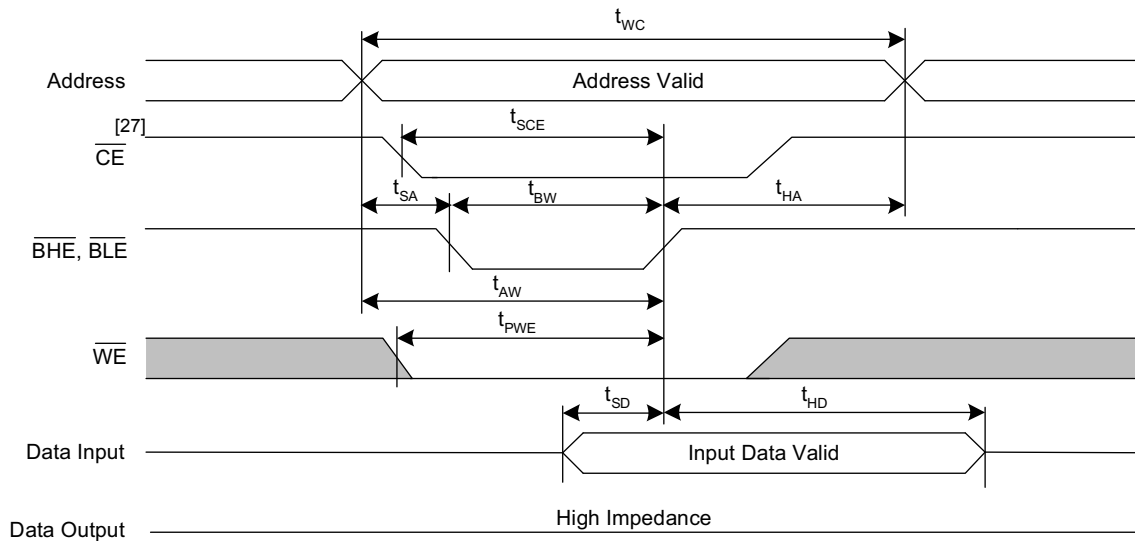
19.  $\overline{WE}$  must be HIGH during SRAM read cycles.

20.  $\overline{HSB}$  must remain HIGH during Read and Write cycles.

21. In this datasheet  $\overline{CE}$  refers to the internal logical combination of  $\overline{CE}_1$  and  $CE_2$  such that when  $\overline{CE}_1$  is LOW and  $CE_2$  is HIGH,  $\overline{CE}$  is LOW. Intermediate voltage levels are not permitted on any of the chip enable pins.

22. If  $\overline{WE}$  is LOW when  $\overline{CE}$  goes LOW, the outputs remain in the high impedance state.

23.  $\overline{CE}$  or  $\overline{WE}$  must be  $\geq V_{IH}$  during address transitions.

**Figure 8. SRAM Write Cycle 2:  $\overline{\text{CE}}$  Controlled**<sup>[ 24, 25, 26]</sup>

**Figure 9. SRAM Write Cycle 3:  $\overline{\text{BHE}}$ ,  $\overline{\text{BLE}}$  Controlled**<sup>[ 24, 25, 26]</sup>

**Notes**

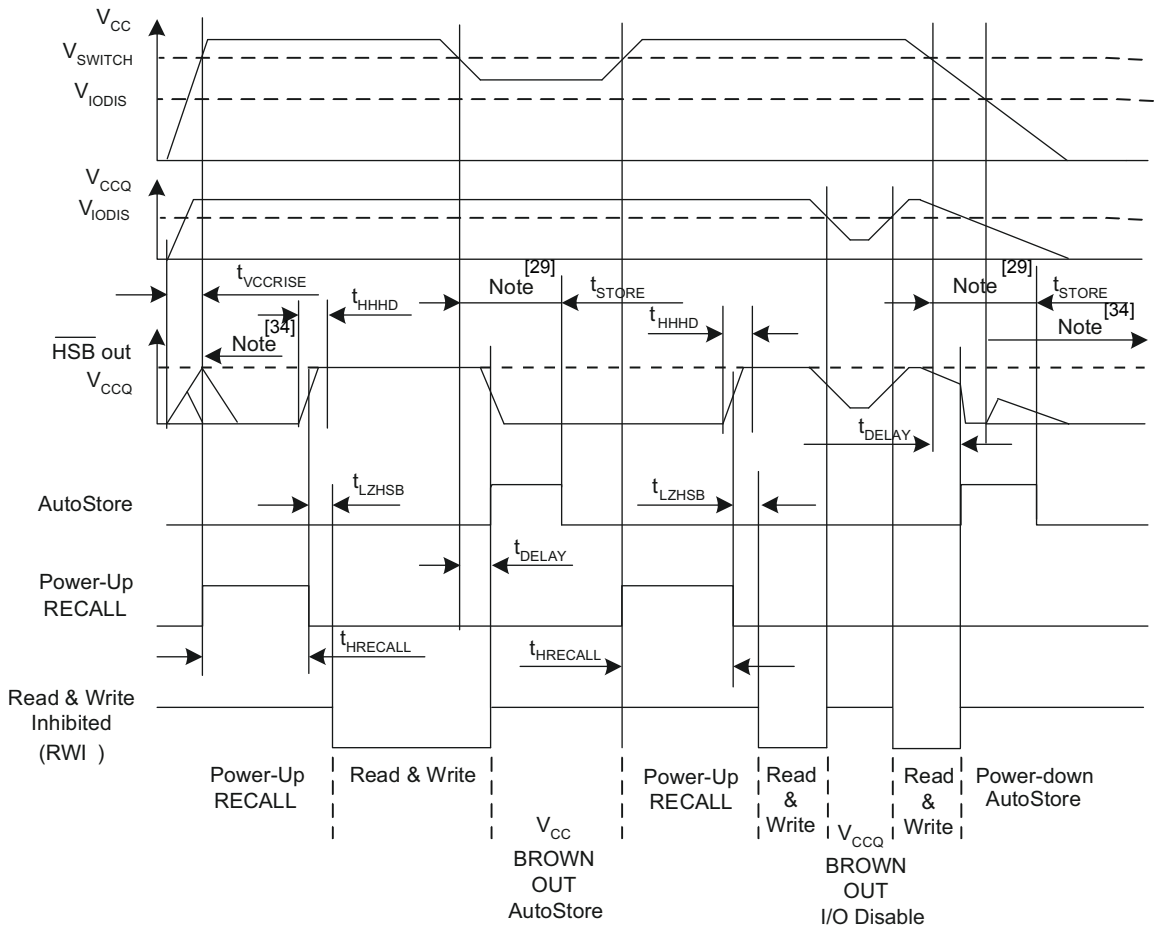
24. If  $\overline{\text{WE}}$  is LOW when  $\overline{\text{CE}}$  goes LOW, the outputs remain in the high-impedance state.
25.  $\overline{\text{HSB}}$  must remain HIGH during Read and Write cycles.
26.  $\overline{\text{CE}}$  or  $\overline{\text{WE}}$  must be  $\geq V_{\text{IH}}$  during address transitions.
27. In this datasheet,  $\overline{\text{CE}}$  refers to the internal logical combination of  $\overline{\text{CE}}_1$  and  $\text{CE}_2$  such that when  $\overline{\text{CE}}_1$  is LOW and  $\text{CE}_2$  is HIGH,  $\overline{\text{CE}}$  is LOW. Intermediate voltage levels are not permitted on any of the chip enable pins.



## Over the Operating Range

Parameter	Description		Min	Max	Unit
t <sub>HRECALL</sub> <sup>[28]</sup>	Power-Up RECALL duration		–	30	ms
t <sub>STORE</sub> <sup>[29]</sup>	STORE cycle duration		–	8	ms
t <sub>DELAY</sub> <sup>[30, 31]</sup>	Time allowed to complete SRAM write cycle		–	25	ns
V <sub>SWITCH</sub>	Low voltage trigger level		–	2.65	V
t <sub>VCCRISE</sub> <sup>[31]</sup>	V <sub>CC</sub> rise time		150	–	μs
V <sub>IODIS</sub> <sup>[32]</sup>	I/O disable voltage on V <sub>CCQ</sub>		–	1.5	V
V <sub>HDIS</sub> <sup>[31]</sup>	HSB output disable voltage		–	1.9	V
t <sub>LZHSB</sub> <sup>[31]</sup>	HSB to output active time		–	5	μs
t <sub>HHHD</sub> <sup>[31]</sup>	HSB HIGH active time		–	500	ns

**Figure 10. AutoStore or Power-Up RECALL<sup>[33]</sup>**



## Notes

28.  $t_{HRECALL}$  starts from the time  $V_{CC}$  rises above  $V_{SWITCH}$ .
29. If an SRAM write has not taken place since the last nonvolatile cycle, no AutoStore or Hardware STORE takes place.
30. On a Hardware STORE and AutoStore initiation, SRAM write operation continues to be enabled for time  $t_{DELAY}$ .
31. These parameters are only guaranteed by design and are not tested.
32. HSB is not defined below  $V_{IODIS}$  voltage.
33. Read and Write cycles are ignored during STORE, RECALL, and while  $V_{CC}$  is below  $V_{SWITCH}$ .
34. During power-up and power-down, HSB glitches when HSB pin is pulled up through an external resistor.

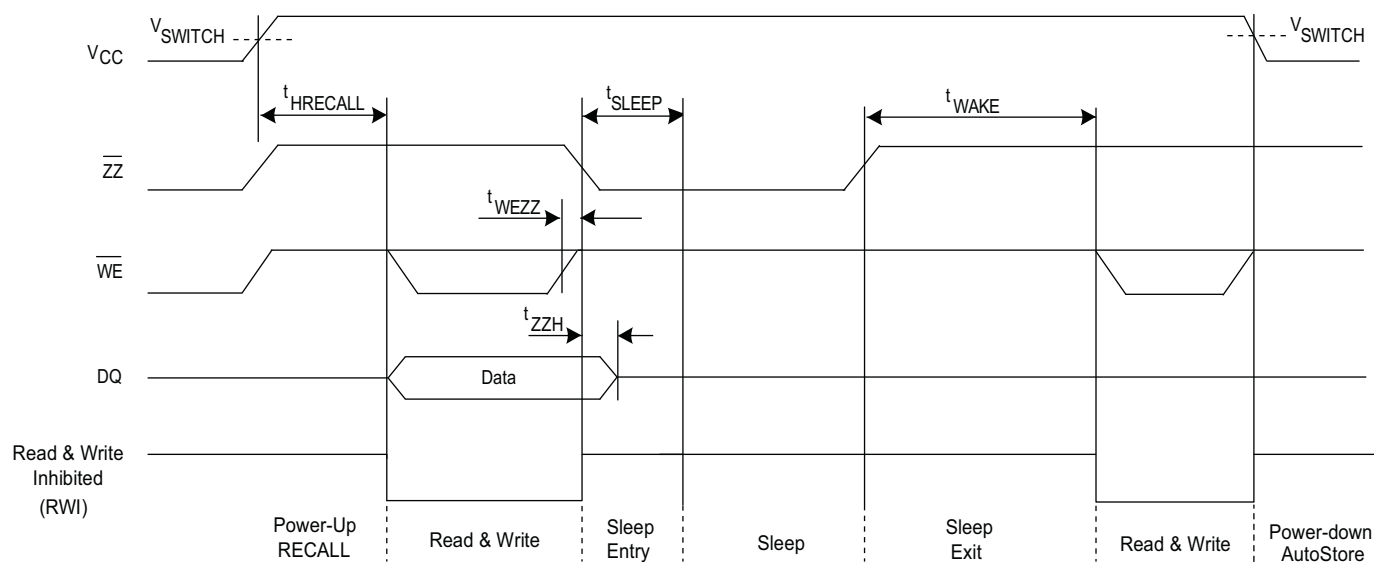


## Sleep Mode Characteristics

Over the [Operating Range](#)

Parameter	Description	Min	Max	Unit
$t_{WAKE}$	Sleep mode exit time ( $\overline{ZZ}$ HIGH to first access after wakeup)	–	30	ms
$t_{SLEEP}$	Sleep mode enter time ( $\overline{ZZ}$ LOW to $\overline{CE}$ don't care)	–	8	ms
$t_{ZZL}$	$\overline{ZZ}$ active LOW time	50	–	ns
$t_{WEZZ}$	Last write to Sleep mode entry time	0	–	$\mu$ s
$t_{ZZH}$	$\overline{ZZ}$ active to DQ Hi-Z time	–	70	ns

**Figure 11. Sleep Mode<sup>[35]</sup>**



**Note**

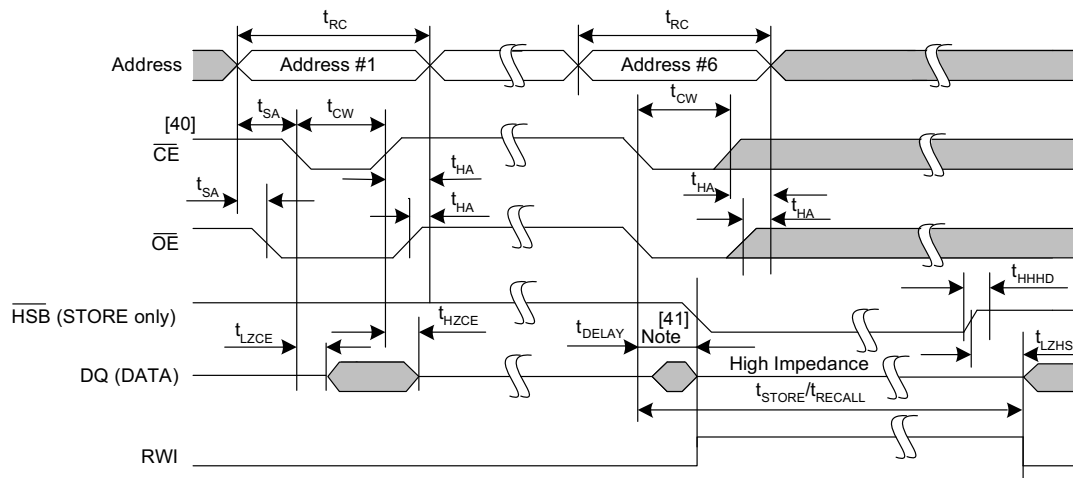
35. Device initiates sleep routine and enters into Sleep mode after  $t_{SLEEP}$  duration.

## Software Controlled STORE and RECALL Characteristics

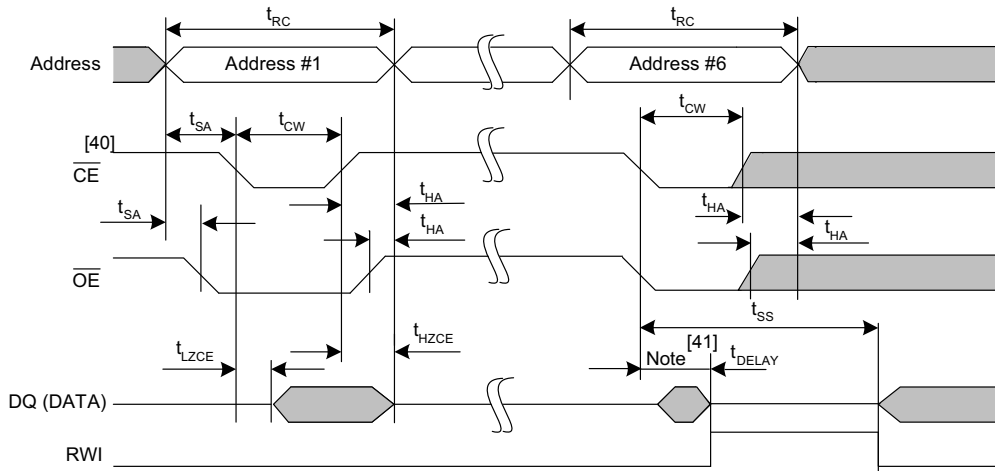
Over the [Operating Range](#)<sup>[36, 37]</sup>

Parameter	Description	30 ns		45 ns		Unit
		Min	Max	Min	Max	
$t_{RC}$	STORE/RECALL initiation cycle time	30	—	45	—	ns
$t_{SA}$	Address setup time	0	—	0	—	ns
$t_{CW}$	Clock pulse width	24	—	30	—	ns
$t_{HA}$	Address hold time	0	—	0	—	ns
$t_{RECALL}$	RECALL duration	—	600	—	600	$\mu$ s
$t_{SS}$ <sup>[38, 39]</sup>	Soft sequence processing time	—	500	—	500	$\mu$ s

**Figure 12.  $\overline{CE}$  and  $\overline{OE}$  Controlled Software STORE and RECALL Cycle<sup>[37]</sup>**



**Figure 13. AutoStore Enable and Disable Cycle**



### Notes

36. The software sequence is clocked with  $\overline{CE}$  controlled or  $\overline{OE}$  controlled reads.

37. The six consecutive addresses must be read in the order listed in [Table 2](#) on page 8.  $\overline{WE}$  must be HIGH during all six consecutive cycles.

38. This is the amount of time it takes to take action on a soft sequence command.  $V_{CC}$  power must remain high to effectively register command.

39. Commands such as STORE and RECALL lock out I/O until the operation is complete which further increases this time. See the specific command.

40. In this datasheet,  $\overline{CE}$  refers to the internal logical combination of  $\overline{CE}_1$  and  $CE_2$  such that when  $\overline{CE}_1$  is LOW and  $CE_2$  is HIGH,  $\overline{CE}$  is LOW. Intermediate voltage levels are not permitted on any of the chip enable pins.

41. DQ output data at the sixth read may be invalid because the output is disabled at  $t_{DELAY}$  time.

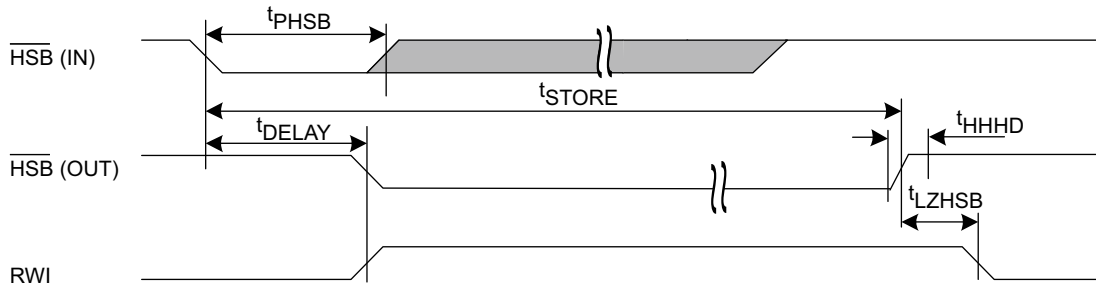
## Hardware STORE Characteristics

Over the [Operating Range](#)

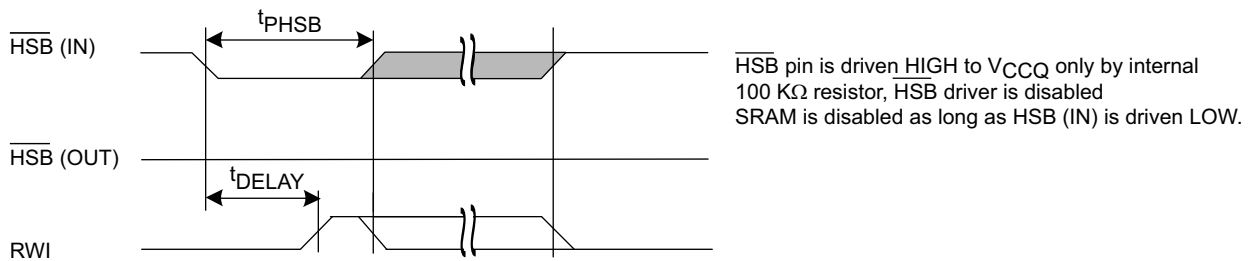
Parameter	Description	Min	Max	Unit
$t_{\text{DHSB}}$	HSB to output active time when write latch not set	–	25	ns
$t_{\text{PHSB}}$	Hardware STORE pulse width	15	–	ns

**Figure 14. Hardware STORE Cycle<sup>[42]</sup>**

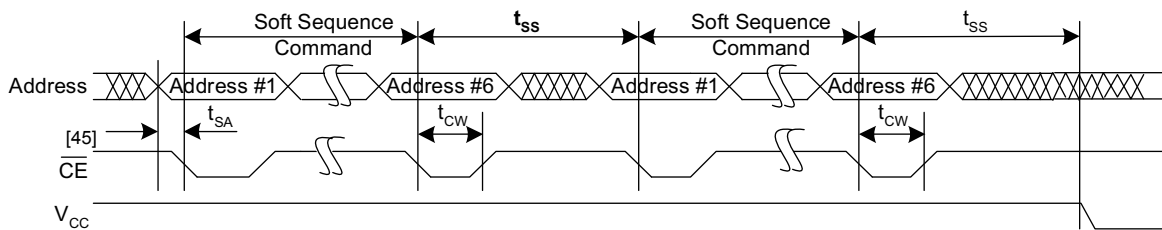
### Write Latch set



### Write Latch not set



**Figure 15. Soft Sequence Processing<sup>[43, 44]</sup>**



### Notes

42. If an SRAM write has not taken place since the last nonvolatile cycle, no AutoStore or Hardware STORE takes place.
43. This is the amount of time it takes to take action on a soft sequence command. Vcc power must remain high to effectively register command.
44. Commands, such as STORE and RECALL, lock out I/O until the operation is complete which further increases this time. See the specific command.
45. In this datasheet,  $\overline{\text{CE}}$  refers to the internal logical combination of  $\overline{\text{CE}}_1$  and  $\text{CE}_2$  such that when  $\overline{\text{CE}}_1$  is LOW and  $\text{CE}_2$  is HIGH,  $\overline{\text{CE}}$  is LOW. Intermediate voltage levels are not permitted on any of the chip enable pins.

## Truth Table For SRAM Operations

$\overline{\text{HSB}}$  should remain HIGH for SRAM Operations.

$\overline{\text{CE}}_1$	$\overline{\text{CE}}_2$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	$\overline{\text{BHE}}$	$\overline{\text{BLE}}$	Inputs and Outputs	Mode	Power
H	X	X	X	X	X	High-Z	Deselect/Power-down	Standby
X	L	X	X	X	X	High-Z	Deselect/Power-down	Standby
L	H	X	X	H	H	High-Z	Output disabled	Active
L	H	H	L	L	L	Data out (DQ <sub>0</sub> –DQ <sub>15</sub> )	Read	Active
L	H	H	L	H	L	Data out (DQ <sub>0</sub> –DQ <sub>7</sub> ); DQ <sub>8</sub> –DQ <sub>15</sub> in High-Z	Read	Active
L	H	H	L	L	H	Data out (DQ <sub>8</sub> –DQ <sub>15</sub> ); DQ <sub>0</sub> –DQ <sub>7</sub> in High-Z	Read	Active
L	H	H	H	X	X	High-Z	Output disabled	Active
L	H	L	X	L	L	Data in (DQ <sub>0</sub> –DQ <sub>15</sub> )	Write	Active
L	H	L	X	H	L	Data in (DQ <sub>0</sub> –DQ <sub>7</sub> ); DQ <sub>8</sub> –DQ <sub>15</sub> in High-Z	Write	Active
L	H	L	X	L	H	Data in (DQ <sub>8</sub> –DQ <sub>15</sub> ); DQ <sub>0</sub> –DQ <sub>7</sub> in High-Z	Write	Active

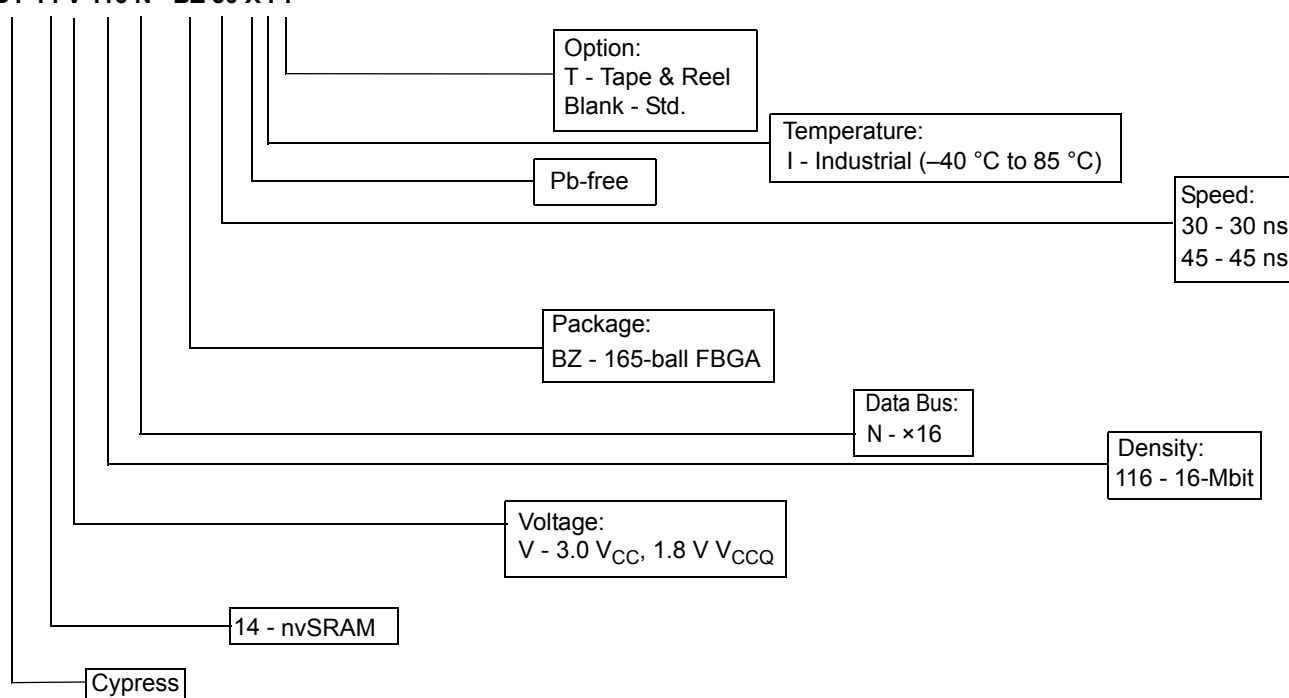
## Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
30	CY14V116N-BZ30XI	51-85195	165-ball FBGA	Industrial
45	CY14V116N-BZ45XI			

All parts are Pb-free. Contact your local Cypress sales representative for availability of these parts.

## Ordering Code Definition

**CY 14 V 116 N - BZ 30 X I T**



**Figure 16. 165-ball FBGA (15 mm × 17 mm × 1.40 mm) Package Outline (51-85195)**



## Acronyms

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
EIA	Electronic Industries Alliance
FBGA	Fine-Pitch Ball Grid Array
I/O	Input/Output
JESD	JEDEC Standards
nvSRAM	nonvolatile Static Random Access Memory
RoHS	Restriction of Hazardous Substances
RWI	Read and Write Inhibited

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	degrees celsius
Hz	hertz
Kbit	kilobit
kHz	kilohertz
kΩ	kiloohm
μA	microampere
mA	milliampere
μF	microfarad
Mbit	megabit
MHz	megahertz
μs	microsecond
ms	millisecond
ns	nanosecond
pF	picofarad
V	volt
Ω	ohm
W	watt

## Document History Page

Document Title: CY14V116N, 16-Mbit (1024 K × 16) nvSRAM Document Number: 001-75791				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	3516347	GVCH	02/03/2011	New data sheet.
*A	3733467	GVCH	09/14/2012	Updated <a href="#">Device Operation</a> (Added <a href="#">Figure 3</a> under <a href="#">Sleep Mode</a> ). Updated <a href="#">Maximum Ratings</a> (Changed “Ambient temperature with power applied” to “Maximum junction temperature”). Updated <a href="#">DC Electrical Characteristics</a> (Added $V_{V_{CAP}}$ parameter and its details, added footnote 9 and referred the same note in $V_{V_{CAP}}$ parameter). Updated <a href="#">Capacitance</a> (Changed maximum value of $C_{IN}$ and $C_{OUT}$ parameters from 7 pF to 11.5 pF). Added <a href="#">Sleep Mode</a> and <a href="#">Switching Waveforms</a> (Corresponding to SLEEP Mode).
*B	3944873	GVCH	03/26/2013	Removed 2.5 V operating range voltage support Removed 25 ns access speed and added 30 ns access speed Changed $V_{CCQ}$ max voltage value from $V_{CC}$ to 1.95 V Removed ×32 configuration support Changed $V_{IH}$ , $V_{IL}$ , $V_{OL}$ , $V_{OH}$ spec values Updated <a href="#">Capacitance</a> (Changed maximum value of $C_{IN}$ and $C_{OUT}$ parameters from 11.5 pF to 8 pF). Changed R1 value from 13636 $\Omega$ to 514 $\Omega$ and R2 value from 11538 $\Omega$ to 720 $\Omega$
*C	4260504	GVCH	01/24/2014	Modified <a href="#">Logic Block Diagram</a> for more clarity. Updated <a href="#">AutoStore Operation (Power-Down)</a> : Removed sentence “The HSB signal is monitored by the system to detect if an AutoStore cycle is in progress.” Modified <a href="#">Figure 3</a> for more clarity. Added $I_{SB}$ max spec value for 45 ns access speed Added footnote 6 Changed $V_{CAP}$ min value from 20 $\mu F$ to 19.8 $\mu F$ Added footnote 13 Updated <a href="#">Figure 10</a> and <a href="#">Figure 11</a> for more clarity Changed $t_{ZZH}$ max value from 20 ns to 70 ns
*D	4417851	GVCH	06/24/2014	<a href="#">DC Electrical Characteristics</a> : Added footnote 7 Updated maximum value of $V_{V_{CAP}}$ parameter from 4.5 V to 5.0 V  <a href="#">Capacitance</a> : Updated $C_{IN}$ and $C_{OUT}$ value from 8 pF to 10 pF Added $C_{IO}$ parameter  Updated <a href="#">Thermal Resistance</a> values
*E	4432183	GVCH	07/07/2014	<a href="#">DC Electrical Characteristics</a> : Updated maximum value of $V_{CAP}$ parameter from 120.0 $\mu F$ to 82.0 $\mu F$
*F	4456803	ZSK	07/31/2014	No content update.
*G	4571551	ZSK	11/17/2014	Added documentation related hyperlink in page 1.
*H	4616093	GVCH	01/07/2015	Changed datasheet status from Preliminary to Final.



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