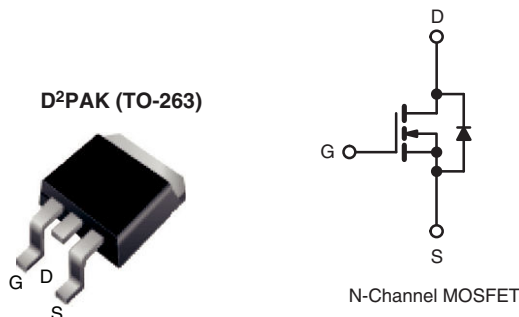


E Series Power MOSFET

PRODUCT SUMMARY

V _{DS} (V) at T _J max.	700	
R _{DS(on)} max. at 25 °C (Ω)	V _{GS} = 10 V	0.145
Q _g max. (nC)	122	
Q _{gs} (nC)	21	
Q _{gd} (nC)	37	
Configuration	Single	



FEATURES

- Low Figure-of-Merit (FOM) R_{on} x Q_g
- Low Input Capacitance (C_{iss})
- Reduced Switching and Conduction Losses
- Ultra Low Gate Charge (Q_g)
- Avalanche Energy Rated (UIS)
- Material categorization: For definitions please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Server and Telecom Power Supplies
- Switch Mode Power Supplies (SMPS)
- Power Factor Correction Power Supplies (PFC)
- Lighting
 - High-Intensity Discharge (HID)
 - Fluorescent Ballast Lighting
- Industrial
 - Welding
 - Induction Heating
 - Motor Drives
 - Battery Chargers
 - Renewable Energy
 - Solar (PV Inverters)

ORDERING INFORMATION

Package	D2PAK (TO-263)
Lead (Pb)-free and Halogen-free	SiHB24N65E-GE3

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V _{DS}	650	V
Gate-Source Voltage	V _{GS}	± 20	
Gate-Source Voltage AC (f > 1 Hz)		30	
Continuous Drain Current (T _J = 150 °C)	V _{GS} at 10 V	T _C = 25 °C	A
		T _C = 100 °C	
Pulsed Drain Current ^a	I _{DM}	70	
Linear Derating Factor		2	W/°C
Single Pulse Avalanche Energy ^b	E _{AS}	508	mJ
Maximum Power Dissipation	P _D	250	W
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to + 150	°C
Drain-Source Voltage Slope	dV/dt	37	V/ns
Reverse Diode dV/dt ^d		11	
Soldering Recommendations (Peak Temperature)	for 10 s	300°	°C

Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- V_{DD} = 50 V, starting T_J = 25 °C, L = 28.2 mH, R_g = 25 Ω, I_{AS} = 6 A.
- 1.6 mm from case.
- I_{SD} ≤ I_D, dI/dt = 100 A/μs, starting T_J = 25 °C.

**THERMAL RESISTANCE RATINGS**

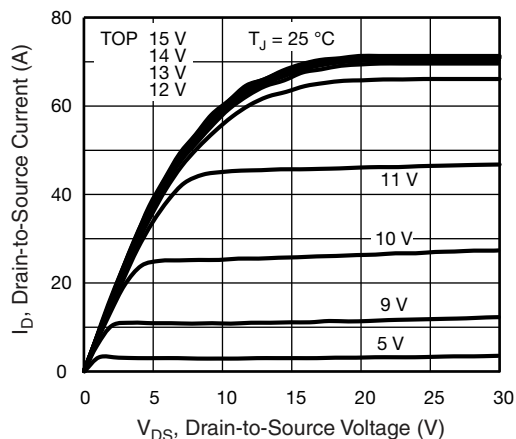
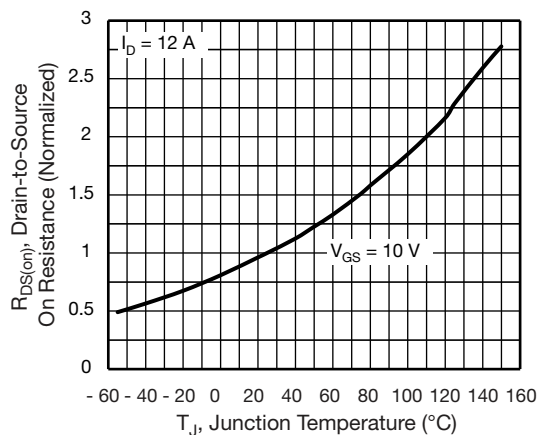
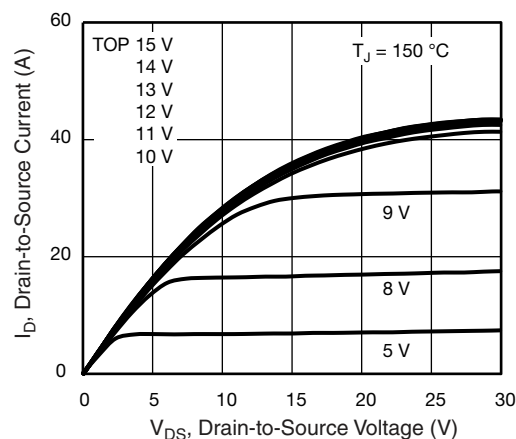
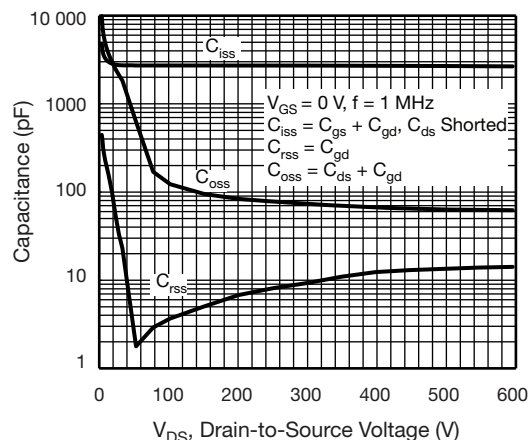
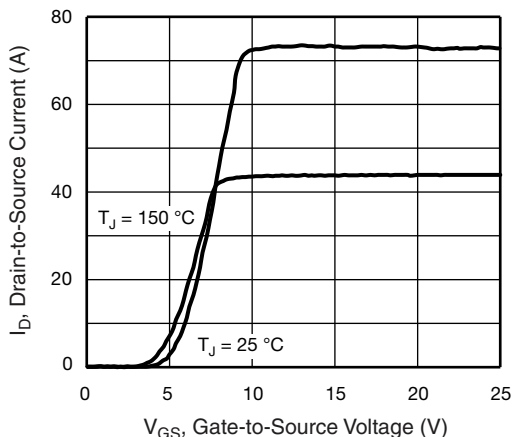
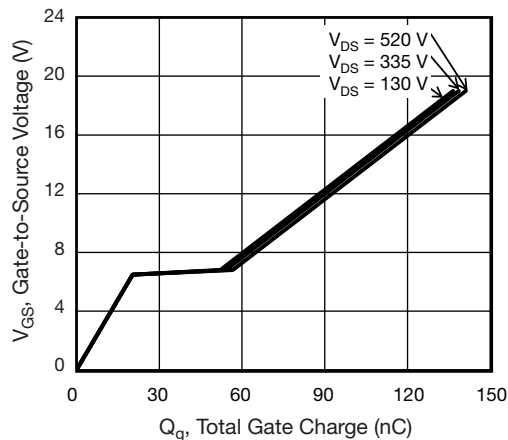
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.5	

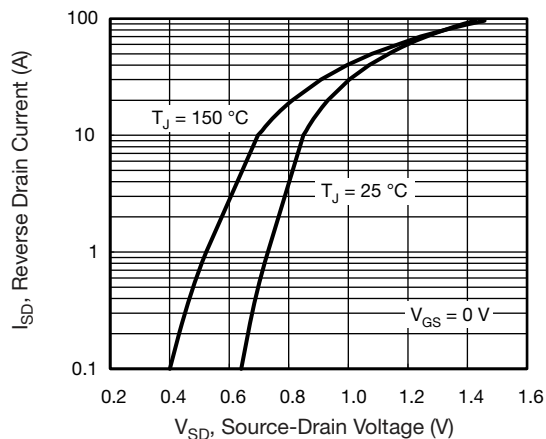
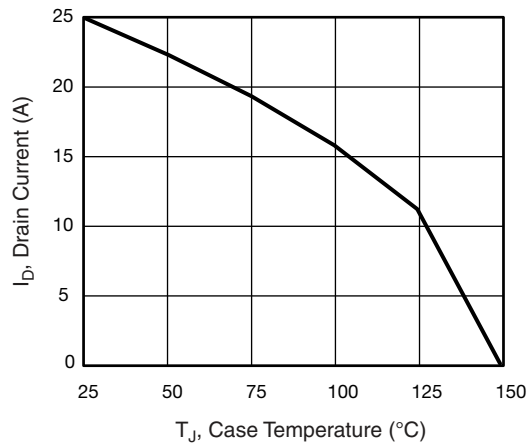
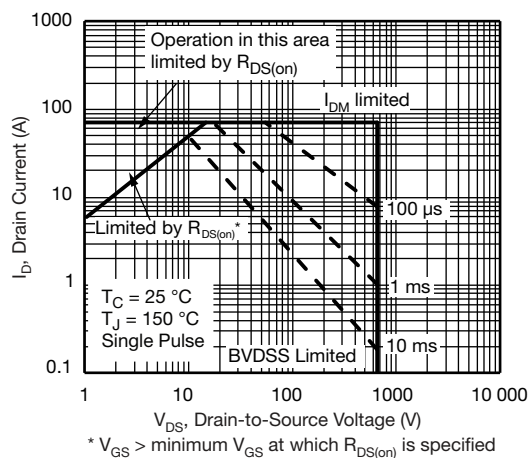
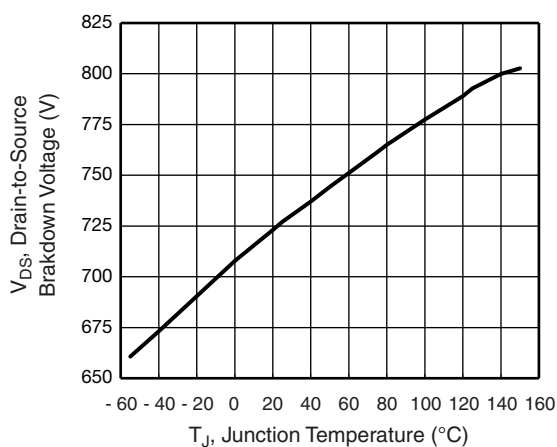
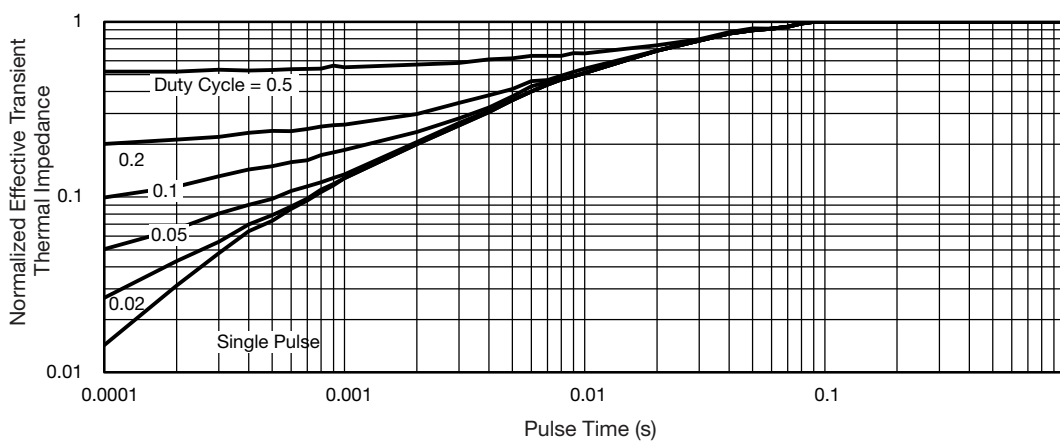
SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

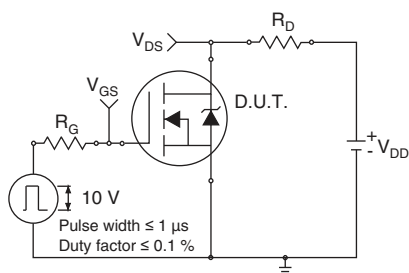
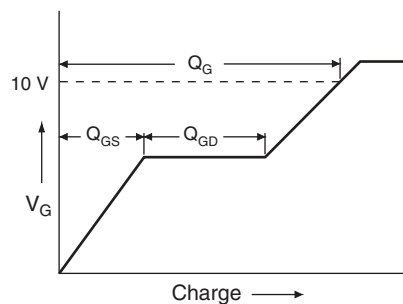
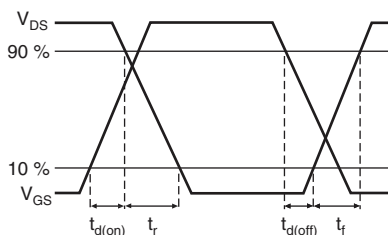
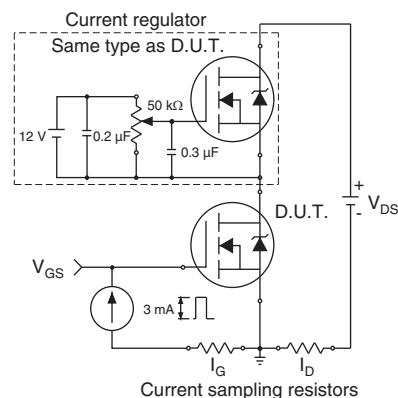
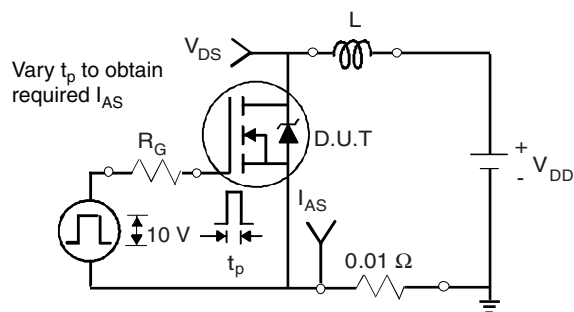
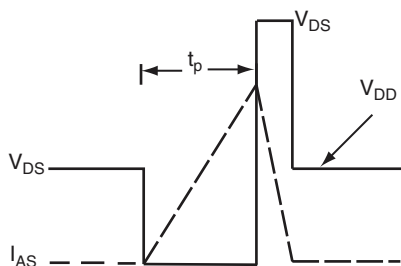
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		650	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 250 μA		-	0.72	-	V/°C
Gate-Source Threshold Voltage (N)	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2	-	4	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 650 V, V _{GS} = 0 V		-	-	1	μA
		V _{DS} = 520 V, V _{GS} = 0 V, T _J = 125 °C		-	-	10	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 12 A	-	0.120	0.145	Ω
Forward Transconductance	g _{fs}	V _{DS} = 8 V, I _D = 5 A		-	7.1	-	S
Dynamic							
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 100 V, f = 1 MHz		-	2740	-	pF
Output Capacitance	C _{oss}			-	122	-	
Reverse Transfer Capacitance	C _{rss}			-	4	-	
Effective Output Capacitance, Energy Related ^a	C _{o(er)}	V _{DS} = 0 V to 520 V, V _{GS} = 0 V		-	93	-	
Effective Output Capacitance, Time Related ^b	C _{o(tr)}			-	352	-	
Total Gate Charge	Q _g	V _{GS} = 10 V	I _D = 12 A, V _{DS} = 520 V	-	81	122	nC
Gate-Source Charge	Q _{gs}			-	21	-	
Gate-Drain Charge	Q _{gd}			-	37	-	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 520 V, I _D = 12 A, V _{GS} = 10 V, R _g = 9.1 Ω		-	24	48	ns
Rise Time	t _r			-	84	126	
Turn-Off Delay Time	t _{d(off)}			-	70	105	
Fall Time	t _f			-	69	104	
Gate Input Resistance	R _g	f = 1 MHz, open drain		-	0.68	-	Ω
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	24	A
Pulsed Diode Forward Current	I _{SM}			-	-	70	
Diode Forward Voltage	V _{SD}	T _J = 25 °C, I _S = 12 A, V _{GS} = 0 V		-	-	1.2	V
Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = I _S = 12 A, dI/dt = 100 A/μs, V _R = 25 V		-	433	-	ns
Reverse Recovery Charge	Q _{rr}			-	7.3	-	μC
Reverse Recovery Current	I _{RRM}			-	28	-	A

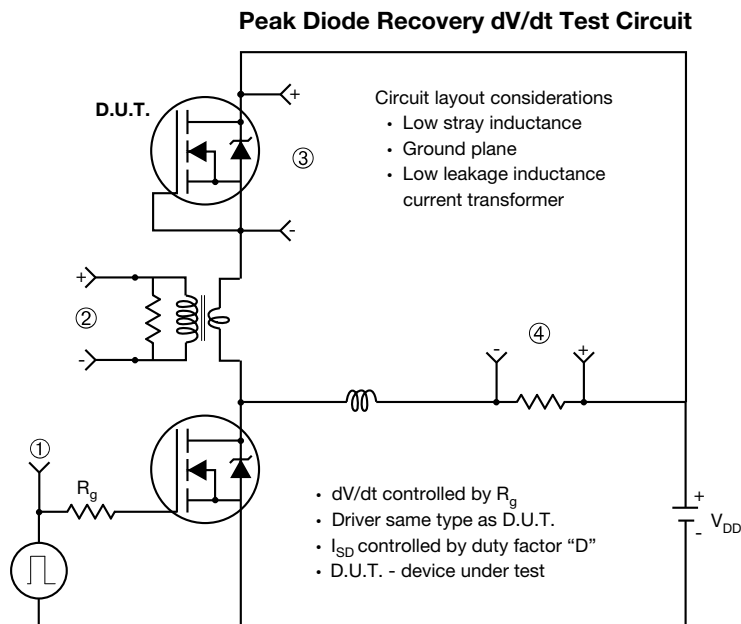
Notes

- a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .
b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics

Fig. 4 - Normalized On-Resistance vs. Temperature

Fig. 2 - Typical Output Characteristics

Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

Fig. 3 - Typical Transfer Characteristics

Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage


Fig. 7 - Typical Source-Drain Diode Forward Voltage

Fig. 9 - Maximum Drain Current vs. Case Temperature

Fig. 8 - Maximum Safe Operating Area

Fig. 10 - Temperature vs. Drain-to-Source Voltage

Fig. 11 - Normalized Thermal Transient Impedance, Junction-to-Case


Fig. 12 - Switching Time Test Circuit

Fig. 16 - Basic Gate Charge Waveform

Fig. 13 - Switching Time Waveforms

Fig. 17 - Gate Charge Test Circuit

Fig. 14 - Unclamped Inductive Test Circuit

Fig. 15 - Unclamped Inductive Waveforms


Note

a. $V_{GS} = 5 V$ for logic level devices

Fig. 18 - For N-Channel

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	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
H	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	-	1.65	-	0.066
L2	-	1.78	-	0.070
L3	0.25 BSC		0.010 BSC	
L4	4.78	5.28	0.188	0.208

—

RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

[Return to Index](#)



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Электрон
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