SN65HVD23x 3.3-V CAN Bus Transceivers

1 Features

- Single 3.3-V Supply Voltage
- Bus Pins Fault Protection Exceeds ±36 V
- Bus Pins ESD Protection Exceeds ±16 kV HBM
- Compatible With ISO 11898-2
- GIFT/ICT Compliant
- Data Rates up to 1 Mbps
- Extended –7 V to 12 V Common Mode Range
- High-Input Impedance Allows for 120 Nodes
- LVTTL I/Os are 5-V Tolerant
- Adjustable Driver Transition Times for Improved Emissions Performance
- Unpowered Node Does Not Disturb the Bus
- Low Current Standby Mode, 200-μA (Typical)
- SN65HVD233: Loopback Mode
- SN65HVD234: Ultra Low Current Sleep Mode
  - 50-nA Typical Current Consumption
- SN65HVD235: Autobaud Loopback Mode
- Thermal Shutdown Protection
- Power up and Down With Glitch-Free Bus Inputs and Outputs
  - High-Input Impedance With Low V_{CC}
  - Monolithic Output During Power Cycling

2 Applications

- Industrial Automation, Control, Sensors, and Drive Systems
- Motor and Robotic Control
- Building and Climate Control (HVAC)
- Backplane Communication and Control
- CAN Bus Standards such as CANopen, DeviceNet, CAN Kingdom, ISO 11783, NMEA 2000, SAE J1939

3 Description

The SN65HVD233, SN65HVD234, and SN65HVD235 are used in applications employing the controller area network (CAN) serial communication physical layer in accordance with the ISO 11898 standard. As a CAN transceiver, each provides transmit and receive capability between the differential CAN bus and a CAN controller, with signaling rates up to 1 Mbps.

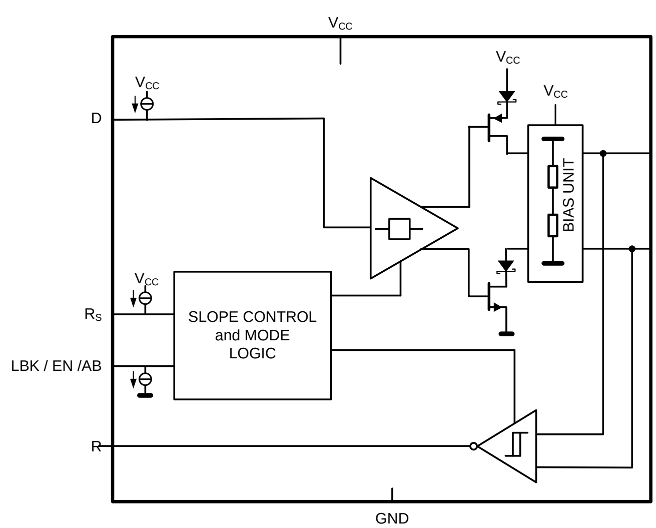
Designed for operation in especially harsh environments, the devices feature cross-wire protection, overvoltage protection up to ±36 V, loss of ground protection, overtemperature (thermal shutdown) protection, and common-mode transient protection of ±100 V. These devices operate over a wide –7 V to 12 V common-mode range. These transceivers are the interface between the host CAN controller on the microprocessor and the differential CAN bus used in industrial, building automation, transportation, and automotive applications.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN65HVD233	SOIC (8)	4.90 mm × 3.91 mm
SN65HVD234		
SN65HVD235		

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Block Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (August 2008) to Revision G **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Changed the Functional Block Diagrams ... 4
- Added the THERMAL SHUTDOWN paragraph to the Application Information section ... 21
- Changed the BUS CABLE paragraph to BUS LOADING, LENGTH AND NUMBER OF NODES paragraph in the Application Information section ... 24
- Added the CAN TERMINATION paragraph to the Application Information section ... 24

Changes from Revision E (October 2007) to Revision F **Page**

- Changed Figure 17, Receiver Test Circuit and Voltage Waveform. From: C_L = 50 pF ±20% to: C_L = 15 pF ±20% ... 13

Changes from Revision D (June 2005) to Revision E **Page**

- Added 60-Ω load test condition to Figure 3 ... 10
- Deleted INTEROPERABILITY WITH 5-V CAN SYSTEMS section ... 26
- Added ISO 11898 COMPLIANCE OF SN65HVD230 FAMILY OF 3.3-V CAN TRANSCEIVERS section ... 26

Changes from Revision C (March 2005) to Revision D **Page**

- Added Features Bullet: GIFT/ICT Compliant (SN65HVD234) ... 1

Changes from Revision B (June 2003) to Revision C — **Page**

- Added I_O, Receiver output current to the Abs Max Table 5

Changes from Revision A (March 2003) to Revision B — **Page**

- Changed the data sheet from Product Preview to Production for part number SN65HVD234 and SN65HVD235. 1
- Added , Thermal Characteristics 5
- Changed the APPLICATION INFORMATION section. 23

Changes from Original (November 2002) to Revision A — **Page**

- Changed the data sheet from Product Preview to Production for part number SN65HVD233. 1

5 Description (continued)

Modes: The R_S pin (pin 8) of the SN65HVD233, SN65HVD234, and SN65HVD235 provides three modes of operation: high-speed, slope control, and low-power standby mode. The high-speed mode of operation is selected by connecting pin 8 directly to ground, allowing the driver output transistors to switch on and off as fast as possible with no limitation on the rise and fall slope. The rise and fall slope can be adjusted by connecting a resistor between the R_S pin and ground. The slope will be proportional to the pin's output current. With a resistor value of 10 kΩ the device driver will have a slew rate of ~15 V/μs and with a value of 100 kΩ the device will have ~2.0 V/μs slew rate. For more information about slope control, refer to *Feature Description*.

The SN65HVD233, SN65HVD234, and SN65HVD235 enter a low-current standby (listen only) mode during which the driver is switched off and the receiver remains active if a high logic level is applied to the R_S pin. If the local protocol controller needs to transmit a message to the bus it will have to return the device to either high-speed mode or slope control mode via the R_S pin.

Loopback (SN65HVD233): A logic high on the loopback (LBK) pin (pin 5) of the SN65HVD233 places the bus output and bus input in a high-impedance state. Internally, the D to R path of the device remains active and available for driver to receiver loopback that can be used for self-diagnostic node functions without disturbing the bus. For more information on the loopback mode, refer to *Feature Description*.

Ultra Low-Current Sleep (SN65HVD234): The SN65HVD234 enters an ultra low-current sleep mode in which both the driver and receiver circuits are deactivated if a low logic level is applied to EN pin (pin 5). The device remains in this sleep mode until the circuit is reactivated by applying a high logic level to pin 5.

Autobaud Loopback (SN65HVD235): The AB pin (pin 5) of the SN65HVD235 implements a bus listen-only loopback feature which allows the local node controller to synchronize its baud rate with that of the CAN bus. In autobaud mode, the bus output of the driver is placed in a high-impedance state while the bus input of the receiver remains active. There is an internal D pin to R pin loopback to assist the controller in baud rate detection, or the autobaud function. For more information on the autobaud mode, refer to *Feature Description*.

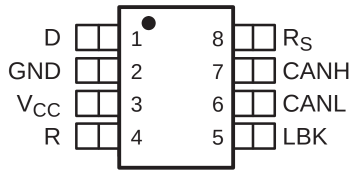
6 Device Options[(1)]

PART NUMBER	LOW POWER MODE	SLOPE CONTROL	DIAGNOSTIC LOOPBACK	AUTOBAUD LOOPBACK
SN65HVD233D	200-μA standby mode	Adjustable	Yes	No
SN65HVD234D	200-μA standby mode or 50-nA sleep mode	Adjustable	No	No
SN65HVD235D	200-μA standby mode	Adjustable	No	Yes

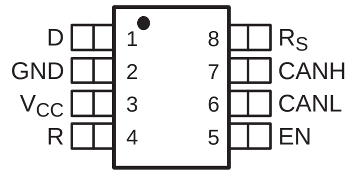
(1) For the most current package and ordering information, see *Mechanical, Packaging, and Orderable Information*, or see the TI web site at www.ti.com.

7 Pin Configuration and Functions

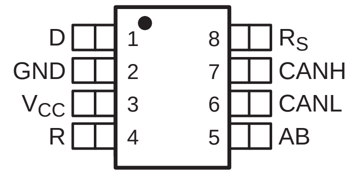
SN65HVD233D
(Marked as VP233)
(TOP VIEW)



SN65HVD234D
(Marked as VP234)
(TOP VIEW)



SN65HVD235D
(Marked as VP235)
(TOP VIEW)



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
D	1	I	CAN transmit data input (LOW for dominant and HIGH for recessive bus states), also called TXD, driver input
GND	2	GND	Ground connection
V_{CC}	3	Supply	Transceiver 3.3-V supply voltage
R	4	O	CAN receive data output (LOW for dominant and HIGH for recessive bus states), also called RXD, receiver output
LBK	5	I	SN65HVD233: Loopback mode input pin
EN		I	SN65HVD234: Enable input pin. Logic high for enabling a normal mode (high speed or slope control) mode. Logic low for sleep mode.
AB		I	SN65HVD235: Autobaud loopback mode input pin
CANL	6	I/O	Low level CAN bus line
CANH	7	I/O	High level CAN bus line
R_S	8	I	Mode select pin: strong pulldown to GND = high speed mode, strong pullup to V_{CC} = low power mode, 10-kΩ to 100-kΩ pulldown to GND = slope control mode

8 Specifications

8.1 Absolute Maximum Ratings(1)(2)

over operating free-air temperature range unless otherwise noted

		MIN	MAX	UNIT
V_{CC}	Supply voltage	–0.3	7	V
	Voltage at any bus terminal (CANH or CANL)	–36	36	V
	Voltage input, transient pulse, CANH and CANL, through 100 Ω (see Figure 18)	–100	100	V
V_I	Input voltage, (D, R_S, EN, LBK, AB)	–0.5	7	V
V_O	Output voltage	–0.5	7	V
I_O	Receiver output current	–10	10	mA
	Continuous total power dissipation	See *Power Dissipation Ratings*		
T_J	Operating junction temperature		150	°C
T_{stg}	Storage temperature		125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground pin.

8.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	CANH, CANL and GND	±16000	V
			All pins	3000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)		±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		3	3.6	V
	Voltage at any bus terminal (separately or common mode)		–7	12	
V_{IH}	High-level input voltage	D, EN, AB, LBK	2	5.5	
V_{IL}	Low-level input voltage	D, EN, AB, LBK	0	0.8	
V_{ID}	Differential input voltage between CANH and CANL		–6	6	
	Resistance from R_S to ground		0	100	kΩ
$V_{I(Rs)}$	Input Voltage at R_S for standby		0.75 V_{CC}	5.5	V
I_{OH}	High-level output current	Driver	–50		mA
		Receiver	–10		
I_{OL}	Low-level output current	Driver		50	mA
		Receiver		10	
T_J	Operating junction temperature	HVD233, HVD234, HVD235		150	°C
T_A	Operating free-air temperature (1)	HVD233, HVD234, HVD235	–40	125	°C

(1) Maximum free-air temperature operation is allowed as long as the device maximum junction temperature is not exceeded.

8.4 Thermal Information

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	VALUE	UNIT
$R_{θJA}$	Junction-to-ambient thermal resistance (1)	Low-K (2) board, no air flow	185	°C/W
		High-K (3) board, no air flow	101	
$R_{θJB}$	Junction-to-board thermal resistance	High-K (3) board, no air flow	82.8	°C/W
$R_{θJC}$	Junction-to-case thermal resistance		26.5	°C/W
$P_{(AVG)}$	Average power dissipation	R_L = 60 Ω, R_S at 0 V, input to D a 1-MHz 50% duty cycle square wave V_{CC} at 3.3 V, T_A = 25°C	36.4	mW
$T_{(SD)}$	Thermal shutdown junction temperature		170	°C

(1) See SZZA003 for an explanation of this parameter.
(2) JESD51-3 low effective thermal conductivity test board for leaded surface mount packages.
(3) JESD51-7 high effective thermal conductivity test board for leaded surface mount packages.

8.5 Power Dissipation Ratings

PACKAGE	CIRCUIT BOARD	T_A ≤ 25°C POWER RATING	DERATING FACTOR (1) ABOVE T_A = 25°C	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
D	Low-K	596.6 mW	5.7 mW/°C	255.7 mW	28.4 mW
D	High-K	1076.9 mW	10.3 mW/°C	461.5 mW	51.3 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

8.6 Electrical Characteristics: Driver

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP[(1)]	MAX	UNIT
$V_{O(D)}$	Bus output voltage (Dominant)	CANH	D at 0 V, R_S at 0 V, See Figure 12 and Figure 13	2.45		V_{CC}	V
		CANL		0.5		1.25	
V_O	Bus output voltage (Recessive)	CANH	D at 3 V, R_S at 0 V, See Figure 12 and Figure 13		2.3		V
		CANL			2.3		
$V_{OD(D)}$	Differential output voltage (Dominant)		D at 0 V, R_S at 0 V, See Figure 12 and Figure 13	1.5	2	3	V
			D at 0 V, R_S at 0 V, See Figure 13 and Figure 14	1.2	2	3	
V_{OD}	Differential output voltage (Recessive)		D at 3 V, R_S at 0 V, See Figure 12 and Figure 13	–120		12	mV
			D at 3 V, R_S at 0 V, No Load	–0.5		0.05	V
$V_{OC(pp)}$	Peak-to-peak common-mode output voltage		See Figure 21		1		V
I_{IH}	High-level input current	D, EN, LBK, AB	D = 2 V or EN = 2 V or LBK = 2 V or AB = 2 V	–30		30	μA
I_{IL}	Low-level input current	D, EN, LBK, AB	D = 0.8 V or EN = 0.8 V or LBK = 0.8 V or AB = 0.8 V	–30		30	μA
I_{OS}	Short-circuit output current		V_{CANH} = –7 V, CANL Open, See Figure 26	–250			mA
			V_{CANH} = 12 V, CANL Open, See Figure 26			1	
			V_{CANL} = –7 V, CANH Open, See Figure 26	–1			
			V_{CANL} = 12 V, CANH Open, See Figure 26			250	
C_O	Output capacitance		See receiver input capacitance				
$I_{IRs(s)}$	R_S input current for standby		R_S at 0.75 V_{CC}	–10			μA
I_{CC}	Supply current	Sleep	EN at 0 V, D at V_{CC}, R_S at 0 V or V_{CC}		0.05	2	μA
		Standby	R_S at V_{CC}, D at V_{CC}, AB at 0 V, LBK at 0 V, EN at V_{CC}		200	600	
		Dominant	D at 0 V, No Load, AB at 0 V, LBK at 0 V, R_S at 0 V, EN at V_{CC}			6	mA
		Recessive	D at V_{CC}, No Load, AB at 0 V, LBK at 0 V, R_S at 0 V, EN at V_{CC}			6	

(1) All typical values are at 25°C and with a 3.3-V supply.

8.7 Electrical Characteristics: Receiver

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage		AB at 0 V, LBK at 0 V, EN at V_{CC}, See Table 1			750	900	mV
V_{IT-}	Negative-going input threshold voltage				500	650		
V_{hys}	Hysteresis voltage ($V_{IT+} – V_{IT-}$)					100		
V_{OH}	High-level output voltage		I_O = –4 mA, See Figure 17		2.4			V
V_{OL}	Low-level output voltage		I_O = 4 mA, See Figure 17				0.4	
I_I	Bus input current		CANH or CANL at 12 V	Other bus pin at 0 V, D at 3 V, AB at 0 V, LBK at 0 V, R_S at 0 V, EN at V_{CC}	150		500	μA
			CANH or CANL at 12 V, V_{CC} at 0 V		200		600	
			CANH or CANL at –7 V		–610		–150	
			CANH or CANL at –7 V, V_{CC} at 0 V		–450		–130	
C_I	Input capacitance (CANH or CANL)		Pin-to-ground, V_I = 0.4 sin (4E6πt) + 0.5 V, D at 3 V, AB at 0 V, LBK at 0 V, EN at V_{CC}			40		pF
C_{ID}	Differential input capacitance		Pin-to-pin, V_I = 0.4 sin (4E6πt) + 0.5 V, D at 3 V, AB at 0 V, LBK at 0 V, EN at V_{CC}			20		
R_{ID}	Differential input resistance		D at 3 V, AB at 0 V, LBK at 0 V, EN at V_{CC}		40		100	kΩ
R_{IN}	Input resistance (CANH or CANL) to ground				20		50	
I_{CC}	Supply current	Sleep	EN at 0 V, D at V_{CC}, R_S at 0 V or V_{CC}			0.05	2	μA
		Standby	R_S at V_{CC}, D at V_{CC}, AB at 0 V, LBK at 0 V, EN at V_{CC}			200	600	
		Dominant	D at 0 V, No Load, R_S at 0 V, LBK at 0 V, AB at 0 V, EN at V_{CC}				6	mA
		Recessive	D at V_{CC}, No Load, R_S at 0 V, LBK at 0 V, AB at 0 V, EN at V_{CC}				6	

(1) All typical values are at 25°C and with a 3.3-V supply.

8.8 Switching Characteristics: Driver

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_S at 0 V, See Figure 15		35	85	ns
		R_S with 10 kΩ to ground, See Figure 15		70	125	
		R_S with 100 kΩ to ground, See Figure 15		500	870	
t_{PHL}	Propagation delay time, high-to-low-level output	R_S at 0 V, See Figure 15		70	120	ns
		R_S with 10 kΩ to ground, See Figure 15		130	180	
		R_S with 100 kΩ to ground, See Figure 15		870	1200	
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} – t_{PLH}\|$)	R_S at 0 V, See Figure 15		35		ns
		R_S with 10 kΩ to ground, See Figure 15		60		
		R_S with 100 kΩ to ground, See Figure 15		370		
t_r	Differential output signal rise time	R_S at 0 V, See Figure 15	20		70	ns
t_f	Differential output signal fall time		20		70	
t_r	Differential output signal rise time	R_S with 10 kΩ to ground, See Figure 15	30		135	ns
t_f	Differential output signal fall time		30		135	
t_r	Differential output signal rise time	R_S with 100 kΩ to ground, See Figure 15	350		1400	ns
t_f	Differential output signal fall time		350		1400	
$t_{en(s)}$	Enable time from standby to dominant	See Figure 19 and Figure 20		0.6	1.5	μs
$t_{en(z)}$	Enable time from sleep to dominant			1	5	

(1) All typical values are at 25°C and with a 3.3-V supply.

8.9 Switching Characteristics: Receiver

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 17		35	60	ns
t_{PHL}	Propagation delay time, high-to-low-level output			35	60	
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} – t_{PLH}\|$)			7		
t_r	Output signal rise time			2	5	
t_f	Output signal fall time			2	5	

(1) All typical values are at 25°C and with a 3.3-V supply.

8.10 Switching Characteristics: Device

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
$t_{(LBK)}$	Loopback delay, driver input to receiver output	HVD233	See Figure 23		7.5	12	ns
$t_{(AB1)}$	Loopback delay, driver input to receiver output	HVD235	See Figure 24		10	20	ns
$t_{(AB2)}$	Loopback delay, bus input to receiver output		See Figure 25		35	60	ns
$t_{(loop1)}$	Total loop delay, driver input to receiver output, recessive to dominant		R_S at 0 V, See Figure 22		70	135	ns
			R_S with 10 kΩ to ground, See Figure 22		105	190	
			R_S with 100 kΩ to ground, See Figure 22		535	1000	
$t_{(loop2)}$	Total loop delay, driver input to receiver output, dominant to recessive		R_S at 0 V, See Figure 22		70	135	ns
			R_S with 10 kΩ to ground, See Figure 22		105	190	
			R_S with 100 kΩ to ground, See Figure 22		535	1000	

(1) All typical values are at 25°C and with a 3.3-V supply.

8.11 Typical Characteristics

Rs, LBK, AB = 0 V; EN = V_{CC}

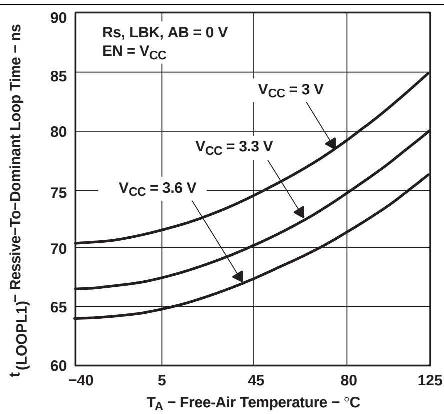


Figure 1. Recessive-to-Dominant Loop Time vs Free-Air Temperature

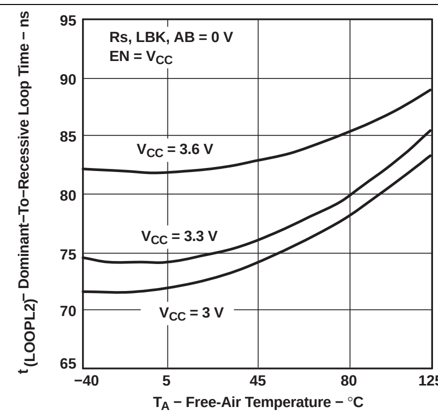
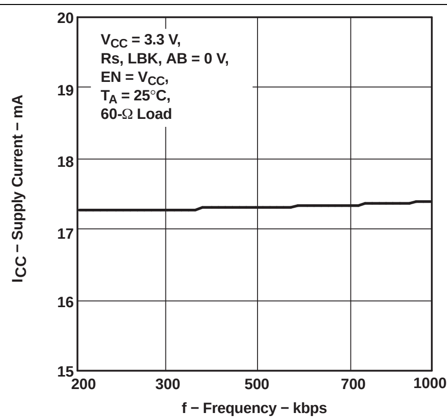
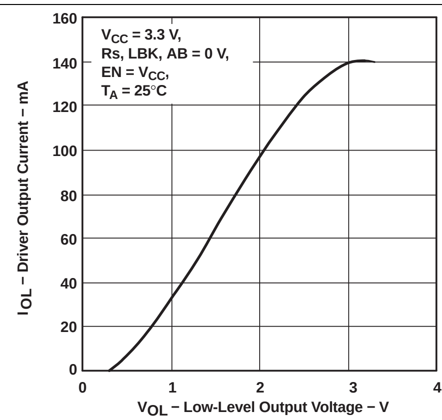


Figure 2. Dominant-to-Recessive Loop Time vs Free-Air Temperature



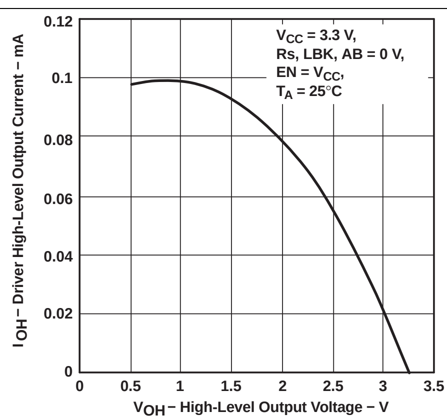
V_{CC} = 3.3 V T_A = 25°C 60-Ω Load

Figure 3. Supply Current vs Frequency



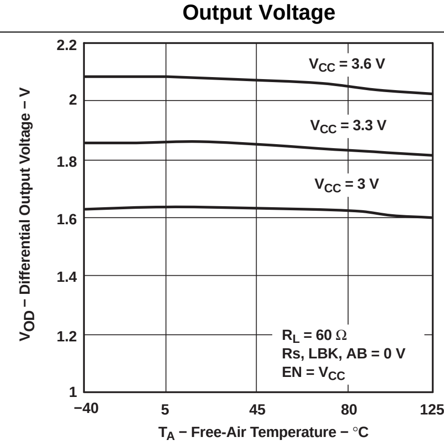
V_{CC} = 3.3 V T_A = 25°C

Figure 4. Driver Low-Level Output Current vs Low-Level Output Voltage



V_{CC} = 3.3 V T_A = 25°C

Figure 5. Driver High-Level Output Current vs High-Level Output Voltage

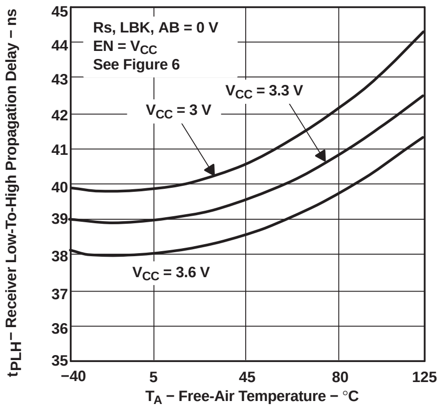


R_L = 60-Ω

Figure 6. Differential Output Voltage vs Free-Air Temperature

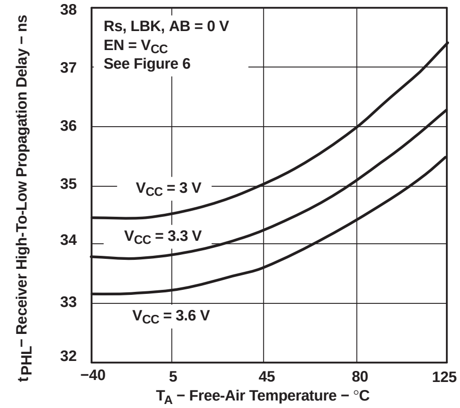
Typical Characteristics (continued)

Rs, LBK, AB = 0 V; EN = V_{CC}



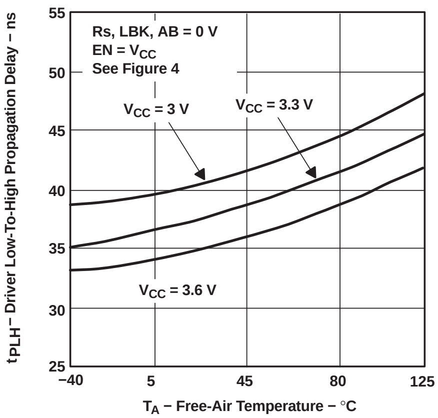
See Figure 3

Figure 7. Receiver Low-to-High Propagation Delay vs Free-Air Temperature



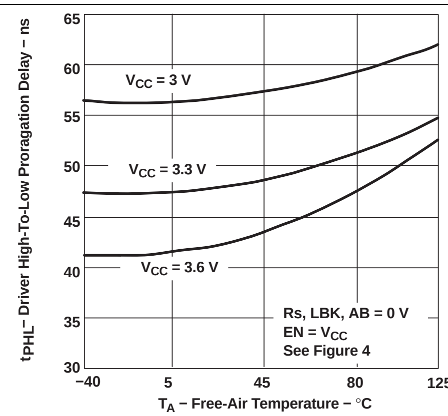
See Figure 3

Figure 8. Receiver High-to-Low Propagation Delay vs Free-Air Temperature



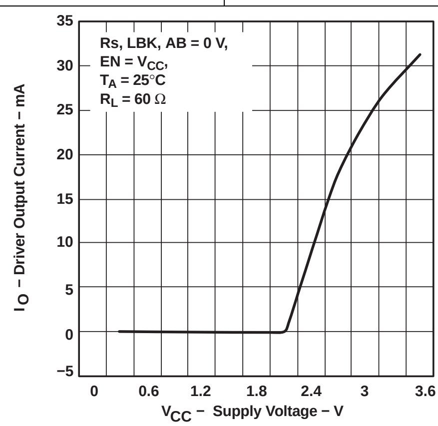
See Figure 1

Figure 9. Driver Low-to-High Propagation Delay vs Free-Air Temperature



See Figure 1

Figure 10. Driver High-to-Low Propagation Delay vs Free-Air Temperature



R_L = 60-Ω T_A = 25°C

Figure 11. Driver Output Current vs Supply Voltage

9 Parameter Measurement Information

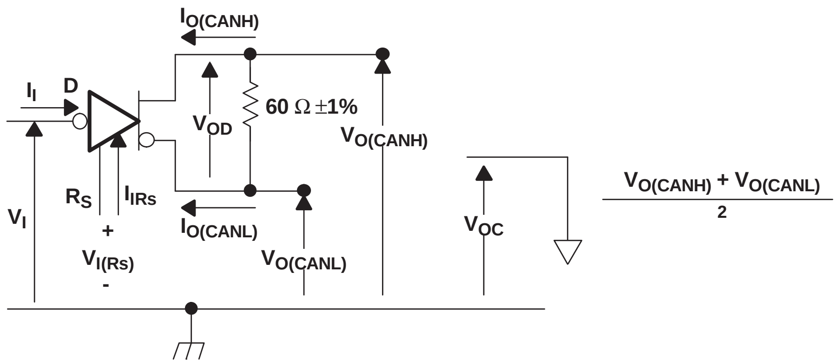


Figure 12. Driver Voltage, Current, and Test Definition

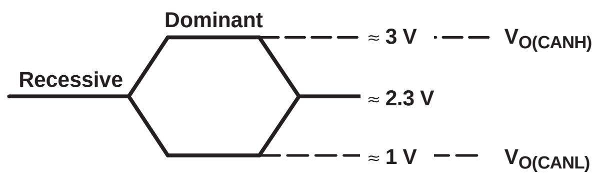


Figure 13. Bus Logic State Voltage Definitions

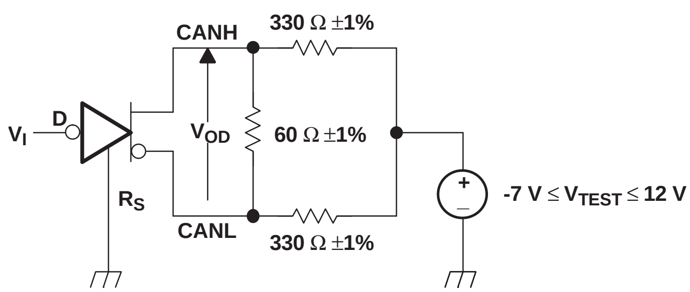
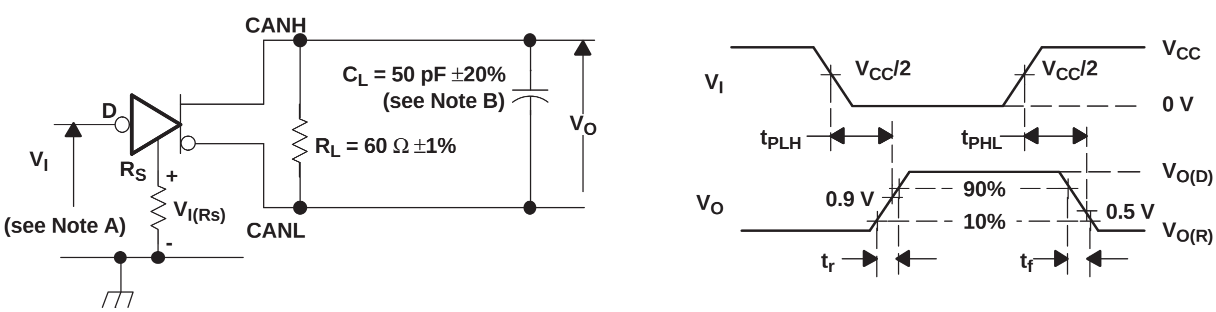


Figure 14. Driver V_{OD}



A. The input pulse is supplied by a generator having the following characteristics: Pulse repetition rate (PRR) ≤ 125 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. C_L includes fixture and instrumentation capacitance.

Figure 15. Driver Test Circuit and Voltage Waveforms

Parameter Measurement Information (continued)

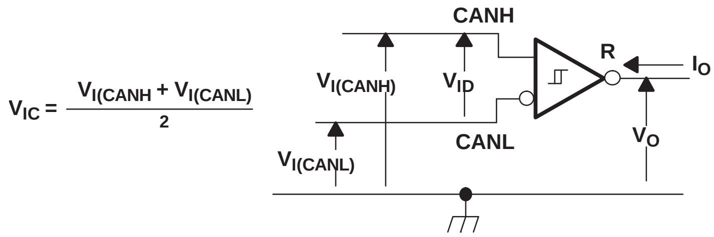
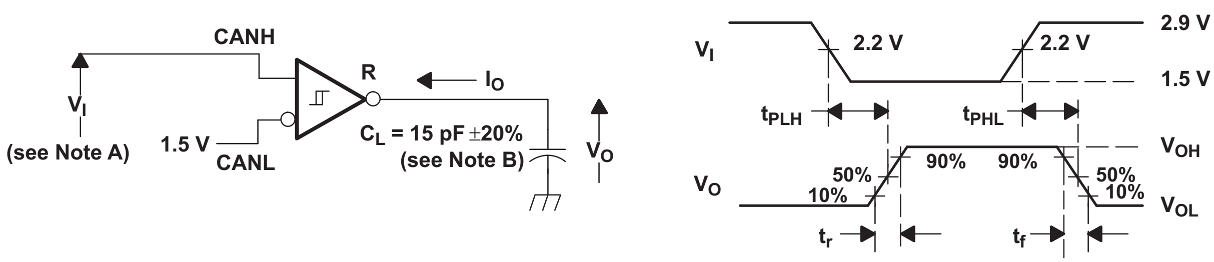


Figure 16. Receiver Voltage and Current Definitions



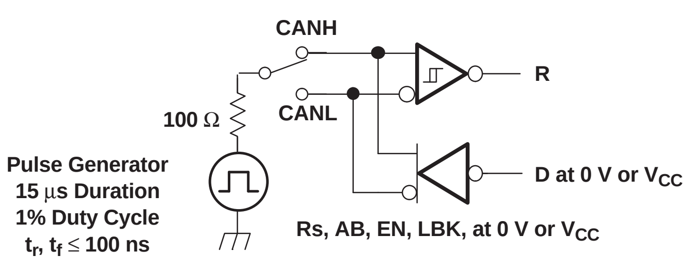
A. The input pulse is supplied by a generator having the following characteristics: Pulse repetition rate (PRR) ≤ 125 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. C_L includes fixture and instrumentation capacitance.

Figure 17. Receiver Test Circuit and Voltage Waveforms

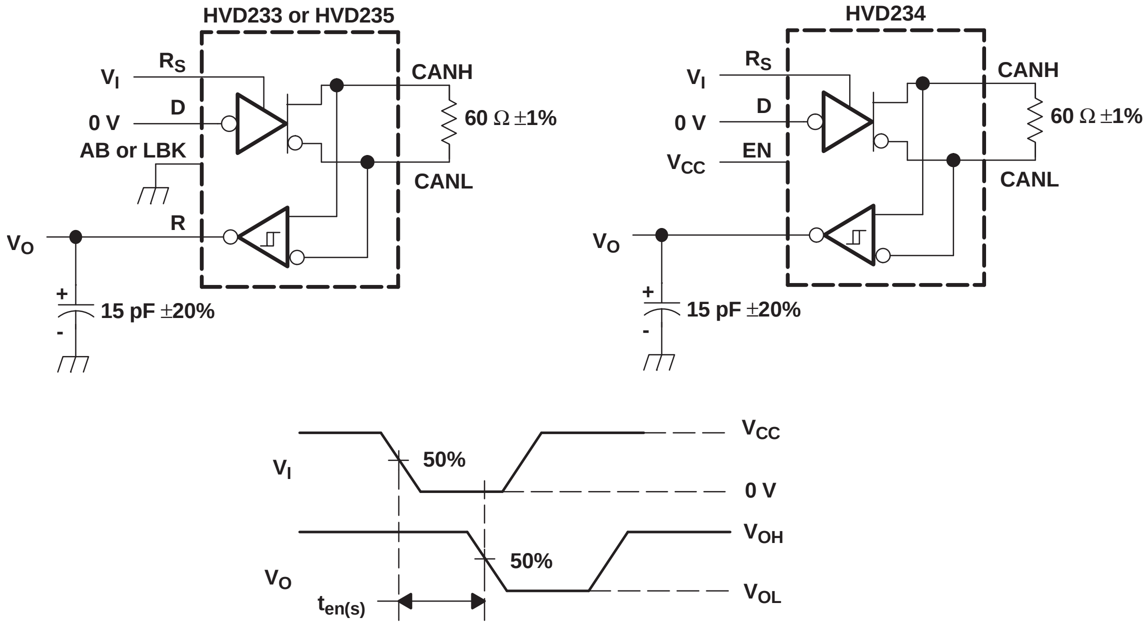
Table 1. Differential Input Voltage Threshold Test

INPUT		OUTPUT		MEASURED
V_{CANH}	V_{CANL}	R		$\lvert V_{ID} \rvert$
–6.1 V	–7 V	L	V_{OL}	900 mV
12 V	11.1 V	L		900 mV
–1 V	–7 V	L		6 V
12 V	6 V	L		6 V
–6.5 V	–7 V	H	V_{OH}	500 mV
12 V	11.5 V	H		500 mV
–7 V	–1 V	H		6 V
6 V	12 V	H		6 V
Open	Open	H		X



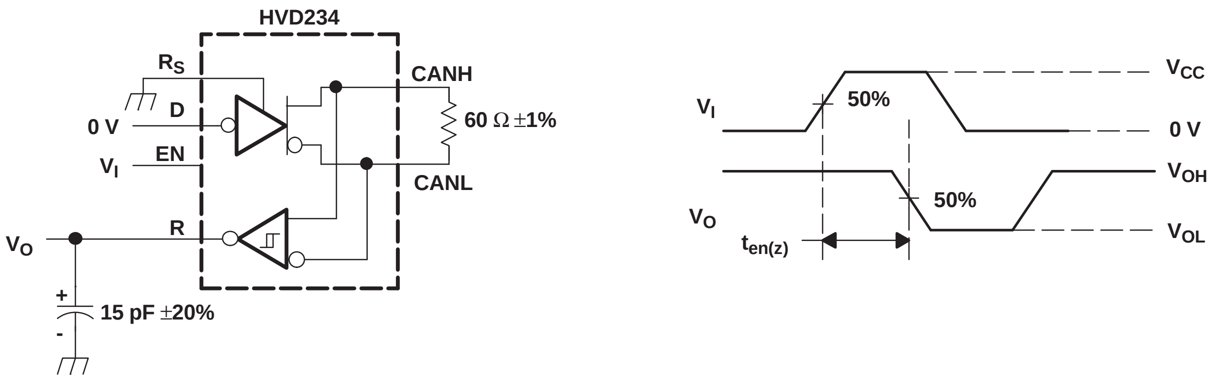
NOTE: This test is conducted to test survivability only. Data stability at the R output is not specified.

Figure 18. Test Circuit, Transient Overvoltage Test



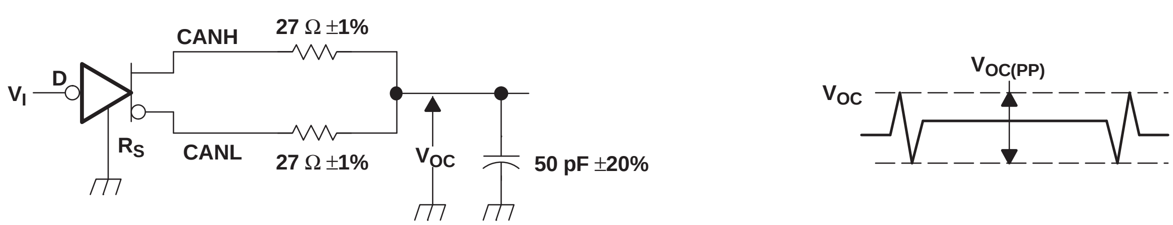
NOTE: All V_I input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 19. $T_{en(s)}$ Test Circuit and Voltage Waveforms



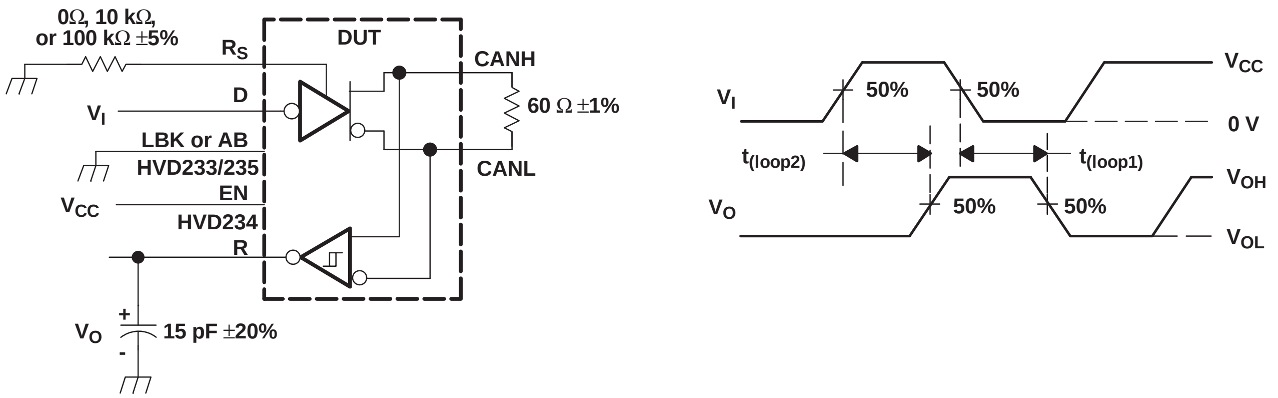
NOTE: All V_I input pulses are supplied by a generator having the following characteristics:
t_r or t_f ≤ 6 ns, pulse repetition rate (PRR) = 50 kHz, 50% duty cycle.

Figure 20. $T_{en(z)}$ Test Circuit and Voltage Waveforms



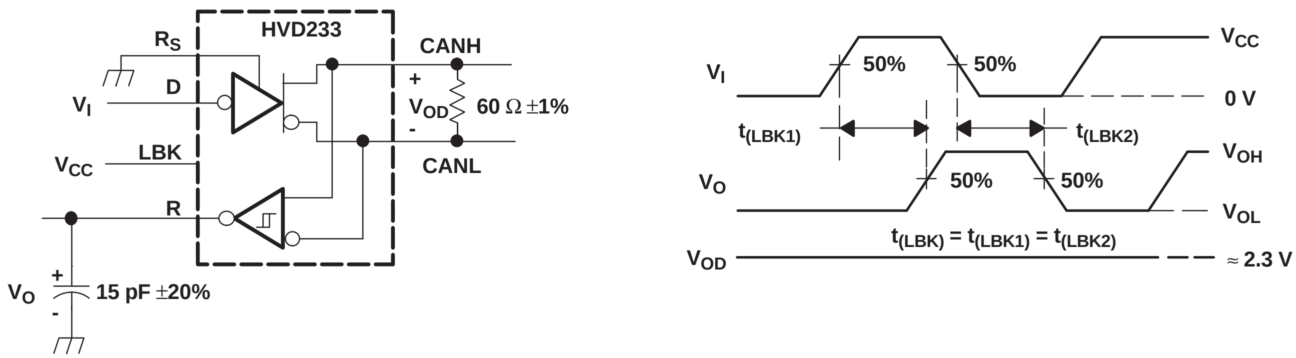
NOTE: All V_I input pulses are supplied by a generator having the following characteristics:
t_r or t_f ≤ 6 ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 21. $V_{OC(pp)}$ Test Circuit and Voltage Waveforms



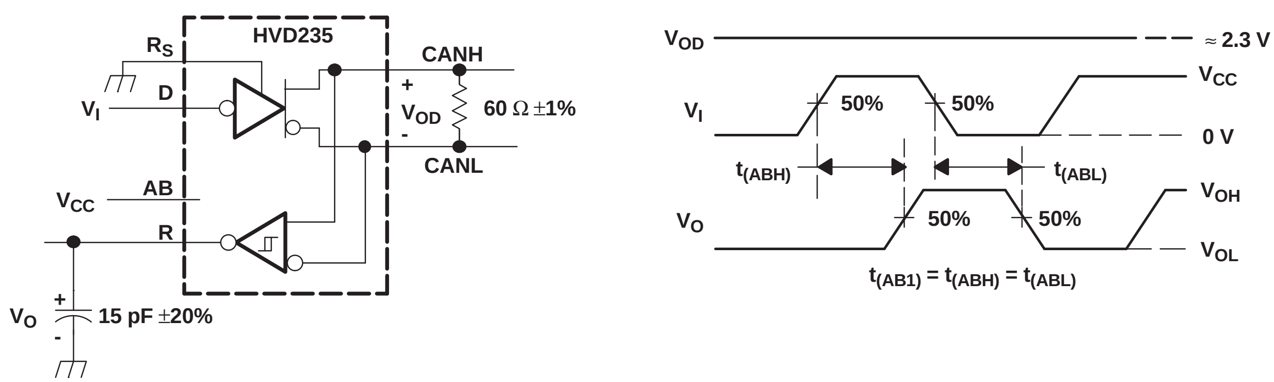
NOTE: All V_I input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 22. $T_{(loop)}$ Test Circuit and Voltage Waveforms



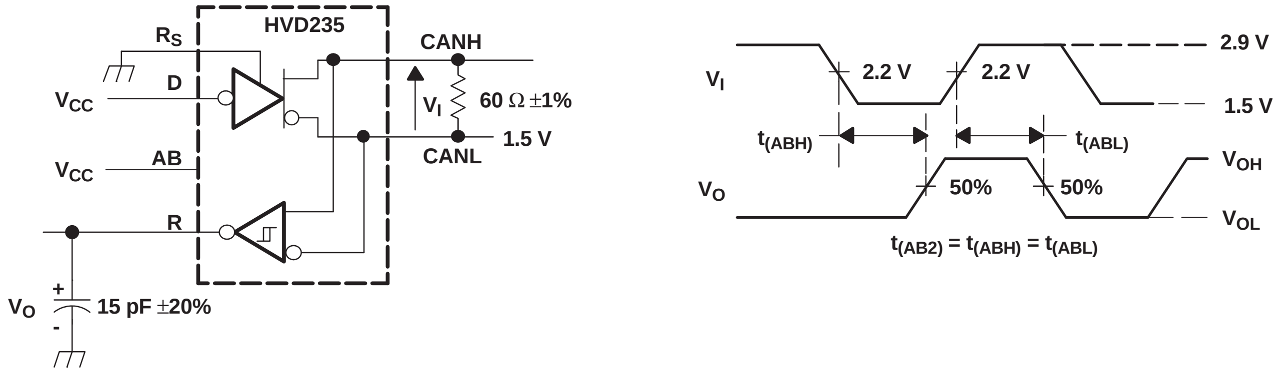
NOTE: All V_I input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 23. $T_{(LBK)}$ Test Circuit and Voltage Waveforms



NOTE: All V_I input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 24. $T_{(AB1)}$ Test Circuit and Voltage Waveforms



NOTE: All V_I input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 6$ ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 25. $T_{(AB2)}$ Test Circuit and Voltage Waveforms

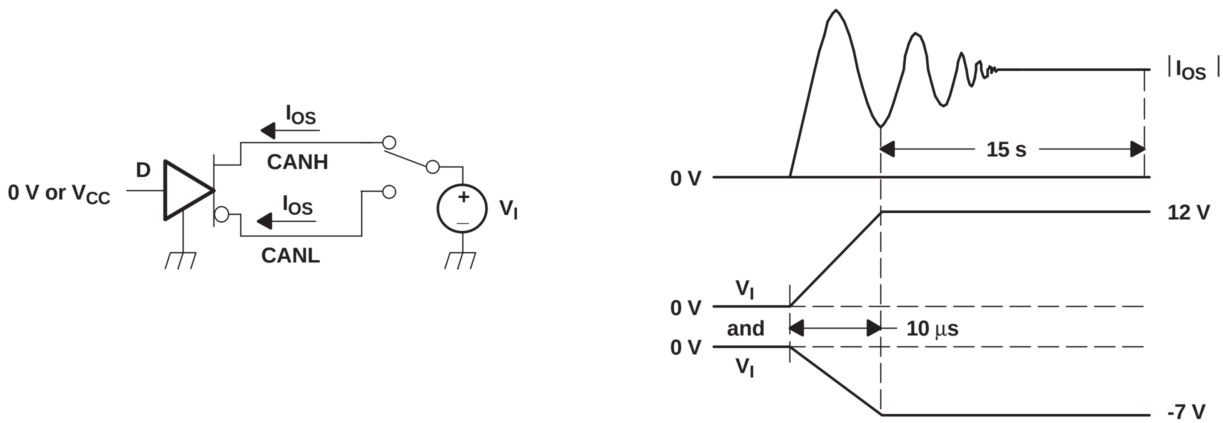
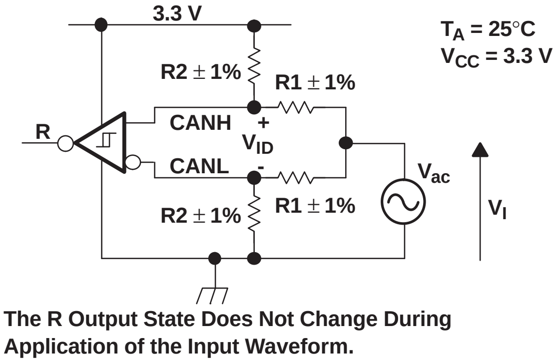
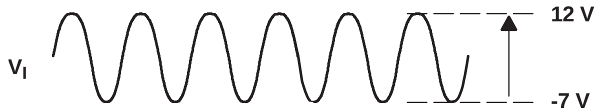


Figure 26. I_{OS} Test Circuit and Waveforms



V_{ID}	R1	R2
500 mV	50 Ω	280 Ω
900 mV	50 Ω	130 Ω



NOTE: All input pulses are supplied by a generator with f ≤ 1.5 MHz.

Figure 27. Common-Mode Voltage Rejection

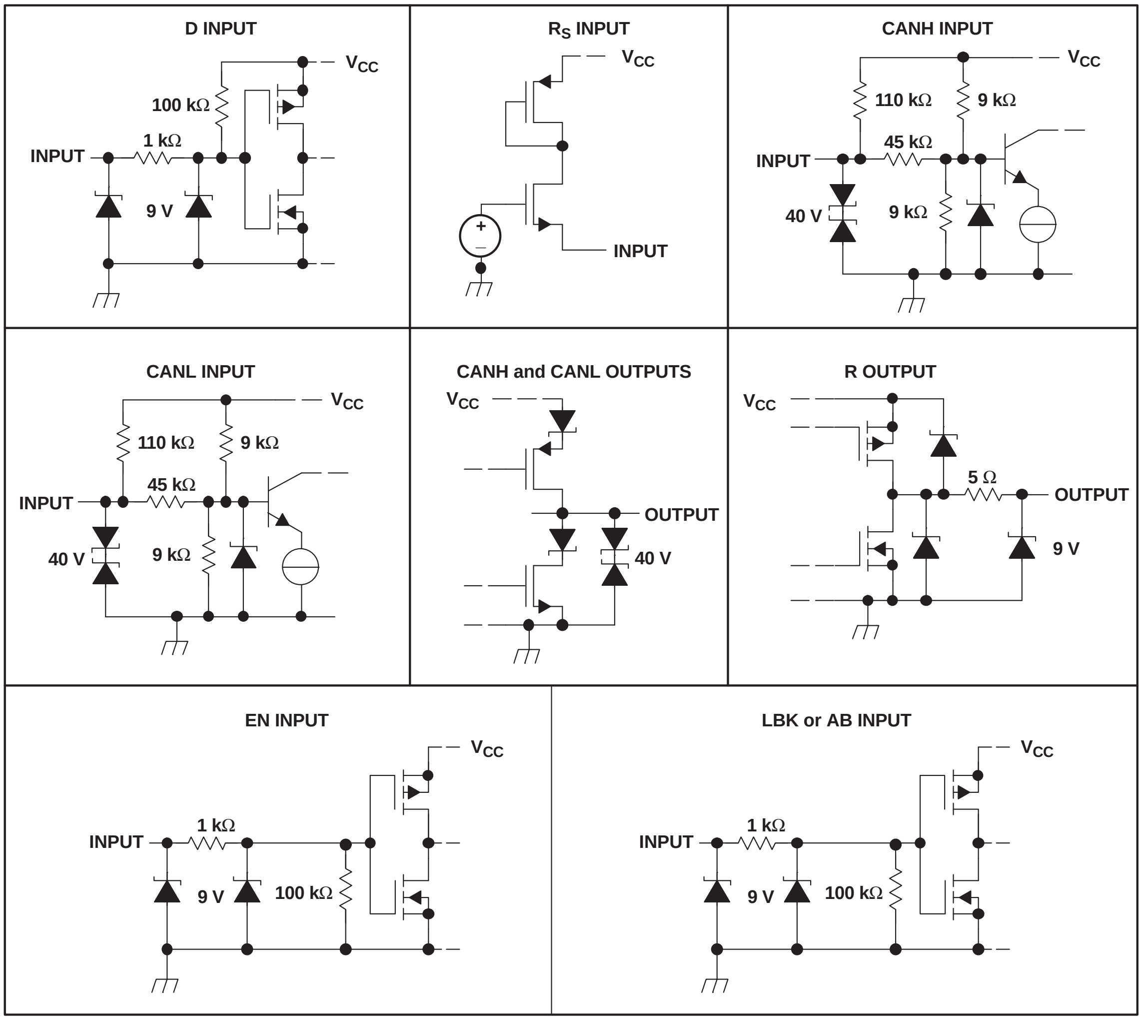


Figure 28. Equivalent Input and Output Schematic Diagrams

10 Detailed Description

10.1 Overview

This family of CAN transceivers is compatible with the ISO11898-2 High-Speed CAN (controller area network) physical layer standard. They are designed to interface between the differential bus lines in CAN and the CAN protocol controller at data rates up to 1 Mpbs.

10.2 Functional Block Diagrams

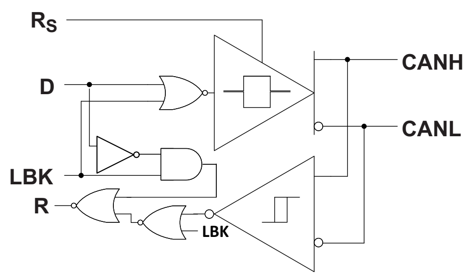


Figure 29. SN65HVD33 Functional Block Diagram

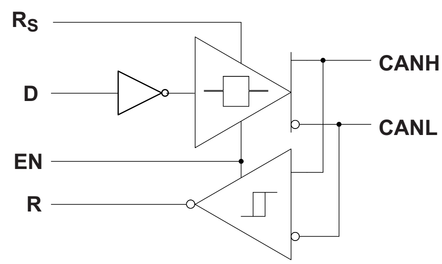


Figure 30. SN65HVD34 Functional Block Diagram

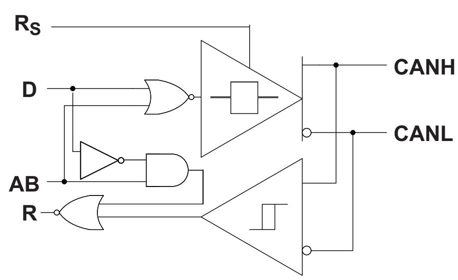


Figure 31. SN65HVD35 Functional Block Diagram

10.3 Feature Description

10.3.1 Diagnostic Loopback (SN65HVD233)

The diagnostic loopback or internal loopback function of the SN65HVD233 is enabled with a high-level input on pin 5, LBK. This mode disables the driver output while keeping the bus pins biased to the recessive state. This mode also redirects the D data input (transmit data) through logic to the received data output pin), thus creating an internal loopback of the transmit to receive data path. This mimics the loopback that occurs normally with a CAN transceiver because the receiver loops back the driven output to the R (receive data) pin. This mode allows the host protocol controller to input and read back a bit sequence or CAN messages to perform diagnostic routines without disturbing the CAN bus. A typical CAN bus application is displayed in Figure 36.

Feature Description (continued)

If the LBK pin is not used it may be tied to ground (GND). However, it is pulled low internally (defaults to a low-level input) and may be left open if not in use.

10.3.2 Autobaud Loopback (SN65HVD235)

The autobaud loopback mode of the SN65HVD235 is enabled by placing a high level input on pin 5, AB. In autobaud mode, the driver output is disabled, thus blocking the D pin to bus path and the bus transmit function of the transceiver. The bus pins remain biased to recessive. The receiver to R pin path or the bus receive function of the device remains operational, allowing bus activity to be monitored. In addition, the autobaud mode adds an internal logic loopback path from the D pin to R pin so the local node may transmit to itself in sync with bus traffic while not disturbing messages on the bus. Thus if the local node's CAN controller generates an error frame, it is not transmitted to the bus, but is detected only by the local CAN controller. This is especially helpful to determine if the local node is set to the same baud rate as the network, and if not adjust it to the network baud rate (autobaud detection).

Autobaud detection is best suited to applications that have a known selection of baud rates. For example, a popular industrial application has optional settings of 125 kbps, 250 kbps, or 500 kbps. Once the SN65HVD235 is placed into autobaud loopback mode the application software could assume the first baud rate of 125 kbps. It then waits for a message to be transmitted by another node on the bus. If the wrong baud rate has been selected, an error message is generated by the local CAN controller because the sample times will not be at the correct time. However, because the bus-transmit function of the device has been disabled, no other nodes receive the error frame generated by this node's local CAN controller.

The application would then make use of the status register indications of the local CAN controller for message received and error warning status to determine if the set baud rate is correct or not. The warning status indicates that the CAN controller error counters have been incremented. A message received status indicates that a good message has been received. If an error is generated, the application would then set the CAN controller with the next possibly valid baud rate, and wait to receive another message. This pattern is repeated until an error free message has been received, thus the correct baud rate has been selected. At this point the application would place the SN65HVD235 in a normal transmitting mode by setting pin 5 to a low-level, thus enabling bus-transmit and bus-receive functions to normal operating states for the transceiver.

If the AB pin is not used it may be tied to ground (GND). However, it is pulled low internally (defaults to a low-level input) and may be left open if not in use.

10.3.3 Slope Control

The rise and fall slope of the SN65HVD233, SN65HVD234, and SN65HVD235 driver output can be adjusted by connecting a resistor from the Rs (pin 8) to ground (GND), or to a low-level input voltage as shown in Figure 32.

The slope of the driver output signal is proportional to the pin's output current. This slope control is implemented with an external resistor value of 10 kΩ to achieve a ~15 V/μs slew rate, and up to 100 kΩ to achieve a ~2.0 V/μs slew rate . A typical slew rate verses pulldown resistance graph is shown in Figure 33. Typical driver output waveforms with slope control are displayed in Figure 39.

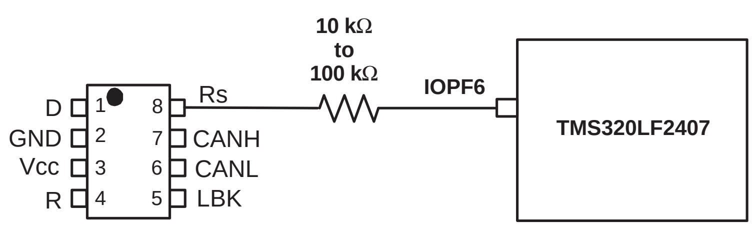


Figure 32. Slope Control/Standby Connection to a DSP

Feature Description (continued)

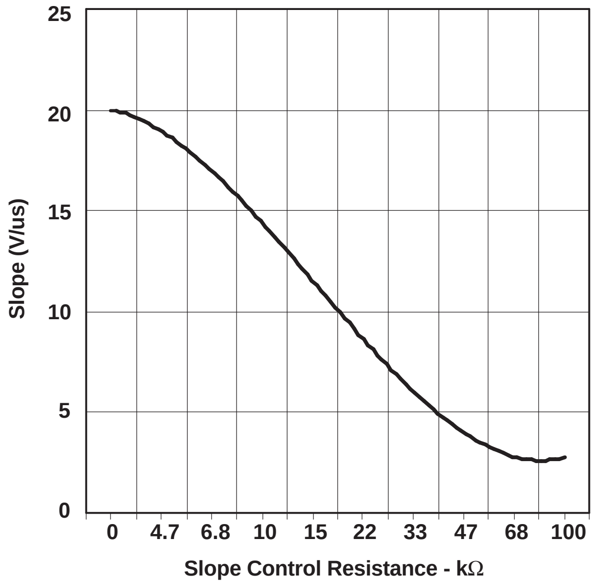


Figure 33. HVD233 Driver Output Signal Slope vs Slope Control Resistance Value

10.3.4 Standby

If a high-level input (> 0.75 V_{CC}) is applied to R_S (pin 8), the circuit enters a low-current, *listen only* standby mode during which the driver is switched off and the receiver remains active. If using this mode to save system power while waiting for bus traffic, the local controller can monitor the R output pin for a falling edge which indicates that a dominant signal was driven onto the CAN bus. The local controller can then drive the R_S pin low to return to slope control mode or high-speed mode.

10.3.5 Thermal Shutdown

If the junction temperature of the device exceeds the thermal shut down threshold the device turns off the CAN driver circuits thus blocking the D pin to bus transmission path. The shutdown condition is cleared when the junction temperature drops below the thermal shutdown temperature of the device. The CAN bus pins are high impedance biased to recessive level during a thermal shutdown, and the receiver to R pin path remains operational.

10.4 Device Functional Modes

Table 2. Driver (SN65HVD233 or SN65HVD235)

INPUTS			OUTPUTS		
D	LBK/AB	R_S	CANH	CANL	BUS STATE
X	X	> 0.75 V_{CC}	Z	Z	Recessive
L	L or open	≤ 0.33 V_{CC}	H	L	Dominant
H or open	X		Z	Z	Recessive
X	H	≤ 0.33 V_{CC}	Z	Z	Recessive

Table 3. Receiver (SN65HVD233)

INPUTS				OUTPUT
BUS STATE	**$V_{ID} = V_{(CANH)} – V_{(CANL)}$**	**LBK**	**D**	**R**
Dominant	$V_{ID} \geq 0.9$ V	L or open	X	L
Recessive	$V_{ID} \leq 0.5$ V or open	L or open	H or open	H
?	0.5 V < V_{ID} <0.9 V	L or open	H or open	?
X	X	H	L	L
X	X		H	H

Table 4. Receiver (SN65HVD235)[(1)]

INPUTS				OUTPUT
BUS STATE	**$V_{ID} = V_{(CANH)} – V_{(CANL)}$**	**AB**	**D**	**R**
Dominant	$V_{ID} \geq 0.9$ V	L or open	X	L
Recessive	$V_{ID} \leq 0.5$ V or open	L or open	H or open	H
?	0.5 V < V_{ID} <0.9 V	L or open	H or open	?
Dominant	$V_{ID} \geq 0.9$ V	H	X	L
Recessive	$V_{ID} \leq 0.5$ V or open	H	H	H
Recessive	$V_{ID} \leq 0.5$ V or open	H	L	L
?	0.5 V < V_{ID} <0.9 V	H	L	L

(1) H = high level; L = low level; Z = high impedance; X = irrelevant; ? = indeterminate

Table 5. Driver (SN65HVD234)

INPUTS			OUTPUTS		
D	**EN**	**R_S**	**CANH**	**CANL**	**BUS STATE**
L	H	≤ 0.33 V_{CC}	H	L	Dominant
H	X	≤ 0.33 V_{CC}	Z	Z	Recessive
Open	X	X	Z	Z	Recessive
X	X	> 0.75 V_{CC}	Z	Z	Recessive
X	L or open	X	Z	Z	Recessive

Table 6. Receiver (SN65HVD234)[(1)]

INPUTS			OUTPUT
BUS STATE	**$V_{ID} = V_{(CANH)} – V_{(CANL)}$**	**EN**	**R**
Dominant	$V_{ID} \geq 0.9$ V	H	L
Recessive	$V_{ID} \leq 0.5$ V or open	H	H
?	0.5 V < V_{ID} <0.9 V	H	?
X	X	L or open	H

(1) H = high level; L = low level; Z = high impedance; X = irrelevant; ? = indeterminate

11 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

11.1 Application Information

The CAN bus has two states during powered operation of the device; *dominant* and *recessive*. A dominant bus state is when the bus is driven differentially, corresponding to a logic low on the D and R pin. A recessive bus state is when the bus is biased to V_{CC} / 2 via the high-resistance internal resistors R_{IN} and R_{ID} of the receiver, corresponding to a logic high on the D and R pins. See *Figure 34* and *Figure 35*.

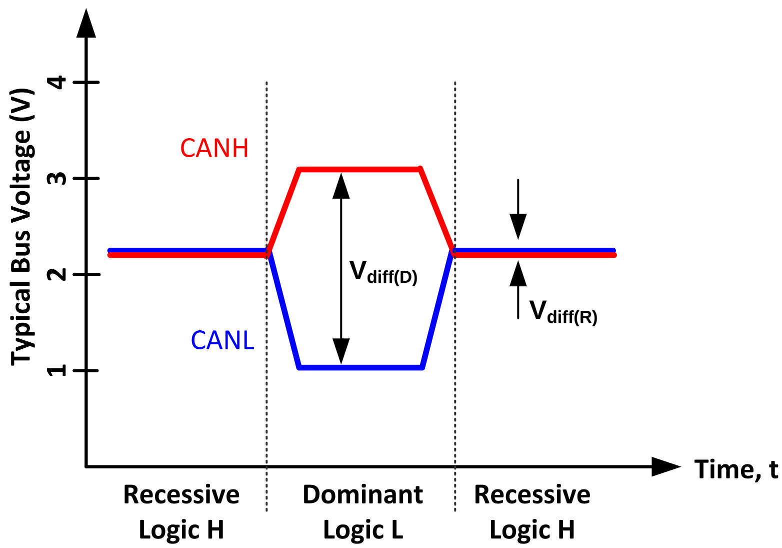


Figure 34. Bus States (Physical Bit Representation)

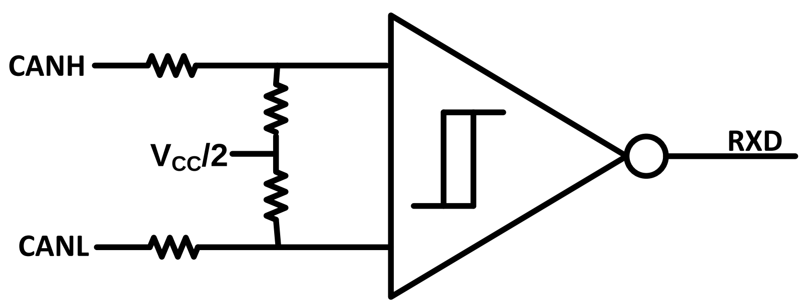


Figure 35. Simplified Recessive Common Mode Bias and Receiver

These CAN transceivers are typically used in applications with a host microprocessor or FPGA that includes the link layer portion of the CAN protocol. The different nodes on the network are typically connected through the use of a 120-Ω characteristic impedance twisted-pair cable with termination on both ends of the bus.

11.2 Typical Application

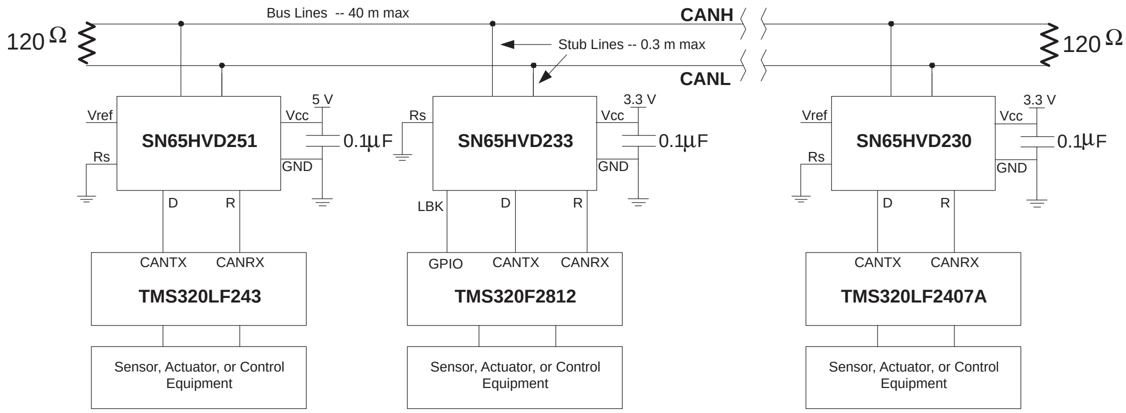


Figure 36. Typical HVD233 Application

11.2.1 Design Requirements

11.2.1.1 Bus Loading, Length and Number of Nodes

The ISO 11898 Standard specifies up to a data rate of 1 Mbps, maximum CAN bus cable length of 40 m, maximum drop line (stub) length of 0.3 m and a maximum of 30 nodes. However, with careful network design, the system may have longer cables, longer stub lengths, and many more nodes to a bus. Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO 11898 standard. They have made system level trade-offs for data rate, cable length, and parasitic loading of the bus. Examples of some of these specifications are ARINC825, CANopen, CAN Kingdom, DeviceNet and NMEA200.

A high number of nodes requires a transceiver with high input impedance and wide common mode range such as the SN65HVD23x CAN family. ISO 11898-2 specifies the driver differential output with a 60-Ω load (two 120-Ω termination resistors in parallel) and the differential output must be greater than 1.5 V. The SN65HVD23x devices are specified to meet the 1.5-V requirement with a 60-Ω load, and additionally specified with a differential output voltage minimum of 1.2 V across a common mode range of –2 V to 7 V through a 330-Ω coupling network. This network represents the bus loading of 120 SN65HVD23x transceivers based on their minimum differential input resistance of 40 kΩ. Therefore, the SN65HVD23x supports up to 120 transceivers on a single bus segment with margin to the 1.2-V minimum differential input voltage requirement at each node.

For CAN network design, margin must be given for signal loss across the system and cabling, parasitic loadings, network imbalances, ground offsets and signal integrity thus a practical maximum number of nodes may be lower. Bus length may also be extended beyond the original ISO 11898 standard of 40 m by careful system design and data rate tradeoffs. For example, CANopen network design guidelines allow the network to be up to 1 km with changes in the termination resistance, cabling, less than 64 nodes and significantly lowered data rate.

This flexibility in CAN network design is one of the key strengths of the various extensions and additional standards that have been built on the original ISO 11898 CAN standard.

11.2.1.2 CAN Termination

The ISO 11898 standard specifies the interconnect to be a twisted-pair cable (shielded or unshielded) with 120-Ω characteristic impedance (Z_O). Resistors equal to the characteristic impedance of the line should be used to terminate both ends of the cable to prevent signal reflections. Unterminated drop lines (stubs) connecting nodes to the bus should be kept as short as possible to minimize signal reflections. The termination may be on the cable or in a node, but if nodes may be removed from the bus the termination must be carefully placed so that it is not removed from the bus.

Typical Application (continued)

11.2.2 Detailed Design Procedure

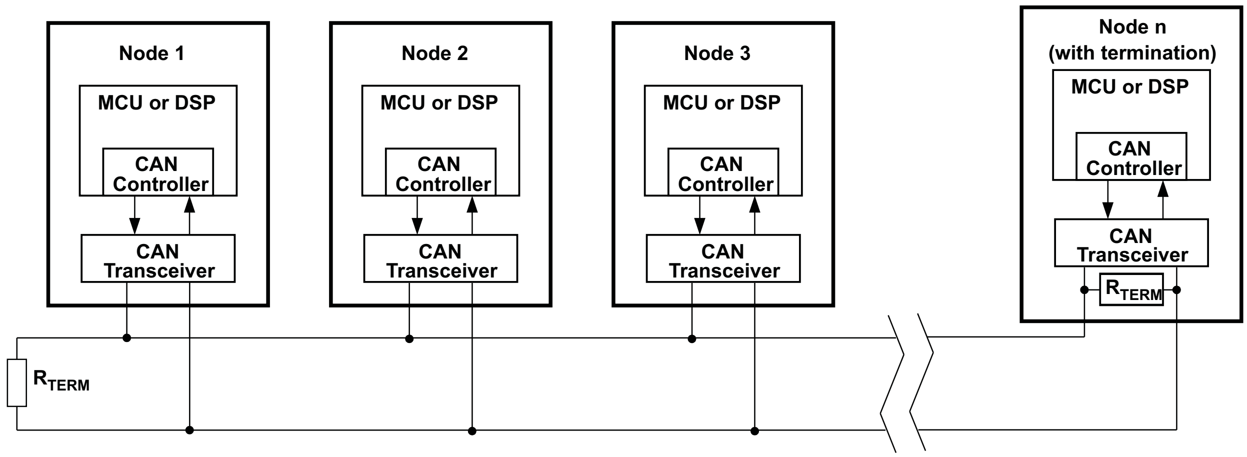


Figure 37. Typical CAN Bus

Termination is typically a 120-Ω resistor at each end of the bus. If filtering and stabilization of the common mode voltage of the bus is desired, then split termination may be used (see Figure 38). Split termination uses two 60-Ω resistors with a capacitor in the middle of these resistors to ground. Split termination improves the electromagnetic emissions behavior of the network by eliminating fluctuations in the bus common mode voltages at the start and end of message transmissions.

Care should be taken in the power ratings of the termination resistors used. Typically the worst case condition would be if the system power supply was shorted across the termination resistance to ground. In most cases the current flow through the resistor in this condition would be much higher than the transceiver's current limit.

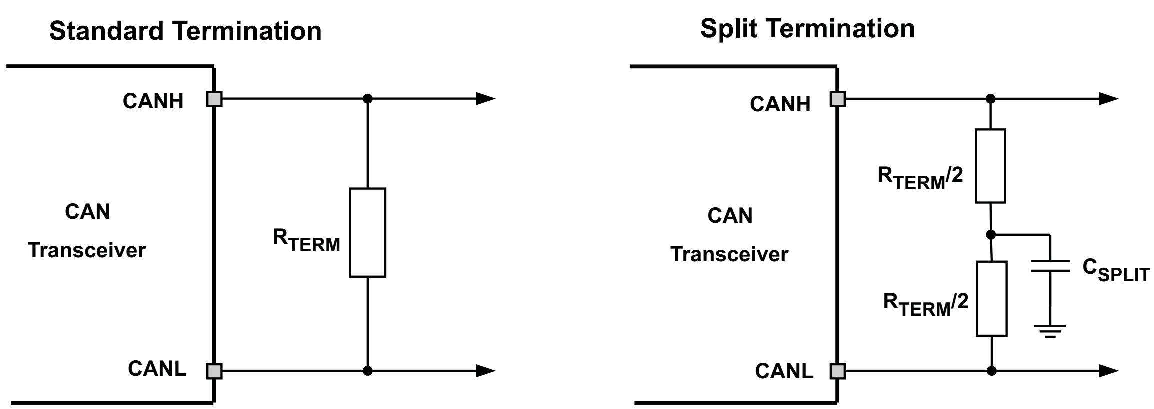


Figure 38. CAN Bus Termination Concepts

11.2.3 Application Curve

Figure 39 shows 3 typical output waveforms for the SN65HVD233 device with three different connections made to the R_S pin. The top waveform show the typical differential signal when transitioning from a recessive level to a dominant level on the CAN bus with R_S tied to GND through a 0-Ω resistor. The second waveform shows the same signal for the condition with a 10-kΩ resistor tied from R_S to ground. The bottom waveform shows the typical differential signal for the case where a 100-kΩ resistor is tied from the R_S pin to ground.

Typical Application (continued)

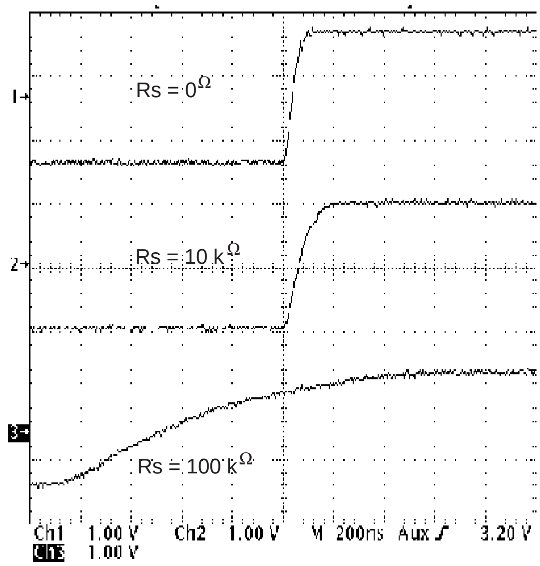


Figure 39. Typical SN65HVD233 Output Waveforms With Different Slope Control Resistor Values

11.3 System Example

11.3.1 ISO 11898 Compliance of SN65HVD23x Family of 3.3-V CAN Transceivers

11.3.1.1 Introduction

Many users value the low power consumption of operating their CAN transceivers from a 3.3-V supply. However, some are concerned about the interoperability with 5 V supplied transceivers on the same bus. This report analyzes this situation to address those concerns.

11.3.1.2 Differential Signal

CAN is a differential bus where complementary signals are sent over two wires and the voltage difference between the two wires defines the logical state of the bus. The differential CAN receiver monitors this voltage difference and outputs the bus state with a single ended logic level output signal.

System Example (continued)

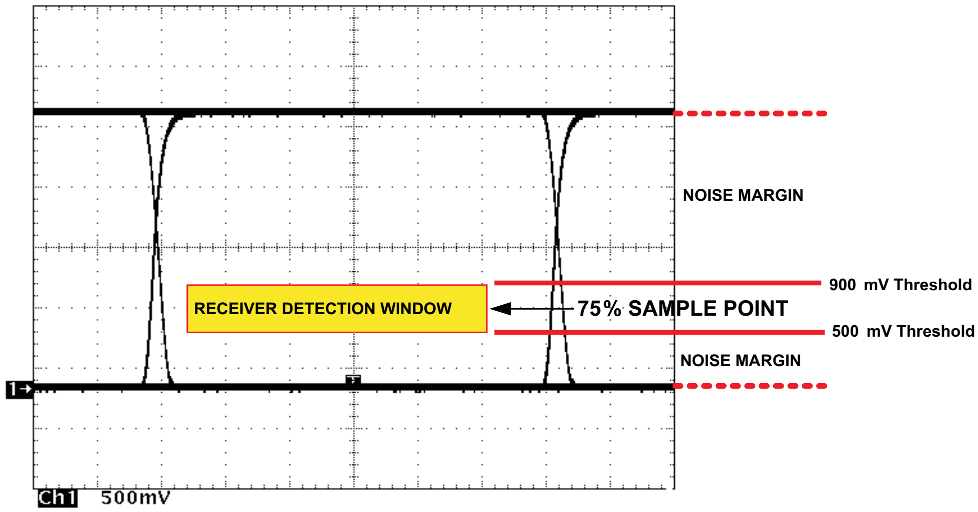


Figure 40. Typical SN65HVD230 Differential Output Voltage Waveform

The CAN driver creates the differential voltage between CANH and CANL in the dominant state. The dominant differential output of the SN65HVD23x is greater than 1.5 V and less than 3 V across a 60 ohm load as defined by the ISO 11898 standard. These are the same limiting values for 5 V supplied CAN transceivers. The bus termination resistors drive the recessive bus state and not the CAN driver.

A CAN receiver is required to output a recessive state when less than 500 mV of differential voltage exists on the bus, and a dominant state when more than 900 mV of differential voltage exists on the bus. The CAN receiver must do this with common-mode input voltages from –2 V to 7 V. The SN65HVD23x family receivers meet these same input specifications as 5 V supplied receivers.

11.3.1.3 Common-Mode Signal

A common-mode signal is an average voltage of the two signal wires that the differential receiver rejects. The common-mode signal comes from the CAN driver, ground noise, and coupled bus noise. Since the bias voltage of the recessive state of the device is dependent on V_{CC}, any noise present or variation of V_{CC} will have an effect on this bias voltage seen by the bus. The SN65HVD23x family has the recessive bias voltage set higher than $0.5*V_{CC}$ to comply with the ISO 11898-2 CAN standard. The caveat to this is that the common mode voltage will drop by a couple hundred millivolts when driving a dominant bit on the bus. This means that there is a common mode shift between the dominant bit and recessive bit states of the device. While this is not ideal, this small variation in the driver common-mode output is rejected by differential receivers and does not effect data, signal noise margins or error rates.

11.3.1.4 Interoperability of 3.3-V CAN in 5-V CAN Systems

The 3.3-V supplied SN65HVD23x family of CAN transceivers are fully compatible with 5-V CAN transceivers. The differential output voltage is the same, the recessive common mode output bias is the same, and the receivers have the same input specifications. The only slight difference is in the dominant common mode output voltage which is a couple hundred millivolts lower for 3.3-V CAN transceiver than 5-V supplied transceiver.

To help ensure the widest interoperability possible, the SN65HVD23x family has successfully passed the internationally recognized GIFT/ICT conformance and interoperability testing for CAN transceivers. Electrical interoperability does not always assure interchangeability however. Most implementers of CAN buses recognize that ISO 11898 does not sufficiently specify the electrical layer and that strict standard compliance alone does not ensure full interchangeability. This comes only with thorough equipment testing.

12 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, each supply should be decoupled with a 100-nF ceramic capacitor located as close to the V_{CC} supply pins as possible. The TPS76333 is a linear voltage regulator suitable for the 3.3 V supply.

13 Layout

13.1 Layout Guidelines

In order for the PCB design to be successful, start with design of the protection and filtering circuitry. Because ESD and EFT transients have a wide frequency bandwidth from approximately 3 MHz to 3 GHz, high frequency layout techniques must be applied during PCB design. On chip IEC ESD protection is good for laboratory and portable equipment but is usually not sufficient for EFT and surge transients occurring in industrial environments. Therefore robust and reliable bus node design requires the use of external transient protection devices at the bus connectors. Placement at the connector also prevents these harsh transient events from propagating further into the PCB and system.

Use V_{CC} and ground planes to provide low inductance.

NOTE

High frequency current follows the path of least inductance and not the path of least resistance.

Design the bus protection components in the direction of the signal path. Do not force the transient current to divert from the signal path to reach the protection device.

An example placement of the Transient Voltage Suppression (TVS) device indicated as D1 (either bi-directional diode or varistor solution) and bus filter capacitors C8 and C9 are shown in Figure 41.

The bus transient protection and filtering components should be placed as close to the bus connector, J1, as possible. This prevents transients, ESD and noise from penetrating onto the board and disturbing other devices.

Bus termination: Figure 41 shows split termination. This is where the termination is split into two resistors, R5 and R6, with the center or split tap of the termination connected to ground via capacitor C7. Split termination provides common mode filtering for the bus. When termination is placed on the board instead of directly on the bus, care must be taken to ensure the terminating node is not removed from the bus as this will cause signal integrity issues of the bus is not properly terminated on both ends. See the application section for information on power ratings needed for the termination resistor(s).

Bypass and bulk capacitors should be placed as close as possible to the supply pins of transceiver, examples C2, C3 (V_{CC}).

Use at least two vias for V_{CC} and ground connections of bypass capacitors and protection devices to minimize trace and via inductance.

To limit current of digital lines, serial resistors may be used. Examples are R1, R2, R3 and R4.

To filter noise on the digital IO lines, a capacitor may be used close to the input side of the IO as shown by C1 and C4.

Since the internal pullup and pulldown biasing of the device is weak for floating pins, an external 1-kΩ to 10-kΩ pullup or pulldown resistor should be used to bias the state of the pin more strongly against noise during transient events.

Pin 1: If an open drain host processor is used to drive the D pin of the device an external pull-up resistor between 1 kΩ and 10 kΩ and V_{CC} should be used to drive the recessive input state of the device.

Pin 8: is shown assuming the mode pin, RS, will be used. If the device will only be used in normal mode or slope control mode, R3 is not needed and the pads of C4 could be used for the pulldown resistor to GND.

13.2 Layout Example

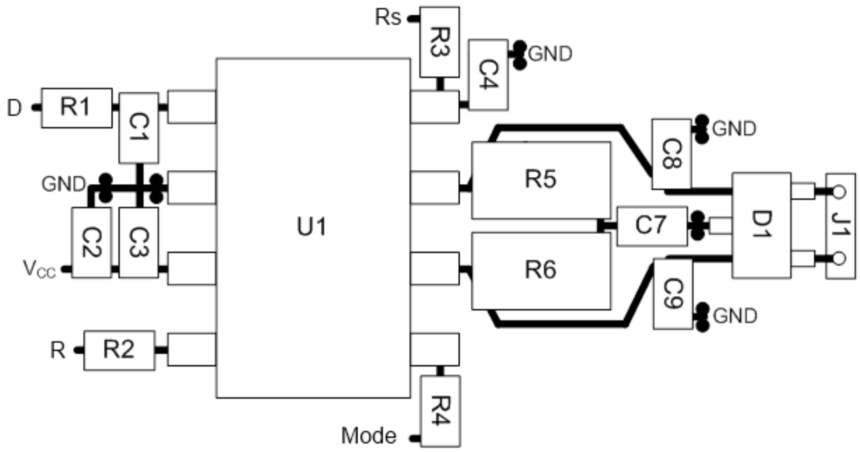


Figure 41. Layout Example Schematic

14 Device and Documentation Support

14.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 7. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN65HVD233	Click here	Click here	Click here	Click here	Click here
SN65HVD234	Click here	Click here	Click here	Click here	Click here
SN65HVD235	Click here	Click here	Click here	Click here	Click here

14.2 Trademarks

All trademarks are the property of their respective owners.

14.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

14.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

15 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN65HVD233D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VP233	Samples
SN65HVD233DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VP233	Samples
SN65HVD233DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VP233	Samples
SN65HVD233DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VP233	Samples
SN65HVD234D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VP234	Samples
SN65HVD234DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VP234	Samples
SN65HVD234DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VP234	Samples
SN65HVD234DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VP234	Samples
SN65HVD235D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VP235	Samples
SN65HVD235DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VP235	Samples
SN65HVD235DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VP235	Samples
SN65HVD235DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VP235	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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OTHER QUALIFIED VERSIONS OF SN65HVD233 :

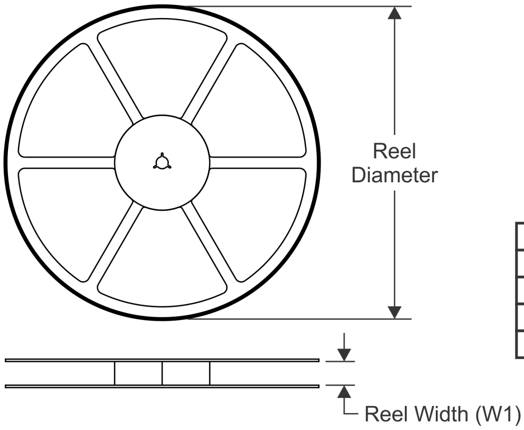
- Enhanced Product: SN65HVD233-EP

NOTE: Qualified Version Definitions:

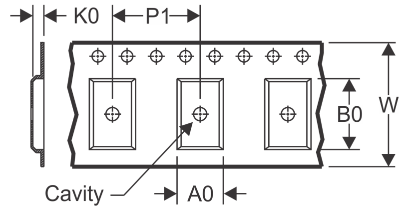
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

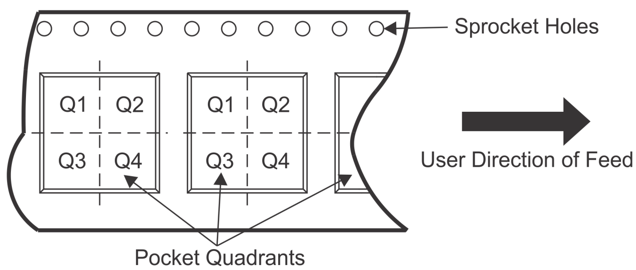


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

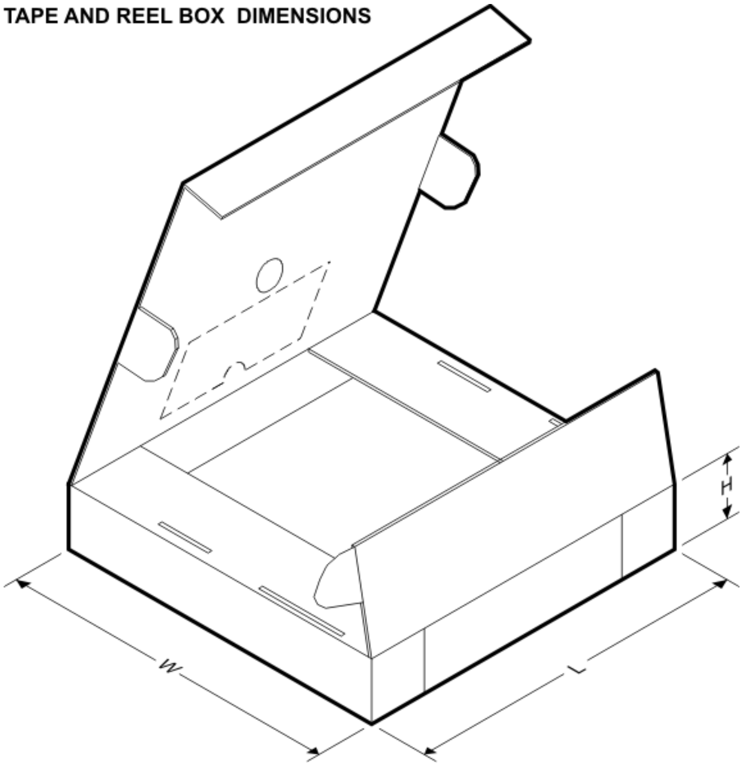
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD233DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD234DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD235DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

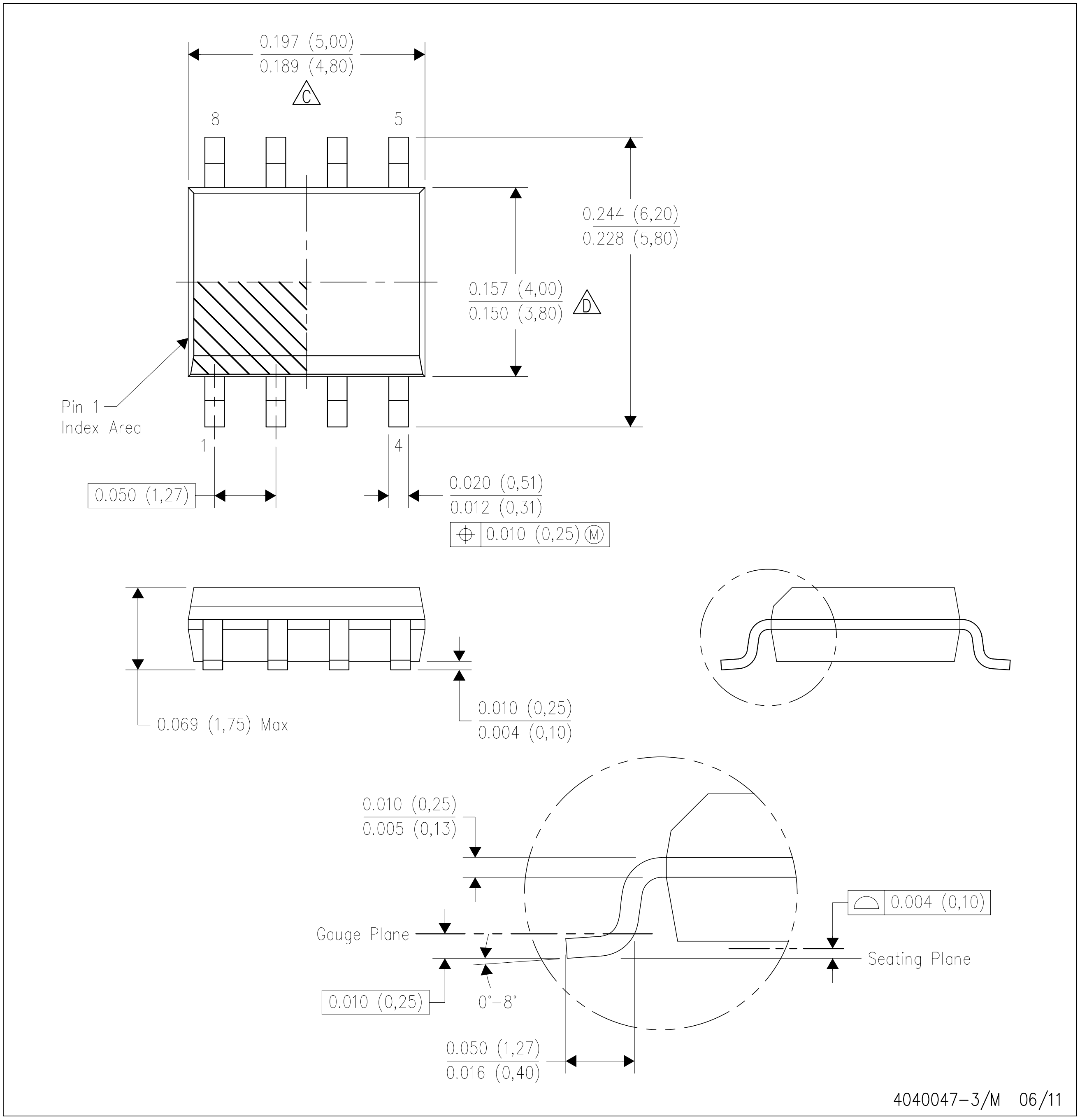
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD233DR	SOIC	D	8	2500	340.5	338.1	20.6
SN65HVD234DR	SOIC	D	8	2500	340.5	338.1	20.6
SN65HVD235DR	SOIC	D	8	2500	340.5	338.1	20.6

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AA.

IMPORTANT NOTICE

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