

PS12012-A

FLAT-BASE TYPE
INSULATED TYPE

PS12012-A



INTEGRATED FUNCTIONS AND FEATURES

- 3-Phase IGBT inverter bridge configured by the latest 3rd. generation IGBT and diode technologies.
- Circuit for dynamic braking of motor regenerative energy.
- Inverter output current capability I_o (Note 1) :

| Type Name | 100% load | 150% over load |
|-----------|------------|------------------|
| PS12012-A | 1.2A (rms) | 1.8A (rms), 1min |

(Note 1) : The inverter output current is assumed to be sinusoidal and the peak current value of each of the above loading cases is defined as : $I_{op} = I_o \times \sqrt{2}$

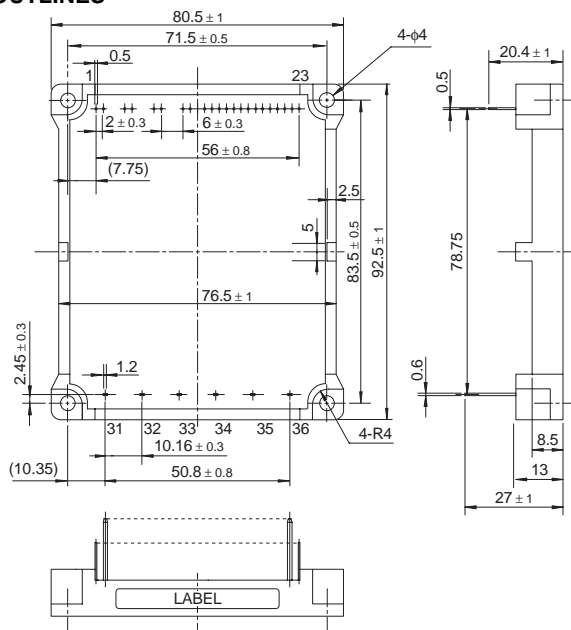
INTEGRATED DRIVE, PROTECTION AND SYSTEM CONTROL FUNCTIONS:

- For P-Side IGBTs : Drive circuit, High-speed photo-couplers, Short circuit protection (SC), Bootstrap circuit supply scheme (Single drive power supply) and Under-voltage protection (UV).
- For N-Side IGBTs : Drive circuit, Short-circuit protection (SC), Control supply Under voltage and Over voltage protection (OV/UV), System Over temperature protection (OT), Fault output signaling circuit (Fo), and Current-Limit warning signal output (CL).
- For Brake circuit IGBT : Drive circuit.
- Warning and Fault signaling :
 - FO1 : Short circuit protection for lower-leg IGBTs and Input interlocking against spurious arm shoot-through.
 - FO2 : N-side control supply abnormality locking (OV/UV)
 - FO3 : System over-temperature protection (OT).
 - CL : Warning for inverter current overload condition
- For system feedback control : Analogue signal feedback reproducing actual inverter output phase current (3ϕ).
- Input Interface : 5V CMOS/TTL compatible, Schmitt trigger input, and Arm-Shoot-Through interlock protection.

APPLICATION

Acoustic noise-less 0.2kW/AC400V Class 3 Phase inverter and other motor control applications.

PACKAGE OUTLINES



Terminals Assignment:

| | | | |
|----|------|----|---|
| 1 | CBU+ | 31 | P |
| 2 | CBU- | 32 | B |
| 3 | CBV+ | 33 | N |
| 4 | CBV- | 34 | U |
| 5 | CBW+ | 35 | V |
| 6 | CBW- | 36 | W |
| 7 | GND | | |
| 8 | VDL | | |
| 9 | VDH | | |
| 10 | CL | | |
| 11 | FO1 | | |
| 12 | FO2 | | |
| 13 | FO3 | | |
| 14 | CU | | |
| 15 | CV | | |
| 16 | CW | | |
| 17 | UP | | |
| 18 | VP | | |
| 19 | WP | | |
| 20 | UN | | |
| 21 | VN | | |
| 22 | WN | | |
| 23 | Br | | |

(Fig. 1)

PS12012-A

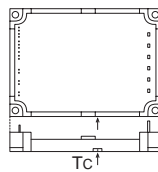
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TOTAL SYSTEM

| Symbol | Item | Condition | Ratings | Unit |
|------------------|-----------------------------------|---|-------------|------|
| T _j | Junction temperature | (Note 2) | -20 ~ +125 | °C |
| T _{stg} | Storage temperature | — | -40 ~ +125 | °C |
| T _c | Module case operating temperature | (Fig. 3) | -20 ~ +100 | °C |
| Viso | Isolation voltage | 60 Hz sinusoidal AC for 1 minute, between all terminals and base plate. | 2500 | Vrms |
| — | Mounting torque | Mounting screw: M3.5 | 0.78 ~ 1.27 | N·m |

Note 2) : The item defines the maximum junction temperature for the power elements (IGBT/Diode) of the ASIPM to ensure safe operation. However, these power elements can endure instantaneous junction temperature as high as 150°C. To make use of this additional temperature allowance, a detailed study of the exact application conditions is required and, accordingly, necessary information is to be provided before use.

CASE TEMPERATURE MEASUREMENT POINT (3mm from the base surface)



(Fig. 3)

THERMAL RESISTANCE

| Symbol | Item | Condition | Ratings | | | Unit |
|-----------------------|-------------------------------------|--|---------|------|-------|------|
| | | | Min. | Typ. | Max. | |
| R _{th(jc)Q} | Junction to case Thermal Resistance | Inverter IGBT (1/6) | — | — | 3.0 | °C/W |
| R _{th(jc)F} | | Inverter FWDi (1/6) | — | — | 7.3 | °C/W |
| R _{th(jc)QB} | | Brake IGBT | — | — | 3.0 | °C/W |
| R _{th(jc)FB} | | Brake FWDi | — | — | 7.3 | °C/W |
| R _{th(c-f)} | Contact Thermal Resistance | Case to fin, thermal grease applied (1 Module) | — | — | 0.040 | °C/W |

ELECTRICAL CHARACTERISTICS (T_j = 25°C, V_{DH} = 15V, V_{DB} = 15V, V_{DL} = 5V unless otherwise noted)

| Symbol | Item | Condition | Ratings | | | Unit |
|------------------------|--|--|---|------|------|------|
| | | | Min. | Typ. | Max. | |
| V _{CE(sat)} | Collector-emitter saturation voltage | V _{DL} = 5V, V _{DH} = V _{DB} = 15V Input = ON, T _j = 25°C, I _c = 5A | — | — | 3.6 | V |
| V _{EC} | FWDi forward voltage | T _j = 25°C, I _c = -5A, Input = OFF | — | — | 3.5 | V |
| V _{CE(sat)Br} | Brake IGBT Collector-emitter saturation voltage | V _{DL} = 5V, V _{DH} = 15V Input = ON, T _j = 25°C, I _c = 5A | — | — | 3.6 | V |
| V _{FBr} | Brake diode forward voltage | T _j = 25°C, I _F = 5A, Input = OFF | — | — | 3.5 | V |
| t _{on} | Switching times | 1/2 Bridge inductive, Input = ON V _{CC} = 600V, I _c = 5A, T _j = 125°C V _{DL} = 5V, V _{DH} = 15V, V _{DB} = 15V Note : t _{on} , t _{off} include delay time of the internal control circuit. | 0.3 | 1.2 | 2.0 | μs |
| t _{c(on)} | | | — | 0.5 | 1.4 | μs |
| t _{off} | | | — | 2.2 | 4.0 | μs |
| t _{c(off)} | | | — | 0.9 | 1.6 | μs |
| t _{rr} | FWD reverse recovery time | | — | 0.2 | — | μs |
| | Short circuit endurance (Output, Arm, and Load, Short Circuit Modes) | V _{CC} ≤ 800V, Input = ON (One-Shot) T _j = 125°C start 13.5V ≤ V _{DH} = V _{DB} ≤ 16.5V | <ul style="list-style-type: none"> • No destruction • FO output by protection operation | | | |
| | Switching SOA | V _{CC} ≤ 800V, T _j ≤ 125°C, I _c < I _{OL} (CL) operation level, Input = ON, 13.5V ≤ V _{DH} = V _{DB} ≤ 16.5V | <ul style="list-style-type: none"> • No destruction • No protecting operation • No FO output | | | |
| I _{DH} | V _{DH} Circuit Current | V _{DL} = 5V, V _{DH} = 15V, V _{CIN} = 5V | — | — | 150 | mA |
| I _{DL} | V _{DL} Circuit Current | V _{DL} = 5V, V _{DH} = 15V, V _{CIN} = 5V | — | — | 50 | mA |
| V _{th(on)} | Input on threshold voltage | | 0.8 | 1.4 | 2.0 | V |
| V _{th(off)} | Input off threshold voltage | | 2.5 | 3.0 | 4.0 | V |
| R _i | Input pull-up resistor | Integrated between input terminal-V _{DH} | — | 150 | — | kΩ |

ELECTRICAL CHARACTERISTICS (T_j = 25°C, V_{DH} = 15V, V_{DB} = 15V, V_{DL} = 5V unless otherwise noted)

| Symbol | Item | Condition | Ratings | | | Unit |
|-----------------------|---|--|---------|-------|-------|------|
| | | | Min. | Typ. | Max. | |
| f _{PWM} | PWM input frequency | T _c ≤ 100°C, T _j ≤ 125°C | 2 | — | 15 | kHz |
| t _{xx} | Allowable input on-pulse width | V _{DH} = 15V, V _{DL} = 5V, T _c = -20°C ~ +100°C (Note 3) | 2 | — | 500 | μs |
| t _{dead} | Allowable input signal dead time for blocking arm shoot-through | Relates to corresponding inputs (Except brake part) T _c = -20°C ~ +100°C | 4.0 | — | — | μs |
| t _{int} | Input inter-lock sensing | Relates to corresponding inputs (Except brake part) | — | 65 | 100 | ns |
| V _{CO} | Analogue signal linearity with output current | I _c = 0A, V _{DH} = 15V | 1.87 | 2.27 | 2.57 | V |
| V _{C+(200%)} | | I _c = I _{OP(200%)} , V _{DL} = 5V | 0.77 | 1.17 | 1.47 | V |
| V _{C-(200%)} | | I _c = -I _{OP(200%)} , T _c = -20 ~ 100°C (Fig.4) | 2.97 | 3.37 | 3.67 | V |
| ΔV _{CO} | Offset change area vs temperature | V _{DH} = 15V, V _{DL} = 5V, T _c = -20 ~ 100°C | — | 15 | — | mV |
| V _{C+} | Analogue signal output voltage limit | I _c > I _{OP(200%)} , V _{DH} = 15V, | — | — | 0.7 | V |
| V _{C-} | | V _{DL} = 5V (Fig. 4) | 4.0 | — | — | V |
| ΔV _{C(200%)} | Analogue signal overall linear variation | V _{CO} -V _{C±(200%)} | — | 1.1 | — | V |
| r _{CH} | Analogue signal data hold accuracy | Correspond to max. 500μs data hold period only, I _c = I _{OP(200%)} (Fig. 5) | -5 | — | 5 | % |
| t _{d(read)} | Analogue signal reading time | After input signal trigger point (Fig. 8) | — | 3 | — | μs |
| I _{CL(H)} | Signal output current of CL operation | Open collector output | Idle | — | 1 | μA |
| I _{CL(L)} | | | Active | — | 1 | — |
| ±I _{OL} | CL warning operation level | V _{DL} = 5V, V _{DH} = 15V, T _c = -20 ~ 100°C (Note 4) | 3.23 | 3.90 | 4.92 | A |
| SC | Short circuit current trip level | T _j = 25°C (Fig. 7), (Note 5) | 5.7 | 8.0 | 11.6 | A |
| OT | Over temperature protection | Trip level | 100 | 110 | 120 | °C |
| OTr | | Reset level | — | 90 | — | °C |
| UV _{DB} | Supply circuit under and over voltage protection | Trip level | 10.0 | 11.0 | 12.0 | V |
| UV _{DBr} | | Reset level | 10.5 | 11.5 | 12.5 | V |
| UV _{DH} | | Trip level | 11.05 | 12.00 | 12.75 | V |
| UV _{DHr} | | Reset level | 11.55 | 12.50 | 13.25 | V |
| OVDH | | Trip level | 18.00 | 19.20 | 20.15 | V |
| OVDHr | | Reset level | 16.50 | 17.50 | 18.65 | V |
| t _{dv} | | Filter time | — | 10 | — | μs |
| I _{FO(H)} | Fault output current | Open collector output | Idle | — | 1 | μA |
| I _{FO(L)} | | | Active | — | 1 | — |

(Note 3) : (a) Allowable minimum input on-pulse width : This item applies to P-side circuit only.

(b) Allowable maximum input on-pulse width : This item applies to both P-side and N-side circuits excluding the brake circuit.

(Note4) : CL output : The "current limit warning (CL) operation circuit outputs warning signal whenever the arm current exceeds this limit. The circuit is reset automatically by the next input signal and thus, it operates on a pulse-by-pulse scheme.

(Note5) : The short circuit protection works instantaneously when a high short circuit current flows through an internal IGBT rising up momentarily. The protection function is, thus meant primarily to protect the ASIPM against short circuit distraction. Therefore, this function is not recommended to be used for any system load current regulation or any over load control as this might, cause a failure due to excessive temperature rise. Instead, the analogue current output feature or the over load warning feature (CL) should be appropriately used for such current regulation or over load control operation. In other words, the PWM signals to the ASIPM should be shut down, in principle, and not to be restarted before the junction temperature would recover to normal, as soon as a fault is feed back from its FO1 pin of the ASIPM indicating a short circuit situation.

RECOMMENDED CONDITIONS

| Symbol | Item | Condition | Ratings | | | Unit |
|--|---------------------------------|---|---------|------|------|------|
| | | | Min. | Typ. | Max. | |
| V _{CC} | Supply voltage | Applied between P-N | — | 600 | 800 | V |
| V _{DH} , V _{DB} | Control supply voltage | Applied between V _{DH} -GND, CBU+-CBU-, CBV+-CBV-, CBW+-CBW- | 13.5 | 15.0 | 16.5 | V |
| V _{DL} | Control supply voltage | Applied between V _{DL} -GND | 4.8 | 5.0 | 5.2 | V |
| ΔV _{DH} , ΔV _{DB} , ΔV _{DL} | Supply voltage ripple | | -1 | — | +1 | V/μs |
| V _{CIN(on)} | Input ON voltage | | — | — | 0.3 | V |
| V _{CIN(off)} | Input OFF voltage | | 4.8 | — | — | V |
| f _{PWM} | PWM Input frequency | Using application circuit | 2 | 10 | 15 | kHz |
| t _{dead} | Arm shoot-through blocking time | Using application circuit | 4.0 | — | — | μs |

Fig. 4 OUTPUT CURRENT ANALOGUE SIGNALING LINEARITY

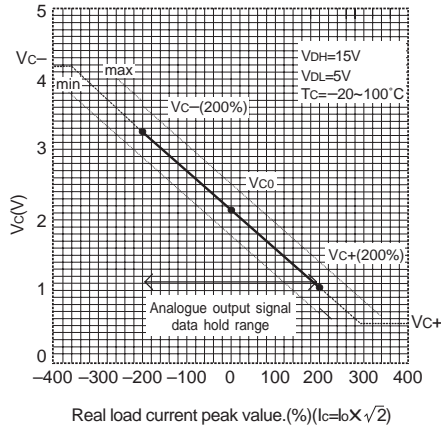
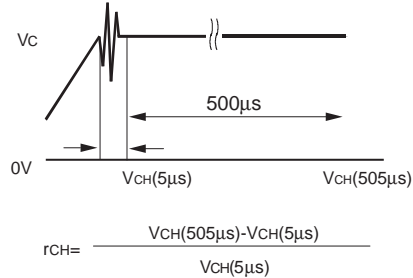
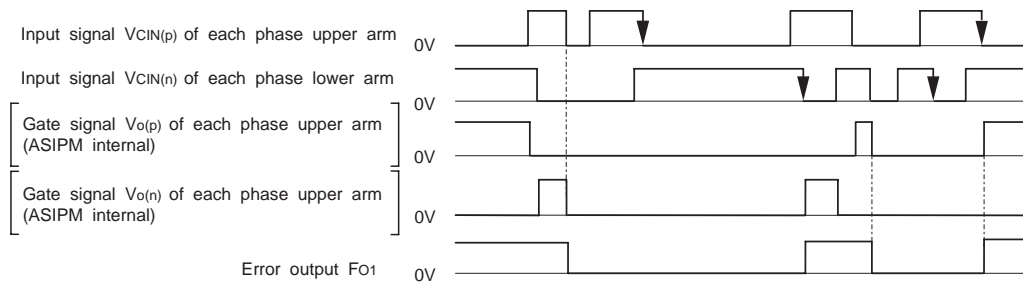


Fig. 5 OUTPUT CURRENT ANALOGUE SIGNALING "DATA HOLD" DEFINITION



Note ; Ringing happens around the point where the signal output voltage changes state from "analogue" to "data hold" due to test circuit arrangement and instrumental trouble. Therefore, the rate of change is measured at a 5 μs delayed point.

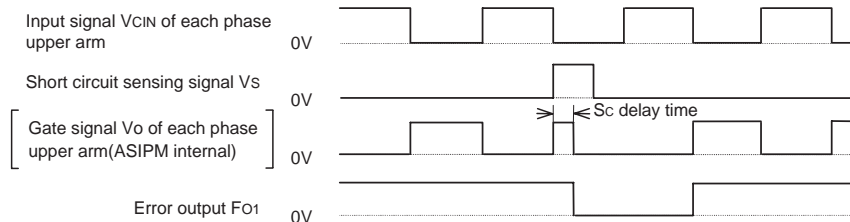
Fig. 6 INPUT INTERLOCK OPERATION TIMING CHART



Note : Input interlock protection circuit ; It is operated when the input signals for any upper-arm / lower-arm pair of a phase are simultaneously in "LOW" level.

By this interlocking, both upper and lower IGBTs of this mal-triggered phase are cut off, and "Fo" signal is outputted. After an "input interlock" operation the circuit is latched. The "Fo" is reset by the high-to-low going edge of either an upper-leg, or a lower-leg input, whichever comes in later.

Fig. 7 TIMING CHART AND SHORT CIRCUIT PROTECTION OPERATION



Note : Short circuit protection operation. The protection operates with "Fo" flag and reset on a pulse-by-pulse scheme. The protection by gate shutdown is given only to the IGBT that senses an overload (excluding the IGBT for the "Brake").

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Fig. 8 INVERTER OUTPUT ANALOGUE CURRENT SENSING AND SIGNALING TIMING CHART.

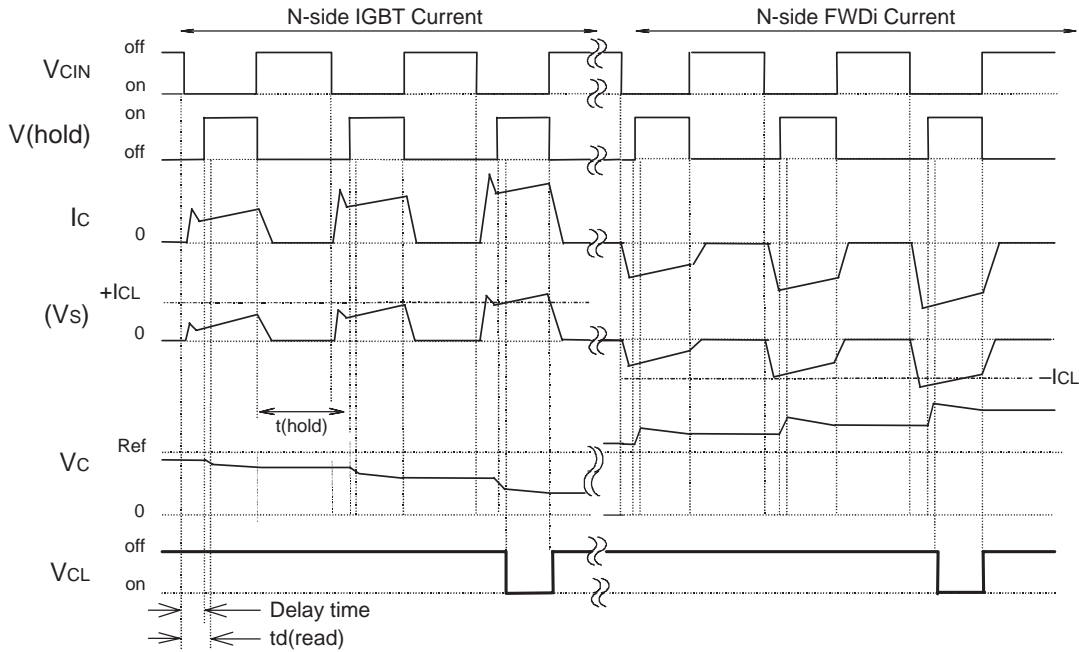
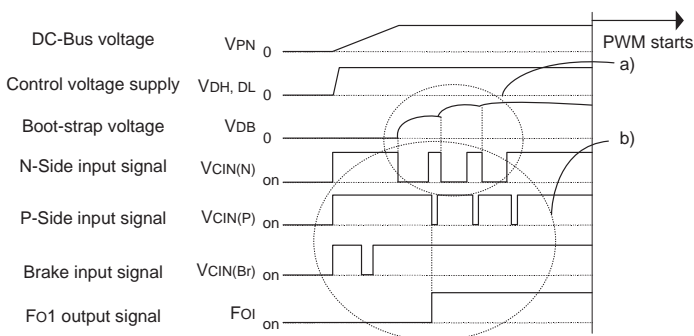


Fig. 9 START-UP SEQUENCE

Normally at start-up, Fo and CL output signals will be pulled-up High to V_{DL} voltage (OFF level); however, Fo1 output may fall to Low (ON) level at the instant of the first ON input pulse to an N-Side IGBT. This can happen particularly when the boot-strap capacitor is of large size. Fo1 resetting sequence (together with the boot-strap charging sequence) is explained in the following graph



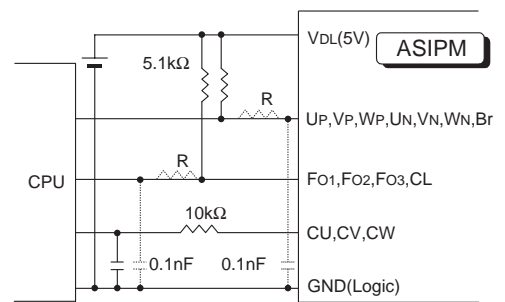
a) Boot-strap charging scheme :

Apply a train of short ON pulses at all N-IGBT input pins for adequate charging (pulse width = approx. $20\mu s$ number of pulses = 10 ~ 500 depending on the boot-strap capacitor size)

b) Fo1 resetting sequence:

Apply ON signals to the following input pins : Br \rightarrow Un/Vn/Wn \rightarrow Up/Vp/Wp in that order.

Fig. 10 RECOMMENDED I/O INTERFACE CIRCUIT





**Стандарт
Электрон
Связь**

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Благодаря сотрудничеству с мировыми поставщиками мы осуществляем комплексные и плановые поставки широчайшего спектра электронных компонентов.

Собственная эффективная логистика и склад в обеспечивает надежную поставку продукции в точно указанные сроки по всей России.

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