

EC103D1

Thyristor, sensitive gate

Rev. 02 — 31 July 2008

Product data sheet

1. Product profile

1.1 General description

Passivated ultra sensitive gate thyristor in a SOT54 plastic package.

1.2 Features

- Ultra sensitive gate
- Direct interfacing to low power gate trigger circuits

1.3 Applications

- Earth leakage circuit breakers or Ground Fault Circuit Interrupters (GFCI)
- Solid state relays
- General purpose switching
- Small engine ignition

1.4 Quick reference data

- $V_{DRM} \leq 400 \text{ V}$
- $V_{RRM} \leq 400 \text{ V}$
- $I_{TSM} \leq 8 \text{ A}$ ($t = 10 \text{ ms}$)
- $I_{T(RMS)} \leq 0.8 \text{ A}$
- $I_{GT} \leq 12 \mu\text{A}$

2. Pinning information

Table 1. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	anode (A)		
2	gate (G)		
3	cathode (K)		

SOT54 (TO-92)

3. Ordering information

Table 2. Ordering information

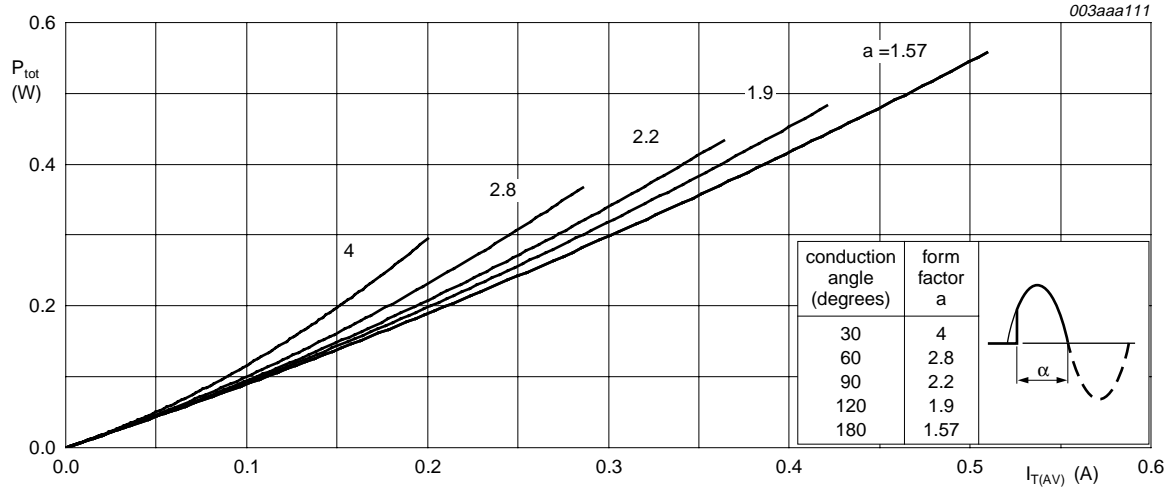
Type number	Package		Version
	Name	Description	
EC103D1	TO-92	plastic single-ended leaded (through hole) package; 3 leads	SOT54

4. Limiting values

Table 3. Limiting values

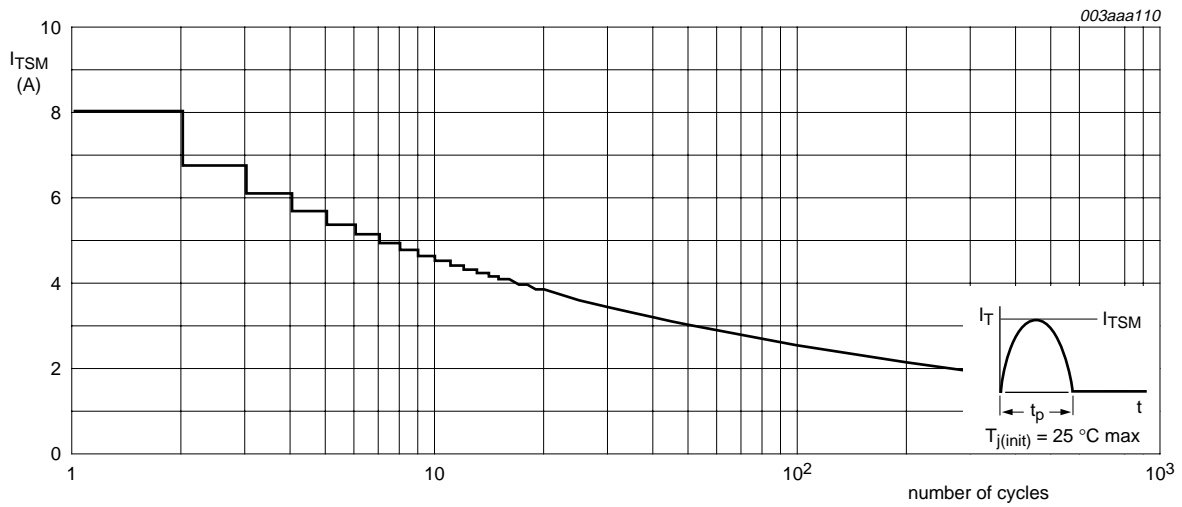
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	400	V
V_{RRM}	repetitive peak reverse voltage		-	400	V
V_{DSM}	non-repetitive peak off-state voltage		-	450	V
V_{RSM}	non-repetitive peak reverse voltage		-	450	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{lead} \leq 92\text{ °C}$; see Figure 1	-	0.5	A
$I_{T(RMS)}$	RMS on-state current	all conduction angles; see Figure 4 and 5	-	0.8	A
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_j = 25\text{ °C}$ prior to surge; see Figure 2 and 3			
		$t = 10\text{ ms}$	-	8	A
		$t = 8.3\text{ ms}$	-	9	A
I^2t	I^2t for fusing	$t_p = 10\text{ ms}$	-	0.32	A ² s
di_T/dt	rate of rise of on-state current	$I_{TM} = 2\text{ A}$; $I_G = 10\text{ mA}$; $di_G/dt = 0.1\text{ A}/\mu\text{s}$	-	50	A/ μs
I_{GM}	peak gate current		-	1	A
V_{RGM}	peak reverse gate voltage		-	5	V
P_{GM}	peak gate power		-	2	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.1	W
T_{stg}	storage temperature		-40	+150	°C
T_j	junction temperature		-	125	°C



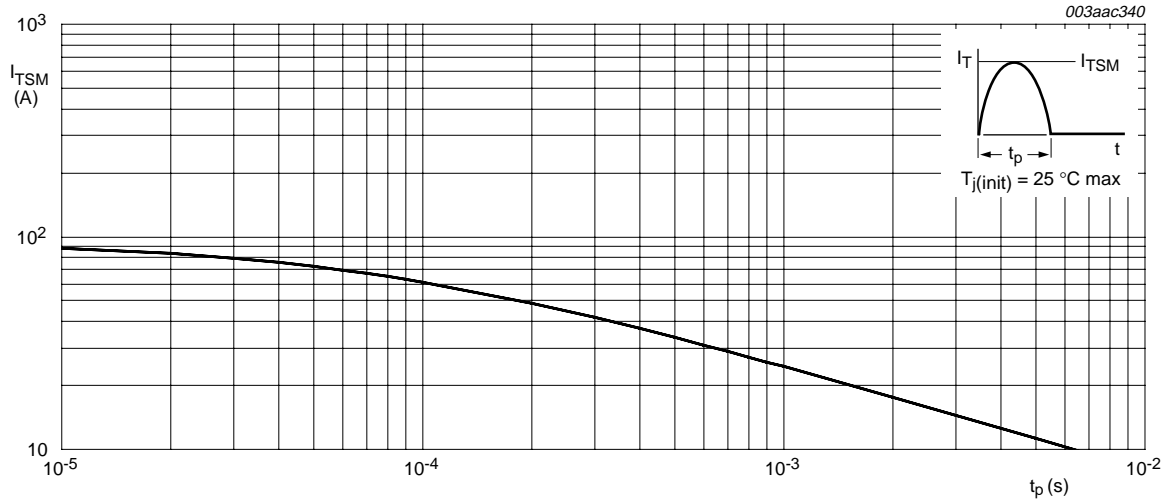
Form factor $a = I_{T(RMS)} / I_{T(AV)}$

Fig 1. Total power dissipation as a function of average on-state current; maximum values



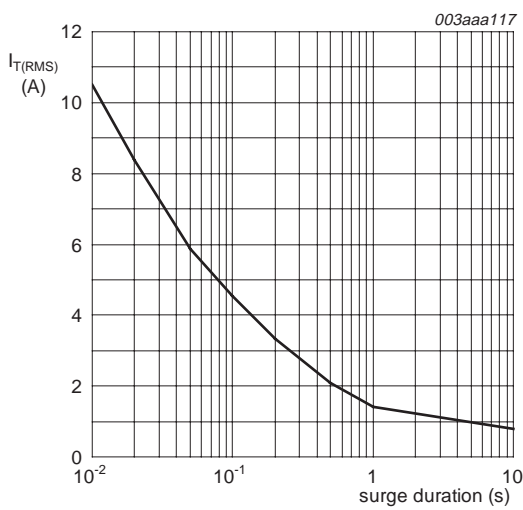
f = 50 Hz

Fig 2. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



$t_p \leq 10\text{ ms}$

Fig 3. Non-repetitive peak on-state current as a function of pulse duration; maximum values



$f = 50\text{ Hz}$
 $T_{lead} = 92\text{ °C}$

Fig 4. RMS on-state current as a function of surge duration; maximum values

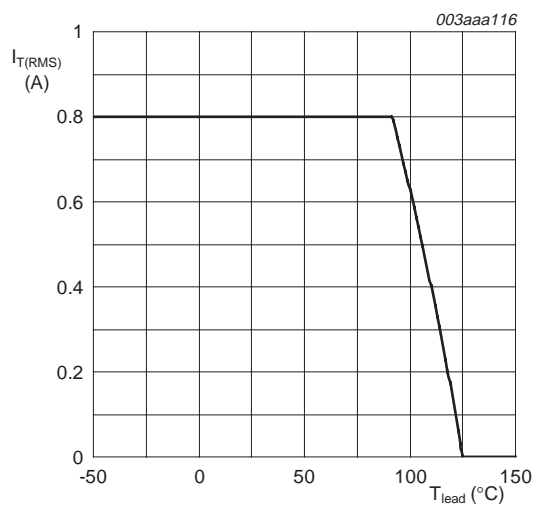
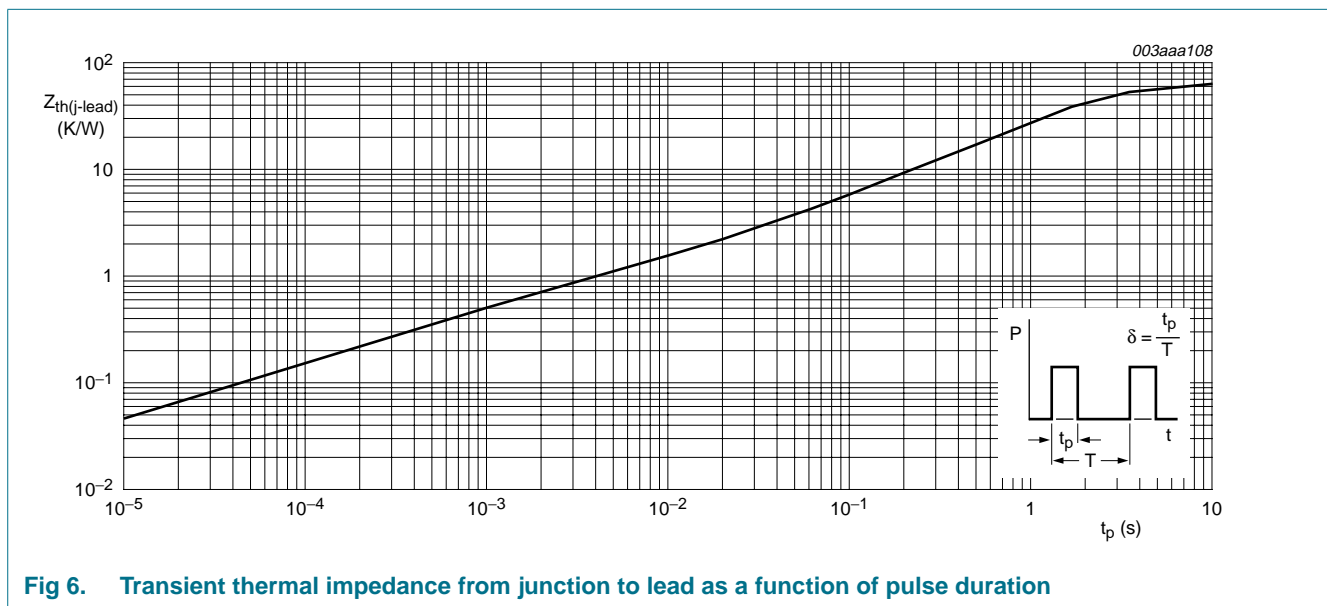


Fig 5. RMS on-state current as a function of lead temperature; maximum values

5. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-lead)}$	thermal resistance from junction to lead	see Figure 6	-	-	60	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	printed-circuit board mounted; lead length 4 mm	-	150	-	K/W



6. Characteristics

Table 5. Characteristics

$T_j = 25\text{ °C}$ unless otherwise stated.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; see Figure 8	-	3	12	μA
I_L	latching current	$V_D = 12\text{ V}$; $I_{GT} = 0.5\text{ mA}$; $R_{GK} = 1\text{ k}\Omega$; see Figure 10	-	2	6	mA
I_H	holding current	$V_D = 12\text{ V}$; $I_{GT} = 0.5\text{ mA}$; $R_{GK} = 1\text{ k}\Omega$; see Figure 11	-	2	5	mA
V_T	on-state voltage	$I_T = 1\text{ A}$	-	1.2	1.35	V
V_{GT}	gate trigger voltage	$I_T = 10\text{ mA}$; see Figure 7				
		$V_D = 12\text{ V}$	-	0.5	0.8	V
		$V_D = V_{DRM(max)}$; $T_j = 125\text{ °C}$	0.2	0.3	-	V
I_D	off-state current	$V_D = V_{DRM(max)}$; $T_j = 125\text{ °C}$; $R_{GK} = 1\text{ k}\Omega$	-	0.05	0.1	mA
I_R	reverse current	$V_R = V_{RRM(max)}$; $T_j = 125\text{ °C}$; $R_{GK} = 1\text{ k}\Omega$	-	0.05	0.1	mA
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 0.67 \times V_{DRM(max)}$; $T_j = 125\text{ °C}$; exponential waveform; $R_{GK} = 1\text{ k}\Omega$; see Figure 12	-	150	-	$\text{V}/\mu\text{s}$
t_{gt}	gate-controlled turn-on time	$I_{TM} = 2\text{ A}$; $V_D = V_{DRM(max)}$; $I_G = 10\text{ mA}$; $dI_G/dt = 0.1\text{ A}/\mu\text{s}$	-	2	-	μs
t_q	commutated turn-off time	$V_{DM} = 0.67 \times V_{DRM(max)}$; $T_j = 125\text{ °C}$; $I_{TM} = 1.6\text{ A}$; $V_R = 35\text{ V}$; $(dI_T/dt)_M = 30\text{ A}/\mu\text{s}$; $dV_D/dt = 2\text{ V}/\mu\text{s}$; $R_{GK} = 1\text{ k}\Omega$	-	100	-	μs

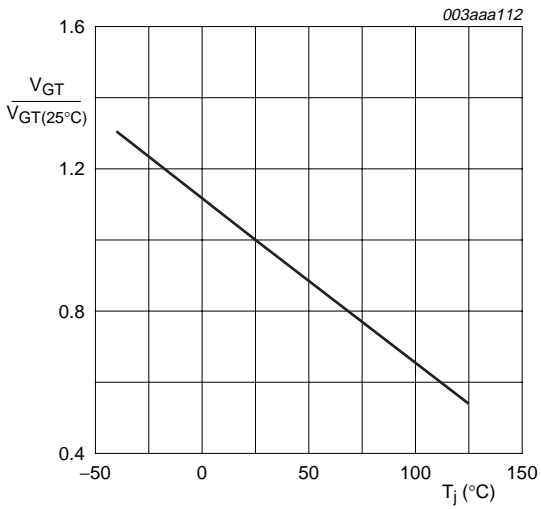


Fig 7. Normalized gate trigger voltage as a function of junction temperature

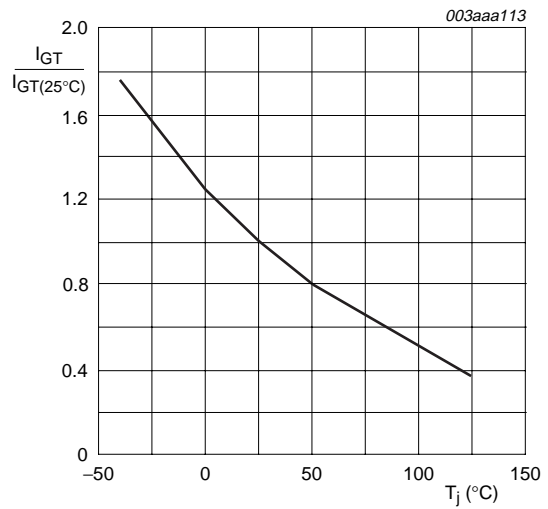
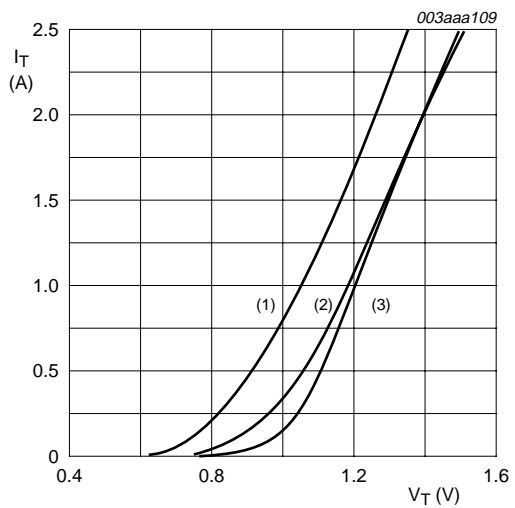


Fig 8. Normalized gate trigger current as a function of junction temperature



$V_o = 0.895\text{ V}$
 $R_s = 0.195\ \Omega$
 (1) $T_j = 125\text{ }^\circ\text{C}$; typical values
 (2) $T_j = 125\text{ }^\circ\text{C}$; maximum values
 (3) $T_j = 25\text{ }^\circ\text{C}$; typical values

Fig 9. On-state current as a function of on-state voltage

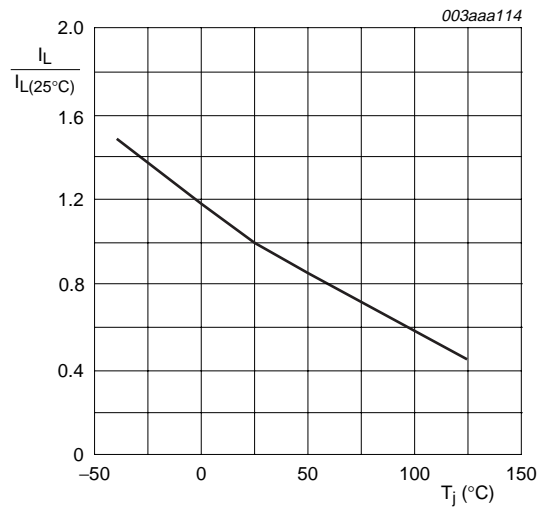
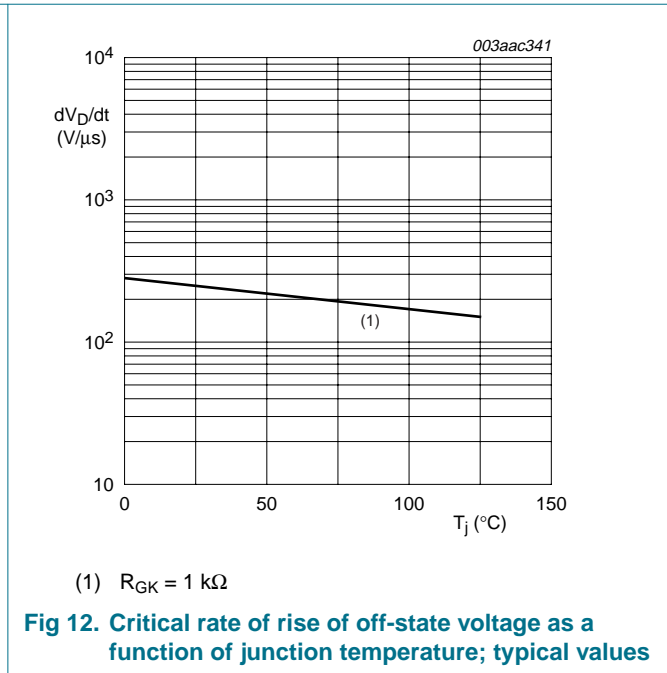
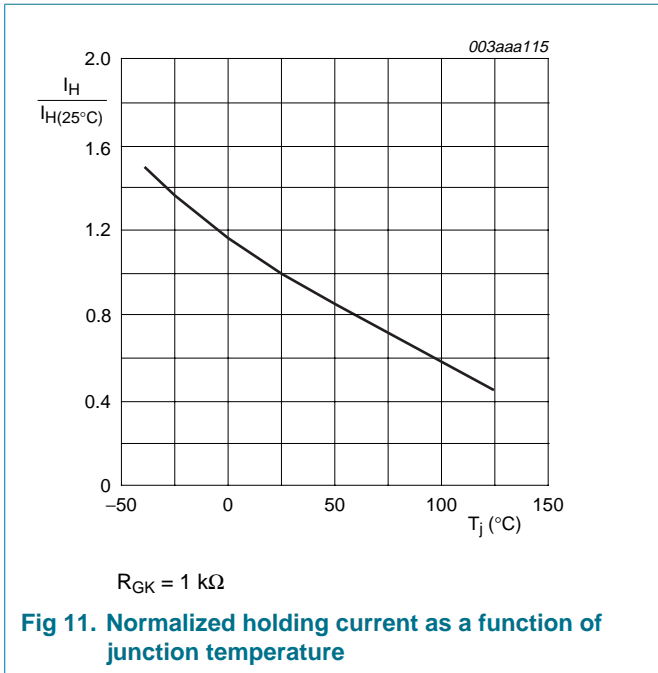


Fig 10. Normalized latching current as a function of junction temperature



7. Package information

Epoxy meets requirements of UL 94 V-0 at 3.175 mm

8. Package outline

Plastic single-ended leaded (through hole) package; 3 leads

SOT54

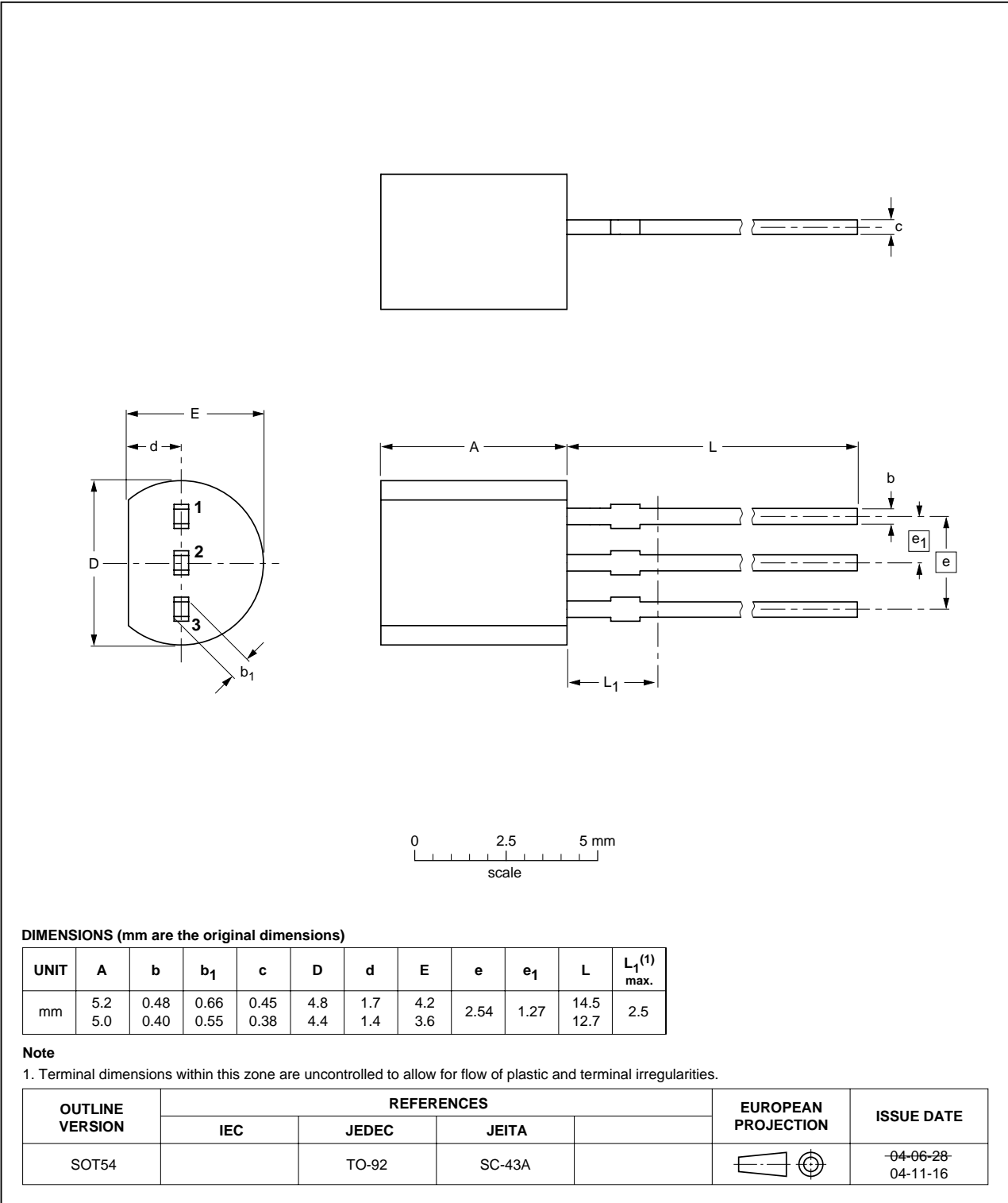


Fig 13. Package outline SOT54 (TO-92)

9. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
EC103D1_2	20080731	Product data sheet	-	EC103D1-01
Modifications:	<ul style="list-style-type: none"> • The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Table 3 “Limiting values” on page 2; V_{DSM} and V_{RSM} added. • Table 5 “Characteristics” on page 6; dV_D/dt updated. • Figure 4 on page 4; graph redrawn. • Figure 6 on page 5; graph redrawn. • Figure 11; graph added. • Figure 12; graph added. 			
EC103D1-01 (9397 750 08574)	20011101	Product data	-	-

10. Legal information

10.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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