CY7C1019D

1-Mbit (128 K × 8) Static RAM

Features

- Pin- and function-compatible with CY7C1019B
- High speed
  - t_{AA} = 10 ns
- Low active power
  - I_{CC} = 80 mA @ 10 ns
- Low CMOS standby power
  - I_{SB2} = 3 mA
- 2.0 V Data retention
- Automatic power-down when deselected
- CMOS for optimum speed/power
- Center power/ground pinout
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- Functionally equivalent to CY7C1019B
- Available in Pb-free 32-pin 400-Mil wide Molded SOJ and 32-pin TSOP II packages

Functional Description

The CY7C1019D [1] is a high-performance CMOS static RAM organized as 131,072 words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable ($\overline{CE}$), an active LOW Output Enable ($\overline{OE}$), and tri-state drivers. This device has an automatic power-down feature that significantly reduces power consumption when deselected. The eight input and output pins (IO_0 through IO_7) are placed in a high-impedance state when:

- Deselected ($\overline{CE}$ HIGH)
- Outputs are disabled ($\overline{OE}$ HIGH)
- When the write operation is active ($\overline{CE}$ LOW, and $\overline{WE}$ LOW).

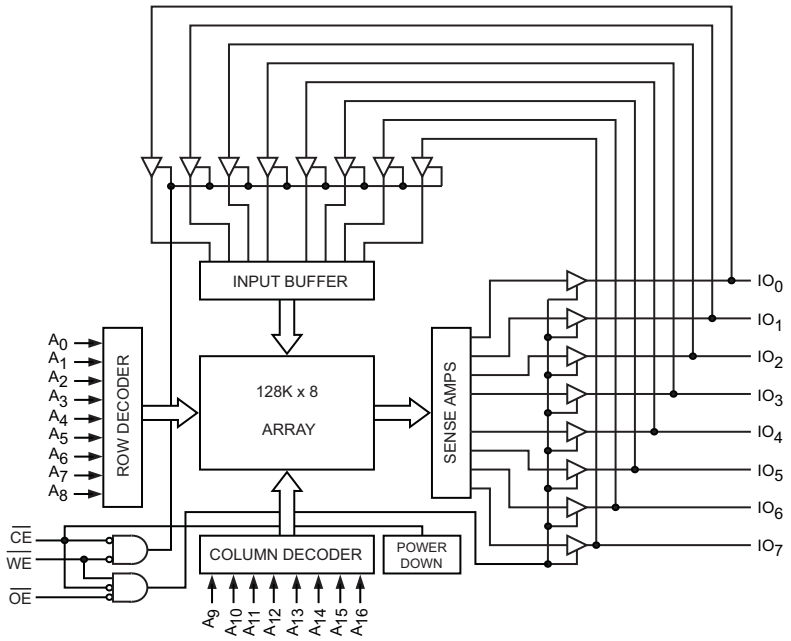
Write to the device by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. Data on the eight IO pins (IO_0 through IO_7) is then written into the location specified on the address pins (A_0 through A_{16}).

Read from the device by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing Write Enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins appears on the IO pins.

The CY7C1019D device is suitable for interfacing with processors that have TTL I/P levels. It is not suitable for processors that require CMOS I/P levels. Please see Electrical Characteristics on page 4 for more details and suggested alternatives.

For a complete list of related documentation, click here.

Logic Block Diagram

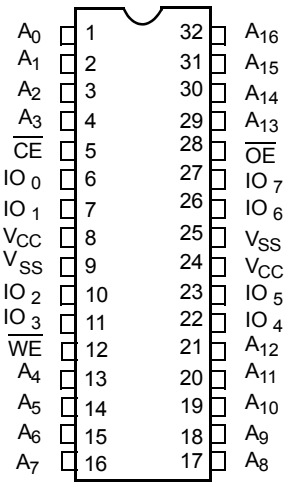


Note
1. For guidelines on SRAM system design, please refer to the 'System Design Guidelines' Cypress application note, available on the internet at www.cypress.com.

Contents

Pin Configuration

Figure 1. 32-pin SOJ / TSOP II pinout (Top View)



Selection Guide

Description	-10 (Industrial)	Unit
Maximum Access Time	10	ns
Maximum Operating Current	80	mA
Maximum Standby Current	3	mA

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... –65 °C to +150 °C

Ambient Temperature with Power Applied ..... –55 °C to +125 °C

Supply Voltage on V_{CC} to Relative GND [2] .....–0.5 V to +6.0 V

DC Voltage Applied to Outputs in High Z State [2] ..... –0.5 V to V_{CC} + 0.5 V

DC Input Voltage [2] ..... –0.5 V to V_{CC} + 0.5 V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage (per MIL-STD-883, Method 3015) ..... > 2001 V

Latch-up Current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}	Speed
Industrial	–40 °C to +85 °C	5 V ± 0.5 V	10 ns

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		-10 (Industrial)		Unit
				Min	Max	
V_{OH}	Output HIGH Voltage	I_{OH} = –4.0 mA		2.4	–	V
		I_{OH} = –0.1 mA		–	3.4 [3]	
V_{OL}	Output LOW Voltage	I_{OL} = 8.0 mA		–	0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage [2]			–0.5	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		–1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		–1	+1	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max, I_{OUT} = 0 mA, f = f_{max} = $1/t_{RC}$	100 MHz	–	80	mA
			83 MHz	–	72	mA
			66 MHz	–	58	mA
			40 MHz	–	37	mA
I_{SB1}	Automatic CE Power-Down Current – TTL Inputs	Max V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{max}		–	10	mA
I_{SB2}	Automatic CE Power-Down Current – CMOS Inputs	Max V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3 V, V_{IN} ≥ V_{CC} – 0.3 V, or V_{IN} ≤ 0.3 V, f = 0		–	3	mA

Note
2. V_{IL} (min) = –2.0 V and V_{IH}(max) = V_{CC} + 1 V for pulse durations of less than 5 ns.
3. Please note that the maximum V_{OH} limit doesnot exceed minimum CMOS VIH of 3.5V. If you are interfacing this SRAM with 5 V legacy processors that require a minimum V_{IH} of 3.5 V, please refer to Application Note AN6081 for technical details and options you may consider.

Capacitance

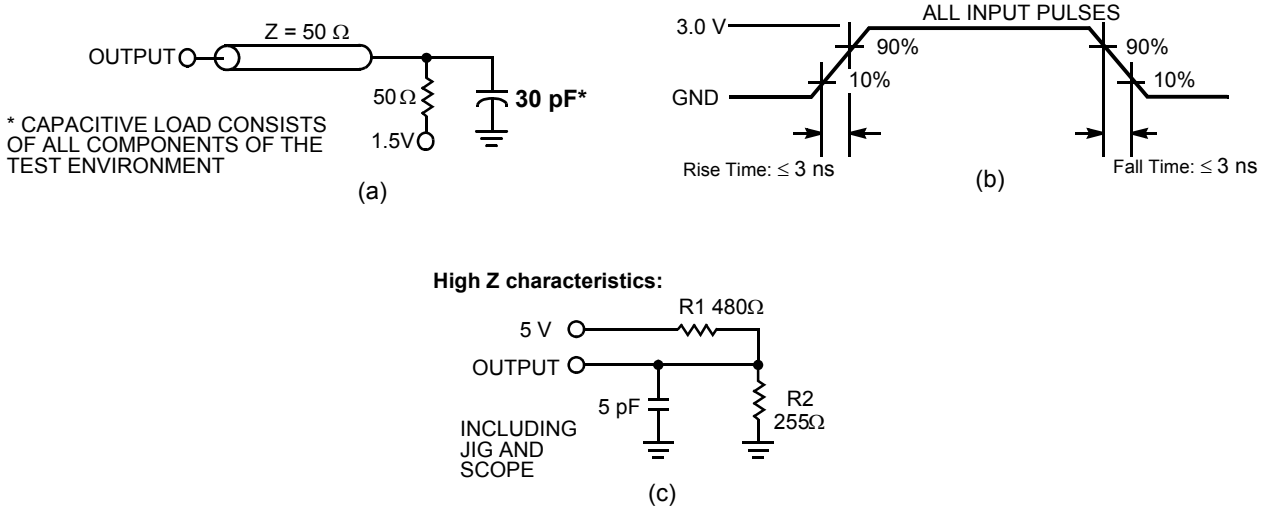
Parameter [4]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 5.0 V	6	pF
C_{OUT}	Output capacitance		8	pF

Thermal Resistance

Parameter [4]	Description	Test Conditions	400-Mil Wide SOJ	TSOP II	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	56.29	62.22	°C/W
Θ_{JC}	Thermal resistance (junction to case)		38.14	21.43	°C/W

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms [5]



Notes
4. Tested initially and after any design or process changes that may affect these parameters.
5. AC characteristics (except High Z) are tested using the load conditions shown in Figure 2 (a). High Z characteristics are tested for all speeds using the test load shown in Figure 2 (c).

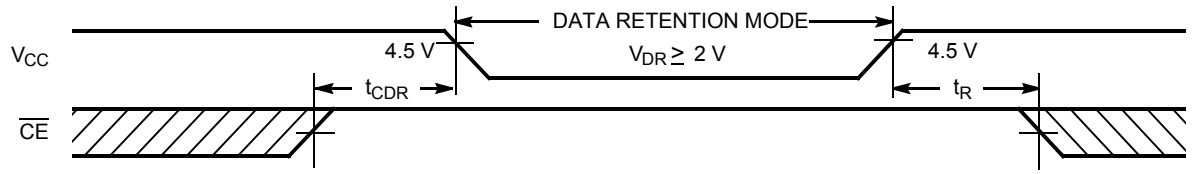
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Max	Unit
V_{DR}	V_{CC} for Data Retention		2.0	–	V
I_{CCDR}	Data Retention Current	$V_{CC} = V_{DR} = 2.0$ V, $\overline{CE} \geq V_{CC} - 0.3$ V, $V_{IN} \geq V_{CC} - 0.3$ V or $V_{IN} \leq 0.3$ V	–	3	mA
t_{CDR} [6]	Chip Deselect to Data Retention Time		0	–	ns
t_R [7]	Operation Recovery Time		t_{RC}	–	ns

Data Retention Waveform

Figure 3. Data Retention Waveform



Notes
6. Tested initially and after any design or process changes that may affect these parameters.
7. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 50$ µs or stable at $V_{CC(min)} \geq 50$ µs.

Switching Characteristics

Over the Operating Range

Parameter [8]	Description	-10 (Industrial)		Unit
		Min	Max	
Read Cycle				
t_{power} [9]	V_{CC}(typical) to the first access	100	–	µs
t_{RC}	Read Cycle Time	10	–	ns
t_{AA}	Address to Data Valid	–	10	ns
t_{OHA}	Data Hold from Address Change	3	–	ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid	–	10	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid	–	5	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z [10, 11]	–	5	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z [11]	3	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z [10, 11]	–	5	ns
t_{PU} [12]	$\overline{CE}$ LOW to Power-Up	0	–	ns
t_{PD} [12]	$\overline{CE}$ HIGH to Power-Down	–	10	ns
Write Cycle [13, 14]				
t_{WC}	Write Cycle Time	10	–	ns
t_{SCE}	$\overline{CE}$ LOW to Write End	7	–	ns
t_{AW}	Address Set-Up to Write End	7	–	ns
t_{HA}	Address Hold from Write End	0	–	ns
t_{SA}	Address Set-Up to Write Start	0	–	ns
t_{PWE}	$\overline{WE}$ Pulse Width	7	–	ns
t_{SD}	Data Set-Up to Write End	6	–	ns
t_{HD}	Data Hold from Write End	0	–	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z [11]	3	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High Z [10, 11]	–	5	ns

Notes

8. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
9. t_{POWER} gives the minimum amount of time that the power supply should be at typical V_{CC} values until the first memory access can be performed.
10. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in (c) of Figure 2 on page 5. Transition is measured when the outputs enter a high impedance state.
11. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
12. This parameter is guaranteed by design and is not tested.
13. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
14. The minimum write cycle time for Write Cycle no. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Switching Waveforms

Figure 4. Read Cycle No. 1 (Address Transition Controlled) [15, 16]

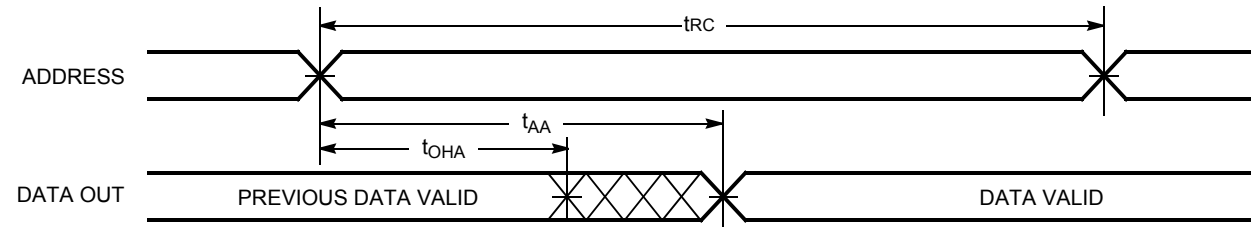
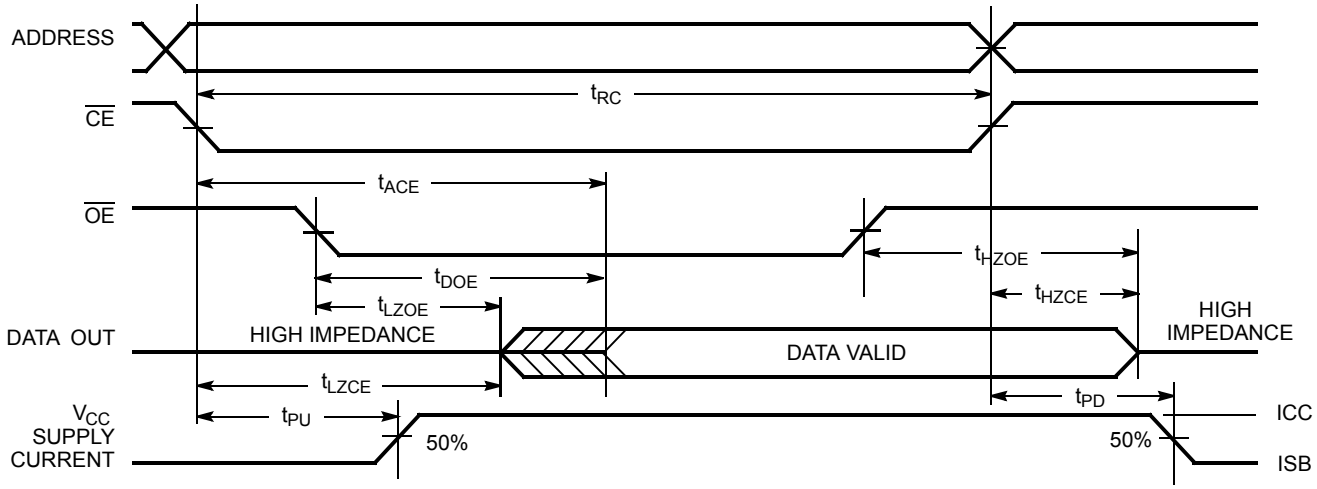


Figure 5. Read Cycle No. 2 ($\overline{OE}$ Controlled) [16, 17]



Notes
15. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
16. $\overline{WE}$ is HIGH for Read cycle.
17. Address valid prior to or coincident with $\overline{CE}$ transition LOW..

Switching Waveforms (continued)

Figure 6. Write Cycle No. 1 ($\overline{CE}$ Controlled) [18, 19]

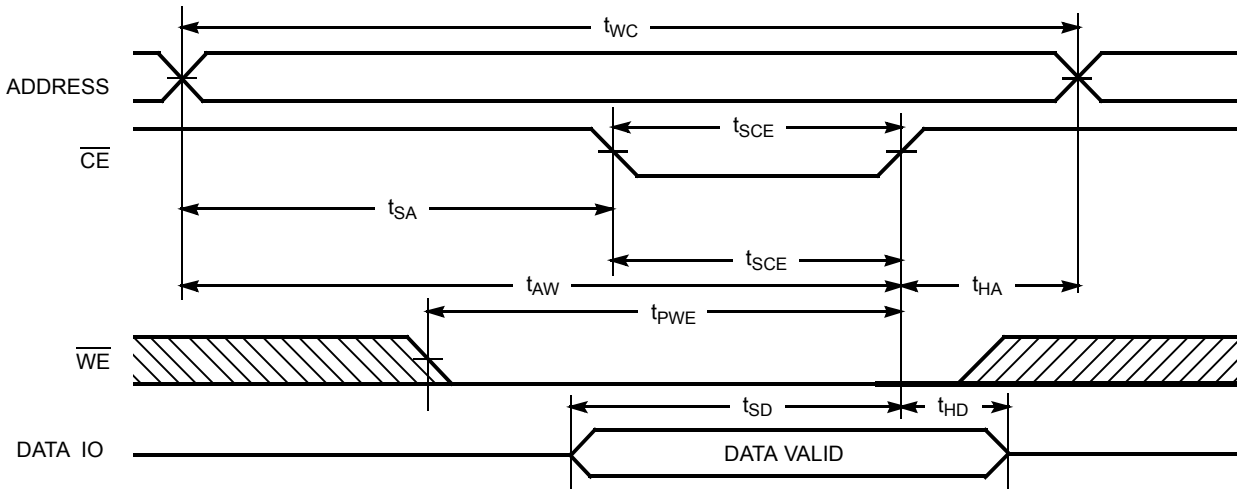
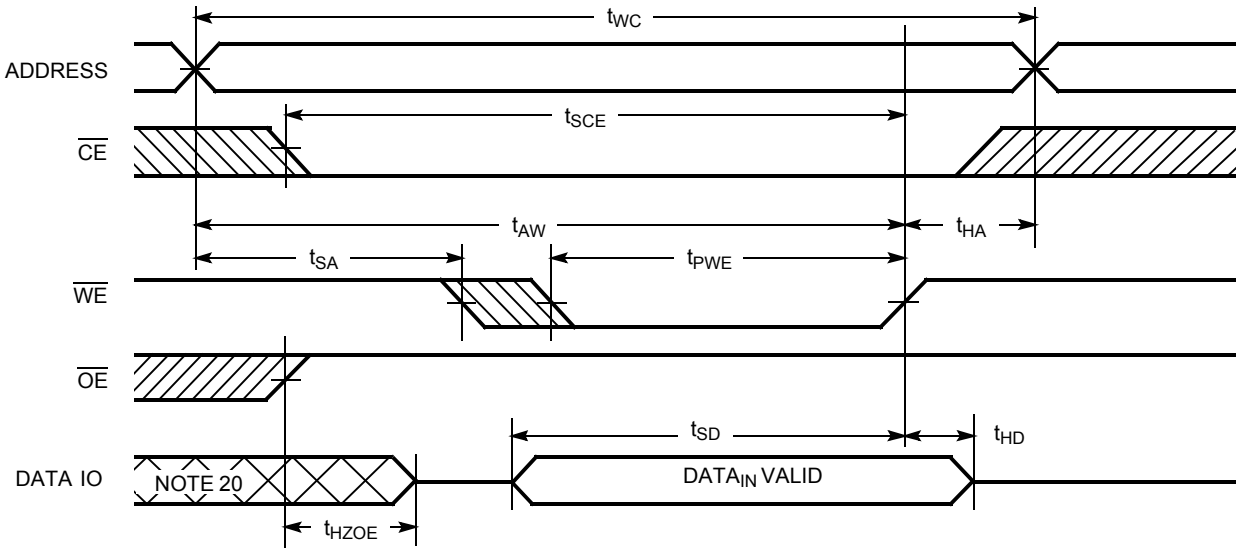


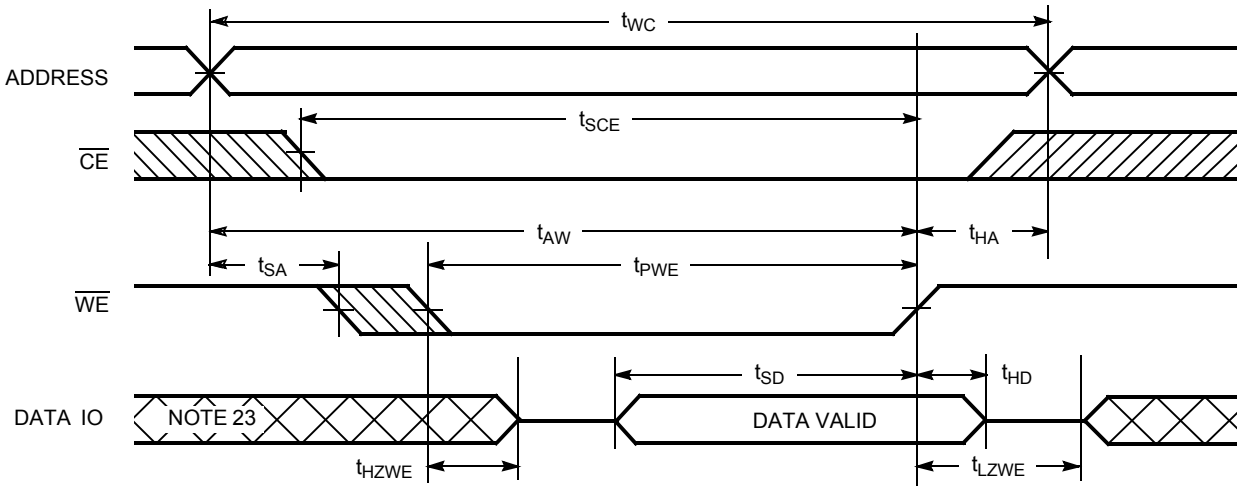
Figure 7. Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write) [18, 19]



Notes
18. Data IO is high impedance if $\overline{OE}$ = V_{IH}.
19. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.
20. During this period the IOs are in the output state and input signals should not be applied.

Switching Waveforms (continued)

Figure 8. Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [21, 22]



Notes
21. The minimum write cycle time for Write Cycle no. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.
22. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.
23. During this period the IOs are in the output state and input signals should not be applied.

Truth Table

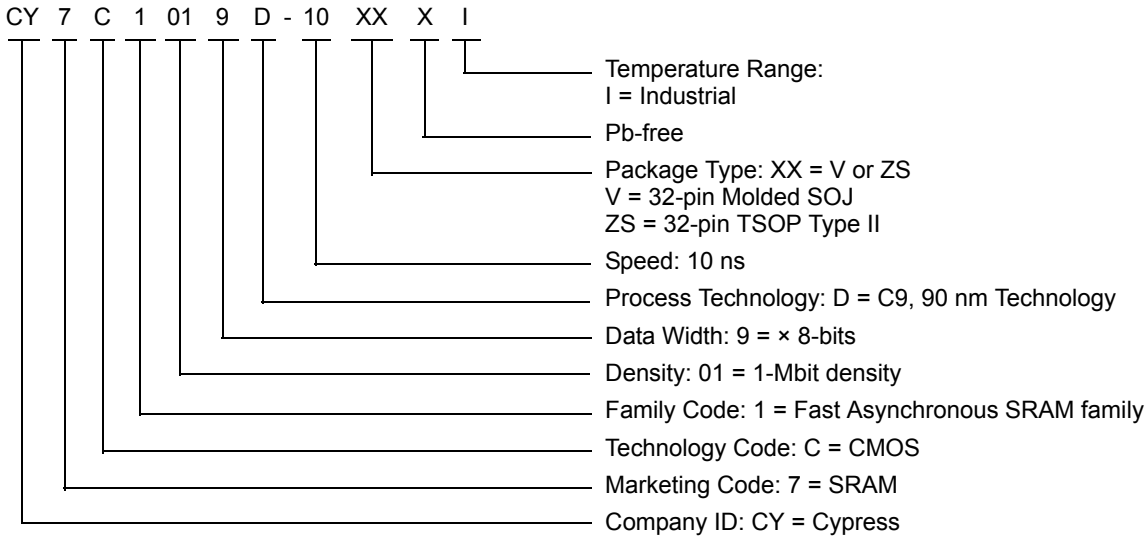
$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	IO_0–IO_7	Mode	Power
H	X	X	High Z	Power-Down	Standby (I_{SB})
L	L	H	Data Out	Read	Active (I_{CC})
L	X	L	Data In	Write	Active (I_{CC})
L	H	H	High Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1019D-10VXI	51-85033	32-pin SOJ (400 Mils) Pb-free	Industrial
	CY7C1019D-10ZSXI	51-85095	32-pin TSOP (Type II) Pb-free	

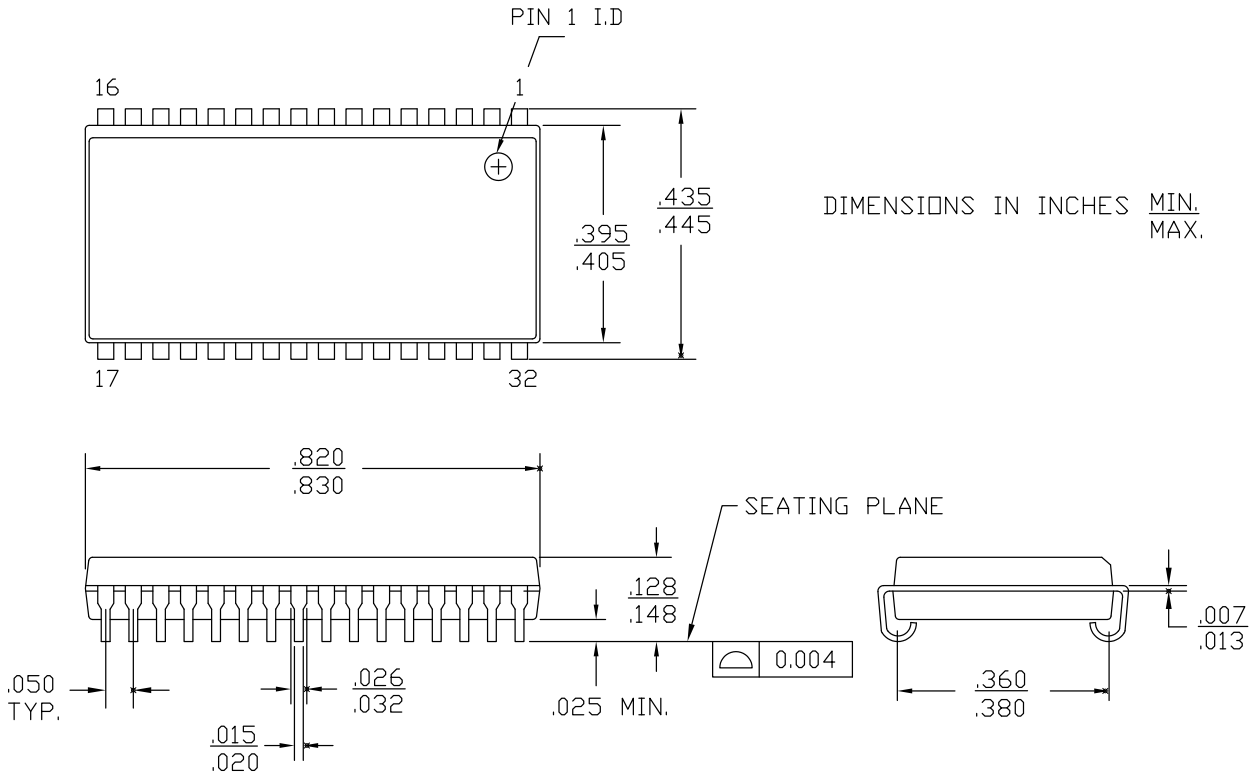
Please contact your local Cypress sales representative for availability of these parts.

Ordering Code Definitions



Package Diagrams

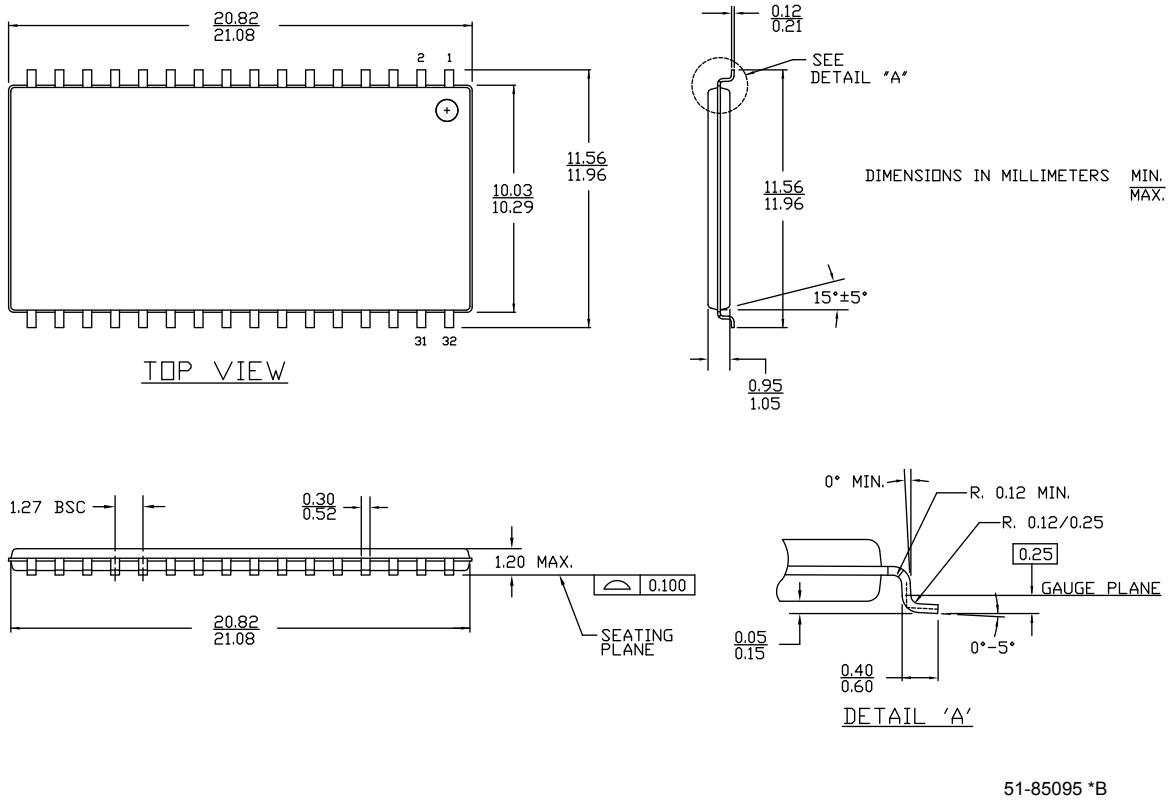
Figure 9. 32-pin SOJ (400 Mils) V32.4 (Molded SOJ V33) Package Outline, 51-85033



51-85033 *E

Package Diagrams (continued)

Figure 10. 32-pin TSOP Type II (20.95 × 11.76 × 1.0 mm) ZS32 Package Outline, 51-85095



Acronyms

Acronym	Description
$\overline{CE}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{OE}$	Output Enable
SOJ	Small Outline J-lead
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
TTL	Transistor-Transistor Logic
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
ms	millisecond
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C1019D, 1-Mbit (128 K × 8) Static RAM Document Number: 38-05464				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	201560	See ECN	SWI	Advance Information data sheet for C9 IPP
*A	233715	See ECN	RKF	DC parameters are modified as per EROS (Spec # 01-2165) Pb-free offering in the Ordering Information
*B	262950	See ECN	RKF	Added T_{power} Spec in Switching Characteristics table Added Data Retention Characteristics table and waveforms Shaded Ordering Information
*C	307598	See ECN	RKF	Reduced Speed bins to -10 and -12 ns
*D	520647	See ECN	VKN	Converted from Preliminary to Final Removed Commercial Operating range Removed 12 ns speed bin Added I_{CC} values for the frequencies 83MHz, 66MHz and 40MHz Updated Thermal Resistance table Updated Ordering Information Table Changed Overshoot spec from V_{CC}+2V to V_{CC}+1V in footnote #2
*E	802877	See ECN	VKN	Changed I_{CC} spec from 60 mA to 80 mA for 100MHz, 55 mA to 72 mA for 83MHz, 45 mA to 58 mA for 66MHz, 30 mA to 37 mA for 40MHz
*F	3110052	12/14/2010	AJU	Added Ordering Code Definitions. Updated Package Diagrams.
*G	3245896	05/02/2011	PRAS	Updated Package Diagrams. Added Acronyms and Units of Measure. Updated in new template.
*H	4038234	06/24/2013	MEMJ	Updated Functional Description. Updated Electrical Characteristics: Added one more Test Condition "I_{OH} = –0.1 mA" for V_{OH} parameter and added maximum value corresponding to that Test Condition. Added Note 3 and referred the same note in maximum value for V_{OH} parameter corresponding to Test Condition "I_{OH} = –0.1 mA". Updated in new template.
*I	4385827	05/21/2014	MEMJ	Updated Package Diagrams: spec 51-85033 – Changed revision from *D to *E. Completing Sunset Review.
*J	4579569	11/26/2014	MEMJ	Added related documentation hyperlink in page 1.

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