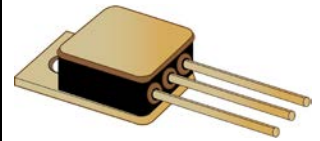


## Radiation Hardened N-Channel MOSFET

*Qualified per MIL-PRF-19500/614*

*Qualified Levels:  
JANSJ, JANSR and  
JANSF*

QPL RANGE and RAD LEVEL			
Radiation Level	JANSJ2N7381	JANSR2N7381	JANSF2N7381
<b>TID</b>	10 Krad	100 Krad	300 Krad



**TO-257AA  
Package**

These products are well suited for Space level applications requiring Total Dose radiation (TID) tolerance and Single Event capability. This 2N7381 is available in three qualified radiation levels and is packaged in a hermetic TO-257 outline. These products have all the same performance features of industry standard MOSFETs and may be used for most voltage control and fast switching applications.

**Important:** For the latest information, visit our website <http://www.microsemi.com>.

### FEATURES

- Ease of paralleling
- Hermetically sealed package
- Low gate charge
- Single event hardened for space applications
- RHA level JANS qualifications available per MIL-PRF-19500/614.  
(See [part nomenclature](#) for all available options.)

### APPLICATIONS / BENEFITS

- Space level DC-DC converters
- Satellite Motor Control circuits
- Synchronous rectification
- Linear-mode applications

### MAXIMUM RATINGS @ T<sub>C</sub> = +25 °C unless otherwise stated

Parameters / Test Conditions	Symbol	Value	Unit
Operating & Storage Junction Temperature Range	T <sub>J</sub> & T <sub>stg</sub>	-55 to +150	°C
Thermal Resistance Junction-to-Case (see <a href="#">Figure 4</a> )	R <sub>θJC</sub>	1.67	°C/W
Total Power Dissipation	P <sub>T</sub>	2 75	W
@ T <sub>A</sub> = +25 °C			
@ T <sub>C</sub> = +25 °C <sup>(1)</sup>			
Gate-Source Voltage, dc	V <sub>GS</sub>	± 20	V
Drain Current, dc @ T <sub>C</sub> = +25 °C <sup>(2)</sup> <sup>(3)</sup>	I <sub>D1</sub>	9.4	A
Drain Current, dc @ T <sub>C</sub> = +100 °C <sup>(2)</sup> <sup>(3)</sup>	I <sub>D2</sub>	6.0	A
Off-State Current (Peak Total Value) <sup>(4)</sup>	I <sub>DM</sub>	37.6	A
Source Current	I <sub>S</sub>	9.4	A

- NOTES:**
1. Derated linearly 0.6 W/°C for T<sub>C</sub> > +25 °C
  2. The following formula derives the maximum theoretical I<sub>D</sub> limit. I<sub>D</sub> is limited by package and internal wires and may also be limited by pin diameter:

$$I_D = \sqrt{\frac{T_J(\text{max}) - T_C}{R_{\theta JC} \times R_{DS(\text{on})} @ T_J(\text{max})}}$$

3. See [Figure 3](#) for maximum drain current graphs
4. I<sub>DM</sub> = 4 X I<sub>D1</sub> as calculated in note (2)

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**MECHANICAL and PACKAGING**

- CASE: Nickel plated copper base & 1020 steel frame
- TERMINALS: Solder dipped copper cored 52 alloy plating
- MARKING: Alpha numeric
- POLARITY: See [Schematic](#) on last page
- WEIGHT: Approximately 3.43 grams
- See [Package Dimensions](#) on last page.

**PART NOMENCLATURE**

**JANSR      2N7381**

**Reliability Level**

JANS D = 10K Rads (Si)  
 JANS R = 100K Rads (Si)  
 JANS F = 300K Rads (Si)

**JEDEC type number**
**SYMBOLS & DEFINITIONS**

Symbol	Definition
$di/dt$	Rate of change of diode current while in reverse-recovery mode, recorded as maximum value.
$I_D$	Drain current, dc: The direct current into the drain terminal.
$I_{DSS}$	Zero-Gate-Voltage Drain Current: The direct current into the gate terminal when the gate-source voltage is zero.
$I_F$	Forward current: The current flowing from the p-type region to the n-type region.
$I_{GSS}$	Reverse-Gate Current, Drain Short-Circuited to Source: The direct current into the gate terminal with a forward gate source voltage applied ( $I_{GSSF}$ ) or reverse gate source voltage applied ( $I_{GSSF}$ ) and the drain terminal short-circuited to the source terminal.
$I_S$	Source current, dc: The direct current into the source terminal.
$r_{DS(on)}$	Static Drain-Source On-State Resistance: The dc resistance between the drain and source terminals with a specified gate-source voltage applied to bias the device to the on state.
$R_G$	Gate drive impedance or Gate resistance
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage: Gate short-circuited to the source terminal.
$V_{DD}$	Drain supply voltage, dc: The dc supply voltage applied to a circuit connected to the drain terminal.
$V_{DG}$	Drain-gate voltage, dc: The dc voltage between the drain and gate terminals.
$V_{DS}$	Drain source voltage, dc: The dc voltage between the drain terminal and the source terminal.
$V_{GS}$	Gate source voltage, dc: The dc voltage between the gate terminal and the source terminal.

**ELECTRICAL CHARACTERISTICS @  $T_A = +25\text{ }^\circ\text{C}$ , unless otherwise noted**

Parameters / Test Conditions	Symbol	Min.	Max.	Unit
<b>PRE-IRRADIATION CHARACTERISTICS</b>				
Drain-Source Breakdown Voltage $V_{GS} = 0\text{ V}, I_D = 1.0\text{ mA}$	$V_{(BR)DSS}$	200		V
Gate-Source Voltage (Threshold) $V_{DS} \geq V_{GS}, I_D = 1\text{ mA}$ $V_{DS} \geq V_{GS}, I_D = 1\text{ mA}, T_J = +125^\circ\text{C}$ $V_{DS} \geq V_{GS}, I_D = 1\text{ mA}, T_J = -55^\circ\text{C}$	$V_{GS(th)1}$ $V_{GS(th)2}$ $V_{GS(th)3}$	2.0 1.0	4.0 5.0	V
Gate Current $V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$ $V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}, T_J = +125^\circ\text{C}$	$I_{GSS1}$ $I_{GSS2}$		$\pm 100$ $\pm 200$	nA
Drain Current $V_{GS} = 0\text{ V}, V_{DS} = 160\text{ V}$	$I_{DSS1}$		25	$\mu\text{A}$
Drain Current $V_{GS} = 0\text{ V}, V_{DS} = 160\text{ V}, T_J = +125\text{ }^\circ\text{C}$	$I_{DSS2}$		0.25	mA
Static Drain-Source On-State Resistance $V_{GS} = 12\text{ V}, I_D = 6.0\text{ A}$ pulsed	$r_{DS(on)1}$		0.40	$\Omega$
Static Drain-Source On-State Resistance $V_{GS} = 12\text{ V}, I_D = 9.4\text{ A}$ pulsed	$r_{DS(on)2}$		0.49	$\Omega$
Static Drain-Source On-State Resistance $T_J = +125^\circ\text{C}$ $V_{GS} = 12\text{ V}, I_D = 6.0\text{ A}$ pulsed	$r_{DS(on)3}$		0.75	$\Omega$
Diode Forward Voltage $V_{GS} = 0\text{ V}, I_D = 9.4\text{ A}$ pulsed	$V_{SD}$		1.4	V

**DYNAMIC CHARACTERISTICS**

Parameters / Test Conditions	Symbol	Min.	Max.	Unit
Gate Charge:				
On-State Gate Charge $V_{GS} = 12\text{ V}, I_D = 9.4\text{ A}, V_{DS} = 100\text{ V}$	$Q_{g(on)}$		50	nC
Gate to Source Charge $V_{GS} = 12\text{ V}, I_D = 9.4\text{ A}, V_{DS} = 100\text{ V}$	$Q_{gs}$		10	nC
Gate to Drain Charge $V_{GS} = 12\text{ V}, I_D = 9.4\text{ A}, V_{DS} = 100\text{ V}$	$Q_{gd}$		25	nC

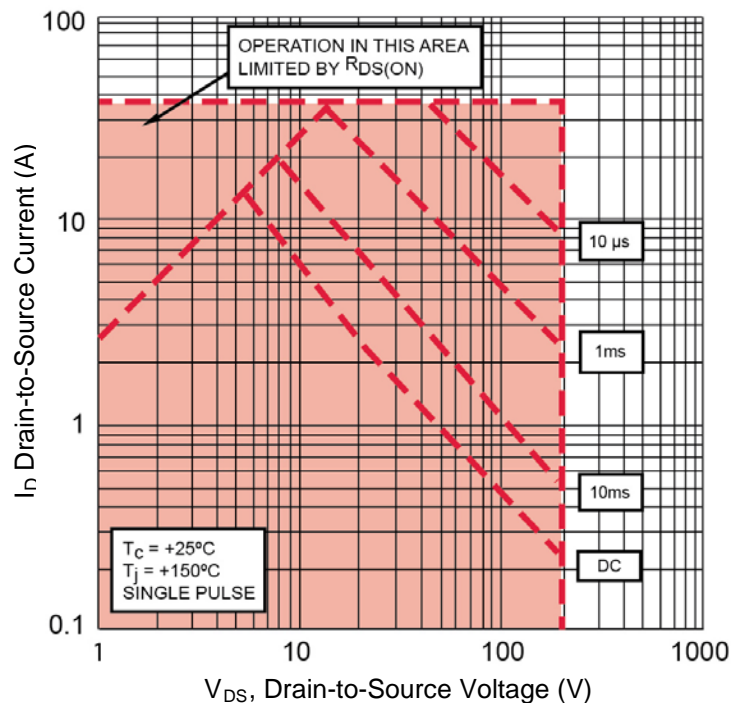
**SWITCHING CHARACTERISTICS**

Parameters / Test Conditions	Symbol	Min.	Max.	Unit
Turn-on delay time $I_D = 9.4\text{ A}, V_{GS} = 12\text{ V}, R_G = 7.5\text{ }\Omega, V_{DD} = 100\text{ V}$	$t_{d(on)}$		25	ns
Rise time $I_D = 9.4\text{ A}, V_{GS} = 12\text{ V}, R_G = 7.5\text{ }\Omega, V_{DD} = 100\text{ V}$	$t_r$		50	ns
Turn-off delay time $I_D = 9.4\text{ A}, V_{GS} = 12\text{ V}, R_G = 7.5\text{ }\Omega, V_{DD} = 100\text{ V}$	$t_{d(off)}$		70	ns
Fall time $I_D = 9.4\text{ A}, V_{GS} = 12\text{ V}, R_G = 7.5\text{ }\Omega, V_{DD} = 100\text{ V}$	$t_f$		60	ns
Diode Reverse Recovery Time $di/dt \leq 100\text{ A}/\mu\text{s}, V_{DD} \leq 50\text{ V}, I_F = 9.4\text{ A}$	$t_{rr}$		460	ns

**ELECTRICAL CHARACTERISTICS @  $T_A = +25\text{ }^\circ\text{C}$ , unless otherwise noted (continued)**
**POST-IRRADIATION <sup>(1)</sup>**

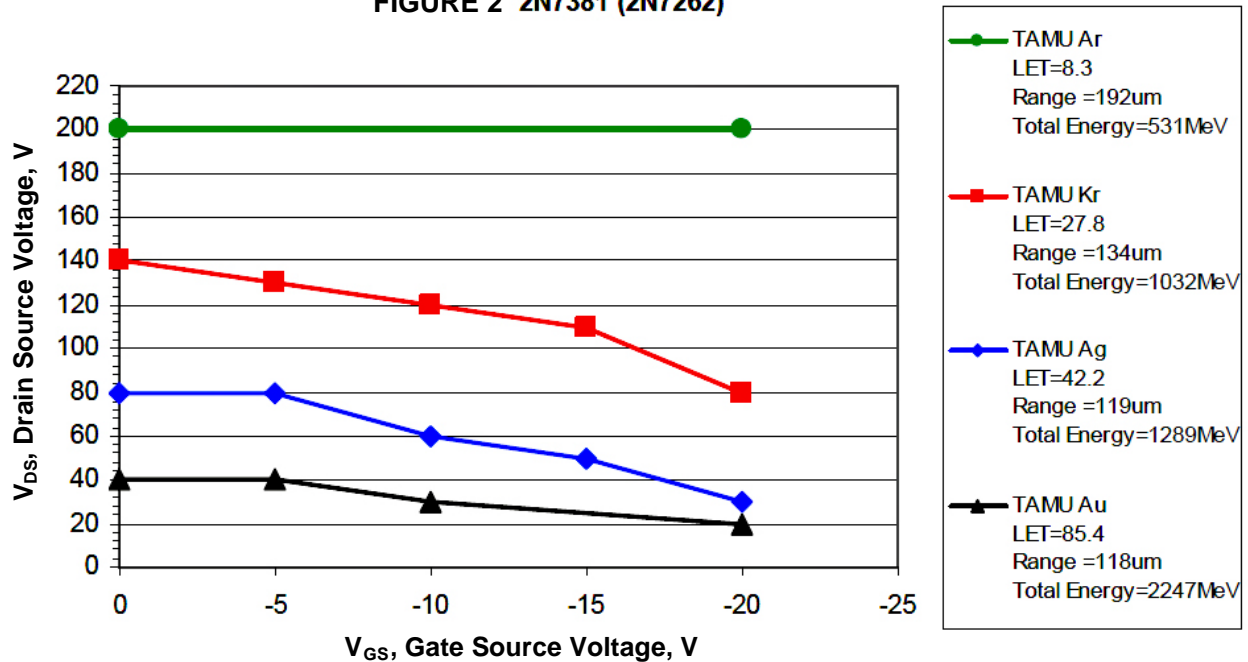
Parameters / Test Conditions	Symbol	Min.	Max.	Unit
Drain-Source Breakdown Voltage $V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	$V_{(BR)DSS}$	200		V
Gate-Source Voltage (Threshold) $V_{DS} \geq V_{GS}, I_D = 1.0\text{ mA}$ JANS D, R $V_{DS} \geq V_{GS}, I_D = 1.0\text{ mA}$ JANS F	$V_{GS(th)1}$ $V_{GS(th)1}$	2.0 1.25	4.0 4.5	V
Gate Current $V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$	$I_{GSS1}$		$\pm 100$	nA
Drain Current $V_{GS} = 0\text{ V}, V_{DS} = 80\%$ of $V_{DS}$ (pre-irradiated) JANS D, R $V_{GS} = 0\text{ V}, V_{DS} = 80\%$ of $V_{DS}$ (pre-irradiated) JANS F	$I_{DSS1}$		25 50	$\mu\text{A}$
Static Drain-Source On-State Voltage $V_{GS} = 12\text{ V}, I_D = 6.0\text{ pulsed}$ JANS D, R $V_{GS} = 12\text{ V}, I_D = 6.0\text{ pulsed}$ JANS F	$r_{DS(on)}$		2.4 3.18	V
Diode Forward Voltage $V_{GS} = 0\text{ V}, I_D = 9.4\text{ pulsed}$	$V_{SD}$		1.4	V

**NOTE:** 1. Post-irradiation electrical characteristics apply to devices subjected to steady state total dose irradiation testing in accordance with MIL-STD-750, method 1019. Separate samples are tested for  $V_{GS}$  bias (12V), and  $V_{DS}$  bias (160V) conditions.

**SAFE OPERATING AREA**

**FIGURE 1**

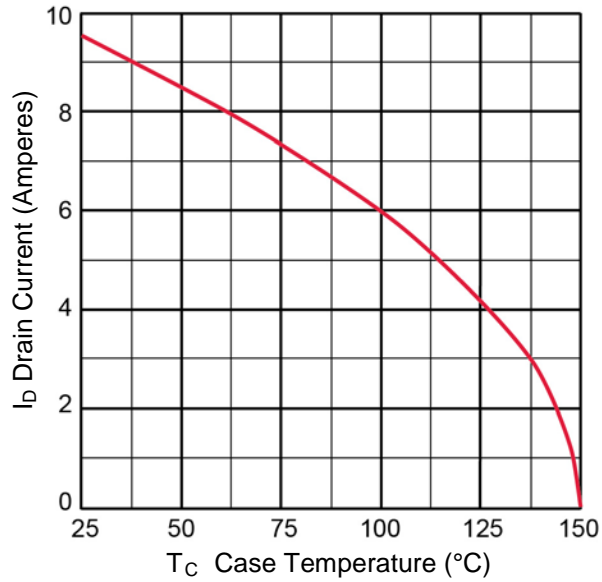
**GRAPHS**
**SEE (Single Event Effect) Typical Response:**

Heavy Ion testing of the 2N7381 device was completed by similarity of die structure to the 2N7262. The 2N7262 has been characterized at the Texas A&M cyclotron. The following SEE curve has been established using the elements, LET, range, and Total Energy conditions as shown:

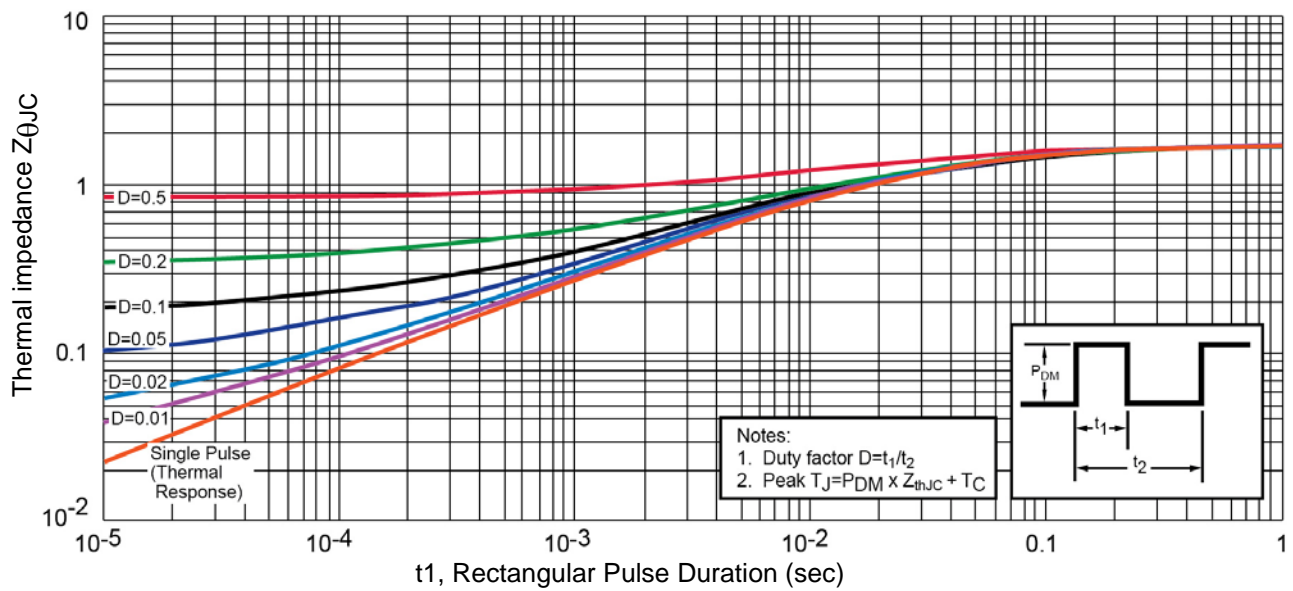
**FIGURE 2 2N7381 (2N7262)**


It should be noted that total energy levels are considered to be a factor in SEE characterization. Comparisons to other datasets should not be based on LET alone. Please consult factory for more information.

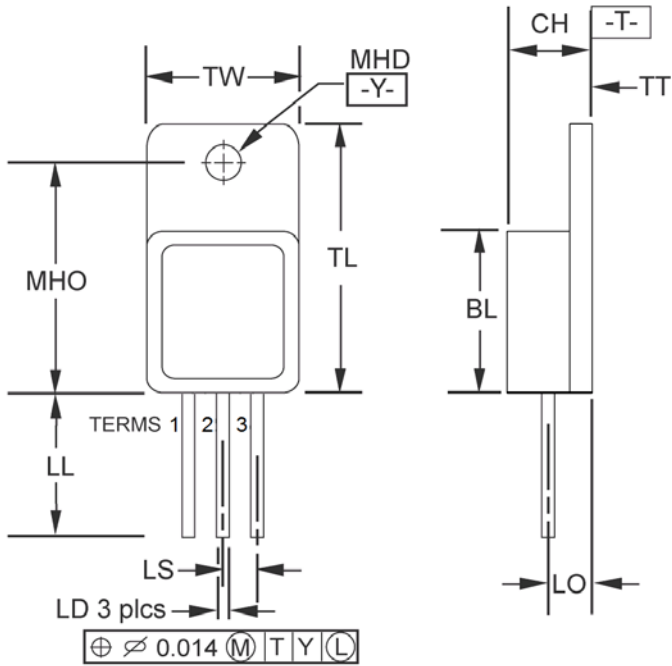
GRAPHS



**FIGURE 3**  
Maximum Drain Current vs Case Temperature



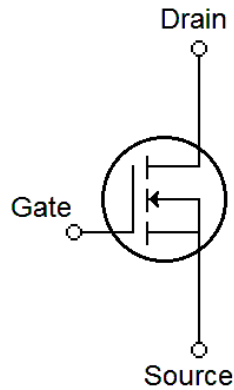
**FIGURE 4**  
Thermal Impedance Curves

**PACKAGE DIMENSIONS**


Ltr	Dimensions			
	Inch		Millimeters	
	Min	Max	Min	Max
BL	0.410	0.430	10.41	10.92
CH	0.190	0.200	4.83	5.08
LD	0.025	0.035	0.64	0.89
LL	0.505	0.595	12.82	15.11
LO	0.120 BSC		3.05 BSC	
LS	0.100 BSC		2.54 BSC	
MHD	0.140	0.150	3.56	3.81
MHO	0.527	0.537	13.39	13.64
TL	0.645	0.665	16.38	16.89
TT	0.035	0.045	0.89	1.14
TW	0.410	0.420	10.41	10.67
TERM 1	DRAIN			
TERM 2	SOURCE			
TERM 3	GATE			

**NOTES:**

1. Dimensions are in inches.
2. Millimeter equivalents are given for information only.
3. Glass meniscus included in dimension TL and BL.

**SCHEMATIC**


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