

3 ch DC/DC for TFT LCD for Automotive Applications

NO.EC-154-141119

OUTLINE

The R1290K is the optimized DC/DC converter IC for TFT LCD displays. R1290K contains one PWM step-up DC/DC converter controller and two diode charge-pump controllers. The charge-pumps can control a boost output and a negative output and have the output voltage regulation function with external resistors. The power-on sequence can be made with setting the delay time with external capacitors for each charge pump channel.

FEATURES

- Temperature Coefficient of VFB (ΔV_{FB}/ΔT) ········· Typ. ±150 ppm/°C (−40°C ≤ Ta ≤ 105°C)
- Temperature Coefficient of VREF (ΔV_{REF}/ΔT)······ Typ. 150 ppm/°C
- Temperature Coefficient of CPPFB (ΔV_{PFB}/ΔT)······ Typ.150 ppm/°C (−40°C ≤ Ta ≤ 105°C, CPVCC=9 V)

[Step-up DC/DC Controller]

- Built-in 2 A Nch-switch ($R_{ON} = 150 \text{ m}\Omega \text{ Typ.}$)
- Overcurrent Protection
- Adjustable V_{OUT} up to 20 V with external resistors
- Adjustable Phase compensation with external components
- Maxduty adjustable with external resistors for DTC pin
- Soft-start time adjustable with external capacitor for SS pin
- Oscillator Frequency: Adjustable frequency with resistors (180 kHz to 1400 kHz)

[Charge-pump]

- Adjustable output voltage with external resistors
- Sequence function: Charge-pump turns on after the main step-up converter voltage outputs. The positive charge-pump and the negative charge-pump turn-on sequence control is adjustable by setting delay time for each channel
- Oscillator Frequency: 1/4 of the main step-up DC/DC converter oscillator frequency

[Controller]

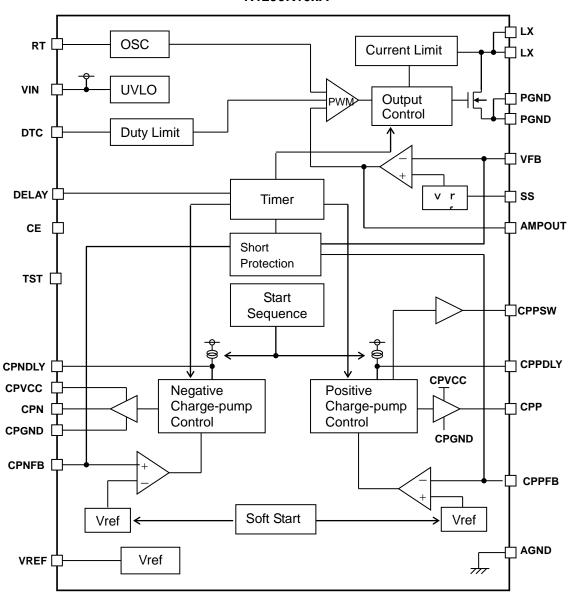
- Under Voltage Lock-Out (UVLO: selectable detector threshold from 1.8 V/2.2 V/2.8 V)
- Reference Voltage (VREF: Typ.1.2 V)
- Short Protection with timer latch function (adjustable delay time with external capacitor)
- Shutdown all the outputs if at least one of three outputs is shorted to the GND.
- Stand-by function by CE pin
- Package Thin 24-pin package QFN0404-24

APPLICATIONS

Power source for LCD and CCD

BLOCK DIAGRAM

R1290K10xA



SELECTION GUIDE

The UVLO threshold voltage is user-selectable.

Product Name	Package	Quantity per Reel	Pb Free	Halogen Free
R1290K10xA -E2-#E	QFN0404-24	1,000 pcs	Yes	Yes

x: Specify the UVLO threshold voltage

1: 1.8 V

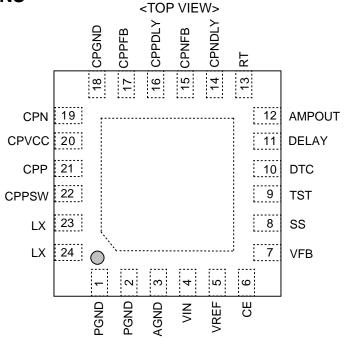
2: 2.2 V

3: 2.8 V

#: Specify the Automotive Class Code

	Operating Temperature Range	Guaranteed Specs Temperature Range	Screening
Α	-40°C to 105°C	25°C	High Temperature

PIN DESCRIPTIONS



Pin No.	Symbol	Description	
1	PGND	Power GND Pin	
2	PGND	Power GND Pin	
3	AGND	Analog GND Pin	
4	VIN	Power Input Pin	
5	VREF	Reference Voltage Output Pin	
6	CE	Chip Enable Pin	
7	VFB	Step-up DC/DC Feedback Pin	
8	SS	Step-up DC/DC Soft-start Pin	
9	TST	TEST Pin	
10	DTC	Step-up DC/DC Maxduty Setting Pin	
11	DELAY	Short Protection Delay Setting Pin	
12	AMPOUT	Amplifier Output Pin For Phase Compensation	
13	RT	Oscillator Frequency Setting Pin	
14	CPNDLY	Negative Charge-pump Delay Setting Pin	
15	CPNFB	Negative Charge-pump Feedback Pin	
16	CPPDLY	Positive Charge-pump Delay Setting Pin	
17	CPPFB	Positive Charge-pump Feedback Pin	
18	CPGND	Charge-pump GND Pin	
19	CPN	Negative Charge-pump Driver Output Pin	
20	CPVCC	Power Pin for Charge-pump	
21	CPP	Positive Charge-pump Driver Output Pin	
22	CPPSW	Output Control Pin for Positive Charge-pump	
23	LX	Step-up DC/DC Driver Output Pin	
24	LX	Step-up DC/DC Driver Output Pin	

^{*} The tab on the bottom of the package enhances thermal performance and is electrically connected to GND (substrate level). It is recommended that the tab be connected to the ground plane on the board, or otherwise be left floating.

ABSOLUTE MAXMUM RATINGS

Symbol	Item		Ratings	Unit
Vin	V _{IN} pin voltage		6.5	V
V _{DTC}	DCT pin voltage		-0.3 to V _{IN} +0.3	V
V _{FB}	V _{FB} pin voltage		-0.3 to V _{IN} +0.3	V
V _{SS}	SS pin voltage		-0.3 to V _{IN} +0.3	V
V _{DELAY}	DELAY pin voltage		-0.3 to V _{IN} +0.3	V
V _{AMP}	AMPOUT pin voltage		-0.3 to V _{IN} +0.3	V
V _{LX}	Lx pin voltage		-0.3 to 24	V
I _L X	Lx pin current		Internally limited	А
V _{REF}	V _{REF} pin voltage		-0.3 to V _{IN} +0.3	V
Vcpvcc	CPVCC pin voltage	CPVCC pin voltage		V
V _{CE}	CE pin voltage		-0.3 to V _{IN} +0.3	V
V _{RT}	RT pin voltage	RT pin voltage		V
V _{CPPDLY}	CPPDLY pin voltage	CPPDLY pin voltage		V
VCPNDLY	CPNDLY pin voltage	CPNDLY pin voltage		V
V _{PFB}	CPPFB pin voltage	CPPFB pin voltage		V
V _{NFB}	CPNFB pin voltage		-0.3 to V _{IN} +0.3	V
V _{CPP}	CPP pin voltage		-0.3 to 24	V
V _{CPN}	CPN pin voltage		-0.3 to 24	V
V _{PSW}	CPPSW pin voltage		-0.3 to 24	V
I _{PSW}	CPPSW pin current-A		20	mA
	D	Standard Land Pattern - A	670	
P _D	Power dissipation (QFN0404-24) *	Standard Land Pattern - B	800	W
	(Q1 110404-24)	Standard Land Pattern - C	1500	
Tj	Junction Temperature		125	°C
Tstg	Storage temperature	Storage temperature range		°C

^{*} Refer to PACKAGE INFORMATION for detailed information.

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause the permanent damages and may degrade the lifetime and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings are not assured.

NO.EC-154-141119

RECOMMENDED OPERATING CONDITIONS

Symbol	Iter	Item		Unit
		R1290K101A	2.0 to 5.5	V
V_{IN}	V _{IN} Input voltage	R1290K102A	2.5 to 5.5	V
		R1290K103A	3.3 to 5.5	V
CPVCC	CPVCC operating voltage		6 to 20	V
Та	Operating temperature		-40 to 105	°C

RECOMMENDED OPERATING CONDITIONS

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if when they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

ELECTRICAL CHARACTERISTICS

 V_{IN} is set as shown below for every version, unless otherwise noted.

R1290K101A: $V_{IN} = 2.5 \text{ V}$ R1290K102A: $V_{IN} = 2.5 \text{ V}$ R1290K103A: $V_{IN} = 3.5 \text{ V}$

The specifications surrounded by are guaranteed by design engineering at −40°C ≤ Ta ≤ 105°C

R1290KxxA (-AE) $(Ta = 25^{\circ}C)$

Symbol	Item		Conditions	Min.	Тур.	Max.	Unit
I _{IN}	V _{IN} Supply Current	V _{IN} =5.5 V, R	RT=24 kΩ		3.5		mA
		R1290K101A		1.69	1.8	1.91	V
V _{UVLO1}	UVLO Detect Voltage (V _{IN} Falling)	R1290K102	A	2.05	2.2	2.35	V
	(VIN Failing)	R1290K103	A	2.6	2.8	3.0	V
		R1290K101	A		V _{UVLO1} +0.09	2.0	V
V _{UVLO2}	UVLO Release Voltage (V _{IN} Rising)	R1290K102	A		V _{UVLO1} +0.15	2.5	V
		R1290K103	A		V _{UVLO1} +0.22	3.2	V
V _{FB}	V _{FB} Voltage			0.960	1.0	1.025	V
V _{FBL}	V _{FB} "L" Output Voltage				V _{FB} ×0.85		V
I _{FB}	V _{FB} Input Current	V _{IN} = 5.5 V,	V _{FB} = 0 V or 5.5 V	-0.1		0.1	μА
V _{DTC0}	Duty = 0% DTC Voltage	RT = 24 kΩ		0.27	0.37	0.49	V
V _{DTC20}	Duty = 20% DTC Voltage	RT = 24 kΩ			0.49		٧
V _{DTC80}	Duty = 80% DTC Voltage	RT = 24 kΩ			0.91		V
Maxduty	Maximum Duty Limit	RT = 24 kΩ,	, V _{DTC} = V _{IN}	84	91	98	%
	AMD "I I" Output Compant	\/ 0.0\/	R1290K101A/102A	1.4	3.2	5.8	mA
Іамрн	AMP "H" Output Current	$V_{FB} = 0.9 V$	R1290K103A	4.7		14.5	mA
I _{AMPL}	AMP "L" Output Current	V _{FB} = 1.1 V		30	80	135	μΑ
Ron	Switch ON Resistance				150		mΩ
I _{LXOFF}	Leakage Current	V _{IN} = 5.5 V, V _{LX} = 20 V				5	μΑ
I _{LIMDC}	Switch Limit Current			1.3			Α
		RT = 110 kΩ		100	180	260	kHz
f _{REQ}	f _{REQ} Oscillator Frequency			600	700	830	kHz
		RT = 10 kΩ		1.2	1.4	1.6	MHz
V_{REF}	V _{REF} Voltage			1.16	1.2	1.23	V
Іоит	V _{REF} Current			2.0			mA

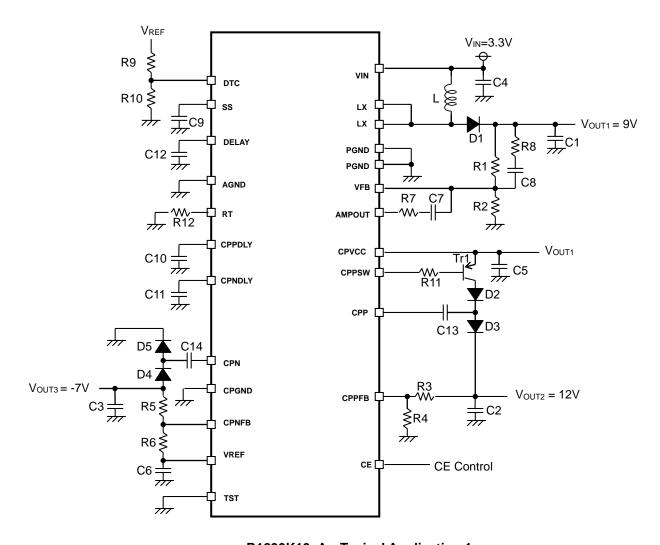
R1290K

NO.EC-154-141119

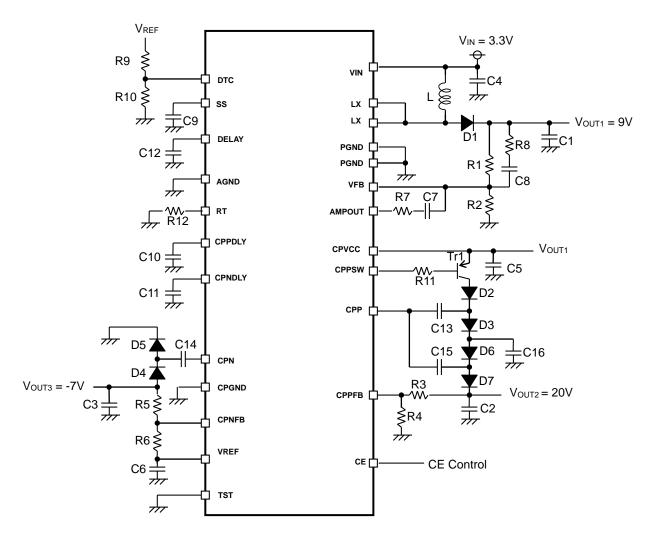
Symbol	Item	Conditions	Min.	Тур.	Max.	Unit
		R1290K101A V _{IN} = 2.0 to 5.5 V				
ΔV _{REF} /ΔV _{IN}	V _{REF} Line Regulation	R1290K102A V _{IN} = 2.5 to 5.5 V		5	15	mV
/ Δ V IIV		R1290K103A V _{IN} = 3.3 to 5.5 V				
$\Delta V_{REF}/\Delta I_{OUT}$	V _{REF} Load Regulation	I _{OUT} = 0.1 mA to 2.0 mA		6	25	mV
Ішм	Short Current Limit			15		mA
ICPVCC	CPVCC Supply Current	CPVCC = 9 V, RT = 24 k Ω		500		μΑ
Iss	Soft-Start Current	CPVCC = 9 V	2.5	5.0	7.5	μΑ
tpss	CPP Soft-Start Time	CPVCC = 9 V		4.0		ms
t _{NSS}	CPN Soft-Start Time	CPVCC = 9 V		4.0		ms
IPDLY	CPPDLY Charge Current	CPVCC = 9 V	2.5	5.0	7.5	μΑ
I _{NDLY}	CPNDLY Charge Current	CPVCC = 9 V	2.5	5.0	7.5	μΑ
V _{PDLY}	CPPDLY Detector Threshold	CPVCC = 9 V	0.95	1.00	1.05	V
V _{NDLY}	CPNDLY Detector Threshold	CPVCC = 9 V	0.95	1.00	1.05	V
V _{PFB}	CPPFB Voltage	CPVCC = 9 V	1.45	1.500	1.535	V
V _{NFB}	CPNFB Voltage	CPVCC = 9 V	-0.035	0.00	0.035	V
V_{PFBL}	CPPFB Fault Voltage	CPVCC = 9 V		V _{PFB} ×0.85		V
V_{NFBL}	CPNFB Fault Voltage	CPVCC = 9 V		0.15		V
Rcpph	CPP "H" ON Resistance	CPVCC = 9 V		5		Ω
RCPPL	CPP "L" ON Resistance	CPVCC = 9 V		10		Ω
RCPNH	CPN "H" ON Resistance	CPVCC = 9 V		5		Ω
RCPNL	CPN "L" ON Resistance	CPVCC = 9 V		10		Ω
freqcp	Charge-pump Frequency	CPVCC = 9 V		f _{REQ} /4		kHz
I _{DELAY1}	DELAY Charge Current	CPVCC = 9 V	2.4	5.0	7.5	μΑ
I _{DELAY2}	DELAY Discharge Current	CPVCC = 9 V		200		μΑ
V _{DELAY}	DELAY Detector Threshold	CPVCC = 9 V	0.94	1.0	1.06	V
V _{PSW}	CPPSW "L" Output Voltage	CPVCC = 9 V, I = 1 mA		0.2		V
Istandby1	Standby Current			0.1	5	μΑ
Istandby2	CPVCC Standby Current			0.1	5	μΑ
V _{CEL}	CE "L" Input Voltage				0.3	V
Vceн	CE "H" Input Voltage	V _{IN} = 5.5 V	1.5			V

All test items listed under Electrical Characteristics are done under the pulse load condition (Tj ≈ Ta = 25°C).

TYPICAL APPLICATION



R1290K10xA Typical Application 1



R1290K10xA Typical Application 2

Recommended External Components

Symbol	Description
1	NR4018T220M (for 180 kHz) / NR4018T4R7M (for 700 kHz) /
-	NR4018T2R2M (for 1.4 MHz), Taiyo Yuden
D1	CRS02, TOSHIBA
D2-D7	1SS374, TOSHIBA
Tr1	2SA1586, TOSHIBA

TECHNICAL NOTES

How to Set the Step-up Converter Output Voltage

 V_{OUT1} of the step-up converter controls the voltage of V_{FB} pin, which should be V_{FB} = 1.0 V. It is possible to set V_{OUT1} voltage according to the following formula of R1 and R2 (refer to the *Typical Application*). V_{OUT1} voltage should be equal to or lower than 20 V. R1 + R2 should be equal to or lower than 500 k Ω .

$$V_{OUT1} = V_{FB} \times (R1 + R2) / R2$$

How to Set the Step-up Charge-pump Output Voltage

 V_{OUT2} of the positive charge pump controls the voltage of C_{PPFB} pin, which should be V_{PFB} = 1.5 V. It is possible to set V_{OUT2} voltage according to the following formula of R3 and R4 (refer to the *Typical Application*). R3 + R4 should be equal to or less than 500 k Ω .

$$V_{OUT2} = V_{PFB} \times (R3 + R4) / R4$$

In the case of *Typical Application 1*, the maximum output voltage can be described as the following formula.

$$V_{OUT2}$$
 (Max.) = CPVCC \times 2 - $V_F \times$ 2 (V_F is the forward voltage for the diodes D2-D3)

Set C15, D6 and D7 of diodes, and C16 (refer to the *Typical Application 2*) if the output voltage needs more than the range above. In this case, the maximum output voltage can be described as the following formula.

$$V_{OUT2}$$
 (Max.) = CPVCC \times 3 - $V_F \times$ 4 (V_F is the forward voltage for diodes D2-D3, D6-D7)

The maximum load current of the boost charge pump is determined by Cfly (C13, C15), the oscillator frequency of charge pump (frequency), and CPP "L" On Resistance (RCPPL) as described in the following formula.

$$I_{OUT2} \text{ (Max.)} = Cfly \times (1 - exp (-1 / (2 \times Cfly \times R_{CPPL} \times f_{REQCP}))) \times (CPVCC \times 2 - V_{OUT2} - V_F \times 2) \times f_{REQCP} \times (1 - exp (-1 / (2 \times Cfly \times R_{CPPL} \times f_{REQCP}))) \times (CPVCC \times 2 - V_{OUT2} - V_F \times 2) \times f_{REQCP} \times (1 - exp (-1 / (2 \times Cfly \times R_{CPPL} \times f_{REQCP}))) \times (CPVCC \times 2 - V_{OUT2} - V_F \times 2) \times f_{REQCP} \times (1 - exp (-1 / (2 \times Cfly \times R_{CPPL} \times f_{REQCP}))) \times (CPVCC \times 2 - V_{OUT2} - V_F \times 2) \times f_{REQCP} \times (1 - exp (-1 / (2 \times Cfly \times R_{CPPL} \times f_{REQCP}))) \times (CPVCC \times 2 - V_{OUT2} - V_F \times 2) \times f_{REQCP} \times (1 - exp (-1 / (2 \times Cfly \times R_{CPPL} \times f_{REQCP}))) \times (CPVCC \times 2 - V_{OUT2} - V_F \times 2) \times f_{REQCP} \times (1 - exp (-1 / (2 \times Cfly \times R_{CPPL} \times f_{REQCP}))) \times (CPVCC \times 2 - V_{OUT2} - V_F \times 2) \times f_{REQCP} \times (1 - exp (-1 / (2 \times Cfly \times R_{CPPL} \times f_{REQCP}))) \times (CPVCC \times 2 - V_{OUT2} - V_F \times 2) \times f_{REQCP} \times (1 - exp (-1 / (2 \times Cfly \times R_{CPPL} \times f_{REQCP}))) \times (CPVCC \times 2 - V_{OUT2} - V_F \times 2) \times f_{REQCP} \times (1 - exp (-1 / (2 \times Cfly \times R_{CPPL} \times f_{REQCP}))) \times (CPVCC \times 2 - V_{OUT2} - V_F \times 2) \times f_{REQCP} \times (1 - exp (-1 / (2 \times Cfly \times R_{CPPL} \times f_{REQCP}))) \times (CPVCC \times 2 - V_{OUT2} - V_F \times 2) \times f_{REQCP} \times (1 - exp (-1 / (2 \times Cfly \times R_{CPPL} \times f_{REQCP}))) \times (CPVCC \times 2 - V_{OUT2} - V_F \times 2) \times f_{REQCP} \times (1 - exp (-1 / (2 \times Cfly \times R_{CPPL} \times f_{REQCP}))) \times (CPVCC \times 2 - V_{OUT2} - V_F \times 2) \times f_{REQCP} \times (1 - exp (-1 / (2 \times Cfly \times R_{CPPL} \times f_{REQCP} \times f_{REQCP}))) \times (CPVCC \times 2 - V_{OUT2} - V_F \times 2) \times f_{REQCP} \times (1 - exp (-1 / (2 \times Cfly \times R_{CPPL} \times f_{REQCP} \times f_{REQCP})))$$

How to Set the Inverting Charge-pump Output Voltage

 V_{OUT3} of the inverting charge-pump controls the voltage of C_{PNFB} pin, which should be $V_{NFB} = 0$ V. It is possible to set V_{OUT3} voltage by the following formula by R5 and R6 that are between V_{REF} pin and V_{OUT3} (refer to the *Typical Application*). R5 + R6 should be equal to or less than 500 k Ω

$$V_{OUT3} = V_{NFB} - (V_{REF} - V_{NFB}) \times R5 / R6$$

The minimum output voltage can be set by the following formula.

$$V_{OUT3}$$
 (Min.) = - (CPVCC - $V_F \times 2$) (V_F is the forward voltage of the diode D4 and D5)

The maximum load current of inverting charge pump is determined by Cfly (C14), the oscillator frequency of charge pump (frequency), and CPN "L" ON Resistance (RCPNL) as described in the following formula.

$$louts (Max.) = Cfly \times (1 - exp (-1 / (2 \times Cfly \times R_{CPNL} \times f_{REQCP}))) \times (CPVCC + V_{OUT3} - V_F \times 2) \times f_{REQCP} \times (1 - exp (-1 / (2 \times Cfly \times R_{CPNL} \times f_{REQCP})))) \times (CPVCC + V_{OUT3} - V_F \times 2) \times f_{REQCP} \times (1 - exp (-1 / (2 \times Cfly \times R_{CPNL} \times f_{REQCP})))) \times (CPVCC + V_{OUT3} - V_F \times 2) \times f_{REQCP} \times (1 - exp (-1 / (2 \times Cfly \times R_{CPNL} \times f_{REQCP})))) \times (CPVCC + V_{OUT3} - V_F \times 2) \times f_{REQCP} \times (1 - exp (-1 / (2 \times Cfly \times R_{CPNL} \times f_{REQCP})))) \times (CPVCC + V_{OUT3} - V_F \times 2) \times f_{REQCP} \times (1 - exp (-1 / (2 \times Cfly \times R_{CPNL} \times f_{REQCP})))) \times (CPVCC + V_{OUT3} - V_F \times 2) \times f_{REQCP} \times (1 - exp (-1 / (2 \times Cfly \times R_{CPNL} \times f_{REQCP})))) \times (CPVCC + V_{OUT3} - V_F \times 2) \times f_{REQCP} \times (1 - exp (-1 / (2 \times Cfly \times R_{CPNL} \times f_{REQCP})))) \times (CPVCC + V_{OUT3} - V_F \times 2) \times f_{REQCP} \times (1 - exp (-1 / (2 \times Cfly \times R_{CPNL} \times f_{REQCP})))) \times (CPVCC + V_{OUT3} - V_F \times 2) \times f_{REQCP} \times (1 - exp (-1 / (2 \times Cfly \times R_{CPNL} \times f_{REQCP})))) \times (CPVCC + V_{OUT3} - V_F \times 2) \times f_{REQCP} \times (1 - exp (-1 / (2 \times Cfly \times R_{CPNL} \times f_{REQCP})))) \times (CPVCC + V_{OUT3} - V_F \times 2) \times f_{REQCP} \times (1 - exp (-1 / (2 \times Cfly \times R_{CPNL} \times f_{REQCP})))) \times (CPVCC + V_{OUT3} - V_F \times 2) \times f_{REQCP} \times (1 - exp (-1 / (2 \times Cfly \times R_{CPNL} \times f_{REQCP})))) \times (CPVCC + V_{OUT3} - V_F \times 2) \times f_{REQCP} \times (1 - exp (-1 / (2 \times Cfly \times R_{CPNL} \times f_{REQCP})))) \times (CPVCC + V_{OUT3} - V_F \times 2) \times f_{REQCP} \times (1 - exp (-1 / (2 \times Cfly \times R_{CPNL} \times f_{REQCP})))) \times (CPVCC + V_{OUT3} - V_F \times 2) \times f_{REQCP} \times (1 - exp (-1 / (2 \times Cfly \times R_{CPNL} \times f_{REQCP})))) \times (CPVCC + V_{OUT3} - V_F \times 2) \times f_{REQCP} \times (1 - exp (-1 / (2 \times Cfly \times R_{CPNL} \times f_{REQCP})))) \times (CPVCC + V_{OUT3} - V_F \times 2) \times f_{REQCP} \times (1 - exp (-1 / (2 \times Cfly \times R_{CPNL} \times f_{REQCP})))) \times (CPVCC + V_{OUT3} - V_F \times 2) \times f_{REQCP} \times (1 - exp (-1 / (2 \times Cfly \times R_{CPNL} \times f_{REQCP}))))$$

R1290K

NO.EC-154-141119

How to set the Step-up DC/DC Converter's Phase Compensation (Refer to Typical Application)

In the DC/DC converter, with the load current and the external components (L and C) the phase may be delayed by 180 degrees. Due to this, the phase margin of system is lost and stability would be worse. Thus, it is necessary to proceed the phase, and keep a certain phase margin.

The phase compensation and the system gain can be set with using the resistor, R7 and capacitors, C7 and C8. The position and the setting values shown in the *Typical Application* are one of the examples.

Select R7 and C7, so that the cut-off frequency of this Zero point may become approximately the cutoff frequency of pole made by the external components (L and C). The following formula shows the pole made by the external components (L and C) and the "Zero" point.

Fpole ~ 1 /
$$\{2 \times \pi \times \sqrt{(L \times C1)}\}$$

Fzero ~
$$1/(2 \times \pi \times R7 \times C7)$$

For example, when L = 10 μ H and Cout (C1) = 10 μ F, the cut-off frequency of the pole is approximately 16 kHz. Then set the cut-off frequency of the Zero point around 16 kHz. In this case, R7 = 4.7 k Ω and C7 = 2200 pF.

The gain can be set with the ratio of the resistance of R7 and combined resistance of R1 and R2 (RT: $RT = R1 \times R2/(R1 + R2)$). If R7 is larger than the combined resistance (RT), the gain becomes high. If the gain is too high, the characteristics of response will be improved but the operating stability will be worse. Set R7 with an appropriate value.

Due to the R1 setting in the gain setting, another Zero point is set by R1 and C7.Set this cut-off frequency of Zero point at the lower frequency than the cut-off frequency by pole made by the external components (L and C). This Zero point is shown in the formula below.

Fzero ~
$$1/(2 \times \pi \times R1 \times C8)$$

Noise Reduction of the Feedback Voltage (Refer to Typical Application)

When the system noise is large, the output noise may be on to the feedback loop, and the operation may become unstable. In this case, set the value of the resistance R1 to R6 low and make the noise into the feedback reduction. It is possible to reduce the noise to the V_{FB} pin by connecting the resistance in the range from 1 k Ω to 5 k Ω around as R8.

Input Voltage

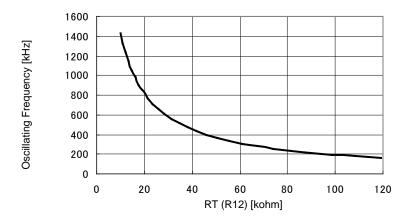
The range of V_{IN} voltage must be between 2.0 V and 5.5 V. For CPVCC pin, it is possible to use input V_{OUT1} or input another voltage of 6 V to 20 V to CPVCC as a power supply. In that case, set a capacitor of 1.0 μ F or more as C16 between GND and CPVCC pin.

How to Set the Oscillator Frequency

Set a resistor (R12) between GND and RT pin. The oscillator frequency of the step-up converter (frequency can be set according to the next formula. This value depends upon the resistance value.

$$f_{REQ} = 2.7 \times 10^{10} / [R12 \times \{0.66 + \sqrt{(0.66^2 + 10800 / R12)}\}]$$

Set the frequency between 180 kHz and 1400 kHz. The oscillator frequency of the charge-pump is one fourth of the oscillator frequency of the main step-up DC/DC converter.



How to Set the Soft-start of Step-up Converter (Refer to the Timing Chart)

The soft-start of the step-up converter operates when V_{IN} is equal to or more than the UVLO release voltage, or when CE signal is "H". External capacitor of SS pin (C9) is charged with the soft-start charge current (I_{SS}). Then the voltage of SS pin is input to the error amplifier as the reference voltage. When the voltage of SS pin reaches to the reference voltage (Typ.1.0 V) in the normal state, the reference voltage of the error amplifier stabilized at 1.0 V, and it changes to the normal state. The soft-start of step-up converter time (I_{SS}) is set by the external capacitor (C9) for the SS pin in the next formula.

$$t_{SS} = C9 \times V_{FB} / I_{SS}$$

How to Set the Start-up Sequence (Refer to the Timing Chart)

When the output voltage of step-up converter is up to 85% of a set value, and the soft-start is finished, the external capacitors (C10 and C11) of the CPPDLY pin and the CPNDLY pin are charged by the CPPDLY charge current (Indly) and the CPNDLY charge current (Indly). When the voltage of the CPPDLY pin and the CPNDLY pin charged up to the CPPDLY detector threshold (VpDLY) and the CPNDLY detector threshold (VnDLY), then the soft-start of the positive charge-pump and the negative charge-pump is operated respectively. After the step-up converter is operated, the delay time (tpDLY and tnDLY) until the soft-start of charge-pump is set by the external capacitors (C10 and C11) of the CPPDLY pin and the CPNDLY pin. The delay time is set by the following formula.

The delay time until the soft-start of positive charge-pump operates: $t_{PDLY} = C10 \times V_{PDLY} / I_{PDLY}$ The delay time until the soft-start of negative charge-pump operates: $t_{NDLY} = C11 \times V_{NDLY} / I_{NDLY}$

Thus, after the main step-up DC/DC converter starts operating, the positive charge-pump and the negative charge-pump can be operated by the arbitrary order.

R1290K

NO.EC-154-141119

Soft-start of the Charge-pump (Refer to Typical Application and Timing Chart)

When the soft-start of boost charge-pump operates, the output of CPPSW changes from "H" to "L". Setting the PNP-Tr1 (Tr1) keeps $V_{OUT2} = 0$ V until the positive charge-pump is started. If it is not required to keep $V_{OUT2} = 0$ V, then PNP-Tr1 is unnecessary. In this case, V_{OUT2} outputs approximately the same voltage as V_{OUT1} . Arrange the resistor (R11) between the CPPSW pin and the base of PNP-Tr1 (Tr1). The maximum current of Tr1 can be set by the R11 value. This value can be calculated in the next formula.

Imax = hFE \times (V_{OUT1} - V_{BE}) / R11 ······[hFE is DC current gain of Tr1 and V_{BE} is base emitter voltage of Tr1.]

Select the appropriate value for R11 since the efficiency gets worse if the value is too small (refer to the *Short Current Protection* section. PNP-Tr1 has some effect on the operation of the short-current protection).

When the positive charge-pump starts, the reference voltage of the error amplifier starts from 0 V, turns on to the reference voltage (= 1.5 V) and becomes stable. Thus, the output voltage of V_{OUT2} can turn on by set output voltage within the time period of soft-start time.

Before the soft-start of the negative charge-pump starts, the reference voltage of the error amplifier rises to V_{REF} voltage (= 1.2 V) and falls down to 0 V in the soft start time fixed internally by the soft-start operation. Thus, the output voltage of V_{OUT3} can turn on by set output voltage within the time period of soft-start time.

How to set the Short Current Protection and Timer Latch Delay Time

If any output among the step-up converter output, the positive charge-pump output or the negative charge-pump output falls, the R1290K detects the short circuit. If this short circuit condition stays for a certain time, the latch-type protection circuit shuts down all the switching outputs (Lx, CPP, CPN) and outputs "H" through the CPPSW pin. Even if the switching stopped, the current path from CPVCC to V_{OUT2} is remained. If PNP-Tr is set on the CPPSW pin, the current path to V_{OUT2} is cut off after shutdown.

The detect voltages of V_{FB}, CPPFB and CPNFB are:

85% of predetermined V_{FB} voltage for V_{FB}

85% of predetermined CPPFB voltage for CPPFB

+ 0.15 V for CPNFB

The latch timer delay is set by an external capacitor (C12) of the DELAY pin. This delay time can be calculated by the next formula.

$$t_{DLY} = C12 \times V_{DLY} / I_{DLY}$$

To release the latch state, set V_{IN} voltage below UVLO detector threshold and restart, or Set the CE pin "L" once and change the CE pin to "H" level.

How to set the Maxduty Limit

The value of maxduty can be set by the input voltage to DTC pin. Set the voltage in which the VREF output divided with the resistors R9 and R10. If the voltage of DTC pin increases more than the limit value, the lower value between the set value and the internally fixed value is selected and in valid.

TEST Pin

In terms of TEST pin, connect the GND level or remain it open.

NO.EC-154-141119

Other Notes

- Use a 1.0 μF or higher capacitor (C4) in between GND and V_{IN} pin. Connect the capacitor as close as possible to the IC. If the noise level is large, use the 4.7 μF or higher capacitor is recommended.
- Use a 1.0 μ F or higher capacitor (C1, C2, and C3) in between GND and each Vout (Vout1, Vout2, and Vout3). The recommended capacitance is C1 = 4.7 μ F to 22 μ F, C2 = C3 = 1 μ F to 2.2 μ F (refer to the *Typical Application*).
- Use a 0.1 μF to 1 μF or higher capacitance (C6) in between VREF and GND.
- To connect the GND of the capacitors (C9, C10, C11, and C12) for setting the delay time as short as possible to the GND of the IC.
- Selection of the diodes and inductors and capcitors should be considered. When Nch-switch turns on, the
 high voltage of spike by an inductor might be generated. Thus, using more than twice of the set output voltage
 for the voltage tolerance of the capacitor connecting to VOUT is recommended. The diode and inductors
 should not exceed the rated value of the voltage, the current and the power (refer to Output Current and
 Selection of External Components).
- Select the diode with low forward voltage such as a Schottky barrier diode. The small reverse current and the fast switching speed type is desirable. Especially, the characteristics of diode (D1) influence the efficiency and the stability of the system.

APPLICATION INFORMATION

Overcurrent Protection

R1290K monitors the Nch-swich current of the step-up DCDC converter and limits the current. If Nch-switch current reaches the current limit, the R1290K immediately turns off Nch-switch. Nch-switch turns on every internal cycle, and the R1290K monitors Nch-switch current and turns off Nch-switch if Nch-switch current reaches the current limit again. By repeating this operation, the R1290K protects itself from the overcurrent.

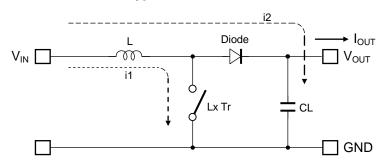
Under Voltage Lock Out (UVLO)

If V_{IN} pin voltage becomes equal to or lower than UVLO detector threshold, the R1290K immediately disables all the switching outputs (Lx, CPP, and CPN) as well as discharges the external capacitors on DTC pin and SS pin down to 0 V immediately, and the system will be reset.

OUTPUT CURRENT AND SELECTION OF EXTERNAL COMPONENTS

Operation and Output Current of Step-up DC/DC Converter

< Typical Circuit >



< Current through L >

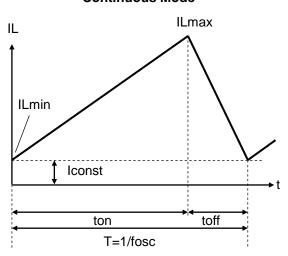
Discontinuous Mode

IL ILmax ILmin Tf

T=1/fosc

toff

Continuous Mode



In PWM step-up DC/DC converter, there are two modes; the discontinuous mode and the continuous mode. These two modes depend upon the continuous characteristic of the inductor current.

While PWM step-up DC/DC converter is turned on, the voltage into the inductance L will be V_{IN} , and the additional current (i1) can be calculated by the next formula.

$$\Delta i1 = V_{IN} \times ton / L$$

ton

In the circuit of the step-up DC/DC converter, during the off time of the switiching, the power is supplied. In this case, the decrease of input current (i2) can be calculated by the next formula:

$$\Delta i2 = (V_{OUT} - V_{IN}) \times Tf / L$$

NO.EC-154-141119

In the PWM switching method, the current of inductor becomes continuous when it is Tf = toff. The operating of DC/DC converter becomes continuous mode. In the continuous mode, the variance of the ratio of current is equal $(\Delta i1 = \Delta i2)$, therefore the DUTY in the continuous mode is calculated by the next formula.

$$duty(\%) = ton / (ton + toff) = (V_{OUT} - V_{IN}) / V_{OUT}$$

If the input power and the output power are equal, the mode becomes continuous when the lout value is larger than the next formula.

$$V_{IN}^2 \times ton / (2 \times L \times V_{OUT})$$

The average of the inductor current when Tf = toff is calculated by the next formula.

i1 (Ave.) =
$$V_{IN} \times ton / (2 \times L)$$

The peak current (ILxmax) of the inductor in the continuous mode can be calculated by the next formula:

```
\begin{aligned} ILxmax &= I_{OUT} \times V_{OUT} / V_{IN} + V_{IN} \times ton / (2 \times L) \\ ILxmax &= I_{OUT} \times V_{OUT} / V_{IN} + V_{IN} \times T \times (V_{OUT} - V_{IN}) / (2 \times L \times V_{OUT}) \end{aligned}
```

As stated above, the value of the peak current becomes larger than the lout value, therefore note that the ILxmax to determine the I/O condition and the components around the I/O.

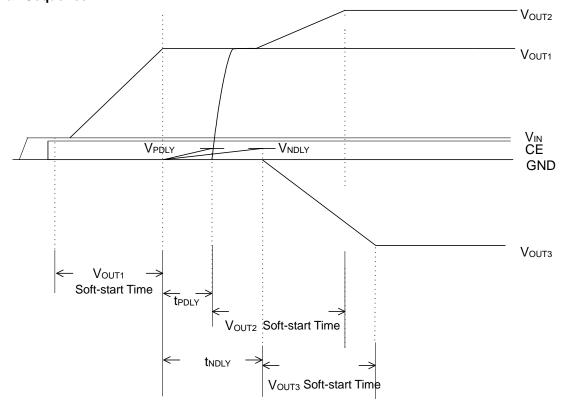
The actual maximum output current is 50 to 80% of the above-mentioned. Especially, in case that the IL is large, or V_{IN} is low, the loss of V_{IN} will be the amount of the ON resistance of the switch. As for the V_{OUT} , it is necessary to consider the V_F of the diode (approximately 0.3 V).

Note: The above-mentioned explanation is based on the calculations of the ideal case. The external components or the loss of Lx switching are not included.

NO.EC-154-141119

TIMING CHART

Overall Sequence



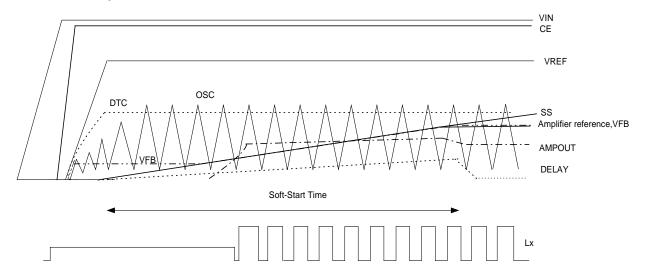
Overall Sequence Timing Chart

The timing chart above describes from the power on to the V_{OUT1} , V_{OUT2} , and V_{OUT3} turn on and until they are stable.

By releasing from the standby mode, V_{OUT1} begins the soft-start, and the output voltage rises gradually. After preset soft-start time passes, and the V_{OUT1} reaches the preset output voltage, the charge to capacitors set to CPPDLY pin and CPNDLY pin will start. CPPDLY pin and CPNDLY pin voltage reach respectively to the CPPDLY detector threshold (V_{PDLY}) and CPNDLY detector threshold (V_{NDLY}), then the soft-start of the charge-pump will begin. The delay time for soft-start of charge pump (t_{PDLY}, t_{NDLY}) can be set respectively.

When each delay time has passed, the soft-start of the charge-pump begins. V_{OUT2} and V_{OUT3} gradually turn on, and when the soft-start time ends, V_{OUT2} and V_{OUT3} reach the preset output voltage.

VOUT1 Soft-start Operation



Vout1 Soft-start Timing Chart

The timing chart above describes from the CE signal turns on until the soft-start of V_{OUT1} ends.

(STEP1)

SS voltage gradually increases with the internal IC's constant current and the external capacitor. During the soft-start time, the amplifier's reference input to the OP AMP becomes an equal voltage as SS, and it gradually increases. Since Vout reaches to the input voltage just after the power on, the VFB voltage rises at the specific voltage determined by the resistance ratio of the input voltage and the feedback part. However, the switching does not begin since AMPOUT is "L".

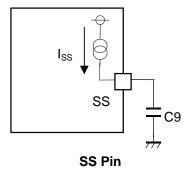
(STEP2)

When the SS becomes the specified voltage determined with the resistance ratio of the input voltage and the feedback part, the switching begins. In this case, the amplifier reference rises as well as SS, therefore Vout rises to balance the amplifier reference and VFB. The DUTY in this case is determined by the three inputs PWM comparator, among the AMPOUT and DTC, the lowest voltage is selected.

(STEP3)

When the SS becomes 1 V, the soft-start ends. After that, the amplifier reference becomes the constant voltage (= 1 V), and the operation changes to the normal switching. At this time, the voltage of the AMPOUT becomes constant. The AMPOUT value is determined by the I/O voltage and the output current.

During the soft-start period, the soft-start time needs to be set shorter than the timer latch delay time due to the charging of DELAY pin. When the preset soft-start time finishes, the charging of DELAY pin stops and discharges to the GND.



PACKAGE INFORMATION

POWER DISSIPATION (QFN0404-24)

Power Dissipation (P_D) depends on conditions of mounting on board. This specification is based on the measurement at the condition below:

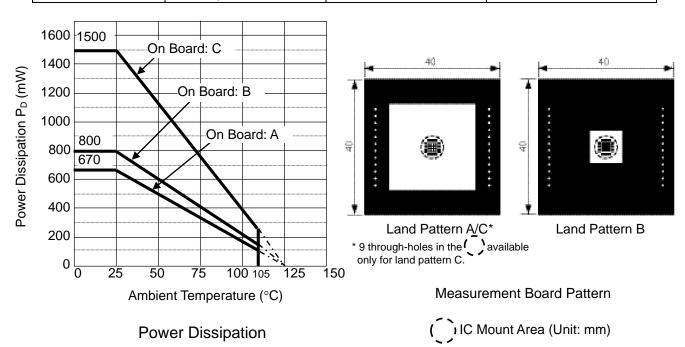
Measurement Conditions

	meacaroment Conduction					
	Land Pattern A	Land Pattern B	Land Pattern C			
Environment	Mounting on Board (W	Mounting on Board (Wind velocity=0m/s)				
Board Material	Glass cloth epoxy plas	Glass cloth epoxy plastic (Double sided)				
Board Dimensions	40mm × 40mm × 1.6mm					
Copper Ratio	Top side: Approx. 50% Back side: Approx. 50%	Top side: Approx. 90% Back side: Approx. 90%	Top side: Approx. 50% Back side: Approx. 100%			
Through-hole	φ0.25mm×24pcs	φ0.25mm×24pcs	φ0.25mm×33pcs			
Remarks	_	_	Top side and back side are connected by 9 through-holes in the tab area.			

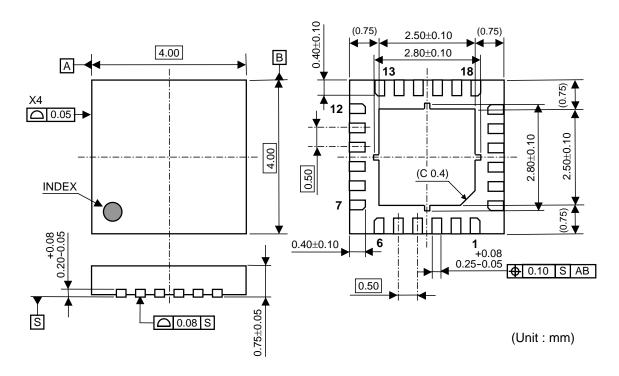
Measurement Result

(Ta=25°C, Tjmax=125°C)

	Land Pattern A	Land Pattern B	Land Pattern C
Power Dissipation	670mW	800mW	1500mW
Thormal Desigtance	θja=150°C/W	0io 125°C/M	0io 670CAN
Thermal Resistance	θjc=15°C/W	θja=125°C/W	θja=67°C/W



PACKAGE DIMENSIONS (QFN0404-24)



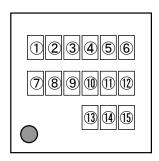
QFN0404-24 Package Dimensions

MARK SPECIFICATION (QFN0404-24)

1234567891 : Product Code ... Refer to MARK SPECIFICATION TABLE

① : Year Code ② : Month Code

③45 : Lot Number ... Alphanumeric Serial Number



- ① Year Code 2006→6 2009→9 2007→7 2010→0 2008→8 2011→1
- Month Code
 Jan, Feb···Dec
 A B M (except I)
- (1)(1): Year/Month Codes are the date when the package assembly consignment document is completed.
- (3)(4)(5): Serial number from 500 to 999 is remained even if Year/Month Code changes.

QFN0404-24 Mark Specification

MARK SPECIFICATION TABLE (QFN0404-24)

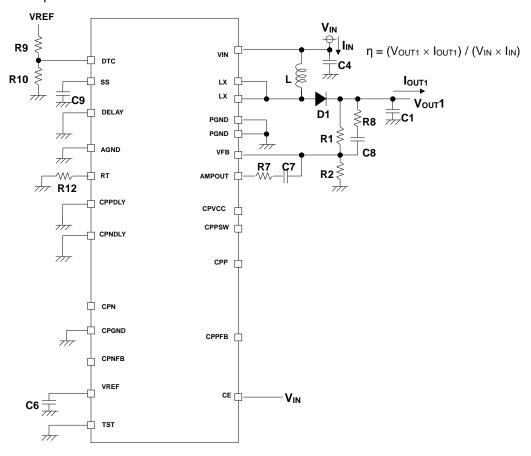
Product Name	0234567890
R1290K101A	R 1 2 9 0 K 1 0 1 A
R1290K102A	R 1 2 9 0 K 1 0 2 A
R1290K103A	R 1 2 9 0 K 1 0 3 A

NO.EC-154-141119

TEST CIRCUIT

V_{OUT1} (DCDC)

- Output Voltage vs. Output Current
- Efficiency vs. Output Current



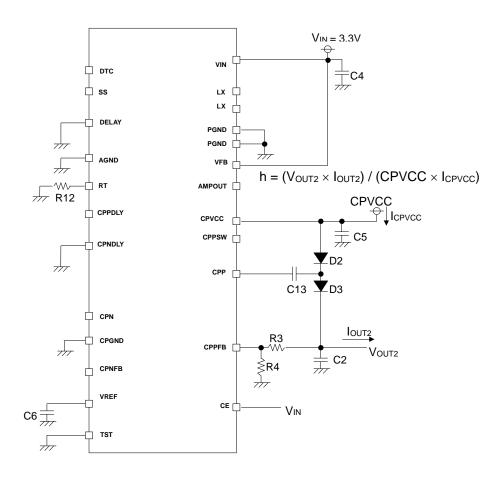
Components

Cumbal	Description					
Symbol	fosc = 180 kHz	fosc = 700 kHz	fosc = 1400 kHz			
R1	For setting voltage of V _{OUT1}					
R2	For setting voltage of V _{OUT2}					
R7	10 kΩ	4.7 kΩ	3.3 kΩ			
R8	4.7 kΩ					
R9	20 kΩ					
R10	100 kΩ					
R12	110 kΩ	24 kΩ	10 kΩ			
C1, C4	4.7 μF, Ceramic					
C6	1 μF, Ceramic					
C7	1000 pF, Ceramic					
C8	1000 pF (V _{OUT1} = 8 V) / 560	$pF(V_{OUT1} = 12 V) / 270 pF(V)$	оит1 = 18 V), Ceramic			
C9	0.022 μF, Ceramic					
L	22 μH, NR4018T220M, TAIYO YUDEN	4.7 μH, NR4018T4R7M, TAIYO YUDEN	2.2 μH, NR4018T2R2M, TAIYO YUDEN			
D1	CRS02, TOSHIBA		•			

V_{OUT2} (Step-up Charge-pump)

- Output Voltage vs. Output Current
- Efficiency vs. Output Current

(1) CPVCC = 8 V and V_{OUT2} = 12 V, CPVCC = 12 V and V_{OUT2} = 18 V

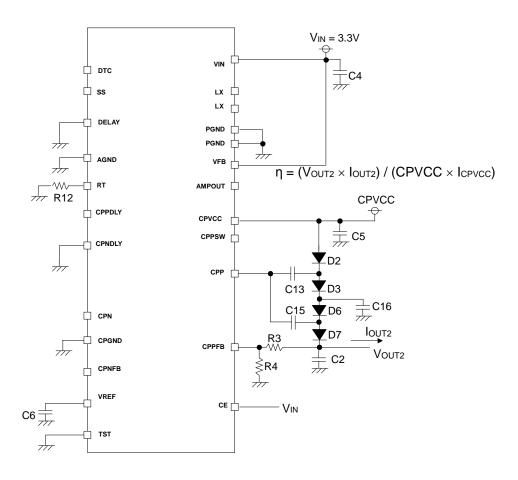


Components

Symbol	Description	
	CPVCC = 8 V, V _{OUT2} = 12 V	$V_{OUT2} = 12 V, V_{OUT2} = 18 V$
R3	For setting voltage of V _{OUT3}	
R4	For setting voltage of V _{OUT4}	
R12	For setting of fosc	
C2, C6	1 μF, Ceramic	
C4, C5	4.7 μF, Ceramic	
C13	For setting Cfly, Ceramic	
D2, D3	1SS374, TOSHIBA	

NO.EC-154-141119

(2) CPVCC = 8 V and V_{OUT2} = 16 V, CPVCC = 12 V and V_{OUT2} = 24 V

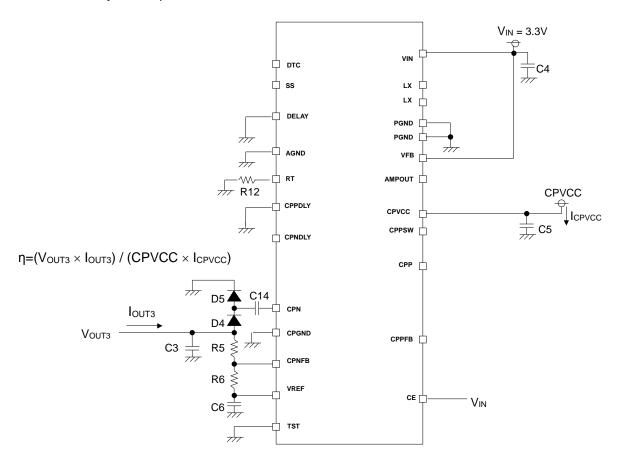


Components

Symbol	Description		
	CPVCC = 8 V, V _{OUT2} = 16 V	$V_{OUT2} = 12 V, V_{OUT2} = 24 V$	
R3	For setting voltage of Vout3		
R4	For setting voltage of V _{OUT4}		
R12	For setting fosc		
C2, C6, C16	1 μF, Ceramic		
C4, C5	4.7 μF, Ceramic		
C13	For setting Cfly, Ceramic		
C15	For setting Cfly, Ceramic		
D2, D3	1SS374, TOSHIBA		

VOUT3 (Inverting Charge-pump)

- Output Voltage vs. Output Current
- Efficiency vs. Output Current



Component

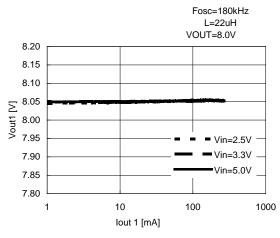
CIIL		
Symbol	Description	
R5	For setting voltage of V _{OUT3}	
R6	For setting voltage of V _{OUT4}	
R12	For setting fosc	
C3, C6	1 μF, Ceramic	
C4, C5	4.7 μF, Ceramic	
C14	For setting Cfly, Ceramic	
D4, D5	1SS374, TOSHIBA	

TYPICAL CHARACTERISTICS

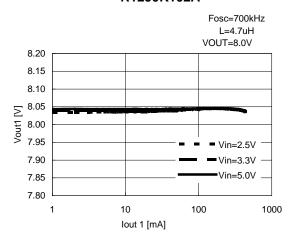
1) Vout1 (DC/DC)

1-1) Output Voltage vs. Output Current

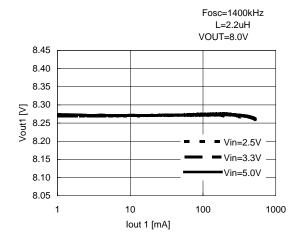




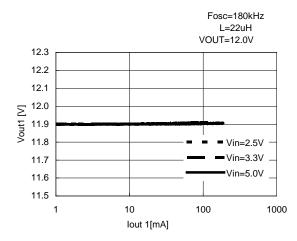
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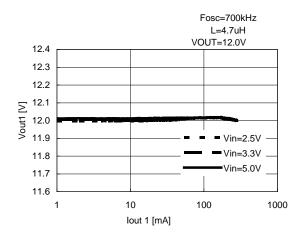
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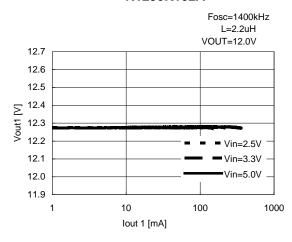


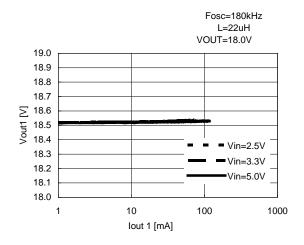
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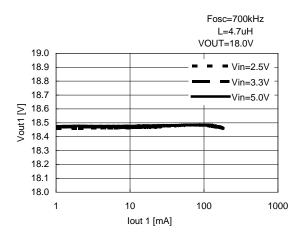
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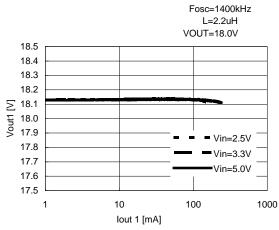




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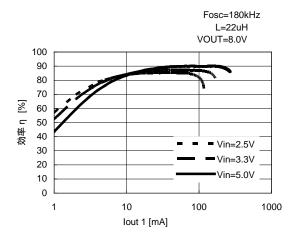


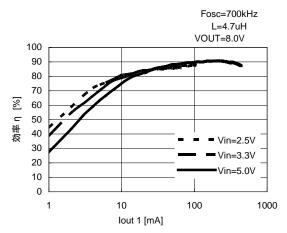
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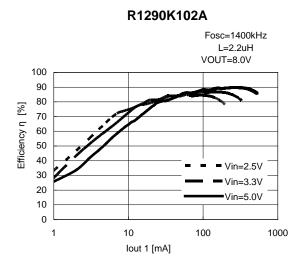


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1-2) Efficiency vs. Output Current R1290K102A





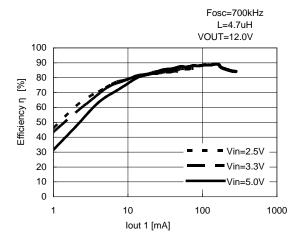


Fosc=180kHz L=22uH VOUT=12.0V 100 90 80 % 70 Efficiency η 60 50 40 ■ Vin=2.5V 30 Vin=3.3V 20 Vin=5.0V 10 0 10 100 1000

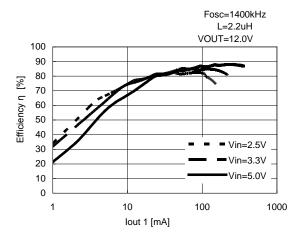
lout 1[mA]

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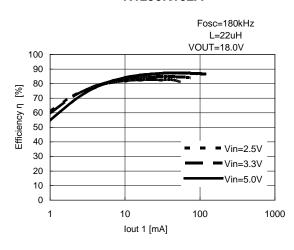
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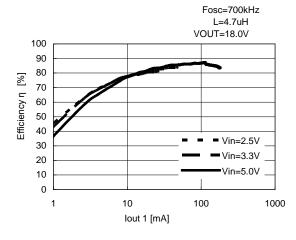


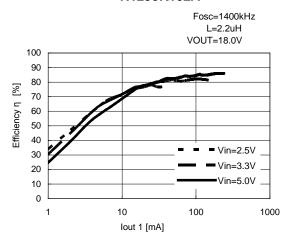
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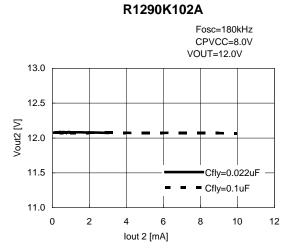
R1290K102A



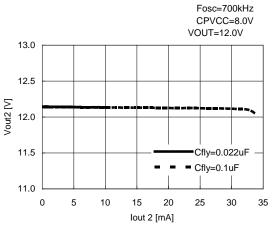




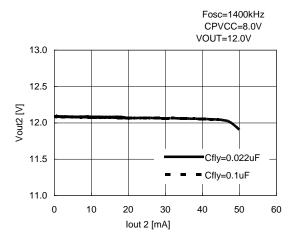
2) Vout2 (Step-up Charge-pump) 2-1) Output Voltage vs. Output Current

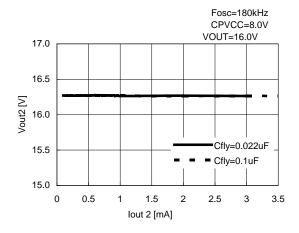


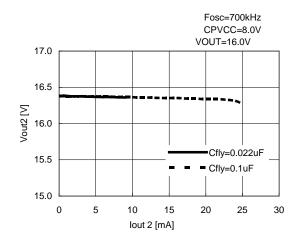
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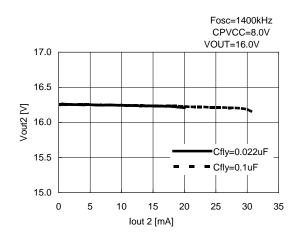
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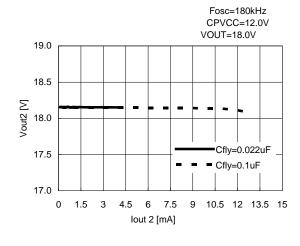




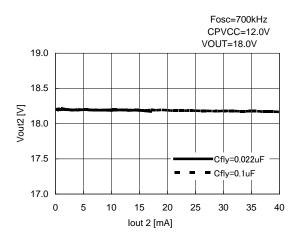
R1290K102A



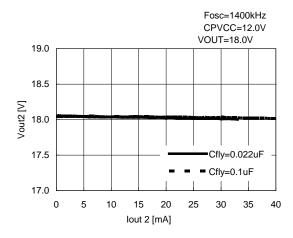
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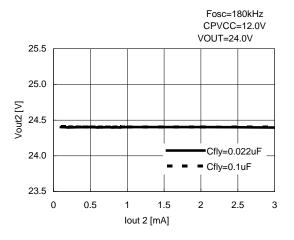


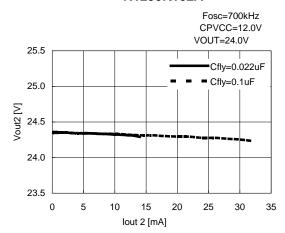
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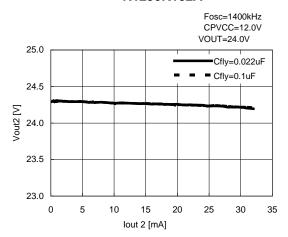
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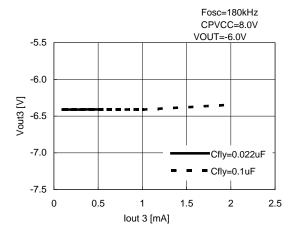


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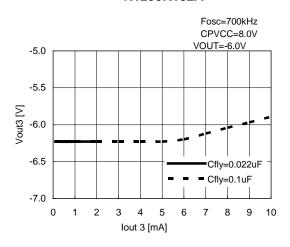


3) Vout3 (Invert Charge-pump)3-1) Output Voltage vs. Output Current

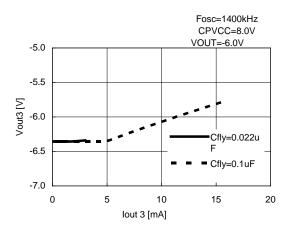
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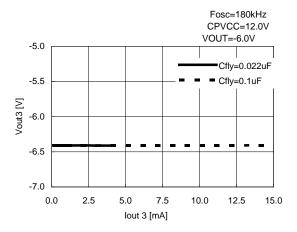


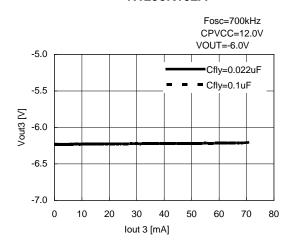
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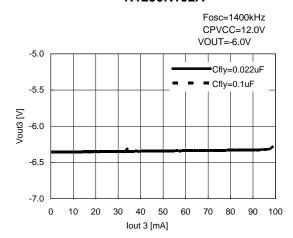
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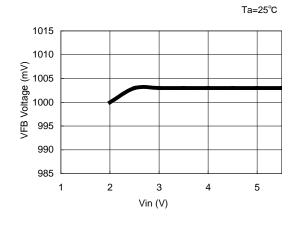


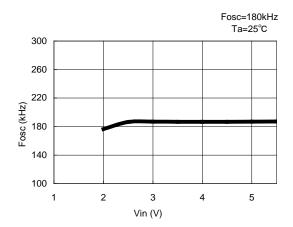
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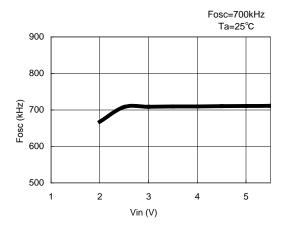
4) VFB Voltage vs. Input Voltage R1290K102A

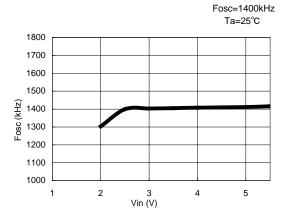
5) Oscillator Frequency vs. Input Voltage R1290K102A



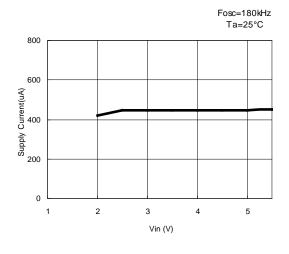


R1290K102A

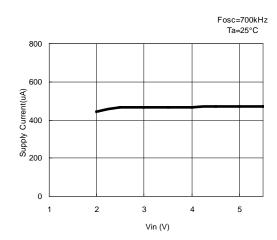




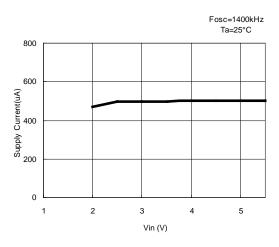
6) Supply Current vs. Input Voltage R1290K102A



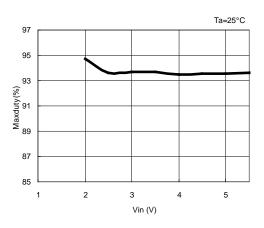
R1290K102A



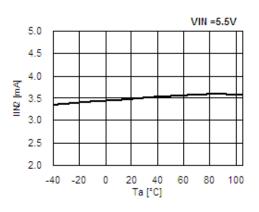
R1290K102A



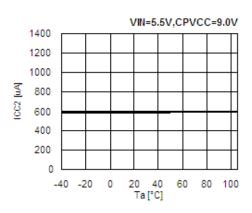
7) Maxduty vs. Input Voltage R1290K102A



8) VIN Supply Current vs. Temperature R1290K102A

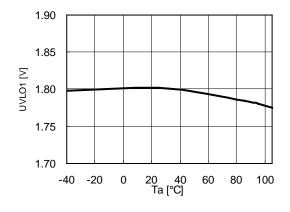


9) CP Supply Current vs. Temperature R1290K102A

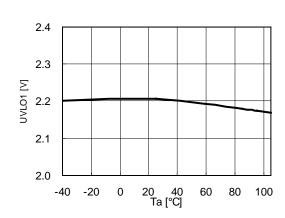


10) UVLO Detect Voltage vs. Temperature

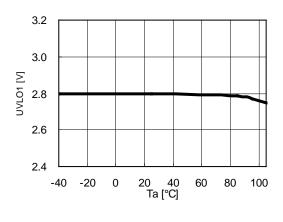
R1290K102A



R1290K102A

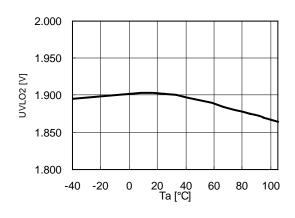


R1290K102A

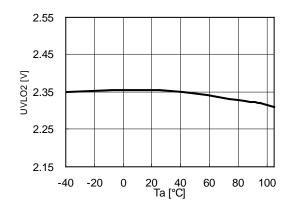


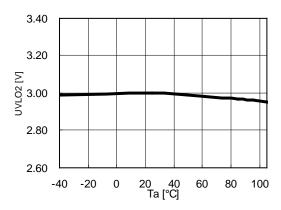
11) UVLO Release Voltage vs. Temperature

R1290K102A



R1290K102A

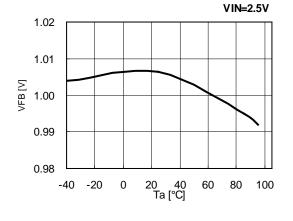




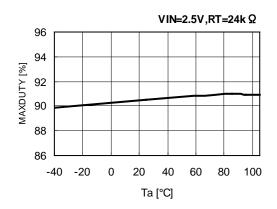
NO.EC-154-141119

12) VFB Voltage vs. Temperature

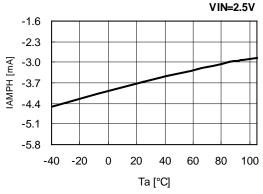
R1290K102A



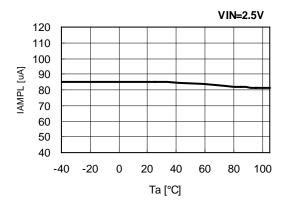
13) Maxduty vs. Temperature



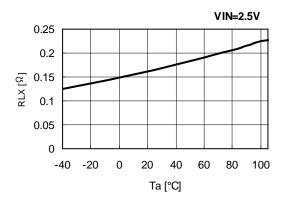
14) AMP "H" Output Current vs. Temperature R1290K102A



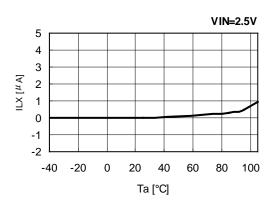
15) AMP "L" Output Current vs. Temperature R1290K102A



16) Switch ON Resistance vs. Temperature R1290K102A



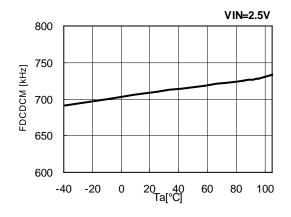
17) Switch Leakage Current vs. Temperature R1290K102A



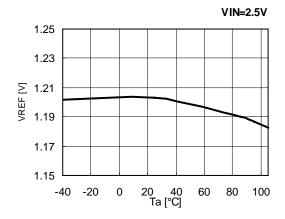
18) Switch Limit Current vs. Temperature R1290K102A

3.5 3 2.5 1.5 1 -40 -20 0 20_{Ta} [°C] 40 60 80 100

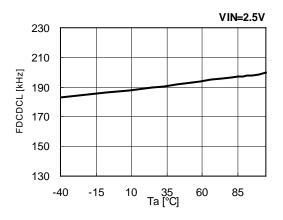
R1290K102A



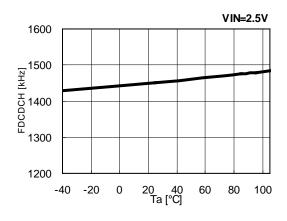
20) VREF Voltage vs. Temperature R1290K102A



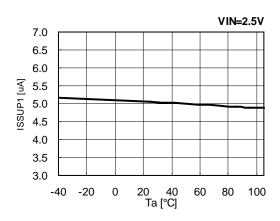
19) Oscillator Frequency vs. Temperature R1290K102A



R1290K102A



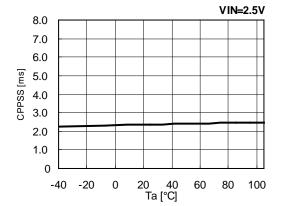
21) SS Pin Charge Current vs. Temperature R1290K102A



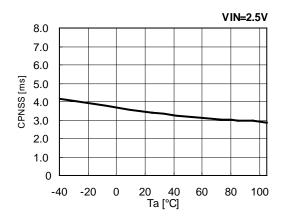
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22) CPP Soft-start vs. Temperature

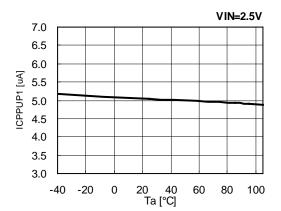
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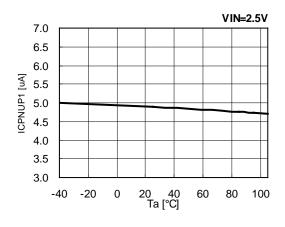
23) CPN Soft-start vs. Temperature



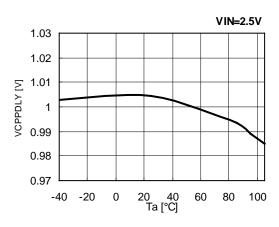
24) CPPDLY Charge Current vs. Temperature R1290K102A



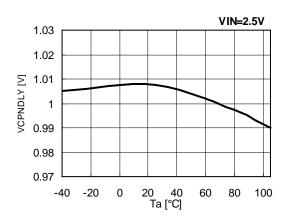
25) CPNDLY Charge Current vs. Temperature R1290K102A



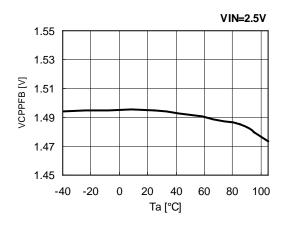
26) CPPDLY Detector Threshold vs. Temperature 27) CPNDLY Detector Threshold vs. Temperature R1290K102A



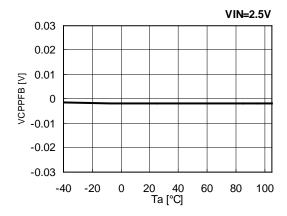
R1290K102A



28) CPPFB Voltage vs. Temperature

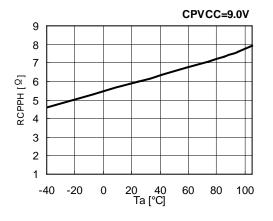


29) CPNFB Voltage vs. Temperature

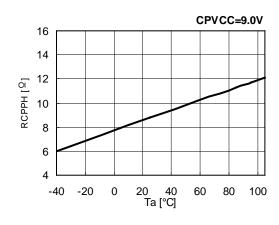


30) CPP "H" ON Resistance vs. Temperature

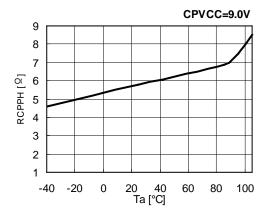
R1290K102A



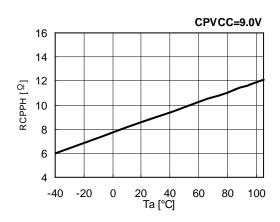
31) CPP "L" ON Resistance vs. Temperature R1290K102A



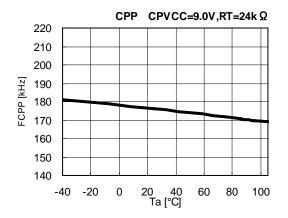
32) CPN "H" ON Resistance vs. Temperature R1290K102A



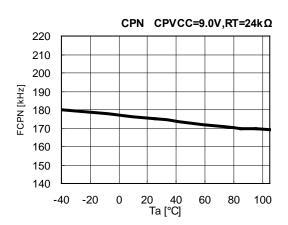
33) CPN "L" ON Resistance vs. Temperature R1290K102A



34) Charge-pump Frequency vs. Temperature



R1290K102A

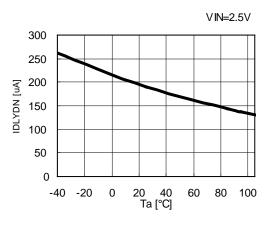


35) DELAY Charge Current vs. Temperature

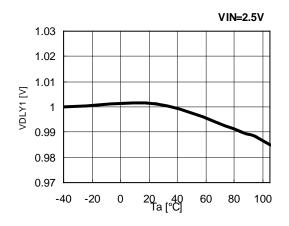
R1290K102A

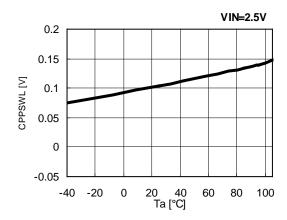
VIN=2.5V 7.0 6.5 6.0 1DLYUP1 [uA] 4.0 3.5 3.0 20 40 Ta [°C] -40 -20 0 100 60 80

36) DELAY Discharge Current vs. Temperature R1290K102A

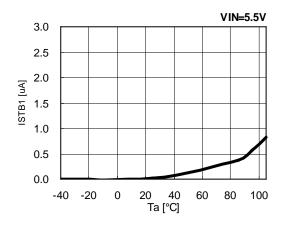


37) DELAY Detector Threshold vs. Temperature 38) CPPSW "L" Output Voltage vs. Temperature R1290K102A R1290K102A





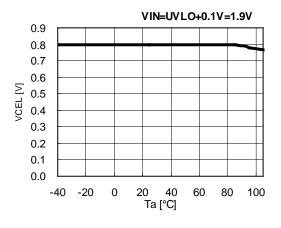
39) Standby Current vs. Temperature



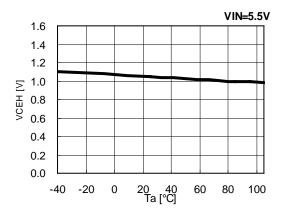
R1290K102A

4.5 3.5 2.5 0.5 -0.5 -40 -20 0 20 40 60 80 100

40) CE "L" Input Voltage vs. Temperature R1290K102A

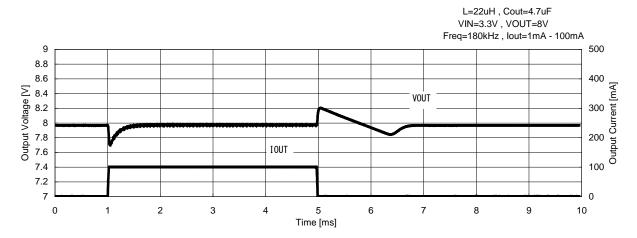


41) CE "H" Input Voltage vs. Temperature R1290K102A

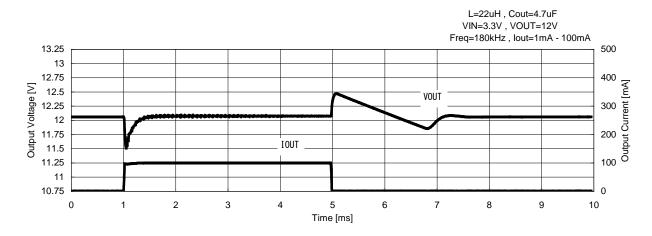


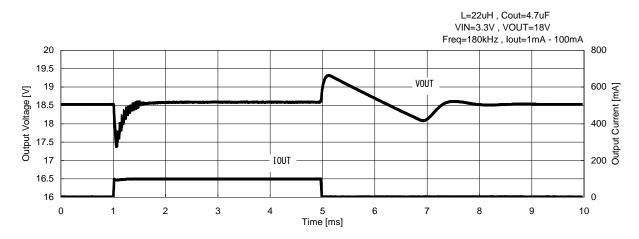
42) Load Transient Response

R1290K102A



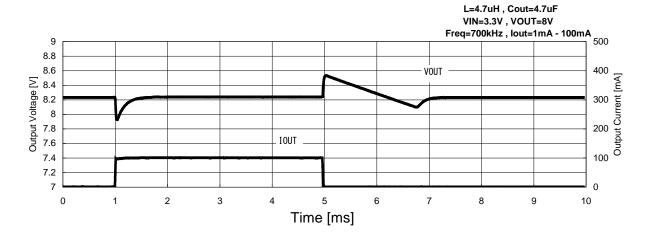
R1290K102A



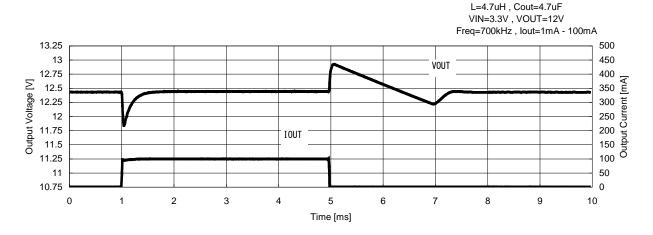


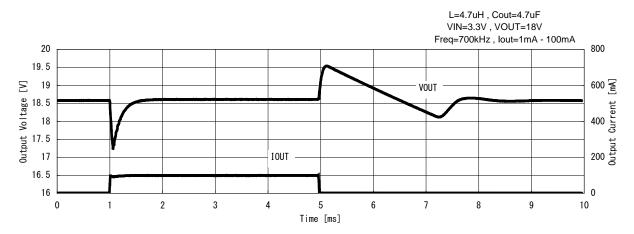
42) Load Transient Response

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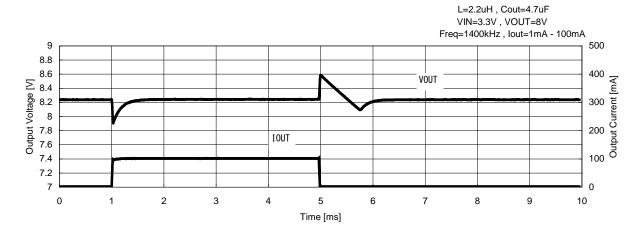
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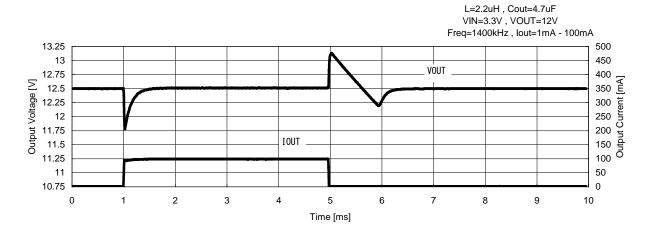


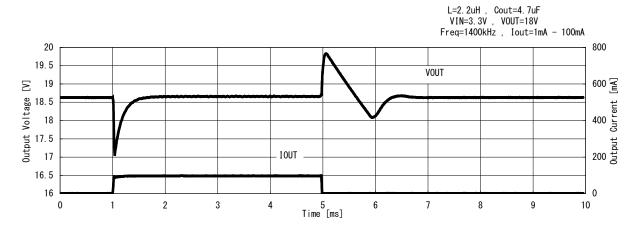
42) Load Transient Response

R1290K102A



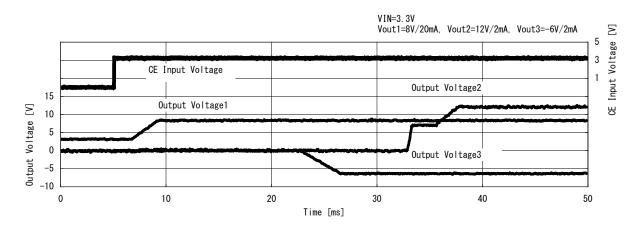
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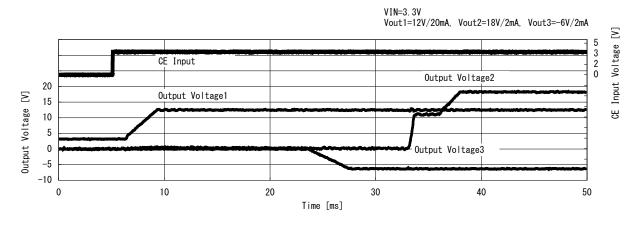


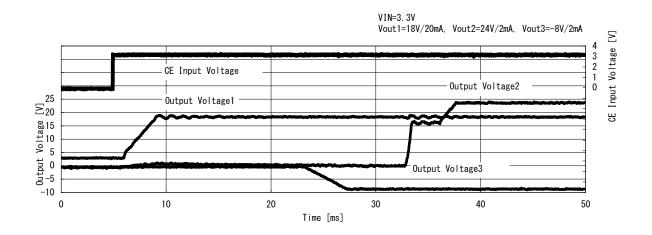
43) CE Switch Response

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