



### FEATURES

- Dual transmitters
- Dual receivers
- Dual input shared observation receiver
- Maximum receiver bandwidth: 200 MHz
- Maximum tunable transmitter synthesis bandwidth: 450 MHz
- Maximum observation receiver bandwidth: 450 MHz
- Fully integrated fractional-N RF synthesizers
- Fully integrated clock synthesizer
- Multichip phase synchronization for RF LO and baseband clocks
- JESD204B datapath interface
- Tuning range (center frequency): 75 MHz to 6000 MHz

### APPLICATIONS

- 3G, 4G, and 5G TDD macrocell base stations
- TDD active antenna systems
- Massive multiple input, multiple output (MIMO)
- Phased array radar
- Electronic warfare
- Military communications
- Portable test equipment

### GENERAL DESCRIPTION

The ADRV9009 is a highly integrated, radio frequency (RF), agile transceiver offering dual transmitters and receivers, integrated synthesizers, and digital signal processing functions. The IC delivers a versatile combination of high performance and low power consumption demanded by 3G, 4G, and 5G macro cell time division duplex (TDD) base station applications.

The receive path consists of two independent, wide bandwidth, direct conversion receivers with state-of-the-art dynamic range. The device also supports a wide bandwidth, time shared observation path receiver (ORx) for use in TDD applications. The complete receive subsystem includes automatic and manual attenuation control, dc offset correction, quadrature error correction (QEC), and digital filtering, thus eliminating the need for these functions in the digital baseband. Several auxiliary functions, such as analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and general-purpose inputs/outputs (GPIOs) for the power amplifier (PA), and RF front-end control are also integrated.

In addition to automatic gain control (AGC), the ADRV9009 also features flexible external gain control modes, allowing significant flexibility in setting system level gain dynamically.

The received signals are digitized with a set of four high dynamic range, continuous time  $\Sigma$ - $\Delta$  ADCs that provide inherent antialiasing. The combination of the direct conversion architecture, which does not suffer from out of band image mixing, and the lack of aliasing, relaxes the requirements of the RF filters when compared to traditional intermediate frequency (IF) receivers.

The transmitters use an innovative direct conversion modulator that achieves high modulation accuracy with exceptionally low noise.

The observation receiver path consists of a wide bandwidth, direct conversion receiver with state-of-the-art dynamic range.

The fully integrated phase-locked loop (PLL) provides high performance, low power, fractional-N RF frequency synthesis for the transmitter (Tx) and receiver (Rx) signal paths. An additional synthesizer generates the clocks needed for the converters, digital circuits, and the serial interface. A multichip synchronization mechanism synchronizes the phase of the RF local oscillator (LO) and baseband clocks between multiple ADRV9009 chips. Precautions are taken to provide the isolation required in high performance base station applications. All voltage controlled oscillators (VCOs) and loop filter components are integrated.

The high speed JESD204B interface supports up to 12.288 Gbps lane rates, resulting in two lanes per transmitter and a single lane per receiver in the widest bandwidth mode. The interface also supports interleaved mode for lower bandwidths, thus reducing the total number of high speed data interface lanes to one. Both fixed and floating point data formats are supported. The floating point format allows internal AGC to be invisible to the demodulator device.

The core of the ADRV9009 can be powered directly from 1.3 V regulators and 1.8 V regulators, and is controlled via a standard 4-wire serial port. Comprehensive power-down modes are included to minimize power consumption in normal use. The ADRV9009 is packaged in a 12 mm  $\times$  12 mm, 196-ball chip scale ball grid array (CSP\_BGA).

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**6/2018—Revision A: Initial Version**

FUNCTIONAL BLOCK DIAGRAM

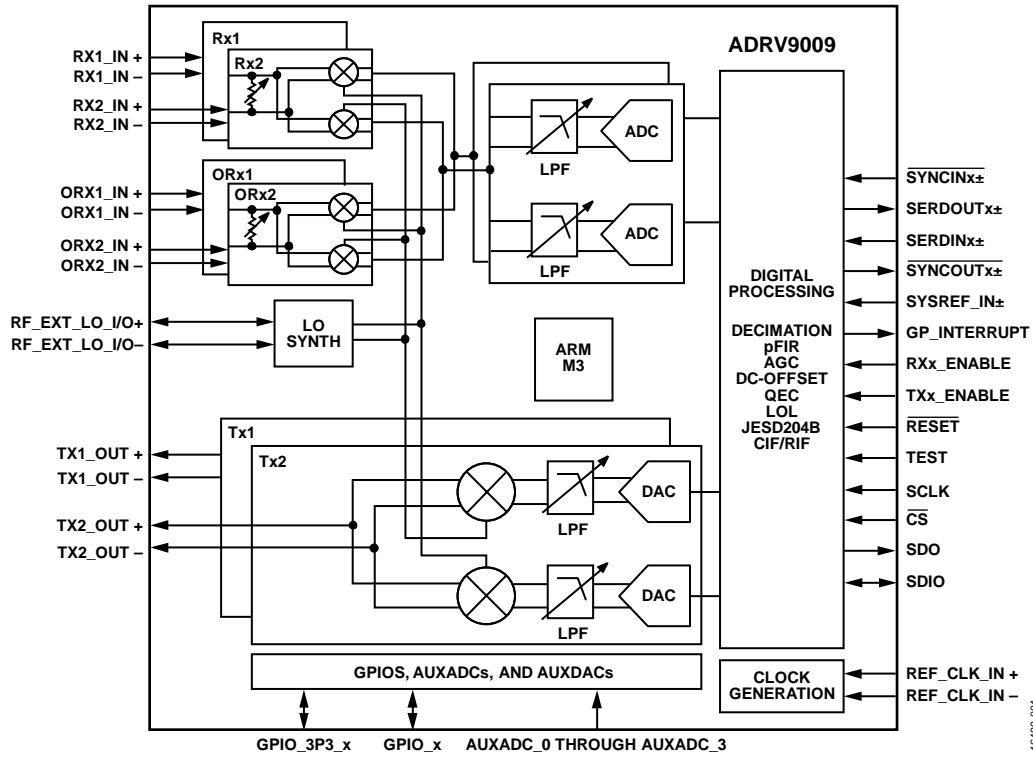


Figure 1.

## SPECIFICATIONS

Electrical characteristics at VDDA1P3<sup>1</sup> = 1.3 V, VDDD1P3\_DIG = 1.3 V, VDDA1P8\_TX = 1.8 V, junction temperature (T<sub>J</sub>) = full operating temperature range. LO frequency (f<sub>LO</sub>) = 1800 MHz, unless otherwise noted. The specifications in Table 1 are not de-embedded. Refer to the Typical Performance Characteristics section for input and output circuit path loss. The device configuration profile for the 75 MHz to 525 MHz frequency range is as follows: receiver = 50 MHz bandwidth (inphase quadrature (IQ) rate = 61.44 MHz), transmitter = 50 MHz transmitter large signal bandwidth and 100 MHz transmitter synthesis bandwidth (IQ rate = 122.88 MHz), observation receiver = 100 MHz bandwidth (IQ rate = 122.88 MHz), JESD204B rate = 9.8304 GSPS, and device clock = 245.76 MHz. Unless otherwise specified, the device configuration for all other frequency ranges is as follows: receiver = 200 MHz bandwidth (IQ rate = 245.76 MHz), transmitter = 200 MHz transmitter large signal bandwidth and 450 MHz transmitter synthesis bandwidth (IQ rate = 491.52 MHz), observation receiver = 450 MHz bandwidth (IQ rate = 491.52 MHz), JESD204B rate = 9.8304 GSPS, and device clock = 245.76 MHz.

**Table 1.**

| Parameter  | Symbol           | Min  | Typ  | Max  | Unit    | Test Conditions/Comments  |
|--|------------------|------|------|------|---------|---|
| <b>TRANSMITTERS</b>  |                  |      |      |      |         |   |
| Center Frequency   |                  | 75   |      | 6000 | MHz     |   |
| Transmitter Synthesis Bandwidth  |                  |      |      | 450  | MHz     |   |
| Transmitter Large Signal Bandwidth   |                  |      |      | 200  | MHz     |   |
| Peak-to-Peak Gain Deviation  |                  |      | 1.0  |      | dB      | 450 MHz bandwidth, compensated by programmable finite impulse response (FIR) filter                   |
| Gain Slope   |                  |      | ±0.1 |      | dB      | Any 20 MHz bandwidth span, compensated by programmable FIR filter                                     |
| Deviation from Linear Phase  |                  |      | 1    |      | Degrees | 450 MHz bandwidth   |
| Transmitter Attenuation Power Control Range                                      |                  | 0    |      | 32   | dB      | Signal-to-noise ratio (SNR) maintained for attenuation between 0 dB and 20 dB                         |
| Transmitter Attenuation Power Control Resolution                                 |                  |      | 0.05 |      | dB      |   |
| Transmitter Attenuation Integral Nonlinearity                                    | INL              |      | 0.1  |      | dB      | For any 4 dB step   |
| Transmitter Attenuation Differential Nonlinearity                                | DNL              |      | 0.04 |      | dB      | Monotonic   |
| Transmitter Attenuation Serial Peripheral Interface 2 (SPI 2) Timing             |                  |      |      |      |         | See Figure 4  |
| Time from $\overline{\text{CS}}$ Going High to Change in Transmitter Attenuation | t <sub>SCH</sub> | 19.5 |      | 24   | ns      |   |
| Time Between Consecutive Microattenuation Steps                                  | t <sub>ACH</sub> | 6.5  |      | 8.1  | ns      | A large change in attenuation can be broken up into a series of smaller attenuation changes           |
| Time Required to Reach Final Attenuation Value                                   | t <sub>DCH</sub> |      |      | 800  | ns      | Time required to complete the change in attenuation from start attenuation to final attenuation value |
| Maximum Attenuation Overshoot During Transition                                  |                  | -1.0 |      | +0.5 | dB      |   |
| Change in Attenuation per Microstep  |                  |      |      | 0.5  | dB      |   |
| Maximum Attenuation Change when $\overline{\text{CS}}$ Goes High                 |                  |      | 32   |      | dB      |   |

| Parameter   | Symbol | Min | Typ    | Max | Unit | Test Conditions/Comments   |
|---|--------|-----|--------|-----|------|--|
| Adjacent Channel Leakage Ratio (ACLR) Long Term Evolution (LTE) |        |     | -67    |     |      | 20 MHz LTE at -12 dBFS   |
|   |        |     | -64    |     |      | 75 MHz < f ≤ 2800 MHz  |
|   |        |     | -60    |     |      | 2800 MHz < f ≤ 4800 MHz  |
| In Band Noise Floor   |        |     |        |     |      | 4800 MHz < f ≤ 6000 MHz  |
|   |        |     |        |     |      | 0 dB attenuation, in band noise falls 1 dB for each dB of attenuation for attenuation between 0 dB and 20 dB   |
|   |        |     | -147   |     |      | 75 MHz < f ≤ 600 MHz   |
|   |        |     | -148   |     |      | 600 MHz < f ≤ 3000 MHz   |
| Out of Band Noise Floor   |        |     | -149   |     |      | 3000 MHz < f ≤ 4800 MHz  |
|   |        |     | -150.5 |     |      | 4800 MHz < f ≤ 6000 MHz  |
|   |        |     | -147   |     |      | 0 dB attenuation, 3 × bandwidth/2 offset   |
|   |        |     | -153   |     |      | 75 MHz < f ≤ 600 MHz   |
| Interpolation Images Transmitter to Transmitter Isolation       |        |     | -154   |     |      | 600 MHz < f ≤ 3000 MHz   |
|   |        |     | -155.5 |     |      | 3000 MHz < f ≤ 4800 MHz  |
|   |        |     | -80    |     |      | 4800 MHz < f ≤ 6000 MHz  |
|   |        |     | 85     |     |      | dBc  |
| Image Rejection Within Large Signal Bandwidth                   |        |     | 75     |     |      | 75 MHz < f ≤ 600 MHz   |
|   |        |     | 70     |     |      | 600 MHz < f ≤ 4800 MHz   |
|   |        |     | 65     |     |      | 4800 MHz < f ≤ 5700 MHz  |
|   |        |     | 56     |     |      | 5700 MHz < f ≤ 6000 MHz  |
| Image Rejection Beyond Large Signal Bandwidth                   |        |     |        |     |      | QEC active   |
|   |        |     | 70     |     |      | 75 MHz < f ≤ 600 MHz   |
|   |        |     | 65     |     |      | 600 MHz < f ≤ 4000 MHz   |
|   |        |     | 62     |     |      | 4000 MHz < f ≤ 4800 MHz  |
| Maximum Output Power  |        |     | 60     |     |      | 4800 MHz < f ≤ 6000 MHz  |
|   |        |     | 40     |     |      | Assumes that distortion power density is 25 dB below desired power density   |
|   |        |     | 9      |     |      | 0 dBFS, continuous wave (CW) tone into 50 Ω load, 0 dB transmitter attenuation   |
|   |        |     | 7      |     |      | 75 MHz < f ≤ 600 MHz   |
| Third-Order Output Intermodulation Intercept Point              | OIP3   |     | 6      |     |      | 600 MHz < f ≤ 3000 MHz   |
|   |        |     | 4.5    |     |      | 3000 MHz < f ≤ 4800 MHz  |
|   |        |     |        |     |      | 4800 MHz < f ≤ 6000 MHz  |
|   |        |     |        |     |      | 0 dB transmitter attenuation   |
| Carrier Leakage   |        |     | 29     |     |      | 75 MHz < f ≤ 600 MHz   |
|   |        |     | 27     |     |      | 600 MHz < f ≤ 4000 MHz   |
|   |        |     | 23     |     |      | 4000 MHz < f ≤ 6000 MHz  |
| Carrier Offset from LO  |        |     |        |     |      | With LO leakage correction active, 0 dB attenuation, scales decibel for decibel with attenuation, measured in 1 MHz bandwidth, resolution bandwidth and video bandwidth = 100 kHz, rms detector, 100 trace average |
|   |        |     | -84    |     |      | 75 MHz < f ≤ 600 MHz   |
|   |        |     | -82    |     |      | 600 MHz < f ≤ 4800 MHz   |
| Carrier on LO   |        |     | -80    |     |      | 4800 MHz < f ≤ 6000 MHz  |
|   |        |     | -71    |     |      | dBFS   |

| Parameter  | Symbol            | Min | Typ   | Max  | Unit    | Test Conditions/Comments  |
|--|-------------------|-----|-------|------|---------|---|
| Error Vector Magnitude<br>(Third Generation Partnership Project<br>(3GPP) Test Signals)<br>75 MHz LO | EVM               |     | 0.5   |      | %       | 300 kHz RF PLL loop bandwidth, test equipment phase noise performance limited   |
| 1900 MHz LO  |                   |     | 0.7   |      | %       | 50 kHz RF PLL loop bandwidth  |
| 3800 MHz LO  |                   |     | 0.7   |      | %       | 300 kHz RF PLL loop bandwidth   |
| 5900 MHz LO  |                   |     | 1.1   |      | %       | 300 kHz RF PLL loop bandwidth   |
| Output Impedance   | Z <sub>OUT</sub>  |     | 50    |      | Ω       | Differential (see Figure 427)   |
| <b>OBSERVATION RECEIVER</b>  | <b>ORx</b>        |     |       |      |         |   |
| Center Frequency   |                   | 75  |       | 6000 | MHz     |   |
| Gain Range   |                   |     | 30    |      | dB      | Third-order input intermodulation intercept point (IIP3) improves decibel for decibel for the first 18 dB of gain attenuation, QEC performance optimized for 0 dB to 6 dB of attenuation only |
| Analog Gain Step   |                   |     | 0.5   |      | dB      | For attenuator steps from 0 dB to 6 dB  |
| Peak-to-Peak Gain Deviation  |                   |     | 1     |      | dB      | 450 MHz bandwidth, compensated by programmable FIR filter   |
| Gain Slope   |                   |     | ±0.1  |      | dB      | Any 20 MHz bandwidth span, compensated by programmable FIR filter   |
| Deviation from Linear Phase  |                   |     | 1     |      | Degrees | 450 MHz RF bandwidth  |
| Observation Receiver Bandwidth   |                   |     |       | 450  | MHz     |   |
| Observation Receiver Alias Band Rejection  |                   | 60  |       |      | dB      | Due to digital filters  |
| Maximum Useable Input Level  | P <sub>HIGH</sub> |     |       |      |         | 0 dB attenuation, increases decibel for decibel with attenuation, CW corresponds to -1 dBFS at ADC  |
|  |                   |     | -11   |      | dBm     | 75 MHz < f ≤ 3000 MHz   |
|  |                   |     | -9.5  |      | dBm     | 3000 MHz < f ≤ 4800 MHz   |
|  |                   |     | -8    |      | dBm     | 4800 MHz < f ≤ 6000 MHz   |
| Integrated Noise   |                   |     | -58.5 |      | dBFS    | 450 MHz integration bandwidth   |
|  |                   |     | -57.5 |      | dBFS    | 491.52 MHz integration bandwidth  |
| Second-Order Input Intermodulation Intercept Point   | IIP2              |     | 62    |      | dBm     | Maximum observation receiver gain, (P <sub>HIGH</sub> - 14 dB) per tone (see the Terminology section), 75 MHz < f ≤ 600 MHz   |
|  |                   |     | 62    |      | dBm     | Maximum observation receiver gain, (P <sub>HIGH</sub> - 8 dB) per tone (see the Terminology section), 600 MHz < f ≤ 3000 MHz  |
| Third-Order Input Intermodulation Intercept Point Narrow Band  | IIP3              |     |       |      |         |   |
|  |                   |     | 4     |      | dBm     | 75 MHz < f ≤ 300 MHz, test condition: (P <sub>HIGH</sub> - 14) dB per tone  |
|  |                   |     | 11    |      | dBm     | 300 MHz < f ≤ 600 MHz, (P <sub>HIGH</sub> - 14) dB per tone   |
|  |                   |     |       |      |         | Third-order intermodulation product (IM3) product < 130 MHz at baseband, (P <sub>HIGH</sub> - 8) dB per tone  |
|  |                   |     | 12    |      | dBm     | 600 MHz < f ≤ 3000 MHz  |
|  |                   |     | 12    |      | dBm     | 3000 MHz < f ≤ 4800 MHz   |
|  |                   |     | 11    |      | dBm     | 4800 MHz < f ≤ 6000 MHz   |

| Parameter   | Symbol | Min | Typ  | Max  | Unit | Test Conditions/Comments   |
|---|--------|-----|------|------|------|--|
| Wide Band   |        |     | 7    |      | dBm  | 600 MHz < f ≤ 3000 MHz   |
|   |        |     | 7    |      | dBm  | 3000 MHz < f ≤ 4800 MHz  |
|   |        |     | 6    |      | dBm  | 4800 MHz < f ≤ 6000 MHz  |
| Third-Order Intermodulation Product   | IM3    |     | -70  |      | dBc  | IM3 product < 130 MHz at baseband, two tones, each at (P <sub>HIGH</sub> - 12) dB  |
|   |        |     | -67  |      | dBc  | 600 MHz < f ≤ 3000 MHz   |
|   |        |     | -62  |      | dBc  | 3000 MHz < f ≤ 4800 MHz  |
|   |        |     | -62  |      | dBc  | 4800 MHz < f ≤ 6000 MHz  |
| Fifth-Order Intermodulation Product (1800 MHz)  | IM5    |     | -80  |      | dBc  | IM5 product < 50 MHz at baseband, two tones, each at (P <sub>HIGH</sub> - 12) dB, 600 MHz < f ≤ 6000 MHz   |
| Seventh-Order Intermodulation Product (1800 MHz)  | IM7    |     | -80  |      | dBc  | IM7 product < 50 MHz at baseband, two tones, each at (P <sub>HIGH</sub> - 12) dB, 600 MHz < f ≤ 6000 MHz   |
| Spurious-Free Dynamic Range   | SFDR   |     | 70   |      | dB   | Non IMx related spurs, does not include HDx, (P <sub>HIGH</sub> - 9) dB input signal, 600 MHz < f ≤ 6000 MHz   |
| Harmonic Distortion Second-Order Harmonic Distortion Product  | HD2    |     | -80  |      | dBc  | (P <sub>HIGH</sub> - 11) dB input signal 75 MHz < f ≤ 600 MHz, (P <sub>HIGH</sub> - 9) dB input signal 600 MHz < f ≤ 6000 MHz, in band harmonic distortion falls within ±100 MHz |
|   |        |     | -80  |      | dBc  | Out of band harmonic distortion falls within ±225 MHz  |
| Third-Order Harmonic Distortion Product   | HD3    |     | -70  |      | dBc  | In band harmonic distortion falls within ±100 MHz  |
|   |        |     | -60  |      | dBc  | Out of band harmonic distortion falls within ±225 MHz  |
| Image Rejection   |        |     |      |      |      | QEC active   |
| Within Large Signal Bandwidth   |        |     | 65   |      | dB   |  |
| Outside Large Signal Bandwidth  |        |     | 55   |      | dB   |  |
| Input Impedance   |        |     | 100  |      | Ω    | Differential (see Figure 428)  |
| Isolation   |        |     |      |      |      |  |
| Transmitter 1 (Tx1) to Observation Receiver 1 (ORx1) and Transmitter 2 (Tx2) to Observation Receiver 2 (ORx2) |        |     | 100  |      | dB   | 75 MHz < f ≤ 600 MHz   |
|   |        |     | 65   |      | dB   | 600 MHz < f ≤ 5300 MHz   |
|   |        |     | 55   |      | dB   | 5300 MHz < f ≤ 6000 MHz  |
| Tx1 to ORx2 and Tx2 to ORx1   |        |     | 105  |      | dB   | 75 MHz < f ≤ 600 MHz   |
|   |        |     | 65   |      | dB   | 600 MHz < f ≤ 5300 MHz   |
|   |        |     | 55   |      | dB   | 5300 MHz < f ≤ 6000 MHz  |
| <b>RECEIVERS</b>  |        |     |      |      |      |  |
| Center Frequency  |        | 75  |      | 6000 | MHz  |  |
| Gain Range  |        |     | 30   |      | dB   |  |
| Analog Gain Step  |        |     | 0.5  |      | dB   | Attenuator steps from 0 dB to 6 dB   |
|   |        |     | 1    |      | dB   | Attenuator steps from 6 dB to 30 dB  |
| Bandwidth Ripple  |        |     | ±0.5 |      | dB   | 200 MHz bandwidth, compensated by programmable FIR filter  |
|   |        |     | ±0.2 |      | dB   | Any 20 MHz bandwidth span, compensated by programmable FIR filter  |



| Parameter  | Symbol            | Min | Typ   | Max | Unit | Test Conditions/Comments  |
|--|-------------------|-----|-------|-----|------|---|
| Receiver Bandwidth   |                   |     |       | 200 | MHz  |   |
| Receiver Alias Band Rejection                              |                   | 80  |       |     | dB   | Due to digital filters  |
| Maximum Useable Input Level                                | P <sub>HIGH</sub> |     |       |     |      | 0 dB attenuation, increases decibel for decibel with attenuation, CW = 1800 MHz, corresponds to -1 dBFS at ADC  |
| Noise Figure   | NF                |     | -11   |     | dBm  | 75 MHz < f ≤ 3000 MHz   |
|  |                   |     | -10.2 |     | dBm  | 3000 MHz < f ≤ 4800 MHz   |
|  |                   |     | -9.5  |     | dBm  | 4800 MHz < f ≤ 6000 MHz   |
|  |                   |     | 11.5  |     | dB   | 75 MHz < f ≤ 600 MHz  |
| Ripple   |                   |     | 12    |     | dB   | 600 MHz < f ≤ 3000 MHz  |
|  |                   |     | 13    |     | dB   | 3000 MHz < f ≤ 4800 MHz   |
|  |                   |     | 15.2  |     | dB   | 4800 MHz < f ≤ 6000 MHz   |
| Third-Order Input Intermodulation Intercept Point          | IIP3              |     |       |     |      |   |
| Difference Product   | IIP3D             |     | 12    |     | dBm  | 75 MHz < f ≤ 600 MHz, (P <sub>HIGH</sub> - 12) dB per tone, 600 MHz < f ≤ 6000 MHz, (P <sub>HIGH</sub> - 10) dB per tone, two tones near band edge                    |
| Sum Product  | IIP3S             |     | 12    |     | dBm  | 75 MHz < f ≤ 600 MHz, (P <sub>HIGH</sub> - 12) dB per tone, 600 MHz < f ≤ 6000 MHz, (P <sub>HIGH</sub> - 10) dB per tone, two tones at bandwidth/6 offset from the LO |
| Third-Order Harmonic Distortion Product                    | HD3               |     |       |     |      | 75 MHz < f ≤ 600 MHz, (P <sub>HIGH</sub> - 6) dB, 600 MHz < f ≤ 6000 MHz, (P <sub>HIGH</sub> - 4) dB, CW tone at bandwidth/6 offset from the LO                       |
| Second-Order Input Intermodulation Intercept Point         | IIP2              |     | -65   |     | dBc  | 75 MHz < f ≤ 600 MHz  |
|  |                   |     | -66   |     | dBc  | 600 MHz < f ≤ 4800 MHz  |
|  |                   |     | -62   |     | dBc  | 4800 MHz < f ≤ 6000 MHz   |
| Image Rejection  |                   |     | 62    |     | dBm  | 75 MHz < f ≤ 600 MHz, (P <sub>HIGH</sub> - 12) dB per tone, 600 MHz < f ≤ 6000 MHz, (P <sub>HIGH</sub> - 10) dB per tone, 0 dB attenuation, complex                   |
| Input Impedance  |                   |     | 75    |     | dB   | QEC active, within 200 MHz receiver bandwidth   |
| Receiver to Receiver Isolation                             |                   |     | 100   |     | Ω    | Differential (see Figure 429)   |
| Receiver Band Spurs Referenced to RF Input at Maximum Gain |                   |     | 77    |     | dB   | 75 MHz < f ≤ 600 MHz  |
|  |                   |     | 65    |     | dB   | 600 MHz < f ≤ 4800 MHz  |
|  |                   |     | 61    |     | dB   | 4800 MHz < f ≤ 6000 MHz   |
| Receiver LO Leakage at Receiver Input at Maximum Gain      |                   |     | -95   |     | dBm  | No more than one spur at this level per 10 MHz of receiver bandwidth  |
| Receiver LO Leakage at Receiver Input at Maximum Gain      |                   |     | -70   |     | dBm  | 75 MHz < f ≤ 600 MHz  |
|  |                   |     | -70   |     | dBm  | 600 MHz < f ≤ 3000 MHz  |
|  |                   |     | -65   |     | dBm  | 3000 MHz < f ≤ 6000 MHz   |

| Parameter                             | Symbol             | Min | Typ    | Max  | Unit   | Test Conditions/Comments  |
|---------------------------------------|--------------------|-----|--------|------|--------|---|
| <b>LO SYNTHESIZER</b>                 |                    |     |        |      |        |   |
| LO Frequency Step                     |                    |     | 2.3    |      | Hz     | 1.5 GHz to 2.8 GHz, 76.8 MHz phase frequency detector (PFD) frequency |
| LO Spur                               |                    |     | -85    |      | dBc    | Excludes integer boundary spurs                                       |
| Integrated Phase Noise                |                    |     |        |      |        | 2 kHz to 18 MHz   |
| 75 MHz LO                             |                    |     | 0.014  |      | °rms   | Narrow PLL loop bandwidth (50 kHz)                                    |
| 1900 MHz LO                           |                    |     | 0.2    |      | °rms   | Narrow PLL loop bandwidth (50 kHz)                                    |
| 3800 MHz LO                           |                    |     | 0.36   |      | °rms   | Wide PLL loop bandwidth (300 kHz)                                     |
| 5900 MHz LO                           |                    |     | 0.54   |      | °rms   | Wide PLL loop bandwidth (300 kHz)                                     |
| Spot Phase Noise                      |                    |     |        |      |        |   |
| 75 MHz LO                             |                    |     |        |      |        | Narrow PLL loop bandwidth   |
| 10 kHz Offset                         |                    |     | -126.5 |      | dBc/Hz |   |
| 100 kHz Offset                        |                    |     | -132.8 |      | dBc/Hz |   |
| 1 MHz Offset                          |                    |     | -150.1 |      | dBc/Hz |   |
| 10 MHz Offset                         |                    |     | -150.7 |      | dBc/Hz |   |
| 1900 MHz LO                           |                    |     |        |      |        | Narrow PLL loop bandwidth   |
| 100 kHz Offset                        |                    |     | -100   |      | dBc/Hz |   |
| 200 kHz Offset                        |                    |     | -115   |      | dBc/Hz |   |
| 400 kHz Offset                        |                    |     | -120   |      | dBc/Hz |   |
| 600 kHz Offset                        |                    |     | -129   |      | dBc/Hz |   |
| 800 kHz Offset                        |                    |     | -132   |      | dBc/Hz |   |
| 1.2 MHz Offset                        |                    |     | -135   |      | dBc/Hz |   |
| 1.8 MHz Offset                        |                    |     | -140   |      | dBc/Hz |   |
| 6 MHz Offset                          |                    |     | -150   |      | dBc/Hz |   |
| 10 MHz Offset                         |                    |     | -153   |      | dBc/Hz |   |
| 3800 MHz LO                           |                    |     |        |      |        | Wide PLL loop bandwidth   |
| 100 kHz Offset                        |                    |     | -104   |      | dBc/Hz |   |
| 1.2 MHz Offset                        |                    |     | -125   |      | dBc/Hz |   |
| 10 MHz Offset                         |                    |     | -145   |      | dBc/Hz |   |
| 5900 MHz LO                           |                    |     |        |      |        | Wide PLL loop bandwidth   |
| 100 kHz Offset                        |                    |     | -99    |      | dBc/Hz |   |
| 1.2 MHz Offset                        |                    |     | -119.7 |      | dBc/Hz |   |
| 10 MHz Offset                         |                    |     | -135.4 |      | dBc/Hz |   |
| <b>LO PHASE SYNCHRONIZATION</b>       |                    |     |        |      |        |   |
| Phase Deviation                       |                    |     | 1.6    |      | ps/°C  | Change in LO delay per temperature change                             |
| <b>EXTERNAL LO INPUT</b>              |                    |     |        |      |        |   |
| Input Frequency                       | f <sub>EXTLO</sub> | 150 |        | 8000 | MHz    | Input frequency must be 2 × the desired LO frequency                  |
| Input Signal Power                    |                    | 0   |        | 12   | dBm    | 50 Ω matching at the source   |
|                                       |                    |     | 3      |      | dBm    | f <sub>EXTLO</sub> ≤ 2 GHz, add 0.5 dBm/GHz above 2 GHz               |
|                                       |                    |     | 6      |      | dBm    | f <sub>EXTLO</sub> = 8 GHz  |
| External LO Input Signal Differential |                    |     |        |      |        | To ensure adequate QEC  |
| Phase Error                           |                    |     |        | 3.6  | ps     |   |
| Amplitude Error                       |                    |     |        | 1    | dB     |   |
| Duty Cycle Error                      |                    |     |        | 2    | %      |   |
| Even Order Harmonics                  |                    |     |        | -50  | dBc    |   |
| <b>CLOCK SYNTHESIZER</b>              |                    |     |        |      |        |   |
| Integrated Phase Noise                |                    |     |        |      |        | 1 kHz to 100 MHz  |
| 1966.08 MHz LO                        |                    |     | 0.4    |      | °rms   | PLL optimized for close in phase noise                                |

| Parameter  | Symbol | Min                        | Typ                    | Max                        | Unit         | Test Conditions/Comments   |
|--|--------|----------------------------|------------------------|----------------------------|--------------|--|
| Spot Phase Noise<br>1966.08 MHz<br>100 kHz Offset<br>1 MHz Offset<br>10 MHz Offset   |        |                            |                        |                            |              |  |
|  |        |                            | -109                   |                            | dBc/Hz       |  |
|  |        |                            | -129                   |                            | dBc/Hz       |  |
|  |        |                            | -149                   |                            | dBc/Hz       |  |
| REFERENCE CLOCK<br>(REF_CLK_IN±)<br>Frequency Range<br>Signal Level  |        | 10<br>0.3                  |                        | 1000<br>2.0                | MHz<br>V p-p | AC-coupled, common-mode voltage (VCM) = 618 mV, for best spurious performance use <1 V p-p input clock |
| AUXILIARY CONVERTERS   |        |                            |                        |                            |              |  |
| ADC  |        |                            |                        |                            |              |  |
| Resolution   |        |                            | 12                     |                            | Bits         |  |
| Input Voltage  |        |                            |                        |                            |              |  |
| Minimum  |        |                            | 0.05                   |                            | V            |  |
| Maximum  |        |                            | VDDA_<br>3P3 –<br>0.05 |                            | V            |  |
| DAC  |        |                            |                        |                            |              |  |
| Resolution   |        |                            | 10                     |                            | Bits         | Includes four offset levels  |
| Output Voltage   |        |                            |                        |                            |              |  |
| Minimum  |        |                            | 0.7                    |                            | V            | 1 V voltage reference (VREF)   |
| Maximum  |        |                            | VDDA_<br>3P3 – 0.3     |                            | V            | 2.5 V VREF   |
| Output Drive Capability  |        |                            | 10                     |                            | mA           |  |
| DIGITAL SPECIFICATIONS<br>(COMPLEMENTARY METAL-<br>OXIDE SEMICONDUCTOR<br>(CMOS)) FOR SPI, GPIO_x,<br>TXx_ENABLE, ORx_ENABLE |        |                            |                        |                            |              |  |
| Logic Inputs   |        |                            |                        |                            |              |  |
| Input Voltage  |        |                            |                        |                            |              |  |
| High Level   |        | VDD_<br>INTERFACE<br>× 0.8 |                        | VDD_<br>INTERFACE          | V            |  |
| Low Level  |        | 0                          |                        | VDD_<br>INTERFACE<br>× 0.2 | V            |  |
| Input Current  |        |                            |                        |                            |              |  |
| High Level   |        | -10                        |                        | +10                        | µA           |  |
| Low Level  |        | -10                        |                        | +10                        | µA           |  |
| Logic Outputs  |        |                            |                        |                            |              |  |
| Output Voltage   |        |                            |                        |                            |              |  |
| High Level   |        | VDD_<br>INTERFACE<br>× 0.8 |                        |                            | V            |  |
| Low Level  |        |                            |                        | VDD_<br>INTERFACE<br>× 0.2 | V            |  |
| Drive Capability   |        |                            | 3                      |                            | mA           |  |

| Parameter  | Symbol           | Min            | Typ  | Max             | Unit | Test Conditions/Comments            |
|--|------------------|----------------|------|-----------------|------|-------------------------------------|
| <b>DIGITAL SPECIFICATIONS (CMOS) FOR GPIO_3P3_x</b>                              |                  |                |      |                 |      |                                     |
| Logic Inputs   |                  |                |      |                 |      |                                     |
| Input Voltage  |                  |                |      |                 |      |                                     |
| High Level   |                  | VDDA_3P3 × 0.8 |      | VDDA_3P3        | V    |                                     |
| Low Level  |                  | 0              |      | VDDA_3P3 × 0.2  | V    |                                     |
| Input Current  |                  |                |      |                 |      |                                     |
| High Level   |                  | -10            |      | +10             | μA   |                                     |
| Low Level  |                  | -10            |      | +10             | μA   |                                     |
| Logic Outputs  |                  |                |      |                 |      |                                     |
| Output Voltage   |                  |                |      |                 |      |                                     |
| High Level   |                  | VDDA_3P3 × 0.8 |      |                 | V    |                                     |
| Low Level  |                  |                |      | VDDA_3P3 × 0.2  | V    |                                     |
| Drive Capability   |                  |                | 4    |                 | mA   |                                     |
| <b>DIGITAL SPECIFICATIONS (LOW VOLTAGE DIFFERENTIAL SIGNALING (LVDS))</b>        |                  |                |      |                 |      |                                     |
| Logic Inputs (SYSREF_IN±, SYNCINx±)  |                  |                |      |                 |      |                                     |
| Input Voltage Range  |                  | 825            |      | 1675            | mV   | Each differential input in the pair |
| Input Differential Voltage Threshold   |                  | -100           |      | +100            | mV   |                                     |
| Receiver Differential Input Impedance  |                  |                | 100  |                 | Ω    | Internal termination enabled        |
| Logic Outputs (SYNCOUTx±)  |                  |                |      |                 |      |                                     |
| Output Voltage   |                  |                |      |                 |      |                                     |
| High   |                  |                |      | 1375            | mV   | Programmable in 75 mV steps         |
| Low  |                  | 1025           |      |                 | mV   |                                     |
| Output Differential Voltage  |                  |                | 225  |                 | mV   |                                     |
| Output Offset Voltage  |                  |                | 1200 |                 | mV   |                                     |
| <b>SPI TIMING</b>  |                  |                |      |                 |      |                                     |
| SCLK Period  | t <sub>CP</sub>  | 20             |      |                 | ns   |                                     |
| SCLK Pulse Width   | t <sub>MP</sub>  | 10             |      |                 | ns   |                                     |
| $\overline{CS}$ Setup to First SCLK Rising Edge                                  | t <sub>SC</sub>  | 3              |      |                 | ns   |                                     |
| Last SCLK Falling Edge to $\overline{CS}$ Hold                                   | t <sub>HC</sub>  | 0              |      |                 | ns   |                                     |
| SDIO Data Input Setup to SCLK  | t <sub>S</sub>   | 2              |      |                 | ns   |                                     |
| SDIO Data Input Hold to SCLK   | t <sub>H</sub>   | 0              |      |                 | ns   |                                     |
| SCLK Rising Edge to Output Data Delay (3-Wire or 4-Wire Mode)                    | t <sub>CO</sub>  | 3              |      | 8               | ns   |                                     |
| Bus Turnaround Time, Read After Baseband Processor (BBP) Drives Last Address Bit | t <sub>HZM</sub> | t <sub>H</sub> |      | t <sub>CO</sub> | ns   |                                     |
| Bus Turnaround Time, Read After ADRV9009 Drives Last Data Bit                    | t <sub>HZS</sub> | 0              |      | t <sub>CO</sub> | ns   |                                     |

| Parameter                                      | Symbol           | Min   | Typ    | Max    | Unit         | Test Conditions/Comments   |
|--|------------------|-------|--------|--------|--------------|--|
| <b>JESD204B DATA OUTPUT TIMING</b>             |                  |       |        |        |              |  |
| Unit Interval                                  | UI               | 81.38 |        | 320    | ps           | AC-coupled   |
| Data Rate per Channel, Nonreturn to Zero (NRZ) |                  | 3125  |        | 12,288 | Mbps         |  |
| Rise Time                                      | $t_R$            | 24    | 39.5   |        | ps           | 20% to 80% in 100 $\Omega$ load  |
| Fall Time                                      | $t_F$            | 24    | 39.4   |        | ps           | 20% to 80% in 100 $\Omega$ load  |
| Output Common-Mode Voltage                     | $V_{CM}$         | 0     |        | 1.8    | V            | AC-coupled   |
| Differential Output Voltage                    | $V_{DIFF}$       | 360   | 600    | 770    | mV           |  |
| Short-Circuit Current                          | $I_{DSHORT}$     | -100  |        | +100   | mA           |  |
| Differential Termination Impedance             |                  | 80    | 94.2   | 120    | $\Omega$     |  |
| Total Jitter                                   |                  |       | 15.13  |        | ps           | Bit error rate (BER) = $10^{-15}$  |
| Uncorrelated Bounded High Probability Jitter   | UBHPJ            |       | 0.56   |        | ps           |  |
| Duty Cycle Distortion                          | DCD              |       | 0.369  |        | ps           |  |
| SYSREF_IN $\pm$ Setup Time to REF_CLK_IN $\pm$ |                  | 2.5   |        |        | ns           | See Figure 2   |
| SYSREF_IN $\pm$ Hold Time to REF_CLK_IN $\pm$  |                  | -1.5  |        |        | ns           | See Figure 2   |
| Latency  | $t_{LAT\_FRM}$   |       | 116.5  |        | Clock cycles | REF_CLK_IN $\pm$ = 245.76 MHz<br>Observation receiver bandwidth = 450 MHz, IQ rate = 491.52 MHz, lane rate = 9830.4 MHz, number of converters (M) = 4, number of lanes (L) = 2, converter resolution (N) = 16, number of samples per converter (S) = 1 |
|  |                  |       | 237.02 |        | ns           |  |
|  |                  |       | 89.4   |        | Clock cycles | Receiver bandwidth = 200 MHz, IQ rate = 245.76 MHz, lane rate = 9830.4 MHz, M = 2, L = 2, N = 16, S = 1  |
|  |                  |       | 364.18 |        | ns           |  |
| <b>JESD204B DATA INPUT TIMING</b>              |                  |       |        |        |              |  |
| Unit Interval                                  | UI               | 81.38 |        | 320    | ps           | AC-coupled   |
| Data Rate per Channel (NRZ)                    |                  | 3125  |        | 12288  | Mbps         |  |
| Differential Voltage                           | $V_{DIFF}$       | 125   |        | 750    | mV           |  |
| Termination Voltage (VTT) Source Impedance     | $Z_{TT}$         |       | 8.9    | 30     | $\Omega$     |  |
| Differential Impedance                         | $Z_{RDIFF}$      | 80    | 105.1  | 120    | $\Omega$     |  |
| Termination Voltage AC-Coupled                 | $V_{TT}$         | 1.267 |        | 1.33   | V            |  |
| Latency  | $t_{LAT\_DEFRM}$ |       | 74.45  |        | Clock cycles | Device clock = 245.76 MHz, transmitter bandwidth = 200 MHz, IQ rate = 491.52 MHz, lane rate = 9830.4 MHz, M = 2, L = 2, N = 16, S = 1  |
|  |                  |       | 153.5  |        | ns           |  |

<sup>1</sup> VDDA1P3 refers to all analog 1.3 V supplies, including: VDDA1P3\_RF\_SYNTH, VDDA1P3\_BB, VDDA1P3\_RX\_RF, VDDA1P3\_RX\_TX, VDDA1P3\_RF\_VCO\_LDO, VDDA1P3\_RF\_LO, VDDA1P3\_DES, VDDA1P3\_SER, VDDA1P3\_CLOCK\_SYNTH, VDDA1P3\_CLOCK\_VCO\_LDO, VDDA1P3\_AUX\_SYNTH, and VDDA1P3\_AUX\_VCO\_LDO.

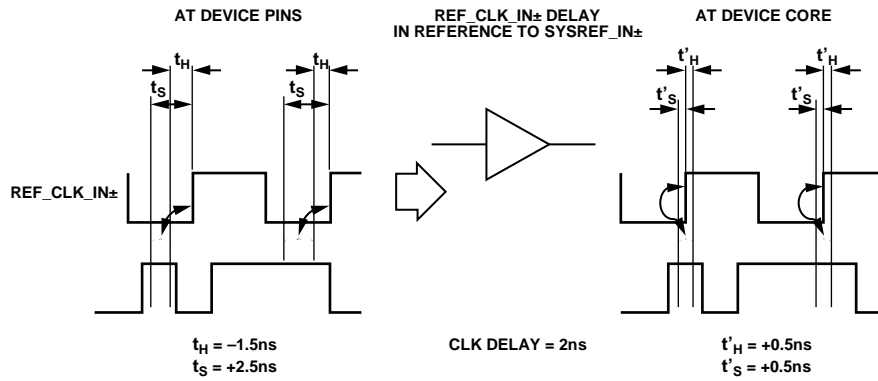
**CURRENT AND POWER CONSUMPTION SPECIFICATIONS**

Table 2.

| Parameter  | Min   | Typ  | Max   | Unit | Test Conditions/Comments  |
|--|-------|------|-------|------|---|
| <b>SUPPLY CHARACTERISTICS</b>                                |       |      |       |      |   |
| VDDA1P3 <sup>1</sup> Analog Supply                           | 1.267 | 1.3  | 1.33  | V    |   |
| VDDD1P3_DIG Supply   | 1.267 | 1.3  | 1.33  | V    |   |
| VDDA1P8_TX Supply  | 1.71  | 1.8  | 1.89  | V    |   |
| VDDA1P8_BB Supply  | 1.71  | 1.8  | 1.89  | V    |   |
| VDD_INTERFACE Supply   | 1.71  | 1.8  | 2.625 | V    | CMOS and LVDS supply, 1.8 V to 2.5 V nominal range  |
| VDDA_3P3 Supply  | 3.135 | 3.3  | 3.465 | V    |   |
| <b>POSITIVE SUPPLY CURRENT</b>                               |       |      |       |      |   |
| 450 MHz Transmitter Bandwidth, Observation Receiver Disabled |       |      |       |      |   |
| VDDA1P3 <sup>1</sup> Analog Supply                           |       | 1520 |       | mA   | LO at 2600 MHz  |
| VDDD1P3_DIG Supply   |       | 619  |       | mA   | Two transmitters enabled  |
| VDDA1P8_TX Supply  |       | 455  |       | mA   | Transmitter QEC active  |
|  |       | 135  |       | mA   | Transmitter RF attenuation = 0 dB, full-scale CW  |
| VDDA1P8_BB Supply  |       | 30   |       | mA   | Transmitter RF attenuation = 15 dB, full-scale CW   |
| VDD_INTERFACE Supply   |       | 8    |       | mA   | VDD_INTERFACE = 2.5 V   |
| VDDA_3P3 Supply  |       | 3    |       | mA   | No Auxiliary DAC x or AUXADC_x enabled, if enabled, AUXADC_x adds 2.7 mA and each Auxiliary DAC x adds 1.5 mA   |
| Total Power Dissipation                                      |       | 3.68 |       | W    | Typical supply voltages, 0 dB transmitter attenuation, transmitter QEC active   |
|  |       | 3.11 |       | W    | Typical supply voltages, 15 dB transmitter attenuation, transmitter QEC active  |
| 450 MHz Transmitter Bandwidth, Observation Receiver Enabled  |       |      |       |      |   |
| VDDA1P3 <sup>1</sup> Analog Supply                           |       | 2073 |       | mA   | Two transmitters enabled, one ORx enabled   |
| VDDD1P3_DIG Supply   |       | 1541 |       | mA   | Transmitter QEC tracking active, observation receiver QEC enabled, transmitter LTE20 centered on LO, observation receiver LTE20 at -16 dBm centered on LO |
|  |       | 2100 |       | mA   | Transmitter two tone = -99 MHz and 100 MHz at -7 dBFS each, observation receiver one tone = 100 MHz at -16 dBm  |
| VDDA1P8_TX Supply  |       | 455  |       | mA   | Transmitter RF attenuation = 0 dB, full scale CW  |
|  |       | 135  |       | mA   | Transmitter RF attenuation = 15 dB, full scale CW   |
| VDDA1P8_BB Supply  |       | 63   |       | mA   |   |
| VDD_INTERFACE Supply   |       | 8    |       | mA   | VDD_INTERFACE = 2.5 V   |
| VDDA_3P3 Power Supply  |       | 3    |       | mA   | No Auxiliary DAC x or AUXADC_x enabled, if enabled, AUXADC_x adds 2.7 mA and each Auxiliary DAC x adds 1.5 mA   |
| Total Power Dissipation                                      |       | 5.66 |       | W    | Typical supply voltages, 0 dB transmitter attenuation, transmitter QEC active   |
|  |       | 5.08 |       | W    | Typical supply voltages, 15 dB transmitter attenuation, transmitter QEC active  |
| 200 MHz Receiver Bandwidth, Observation Receiver Disabled    |       |      |       |      |   |
| VDDA1P3 <sup>1</sup> Analog Supply                           |       | 1645 |       | mA   | Two receivers enabled   |
| VDDD1P3_DIG Supply   |       | 984  |       | mA   | Receiver QEC active   |
| VDDA1P8_TX Supply  |       | 0.4  |       | mA   |   |
| VDDA1P8_BB Supply  |       | 68   |       | mA   |   |
| VDD_INTERFACE Supply   |       | 8    |       | mA   |   |
| VDDA_3P3 Supply  |       | 3    |       | mA   | No Auxiliary DAC x or AUXADC_x enabled, if enabled, AUXADC_x adds 2.7 mA and each Auxiliary DAC x adds 1.5 mA   |
| Total Power Dissipation                                      |       | 3.57 |       | W    | Typical supply voltages, receiver QEC active  |

<sup>1</sup> VDDA1P3 refers to all analog 1.3 V supplies, including: VDDA1P3\_RF\_SYNTH, VDDA1P3\_BB, VDDA1P3\_RX\_RF, VDDA1P3\_RX\_TX, VDDA1P3\_RF\_VCO\_LDO, VDDA1P3\_RF\_LO, VDDA1P3\_DES, VDDA1P3\_SER, VDDA1P3\_CLOCK\_SYNTH, VDDA1P3\_CLOCK\_VCO\_LDO, VDDA1P3\_AUX\_SYNTH, and VDDA1P3\_AUX\_VCO\_LDO.

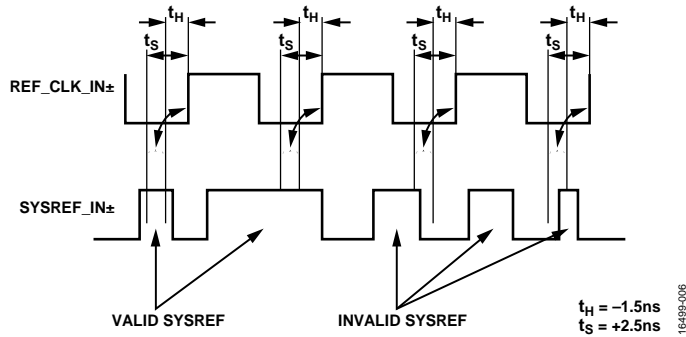
TIMING DIAGRAMS



NOTES  
1.  $t_H$  AND  $t_S$  ARE THE HOLD AND SETUP TIMES FOR THE REF\_CLK\_IN± PINS.  $t'_H$  AND  $t'_S$  REFER TO THE DELAYED HOLD AND SETUP TIMES AT THE DEVICE CORE IN REFERENCE TO THE SYSREF\_N± SIGNALS DUE TO AN INTERNAL BUFFER THAT THE SIGNAL PASSES THROUGH.

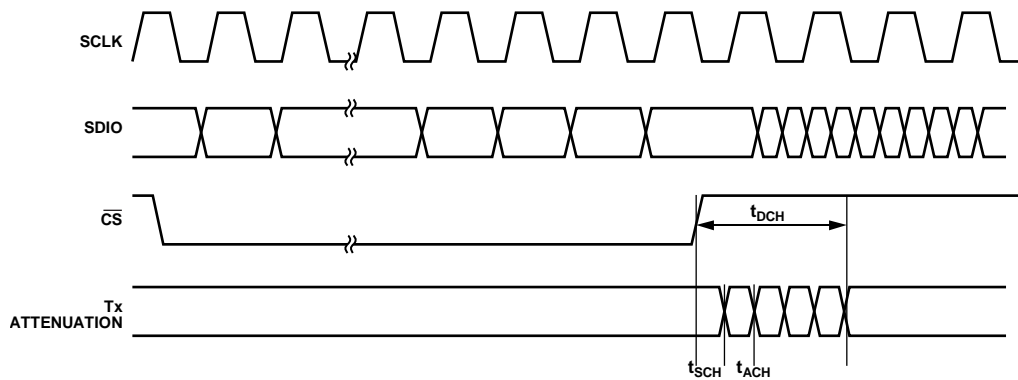
16499-005

Figure 2. SYSREF\_IN± Setup and Hold Timing



16499-006

Figure 3. SYSREF\_IN± Setup and Hold Timing Examples, Relative to Device Clock



16499-007

Figure 4. Transmitter Attenuation Update via SPI 2 Port

## ABSOLUTE MAXIMUM RATINGS

Table 3.

| Parameter  | Rating                          |
|--|---------------------------------|
| VDDA1P3 <sup>1</sup> to VSSA                           | -0.3 V to +1.4 V                |
| VDDD1P3_DIG to VSSD                                    | -0.3 V to +1.4 V                |
| VDD_INTERFACE to VSSA                                  | -0.3 V to +3.0 V                |
| VDDA_3P3 to VSSA                                       | -0.3 V to +3.9 V                |
| VDDA1P8_TX to VSSA                                     | -0.3 V to +2.0 V                |
| VDD_INTERFACE Logic Inputs and Outputs to VSSD         | -0.3 V to VDD_INTERFACE + 0.3 V |
| JESD204B Logic Outputs to VSSA                         | -0.3 V to VDDA1P3_SER           |
| JESD204B Logic Inputs to VSSA                          | -0.3 V to VDDA1P3_DES +0.3 V    |
| Input Current to any Pin Except Supplies               | ±10 mA                          |
| Maximum Input Power into RF Port                       | 23 dBm (peak)                   |
| Maximum Transmitter Voltage Standing Wave Ratio (VSWR) | 3:1                             |
| Maximum T <sub>J</sub>                                 | 110°C                           |
| Storage Temperature Range                              | -65°C to +150°C                 |

<sup>1</sup> VDDA1P3 refers to all analog 1.3 V supplies.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

### REFLOW PROFILE

The ADRV9009 reflow profile is in accordance with the JEDEC JESD204B criteria for Pb-free devices. The maximum reflow temperature is 260°C.

### THERMAL MANAGEMENT

The ADRV9009 is a high power device that can dissipate over 3 W depending on the user application and configuration. Because of the power dissipation, the ADRV9009 uses an exposed die package to provide the customer with the most effective method of controlling the die temperature. The exposed die allows cooling of the die directly. Figure 5 shows the profile view of the device mounted to a user printed circuit board (PCB) and a heat sink (typically the aluminum case) to keep the junction (exposed die) below the maximum T<sub>J</sub> detailed in Table 3. The device is designed for a lifetime of 10 years when operating at the maximum T<sub>J</sub>.

### THERMAL RESISTANCE

Thermal performance is directly linked to PCB design and operating environment. Careful attention to PCB thermal design is required.

θ<sub>JA</sub> is the natural convection junction to ambient thermal resistance measured in a circuit board for surface-mount packages.

θ<sub>JC\_TOP</sub> is the conduction thermal resistance from junction to case where the case temperature is measured at the top of the package.

Thermal resistance data for the ADRV9009 mounted on both a JEDEC 2S2P test board and a 10-layer Analog Devices, Inc., evaluation board is listed in Table 4. Do not exceed the absolute maximum T<sub>J</sub> rating in Table 3. Ten-layer PCB entries refer to the 10-layer Analog Devices evaluation board, which more accurately reflects the PCB used in customer applications.

Table 4. Thermal Resistance<sup>1,2</sup>

| Package Type | θ <sub>JA</sub> | θ <sub>JC_TOP</sub> | θ <sub>JB</sub> | ψ <sub>JT</sub> | ψ <sub>JB</sub> | Unit |
|--------------|-----------------|---------------------|-----------------|-----------------|-----------------|------|
| BC-196-13    | 21.1            | 0.04                | 4.9             | 0.3             | 4.9             | °C/W |

<sup>1</sup> For the θ<sub>JC</sub> test, 100 μm thermal interface material (TIM) is used. TIM is assumed to have 3.6 thermal conductivity watts/(meter × Kelvin).

<sup>2</sup> Using enhanced heat removal techniques such as PCB, heat sink, and airflow improves the thermal resistance values.

### ESD CAUTION



#### ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

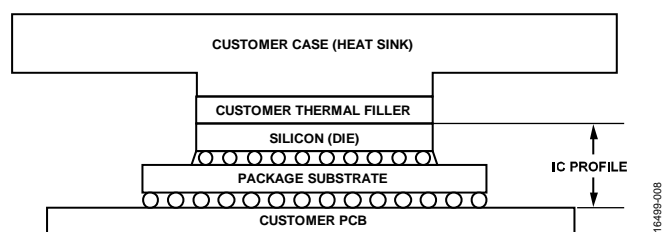


Figure 5. Typical Thermal Management Solution



### PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

|   | 1                     | 2          | 3             | 4          | 5                   | 6                  | 7                | 8                 | 9              | 10                  | 11       | 12            | 13         | 14          |
|---|-----------------------|------------|---------------|------------|---------------------|--------------------|------------------|-------------------|----------------|---------------------|----------|---------------|------------|-------------|
| A | VSSA                  | ORX2_IN+   | ORX2_IN-      | VSSA       | RX2_IN+             | RX2_IN-            | VSSA             | VSSA              | RX1_IN+        | RX1_IN-             | VSSA     | ORX1_IN+      | ORX1_IN-   | VSSA        |
| B | VDDA1P3_RX_RF         | VSSA       | VSSA          | VSSA       | VSSA                | VSSA               | RF_EXT_LO_I/O-   | RF_EXT_LO_I/O+    | VSSA           | VSSA                | VSSA     | VSSA          | VSSA       | VSSA        |
| C | GPIO_3P3_0            | GPIO_3P3_3 | VDDA1P3_RX_TX | VSSA       | VDDA1P3_RF_VCO_LDO  | VDDA1P3_RF_VCO_LDO | VDDA1P1_RF_VCO   | VDDA1P3_RF_LO     | VSSA           | VDDA1P3_AUX_VCO_LDO | VSSA     | VDDA_3P3      | GPIO_3P3_9 | RBIAS       |
| D | GPIO_3P3_1            | GPIO_3P3_4 | VSSA          | VSSA       | VSSA                | VSSA               | VSSA             | VSSA              | VSSA           | VDDA1P1_AUX_VCO     | VSSA     | VSSA          | GPIO_3P3_8 | GPIO_3P3_10 |
| E | GPIO_3P3_2            | GPIO_3P3_5 | GPIO_3P3_6    | VDDA1P8_BB | VDDA1P3_BB          | VSSA               | REF_CLK_IN+      | REF_CLK_IN-       | VSSA           | AUX_SYNTH_OUT       | AUXADC_3 | VDDA1P8_TX    | GPIO_3P3_7 | GPIO_3P3_11 |
| F | VSSA                  | VSSA       | AUXADC_0      | AUXADC_1   | VSSA                | VSSA               | VSSA             | VSSA              | VSSA           | VSSA                | AUXADC_2 | VSSA          | VSSA       | VSSA        |
| G | VSSA                  | VSSA       | VSSA          | VSSA       | VDDA1P3_CLOCK_SYNTH | VSSA               | VDDA1P3_RF_SYNTH | VDDA1P3_AUX_SYNTH | RF_SYNTH_VTUNE | VSSA                | VSSA     | VSSA          | VSSA       | VSSA        |
| H | TX2_OUT-              | VSSA       | VSSA          | VSSA       | VSSA                | VSSA               | VSSA             | VSSA              | VSSA           | VSSA                | GPIO_12  | GPIO_11       | VSSA       | TX1_OUT+    |
| J | TX2_OUT+              | VSSA       | GPIO_18       | RESET      | GP_INTERRUPT        | TEST               | GPIO_2           | GPIO_1            | SDIO           | SDO                 | GPIO_13  | GPIO_10       | VSSA       | TX1_OUT-    |
| K | VSSA                  | VSSA       | SYSREF_IN+    | SYSREF_IN- | GPIO_5              | GPIO_4             | GPIO_3           | GPIO_0            | SCLK           | CS                  | GPIO_14  | GPIO_9        | VSSA       | VSSA        |
| L | VSSA                  | VSSA       | SYNCIN1-      | SYNCIN1+   | GPIO_6              | GPIO_7             | VSSD             | VDDD1P3_DIG       | VDDD1P3_DIG    | VSSD                | GPIO_15  | GPIO_8        | SYNCOUT1-  | SYNCOUT1+   |
| M | VDDA1P1_CLOCK_VCO     | VSSA       | SYNCIN0-      | SYNCIN0+   | RX1_ENABLE          | TX1_ENABLE         | RX2_ENABLE       | TX2_ENABLE        | VSSA           | GPIO_17             | GPIO_16  | VDD_INTERFACE | SYNCOUT0-  | SYNCOUT0+   |
| N | VDDA1P3_CLOCK_VCO_LDO | VSSA       | SERDOUT3-     | SERDOUT3+  | SERDOUT2-           | SERDOUT2+          | VSSA             | VDDA1P3_SER       | VDDA1P3_DES    | SERDIN1-            | SERDIN1+ | SERDIN0-      | SERDIN0+   | VSSA        |
| P | AUX_SYNTH_VTUNE       | VSSA       | VSSA          | SERDOUT1-  | SERDOUT1+           | SERDOUT0-          | SERDOUT0+        | VDDA1P3_SER       | VDDA1P3_DES    | VSSA                | SERDIN3- | SERDIN3+      | SERDIN2-   | SERDIN2+    |

ADRV9009

Figure 6. Pin Configuration

Table 5. Pin Function Descriptions

| Pin No.  | Type  | Mnemonic           | Description   |
|--|-------|--------------------|---|
| A1, A4, A7, A8, A11, A14, B2 to B6, B9 to B14, C4, C9, C11, D3 to D9, D11, D12, E6, E9, F1, F2, F5 to F10, F12 to F14, G1 to G4, G6, G10 to G14, H2 to H10, H13, J2, J13, K1, K2, K13, K14, L1, L2, M2, M9, N2, N7, N14, P2, P3, P10 | Input | VSSA               | Analog Supply Voltage (V <sub>SS</sub> ).   |
| A2, A3   | Input | ORX2_IN+, ORX2_IN- | Differential Input for Observation Receiver 2. When unused, connect these pins to ground. |

| Pin No.  | Type             | Mnemonic                           | Description  |
|----------|------------------|------------------------------------|--|
| A5, A6   | Input            | RX2_IN+, RX2_IN-                   | Differential Input for Main Receiver 2. When unused, connect these pins to ground.   |
| A9, A10  | Input            | RX1_IN+, RX1_IN-                   | Differential Input for Main Receiver 1. When unused, connect these pins to ground.   |
| A12, A13 | Input            | ORX1_IN+, ORX1_IN-                 | Differential Input for Observation Receiver 1. When unused, connect these pins to ground.  |
| B1       | Input            | VDDA1P3_RX_RF                      | Observation Receiver Supply.   |
| B7, B8   | Input            | RF_EXT_LO_I/O-,<br>RF_EXT_LO_I/O+, | Differential External LO Input/Output. If these pins are used for the external LO, the input frequency must be 2x the desired carrier frequency. When unused, do not connect these pins.   |
| C1       | Input/<br>output | GPIO_3P3_0                         | GPIO Pin Referenced to 3.3 V Supply. The alternate function is AUXDAC_4. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or this pin can be left floating, programmed as outputs, and driven low.     |
| C2       | Input/<br>output | GPIO_3P3_3                         | GPIO Pin Referenced to 3.3 V Supply. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or these pins can be left floating, programmed as outputs, and driven low.                                       |
| C13      | Input/<br>output | GPIO_3P3_9                         | GPIO Pin Referenced to 3.3 V Supply. The alternative function is AUXDAC_9. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or these pins can be left floating, programmed as outputs, and driven low. |
| D1       | Input/<br>output | GPIO_3P3_1                         | GPIO Pin Referenced to 3.3 V Supply. The alternative function is AUXDAC_5. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or these pins can be left floating, programmed as outputs, and driven low. |
| D2       | Input/<br>output | GPIO_3P3_4                         | GPIO Pin Referenced to 3.3 V Supply. The alternative function is AUXDAC_6. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or these pins can be left floating, programmed as outputs, and driven low. |
| D13      | Input/<br>output | GPIO_3P3_8                         | GPIO Pin Referenced to 3.3 V Supply. The alternative function is AUXDAC_1. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or these pins can be left floating, programmed as outputs, and driven low. |
| D14      | Input/<br>output | GPIO_3P3_10                        | GPIO Pin Referenced to 3.3 V Supply. The alternative function is AUXDAC_0. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or these pins can be left floating, programmed as outputs, and driven low. |
| E1       | Input/<br>output | GPIO_3P3_2                         | GPIO Pin Referenced to 3.3 V Supply. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or these pins can be left floating, programmed as outputs, and driven low.                                       |
| E2       | Input/<br>output | GPIO_3P3_5                         | GPIO Pin Referenced to 3.3 V Supply. The alternative function is AUXDAC_7. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or these pins can be left floating, programmed as outputs, and driven low. |
| E3       | Input/<br>output | GPIO_3P3_6                         | GPIO Pin Referenced to 3.3 V Supply. The alternative function is AUXDAC_8. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or these pins can be left floating, programmed as outputs, and driven low. |

| Pin No.          | Type         | Mnemonic                    | Description  |
|------------------|--------------|-----------------------------|--|
| E13              | Input/output | GPIO_3P3_7                  | GPIO Pin Referenced to 3.3 V Supply. The alternative function is AUXDAC_2. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or these pins can be left floating, programmed as outputs, and driven low. |
| E14              | Input/output | GPIO_3P3_11                 | GPIO Pin Referenced to 3.3 V Supply. The alternative function is AUXDAC_3. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or these pins can be left floating, programmed as outputs, and driven low. |
| C3               | Input        | VDDA1P3_RX_TX               | 1.3 V Supply for Transmitter/Receiver Baseband Circuits, Transimpedance Amplifier (TIA), Transmitter Transconductance (GM), Baseband Filters, and Auxiliary DACs.  |
| C5, C6           | Input        | VDDA1P3_RF_VCO_LDO          | RF VCO LDO Supply Inputs. Connect Pin C5 to Pin C6. Use a separate trace on the PCB back to a common supply point.   |
| C7               | Input        | VDDA1P1_RF_VCO              | 1.1 V VCO Supply. Decouple this pin with 1 $\mu$ F.  |
| C8               | Input        | VDDA1P3_RF_LO               | 1.3 V LO Generator for the RF Synthesizer. This pin is sensitive to supply noise.  |
| C10              | Input        | VDDA1P3_AUX_VCO_LDO         | 1.3 V Supply.  |
| C12              | Input        | VDDA_3P3                    | General-Purpose Output Pull-Up Voltage and Auxiliary DAC Supply Voltage.   |
| C14              | Input/output | RBIAS                       | Bias Resistor. Tie this pin to ground using a 14.3 k $\Omega$ resistor. This pin generates an internal current based on an external 1% resistor.   |
| D10              | Input        | VDDA1P1_AUX_VCO             | 1.1 V VCO Supply. Decouple this pin with 1 $\mu$ F.  |
| E4               | Input        | VDDA1P8_BB                  | 1.8 V Supply for the ADC and DAC.  |
| E5               | Input        | VDDA1P3_BB                  | 1.3 V Supply for the ADC, DAC, and AUXADC.   |
| E7, E8           | Input        | REF_CLK_IN+,<br>REF_CLK_IN- | Device Clock Differential Input.   |
| E10              | Output       | AUX_SYNTH_OUT               | Auxiliary PLL Output. When unused, do not connect this pin.  |
| E12              | Input        | VDDA1P8_TX                  | 1.8 V Supply for Transmitter.  |
| F3, F4, F11, E11 | Input        | AUXADC_0 to AUXADC_3        | Auxiliary ADC Input. When unused, connect these pins to ground with a pull-down resistor, or connect directly to ground.   |
| G5               | Input        | VDDA1P3_CLOCK_SYNTH         | 1.3 V Supply Input for Clock Synthesizer. Use a separate trace on the PCB back to a common supply point.   |
| G7               | Input        | VDDA1P3_RF_SYNTH            | 1.3 V RF Synthesizer Supply Input. This pin is sensitive to supply noise.  |
| G8               | Input        | VDDA1P3_AUX_SYNTH           | 1.3 V Auxiliary Synthesizer Supply Input.  |
| G9               | Output       | RF_SYNTH_VTUNE              | RF Synthesizer VTUNE Output.   |
| H11              | Input/output | GPIO_12                     | Digital GPIO, 1.8 V to 2.5 V. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or it can be left floating, programmed as output, and driven low.   |
| H12              | Input/output | GPIO_11                     | Digital GPIO, 1.8 V to 2.5 V. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or it can be left floating, programmed as output, and driven low.   |
| J11              | Input/output | GPIO_13                     | Digital GPIO, 1.8 V to 2.5 V. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or it can be left floating, programmed as output, and driven low.   |
| J12              | Input/output | GPIO_10                     | Digital GPIO, 1.8 V to 2.5 V. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or it can be left floating, programmed as output, and driven low.   |

| Pin No. | Type         | Mnemonic | Description   |
|---------|--------------|----------|---|
| J3      | Input/output | GPIO_18  | Digital GPIO, 1.8 V to 2.5 V. The joint test action group (JTAG) function is TCLK. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or it can be left floating, programmed as output, and driven low. |
| J7      | Input/output | GPIO_2   | Digital GPIO, 1.8 V to 2.5 V. The user sets the JTAG function to 0. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or it can be left floating, programmed as output, and driven low.                |
| J8      | Input/output | GPIO_1   | Digital GPIO, 1.8 V to 2.5 V. The user sets the JTAG function to 0. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or it can be left floating, programmed as output, and driven low.                |
| K5      | Input/output | GPIO_5   | Digital GPIO, 1.8 V to 2.5 V. The JTAG function is TDO. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or it can be left floating, programmed as output, and driven low.                            |
| K6      | Input/output | GPIO_4   | Digital GPIO, 1.8 V to 2.5 V. The JTAG function is $\overline{\text{TRST}}$ . Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or it can be left floating, programmed as output, and driven low.      |
| K7      | Input/output | GPIO_3   | Digital GPIO, 1.8 V to 2.5 V. The user sets the JTAG function to 1. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or it can be left floating, programmed as output, and driven low.                |
| K8      | Input/output | GPIO_0   | Digital GPIO, 1.8 V to 2.5 V. The user sets the JTAG function to 1. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or it can be left floating, programmed as output, and driven low.                |
| K11     | Input/output | GPIO_14  | Digital GPIO, 1.8 V to 2.5 V. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or it can be left floating, programmed as output, and driven low.  |
| K12     | Input/output | GPIO_9   | Digital GPIO, 1.8 V to 2.5 V. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or it can be left floating, programmed as output, and driven low.  |
| L5      | Input/output | GPIO_6   | Digital GPIO, 1.8 V to 2.5 V. The JTAG function is TDI. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or it can be left floating, programmed as output, and driven low.                            |
| L6      | Input/output | GPIO_7   | Digital GPIO, 1.8 V to 2.5 V. The JTAG function is TMS. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or it can be left floating, programmed as output, and driven low.                            |
| L11     | Input/output | GPIO_15  | Digital GPIO, 1.8 V to 2.5 V. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or it can be left floating, programmed as output, and driven low.  |

| Pin No.  | Type         | Mnemonic               | Description  |
|----------|--------------|------------------------|--|
| L12      | Input/output | GPIO_8                 | Digital GPIO, 1.8V to 2.5V. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or it can be left floating, programmed as output, and driven low. |
| M10      | Input/output | GPIO_17                | Digital GPIO, 1.8V to 2.5V. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or it can be left floating, programmed as output, and driven low. |
| M11      | Input/output | GPIO_16                | Digital GPIO, 1.8V to 2.5V. Because this pin contains an input stage, the voltage on the pin must be controlled. When unused, this pin can be tied to ground through a resistor (to safeguard against misconfiguration), or it can be left floating, programmed as output, and driven low. |
| H14, J14 | Output       | TX1_OUT+, TX1_OUT-     | Transmitter 1 Output. When unused, do not connect these pins.  |
| H1, J1   | Output       | TX2_OUT-, TX2_OUT+     | Transmitter 2 Output. When unused, do not connect these pins.  |
| J4       | Input        | RESET                  | Active Low Chip Reset.   |
| J5       | Output       | GP_INTERRUPT           | General-Purpose Digital Interrupt Output Signal. When unused, do not connect this pin.   |
| J6       | Input        | TEST                   | Pin Used for JTAG Boundary Scan. When unused, connect this pin to ground.  |
| J9       | Input/output | SDIO                   | Serial Data Input in 4-Wire Mode or Input/Output in 3-Wire Mode.   |
| J10      | Output       | SDO                    | Serial Data Output. In SPI 3-wire mode, do not connect this pin.   |
| K3, K4   | Input        | SYSREF_IN+, SYSREF_IN- | LVDS Input.  |
| K9       | Input        | SCLK                   | Serial Data Bus Clock.   |
| K10      | Input        | CS                     | Serial Data Bus Chip Select, Active Low.   |
| L3, L4   | Input        | SYNCIN1-, SYNCIN1+     | LVDS Input. These pins form the sync signal associated with receiver channel data on the JESD204B interface. When unused, connect these pins to ground with a pull-down resistor, or connect these pins directly to ground.  |
| L7, L10  | Input        | VSSD                   | Digital V <sub>SS</sub> .  |
| L8, L9   | Input        | VDDD1P3_DIG            | 1.3 V Digital Core. Connect Pin L8 and Pin L9 together. Use a wide trace to connect to a separate power supply domain.   |
| L13, L14 | Output       | SYNCOUT1-, SYNCOUT1+   | LVDS Output. These pins form the sync signal associated with transmitter channel data on the JESD204B interface. When unused, do not connect these pins.   |
| M1       | Input        | VDDA1P1_CLOCK_VCO      | 1.1 V VCO Supply. Decouple this pin with 1 μF.   |
| M3, M4   | Input        | SYNCIN0-, SYNCIN0+     | LVDS Input. These pins form the sync signal associated with receiver channel data on the JESD204B interface. When unused, connect these pins to ground with a pull-down resistor, or connect these pins directly to ground.  |
| M5       | Input        | RX1_ENABLE             | Receiver 1 Enable Pin. When unused, connect this pin to ground with a pull-down resistor, or connect this pin directly to ground.  |
| M6       | Input        | TX1_ENABLE             | Transmitter 1 Enable Pin. When unused, connect this pin to ground with a pull-down resistor, or connect this pin directly to ground.   |
| M7       | Input        | RX2_ENABLE             | Receiver 2 Enable Pin. When unused, connect this pin to ground with a pull-down resistor, or connect this pin directly to ground.  |
| M8       | Input        | TX2_ENABLE             | Transmitter 2 Enable Pin. When unused, connect this pin to ground with a pull-down resistor, or connect this pin directly to ground.   |
| M12      | Input        | VDD_INTERFACE          | Input/Output Interface Supply, 1.8V to 2.5V.   |
| M13, M14 | Output       | SYNCOUT0-, SYNCOUT0+   | LVDS Output. These pins form the sync signal associated with transmitter channel data on the JESD204B interface. When unused, do not connect these pins.   |

| <b>Pin No.</b> | <b>Type</b> | <b>Mnemonic</b>           | <b>Description</b>   |
|----------------|-------------|---------------------------|--|
| N1             | Input       | VDDA1P3_CLOCK_<br>VCO_LDO | 1.3 V Use Separate Trace to Common Supply Point.   |
| N3, N4         | Output      | SERDOUT3-, SERDOUT3+      | RF Current Mode Logic (CML) Differential Output 3. When unused, do not connect these pins. |
| N5, N6         | Output      | SERDOUT2-, SERDOUT2+      | RF CML Differential Output 2. When unused, do not connect these pins.                      |
| N8, P8         | Input       | VDDA1P3_SER               | 1.3 V Supply for JESD204B Serializer.  |
| N9, P9         | Input       | VDDA1P3_DES               | 1.3 V Supply for JESD204B Deserializer.  |
| N10, N11       | Input       | SERDIN1-, SERDIN1+        | RF CML Differential Input 1. When unused, do not connect these pins.                       |
| N13, N12       | Input       | SERDIN0+, SERDIN0-        | RF CML Differential Input 0. When unused, do not connect these pins.                       |
| P1             | Output      | AUX_SYNTH_VTUNE           | Auxiliary Synthesizer VTUNE Output.  |
| P4, P5         | Output      | SERDOUT1-, SERDOUT1+,     | RF CML Differential Output 1. When unused, do not connect these pins.                      |
| P6, P7         | Output      | SERDOUT0-,<br>SERDOUT0+,  | RF CML Differential Output 0. When unused, do not connect these pins.                      |
| P11, P12       | Input       | SERDIN3-, SERDIN3+        | RF CML Differential Input 3. When unused, do not connect these pins.                       |
| P13, P14       | Input       | SERDIN2-, SERDIN2+        | RF CML Differential Input 2. When unused, do not connect these pins.                       |

# TYPICAL PERFORMANCE CHARACTERISTICS

The temperature settings refer to the die temperature

## 75 MHz TO 525 MHz BAND

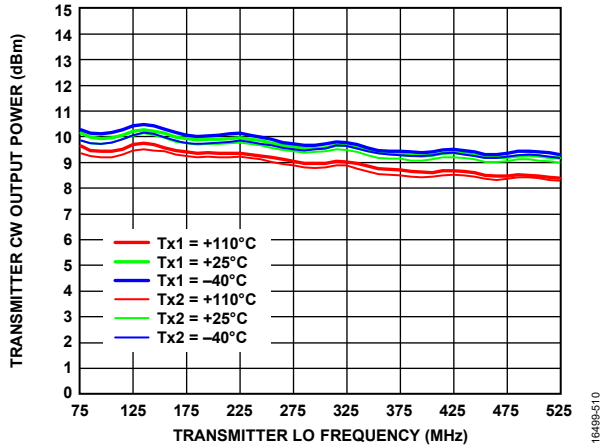


Figure 7. Transmitter CW Output Power vs. Transmitter LO Frequency, Transmitter QEC and External LO Leakage Active, Transmitter 50 MHz/100 MHz Bandwidth Mode, IQ Rate = 122.88 MHz, Attenuation = 0 dB, Not De-Embedded

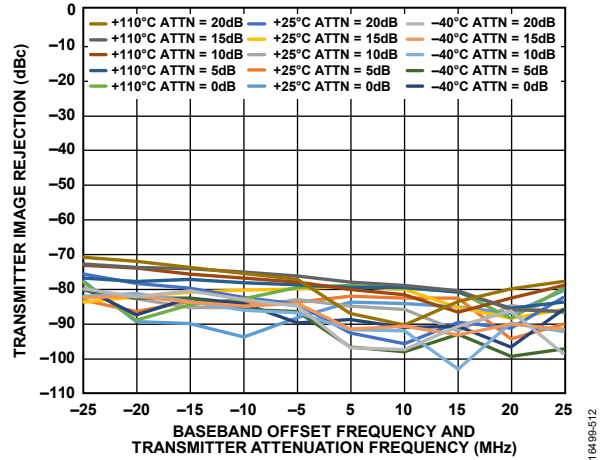


Figure 9. Transmitter Image Rejection vs. Baseband Offset Frequency and Transmitter Attenuation, QEC Trained with Three Tones Placed at 10 MHz, 48 MHz, and 100 MHz (Tracking On), Total Combined Power = -10 dBFS, Correction Then Frozen (Tracking Turned Off), CW Tone Swept Across Large Signal Bandwidth, LO = 300 MHz

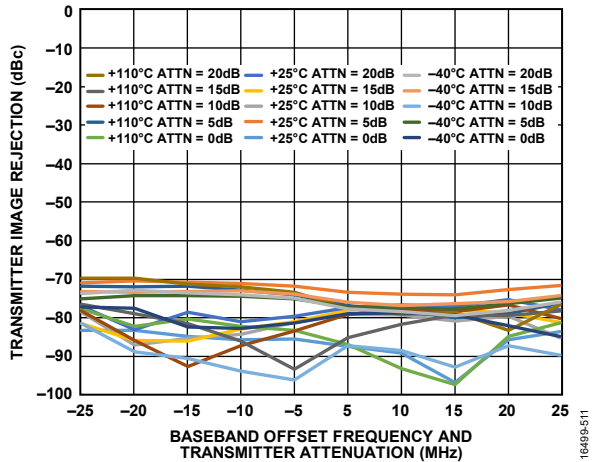


Figure 8. Transmitter Image Rejection vs. Baseband Offset Frequency and Transmitter Attenuation, QEC Trained with Three Tones Placed at 10 MHz, 48 MHz, and 100 MHz (Tracking On), Total Combined Power = -10 dBFS, Correction Then Frozen (Tracking Turned Off), CW Tone Swept Across Large Signal Bandwidth, LO = 75.2 MHz

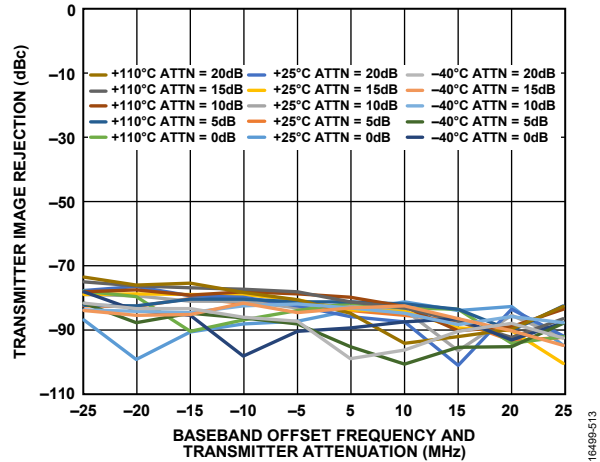


Figure 10. Transmitter Image Rejection vs. Baseband Offset Frequency and Transmitter Attenuation, QEC Trained with Three Tones Placed at 10 MHz, 48 MHz, and 100 MHz (Tracking On), Total Combined Power = -10 dBFS, Correction Then Frozen (Tracking Turned Off), CW Tone Swept Across Large Signal Bandwidth, LO = 525 MHz

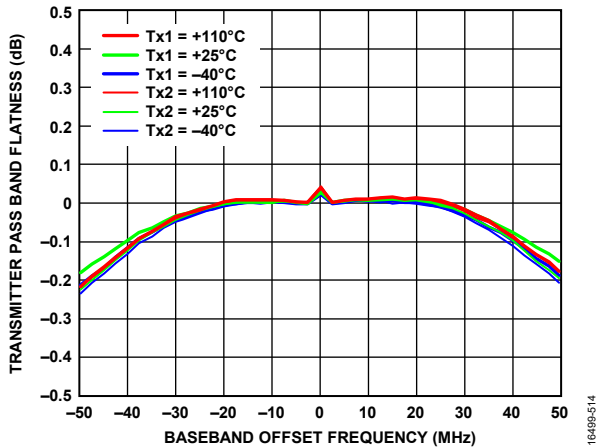


Figure 11. Transmitter Pass Band Flatness vs. Baseband Offset Frequency, Off Chip Match Response De-Embedded, LO = 300 MHz, Calibrated at 25°C

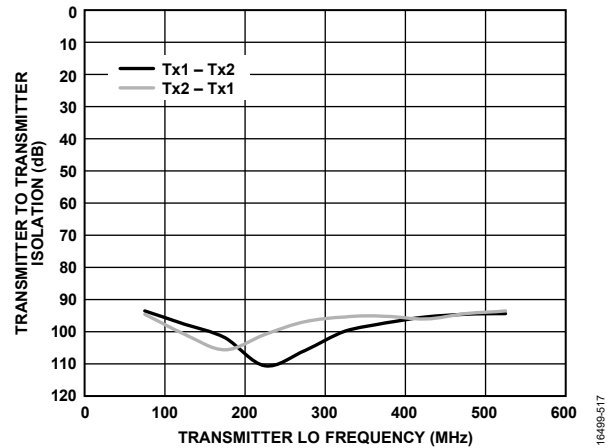


Figure 14. Transmitter to Transmitter Isolation vs. Transmitter LO Frequency, Temperature = 25°C

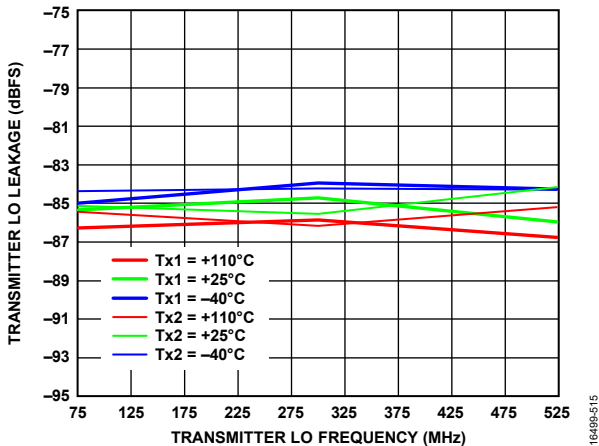


Figure 12. Transmitter LO Leakage vs. Transmitter LO Frequency, Transmitter Attenuation = 0 dB, Baseband Tone Frequency = 10 MHz, Tracked

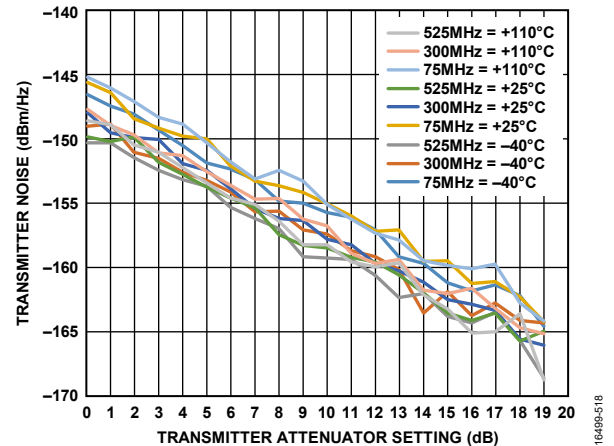


Figure 15. Transmitter Noise vs. Transmitter Attenuator Setting, Offset = 50 MHz

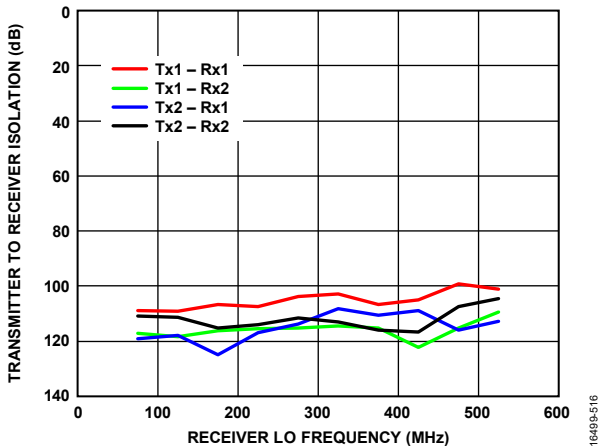


Figure 13. Transmitter to Receiver Isolation vs. Receiver LO Frequency, Temperature = 25°C

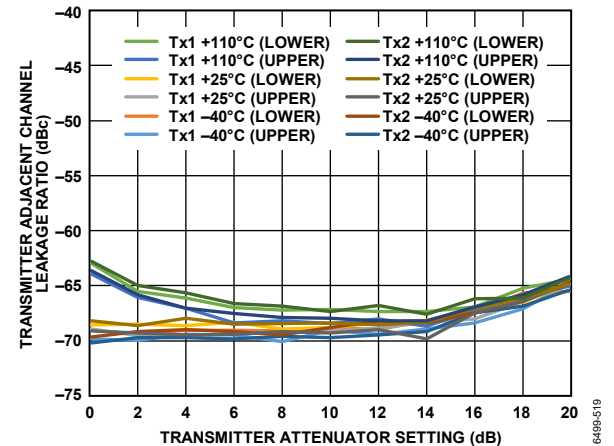


Figure 16. Transmitter Adjacent Channel Leakage Ratio vs. Transmitter Attenuator Setting, Signal Offset = 0 MHz, LO = 75 MHz, LTE = 20 MHz, Peak to Average Ratio (PAR) = 12 dB, DAC Boost Normal, Upper Side and Lower Side, Performance Limited by Spectrum Analyzer at Higher Attenuation Settings



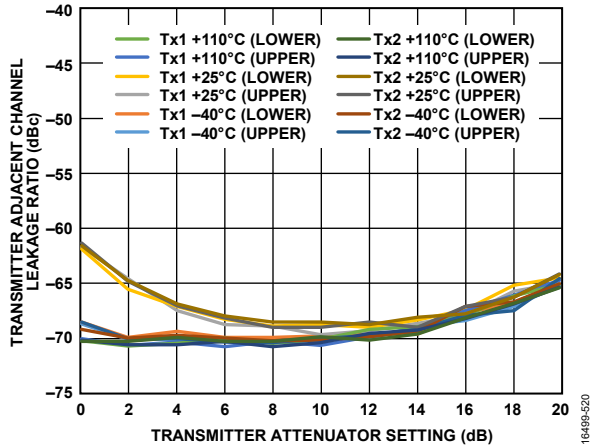


Figure 17. Transmitter Adjacent Channel Leakage Ratio vs. Transmitter Attenuator Setting, Signal Offset = 0 MHz, LO = 300 MHz, LTE = 20 MHz, PAR = 12 dB, DAC Boost Normal, Upper Side and Lower Side, Performance Limited by Spectrum Analyzer at Higher Attenuation Settings

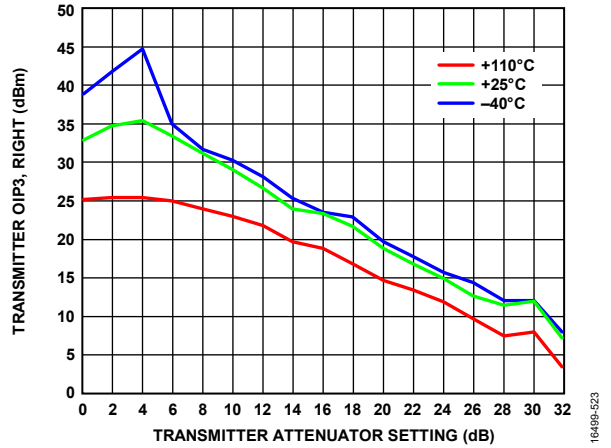


Figure 20. Transmitter OIP3 Right vs. Transmitter Attenuator Setting, LO = 300 MHz, Total RMS Power = -12 dBFS, 20 MHz/25 MHz Tones

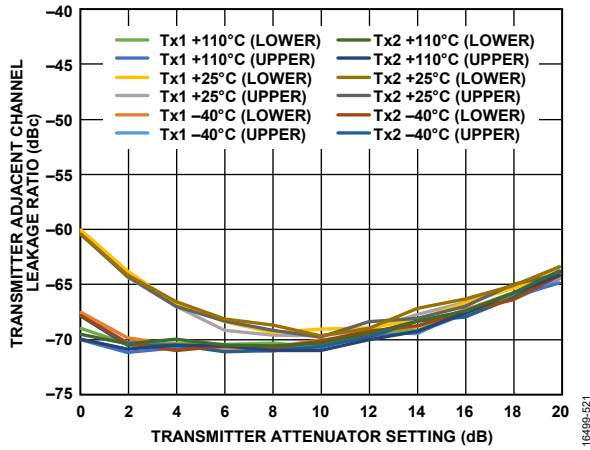


Figure 18. Transmitter Adjacent Channel Leakage Ratio vs. Transmitter Attenuator Setting, Signal Offset = 0 MHz, LO = 525 MHz, LTE = 20 MHz, PAR = 12 dB, DAC Boost Normal, Upper Side and Lower Side, Performance Limited by Spectrum Analyzer at Higher Attenuation Settings

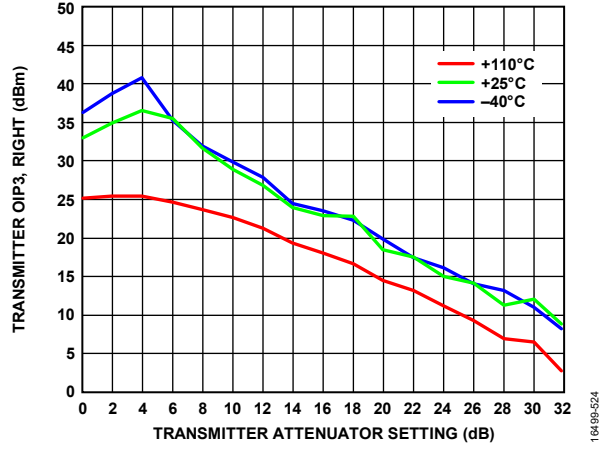


Figure 21. Transmitter OIP3 Right vs. Transmitter Attenuator Setting, LO = 525 MHz, Total RMS Power = -12 dBFS, 20 MHz/25 MHz Tones

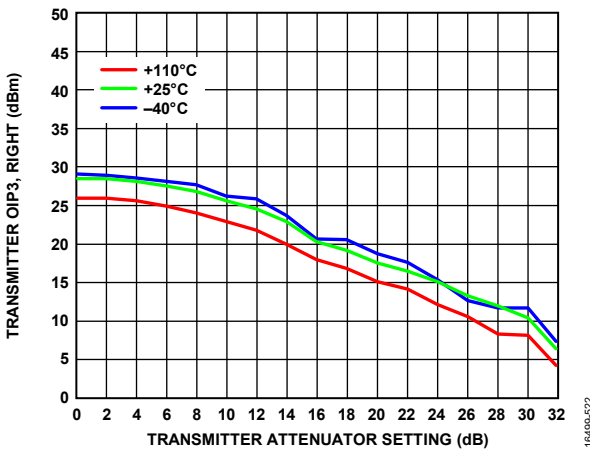


Figure 19. Transmitter OIP3 Right vs. Transmitter Attenuator Setting, LO = 75 MHz, Total Root Mean Square (RMS) Power = -12 dBFS, 20 MHz/25 MHz Tones

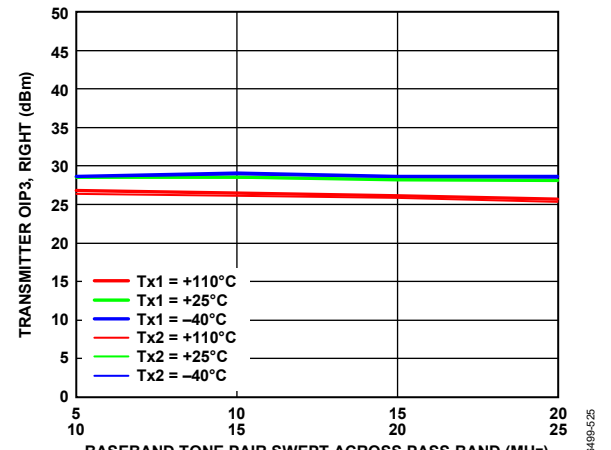


Figure 22. Transmitter OIP3 Right vs. Baseband Tone Pair Swept Across Pass Band, LO = 75 MHz, Total RMS Power = -12 dBFS, Transmitter Attenuation = 4 dB

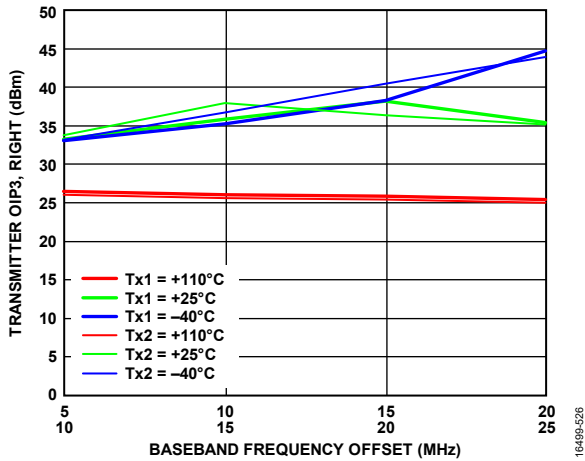


Figure 23. Transmitter OIP3 Right vs. Baseband Frequency Offset, LO = 300 MHz, Total RMS Power = -12 dBFS, Transmitter Attenuation = 4 dB

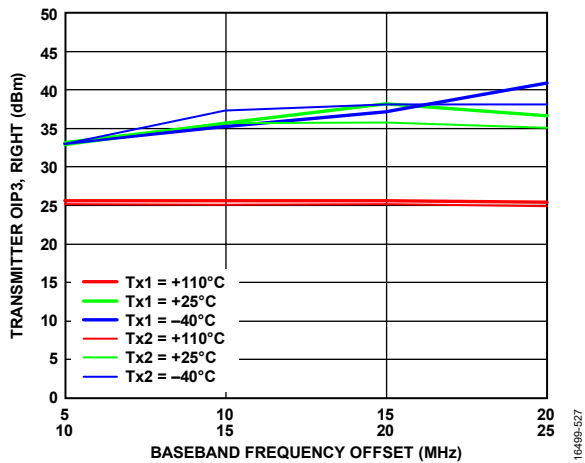


Figure 24. Transmitter OIP3 Right vs. Baseband Frequency Offset, LO = 525 MHz, Total RMS Power = -12 dBFS, Transmitter Attenuation = 4 dB

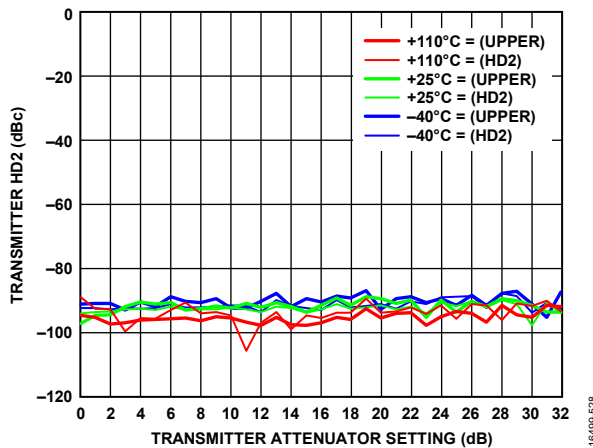


Figure 25. Transmitter HD2 vs. Transmitter Attenuator Setting, Baseband Frequency = 10 MHz, LO = 75 MHz, CW = -15 dBFS

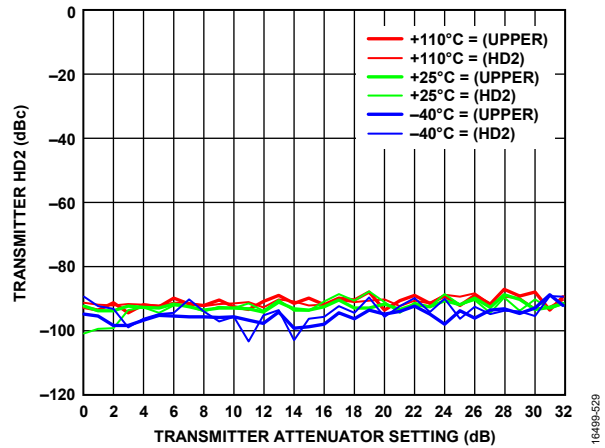


Figure 26. Transmitter HD2 vs. Transmitter Attenuator Setting, Baseband Frequency = 10 MHz, LO = 300 MHz, CW = -15 dBFS

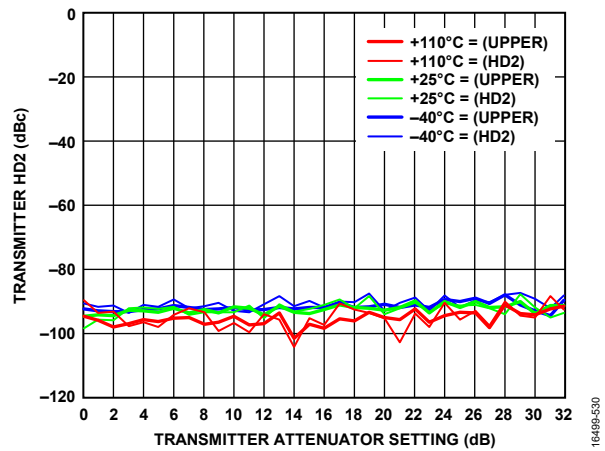


Figure 27. Transmitter HD2 vs. Transmitter Attenuator Setting, Baseband Frequency = 10 MHz, LO = 525 MHz, CW = -15 dBFS

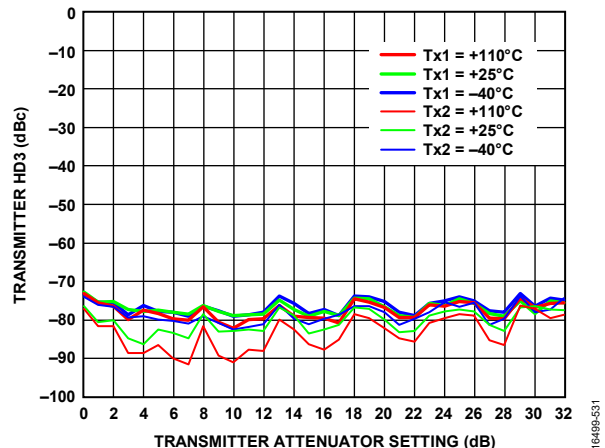


Figure 28. Transmitter HD3 vs. Transmitter Attenuator Setting, LO = 75 MHz, CW = -15 dBFS, Baseband Frequency = 10 MHz

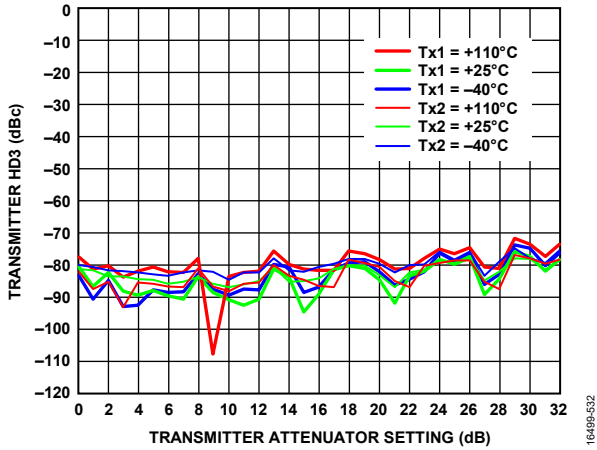


Figure 29. Transmitter HD3 vs. Transmitter Attenuator Setting, LO = 300 MHz, CW = -15 dBFS, Baseband Frequency = 10 MHz

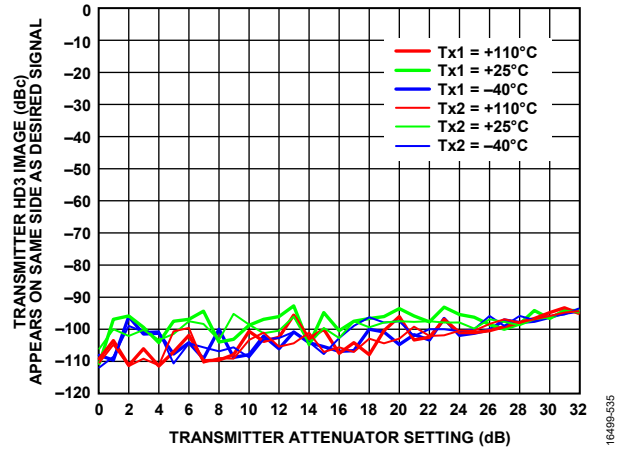


Figure 32. Transmitter HD3 Image Appears on Same Side as Desired Signal vs. Transmitter Attenuator Setting, LO = 300 MHz, CW = -15 dBFS

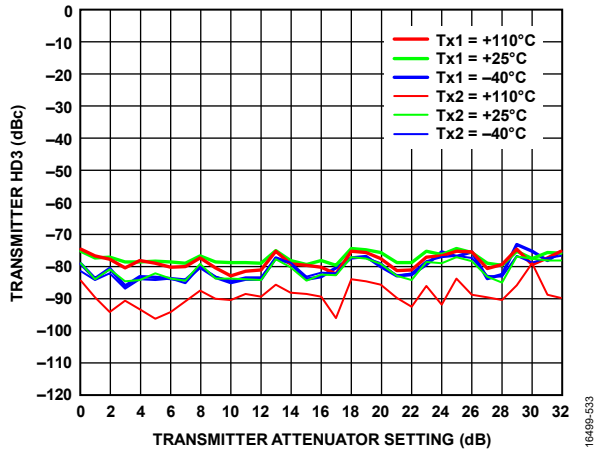


Figure 30. Transmitter HD3 vs. Transmitter Attenuator Setting, LO = 525 MHz, CW = -15 dBFS, Baseband Frequency = 10 MHz

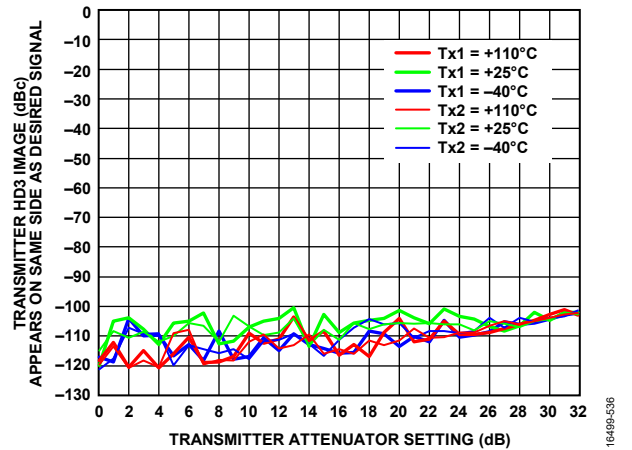


Figure 33. Transmitter HD3 Image Appears on Same Side as Desired Signal vs. Transmitter Attenuator Setting, LO = 525 MHz, CW = -15 dBFS

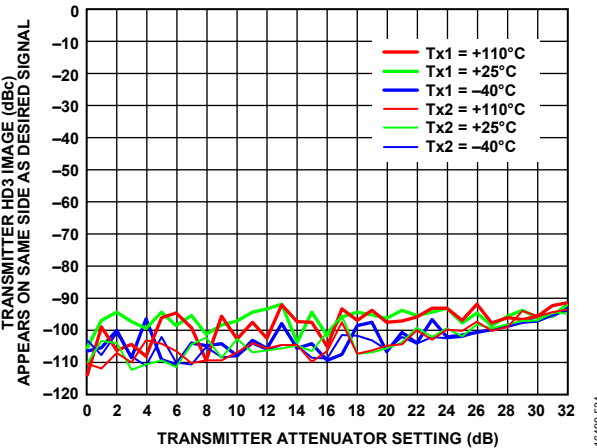


Figure 31. Transmitter HD3 Image Appears on Same Side as Desired Signal vs. Transmitter Attenuator Setting, LO = 75 MHz, CW = -15 dBFS

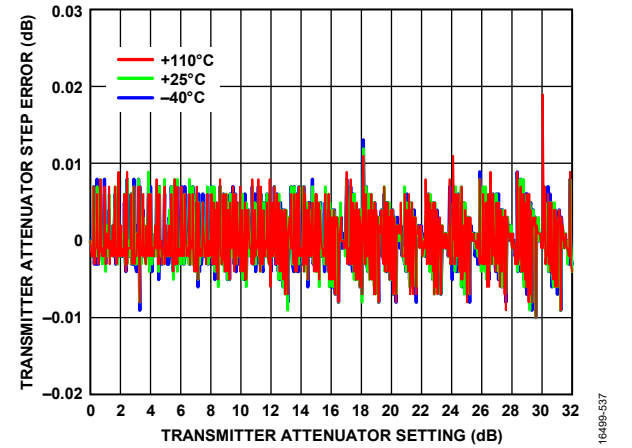


Figure 34. Transmitter Attenuator Step Error vs. Transmitter Attenuator Setting, LO = 75 MHz, Baseband Frequency = 10 MHz, Backoff = 15 dBFS

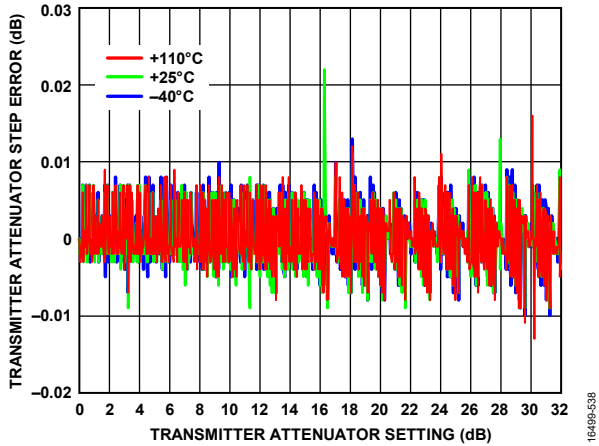


Figure 35. Transmitter Attenuator Step Error vs. Transmitter Attenuator Setting, LO = 300 MHz, Baseband Frequency = 10 MHz, Backoff = 15 dBFS

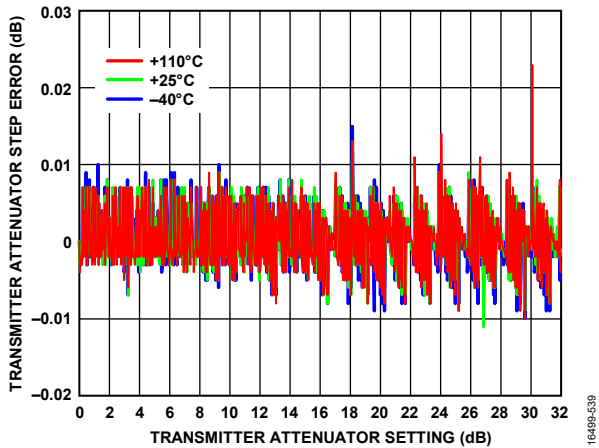


Figure 36. Transmitter Attenuator Step Error vs. Transmitter Attenuator Setting, LO = 525 MHz, Baseband Frequency = 10 MHz, Backoff = 15 dBFS

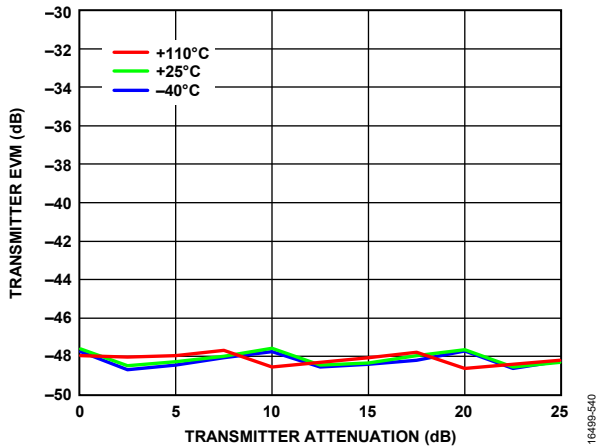


Figure 37. Transmitter EVM vs. Transmitter Attenuation, LTE = 20 MHz, Signal Centered on DC, LO = 75 MHz

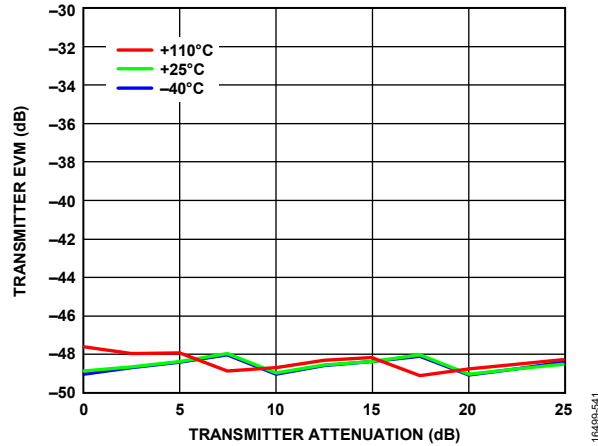


Figure 38. Transmitter EVM vs. Transmitter Attenuation, LTE = 20 MHz, Signal Centered on DC, LO = 300 MHz

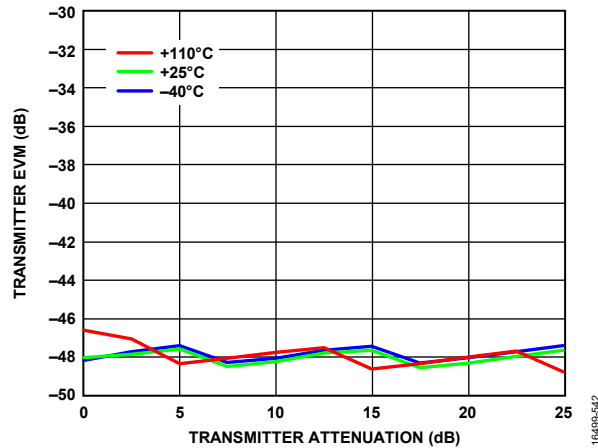


Figure 39. Transmitter EVM vs. Transmitter Attenuation, LTE = 20 MHz, Signal Centered on DC, LO = 525 MHz

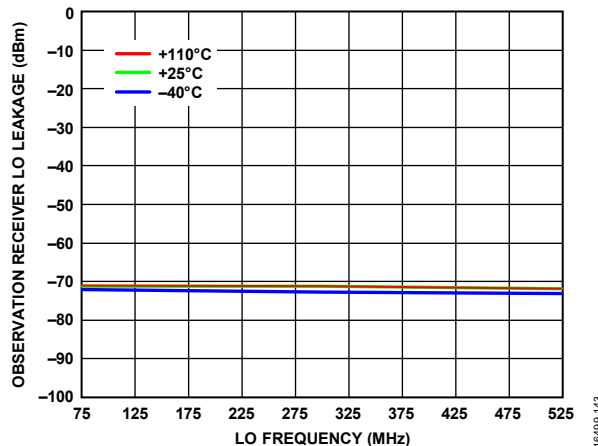


Figure 40. Observation Receiver LO Leakage vs. LO Frequency, LO = 75 MHz, 300 MHz, and 525 MHz, Attenuation = 0 dB

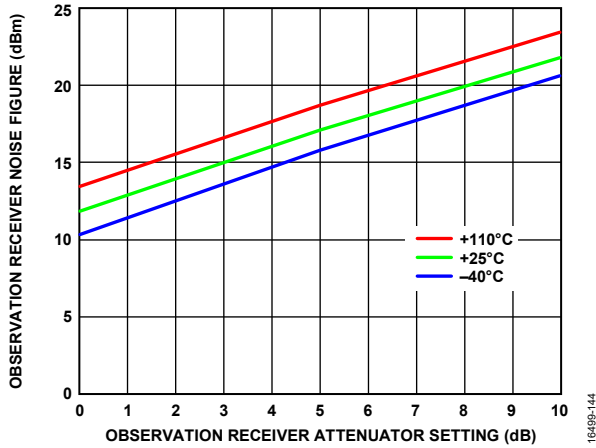


Figure 41. Observation Receiver Noise Figure vs. Observation Receiver Attenuator Setting, LO = 75 MHz, Total Nyquist Integration Bandwidth

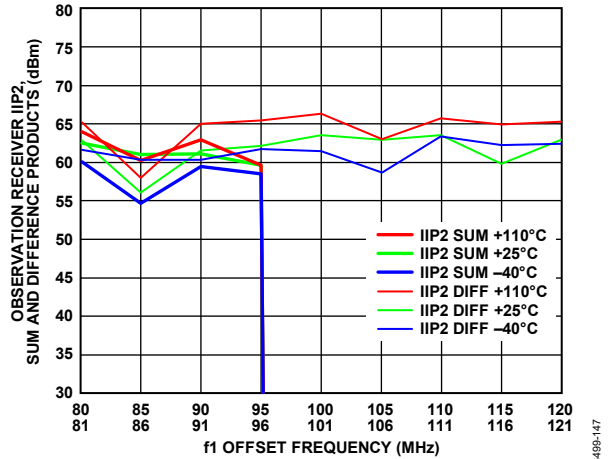


Figure 44. Observation Receiver IIP2, Sum and Difference Products vs.  $f_1$  Offset Frequency, Tones Separated by 1 MHz Swept Across Pass Band at -25 dBm Each, LO = 75 MHz, Attenuation = 0 dB

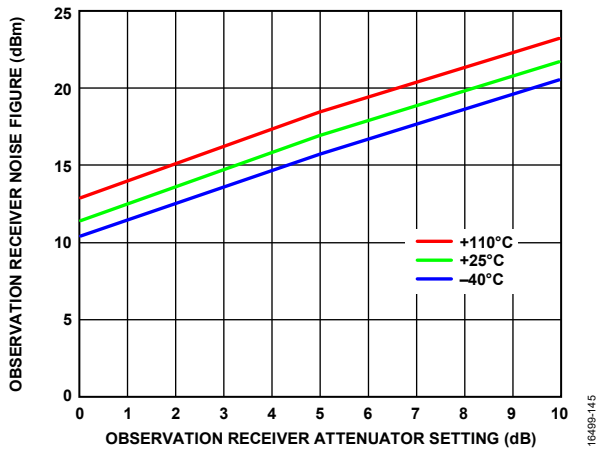


Figure 42. Observation Receiver Noise Figure vs. Observation Receiver Attenuator Setting, LO = 300 MHz, Total Nyquist Integration Bandwidth

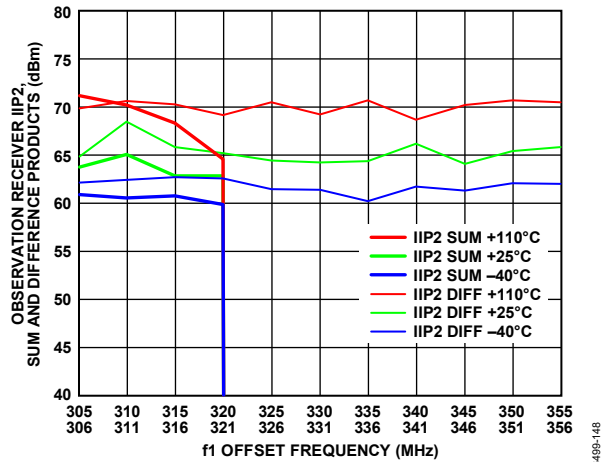


Figure 45. Observation Receiver IIP2, Sum and Difference Products vs.  $f_1$  Offset Frequency, Tones Separated by 1 MHz Swept Across Pass Band at -25 dBm Each, LO = 300 MHz, Attenuation = 0 dB

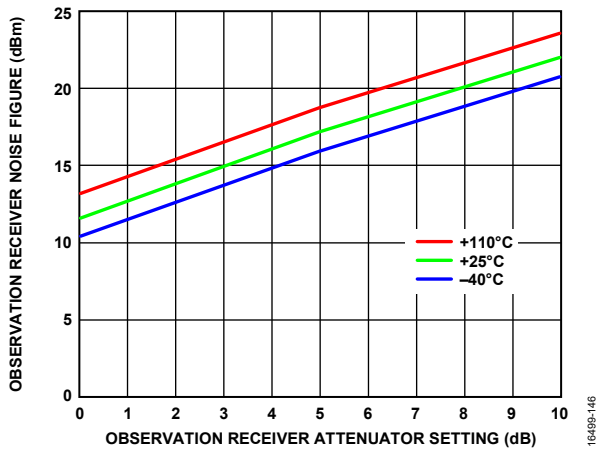


Figure 43. Observation Receiver Noise Figure vs. Observation Receiver Attenuator Setting, LO = 525 MHz, Total Nyquist Integration Bandwidth

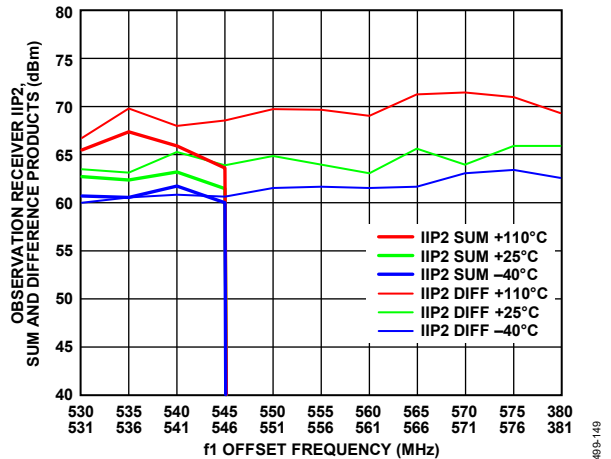


Figure 46. Observation Receiver IIP2, Sum and Difference Products vs.  $f_1$  Offset Frequency, Tones Separated by 1 MHz Swept Across Pass Band at -25 dBm Each, LO = 525 MHz, Attenuation = 0 dB

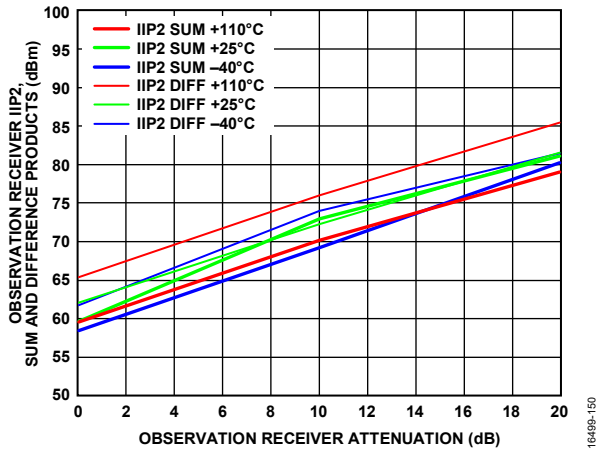


Figure 47. Observation Receiver IIP2, Sum and Difference Products vs. Observation Receiver Attenuation, LO = 75 MHz, Tone 1 = 95 MHz, Tone 2 = 96 MHz at -25 dBm Plus Attenuation

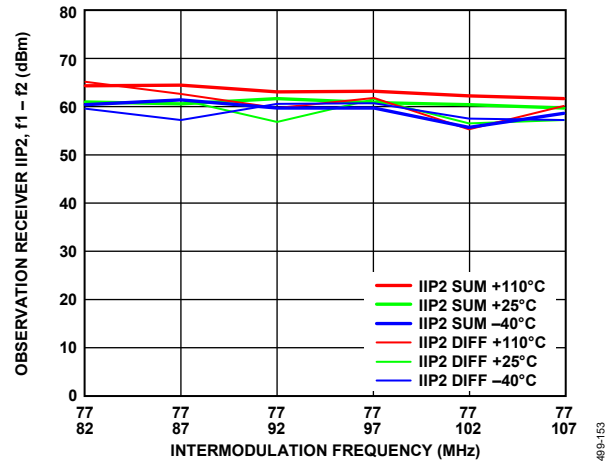


Figure 50. Observation Receiver IIP2,  $f_1 - f_2$  (Where  $f_2$  is Frequency 2) vs. Intermodulation Frequency, LO = 75 MHz, Tone 1 = 77 MHz, Tone 2 = Swept, -25 dBm Each, Attenuation = 0 dB

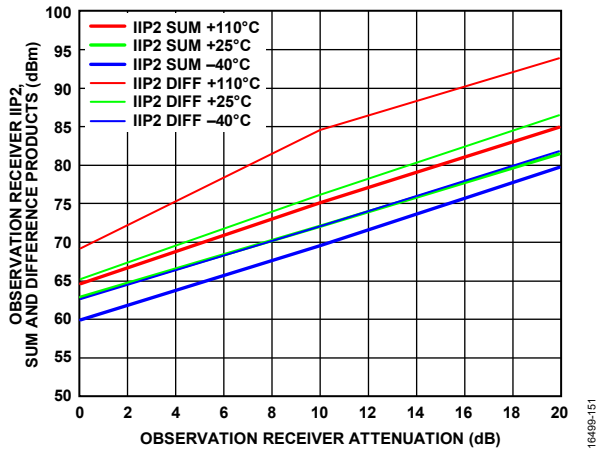


Figure 48. Observation Receiver IIP2, Sum and Difference Products vs. Observation Receiver Attenuation, LO = 300 MHz, Tone 1 = 320 MHz, Tone 2 = 321 MHz at -25 dBm Plus Attenuation

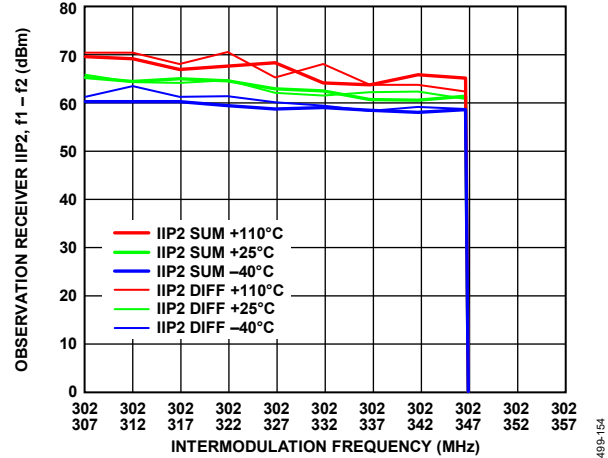


Figure 51. Observation Receiver IIP2,  $f_1 - f_2$  vs. Intermodulation Frequency, LO = 300 MHz, Tone 1 = 302 MHz, Tone 2 = Swept, -25 dBm Each, Attenuation = 0 dB

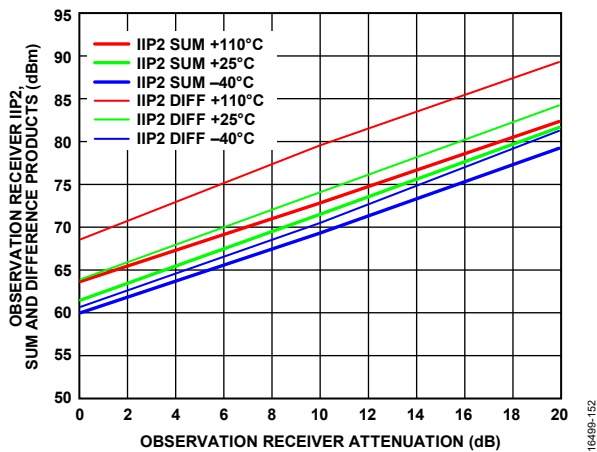


Figure 49. Observation Receiver IIP2, Sum and Difference Products vs. Observation Receiver Attenuation, LO = 525 MHz, Tone 1 = 545 MHz, Tone 2 = 546 MHz at -25 dBm Plus Attenuation

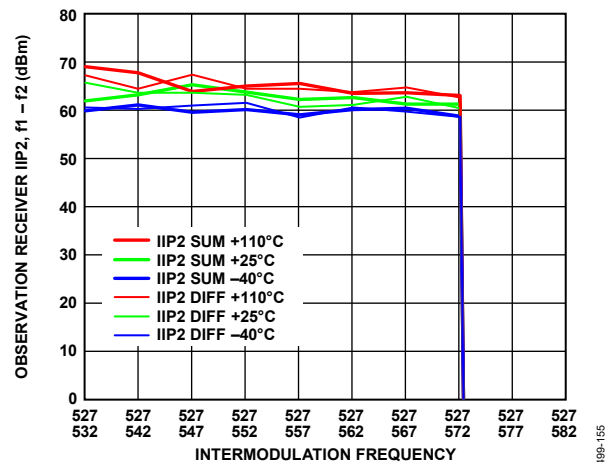


Figure 52. Observation Receiver IIP2,  $f_1 - f_2$  vs. Intermodulation Frequency, LO = 525 MHz, Tone 1 = 527 MHz, Tone 2 = Swept, -25 dBm Each, Attenuation = 0 dB

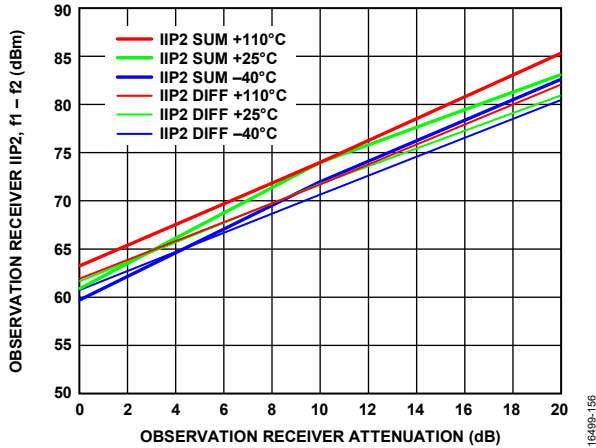


Figure 53. Observation Receiver IIP2,  $f_1 - f_2$  vs. Observation Receiver Attenuation, LO = 75 MHz, Tone 1 = 77 MHz, Tone 2 = 97 MHz at -25 dBm Plus Attenuation

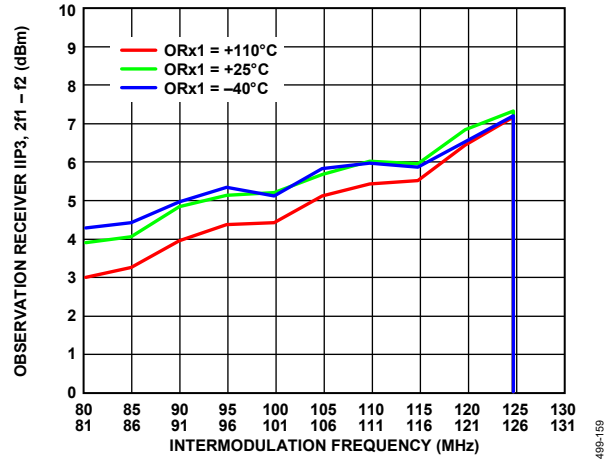


Figure 56. Observation Receiver IIP3,  $2f_1$  (Where  $2f_1$  is  $2 \times f_1$ ) -  $f_2$  vs. Intermodulation Frequency, LO = 75 MHz, Attenuation = 0 dB, Tones Separated by 1 MHz Swept Across Pass Band at -25 dBm Each

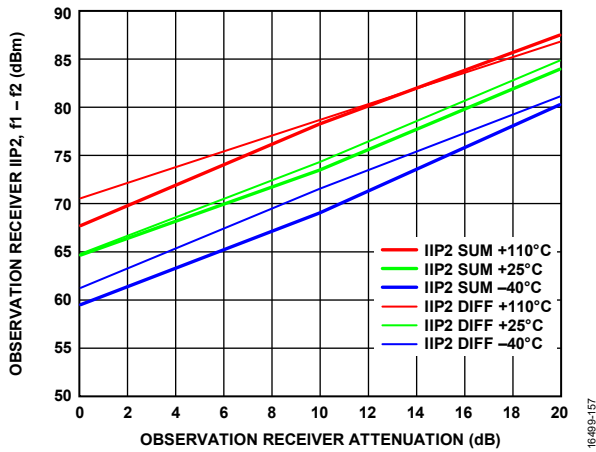


Figure 54. Observation Receiver IIP2,  $f_1 - f_2$  vs. Observation Receiver Attenuation, LO = 300 MHz, Tone 1 = 302 MHz, Tone 2 = 322 MHz at -25 dBm Plus Attenuation

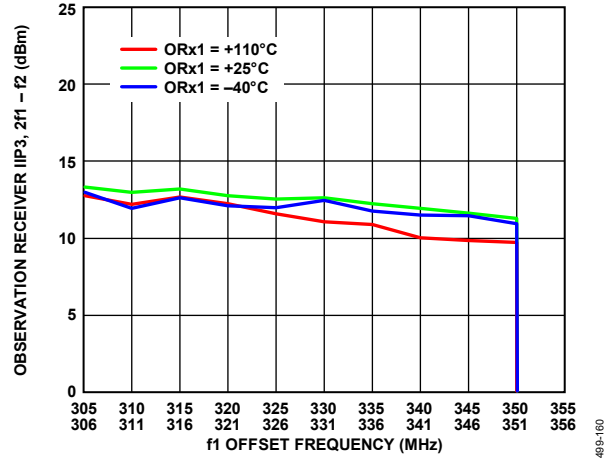


Figure 57. Observation Receiver IIP3,  $2f_1 - f_2$  vs.  $f_1$  Offset Frequency, LO = 300 MHz, Attenuation = 0 dB, Tones Separated by 1 MHz Swept Across Pass Band at -25 dBm Each

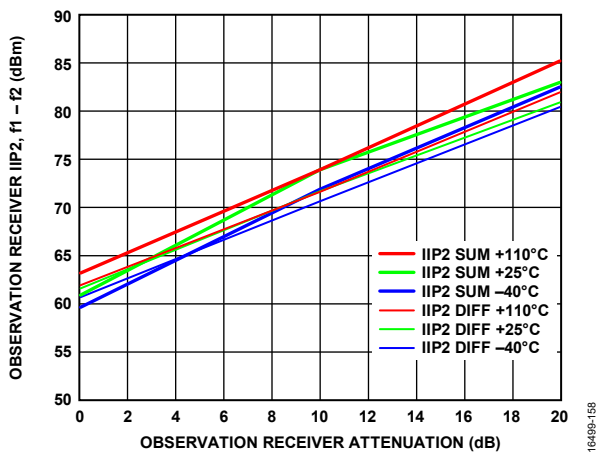


Figure 55. Observation Receiver IIP2,  $f_1 - f_2$  vs. Observation Receiver Attenuation, LO = 525 MHz, Tone 1 = 527 MHz, Tone 2 = 547 MHz at -25 dBm Plus Attenuation

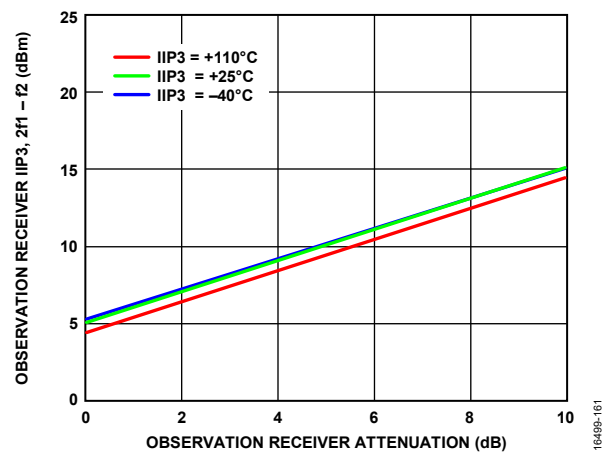


Figure 58. Observation Receiver IIP3,  $2f_1 - f_2$  vs. Observation Receiver Attenuation, LO = 75 MHz, Tone 1 = 100 MHz, Tone 2 = 101 MHz at -24 dBm Plus Attenuation

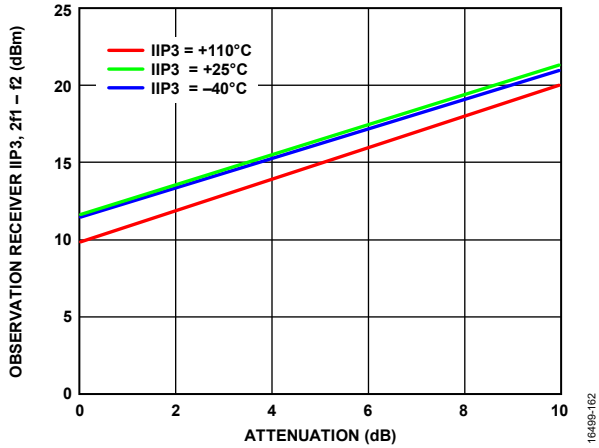


Figure 59. Observation Receiver IIP3, 2f1 – f2 vs. Attenuation, LO = 300 MHz, Tone 1 = 345 MHz, Tone 2 = 346 MHz at –24 dBm Plus Attenuation

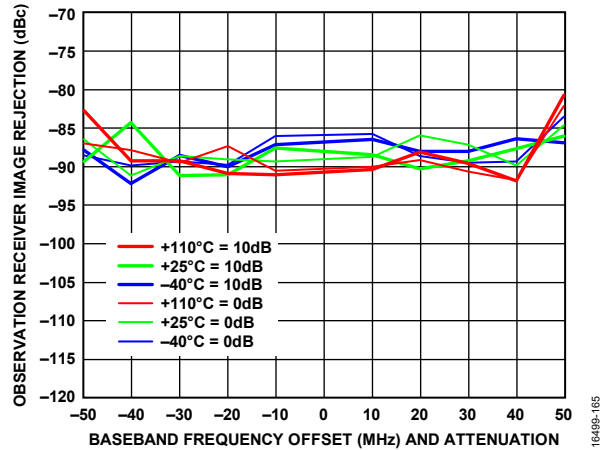


Figure 62. Observation Receiver Image Rejection vs. Baseband Frequency Offset and Attenuation, CW Signal Swept Across the Pass Band, LO = 75 MHz

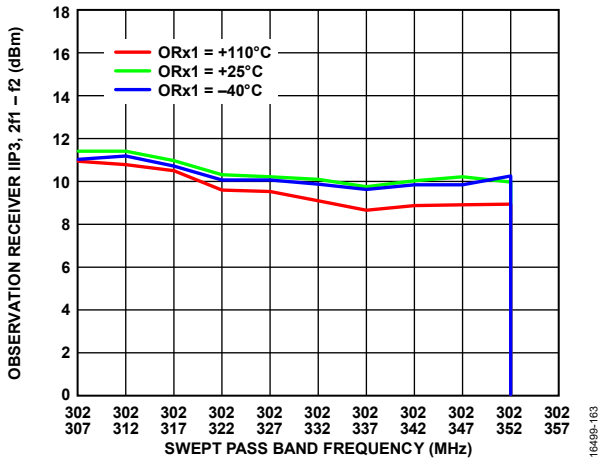


Figure 60. Observation Receiver IIP3, 2f1 – f2 vs. Swept Pass Band Frequency, LO = 300 MHz, Attenuation = 0 dB, Tone 1 = 302 MHz, Tone 2 = Swept Across the Pass Band, Tones Separated by 1 MHz Swept Across Pass Band at –19 dBm Each

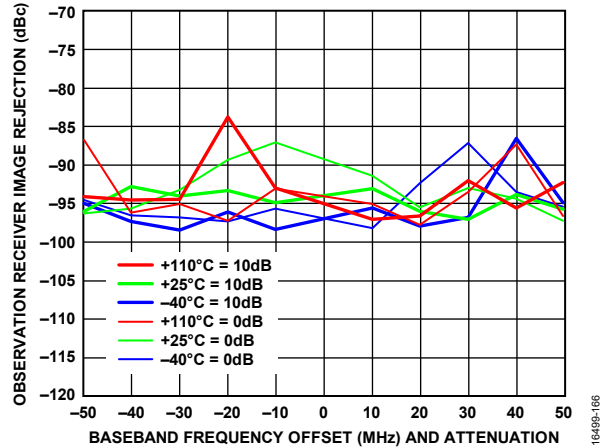


Figure 63. Observation Receiver Image Rejection vs. Baseband Frequency Offset and Attenuation, CW Signal Swept Across the Pass Band, LO = 300 MHz

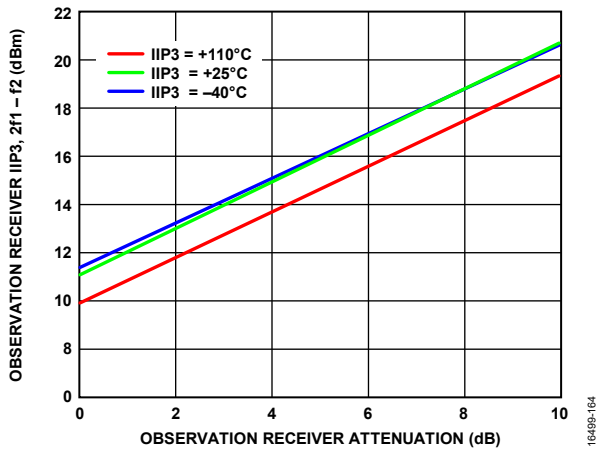


Figure 61. Observation Receiver IIP3, 2f1 – f2 vs. Observation Receiver Attenuation, LO = 300 MHz, Tone 1 = 302 MHz, Tone 2 = 352 MHz at –19 dBm Plus Attenuation

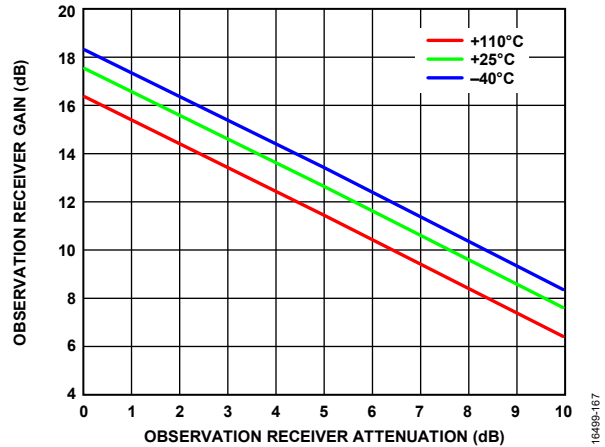


Figure 64. Observation Receiver Gain vs. Observation Receiver Attenuation, LO = 75 MHz



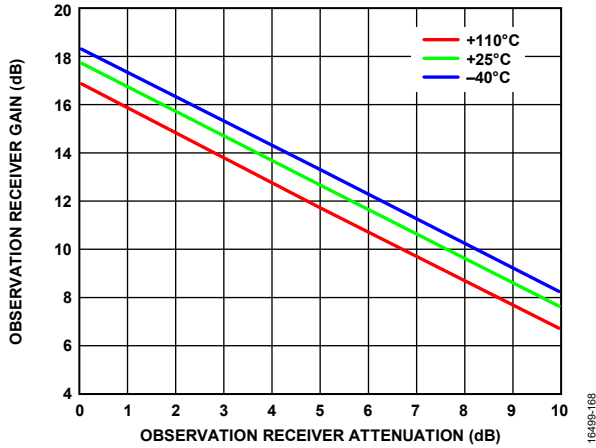


Figure 65. Observation Receiver Gain vs. Observation Receiver Attenuation, LO = 300 MHz

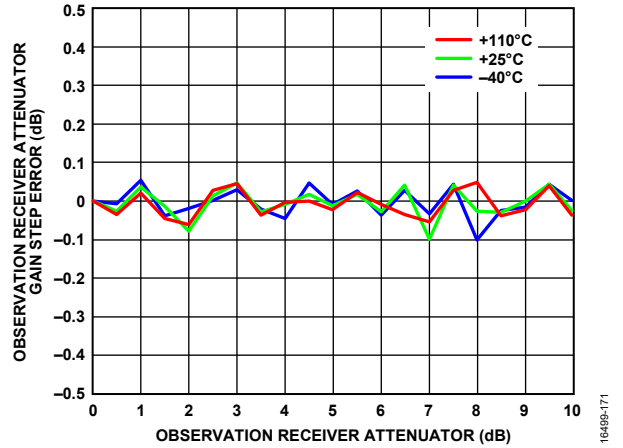


Figure 68. Observation Receiver Attenuator Gain Step Error vs. Observation Receiver Attenuator, LO = 525 MHz

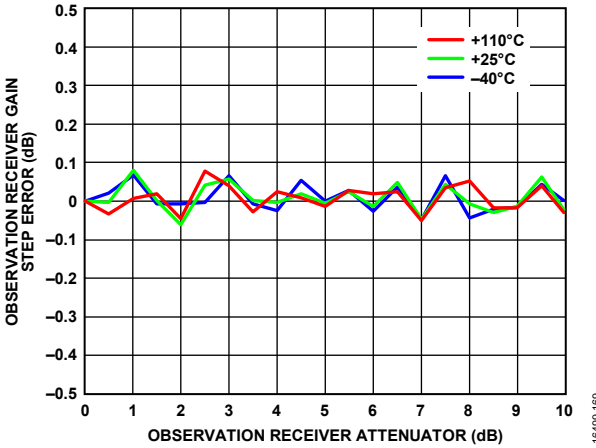


Figure 66. Observation Receiver Gain Step Error vs. Observation Receiver Attenuator, LO = 75 MHz

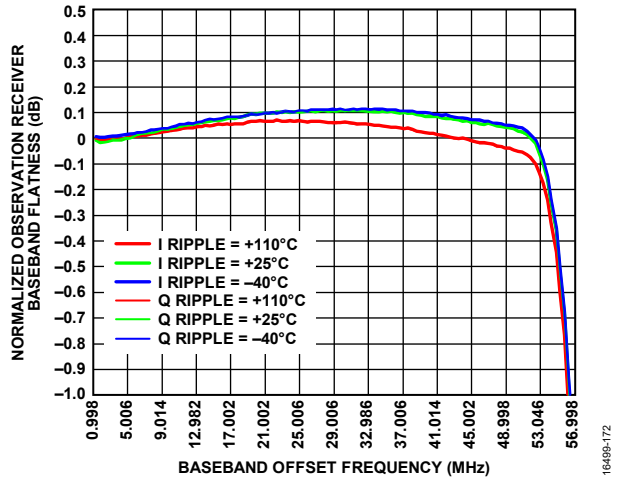


Figure 69. Normalized Observation Receiver Baseband Flatness vs. Baseband Offset Frequency, LO = 75 MHz, Attenuation = 0 dB

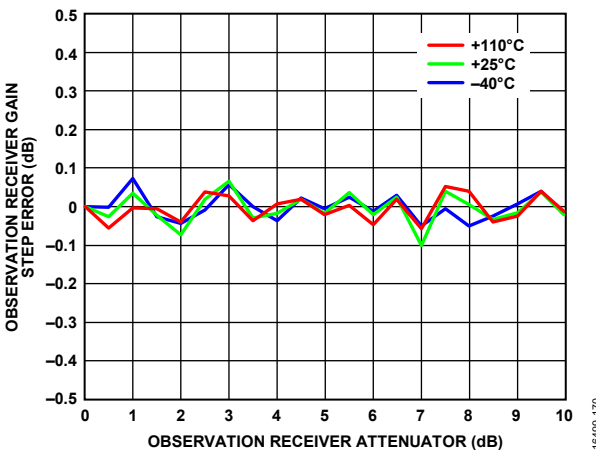


Figure 67. Observation Receiver Gain Step Error vs. Observation Receiver Attenuator, LO = 325 MHz

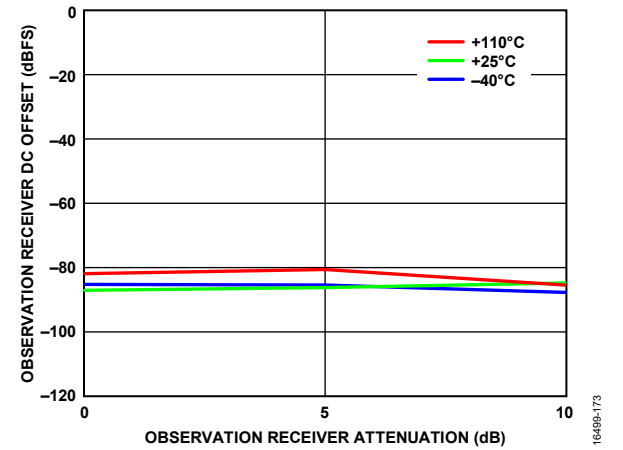


Figure 70. Observation Receiver DC Offset vs. Observation Receiver Attenuation, LO = 75 MHz, Baseband Frequency = 50 MHz

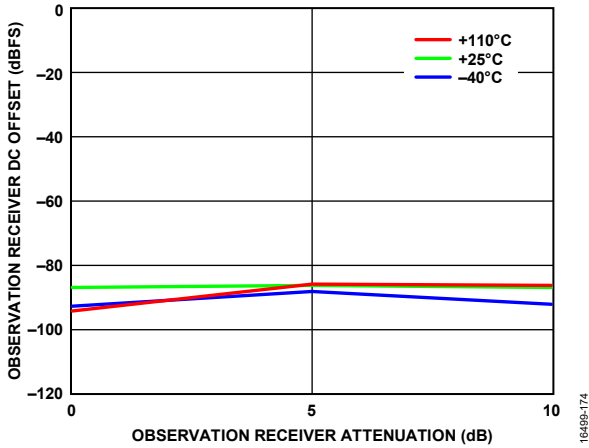


Figure 71. Observation Receiver DC Offset vs. Observation Receiver Attenuation, LO = 325 MHz, Baseband Frequency = 50 MHz

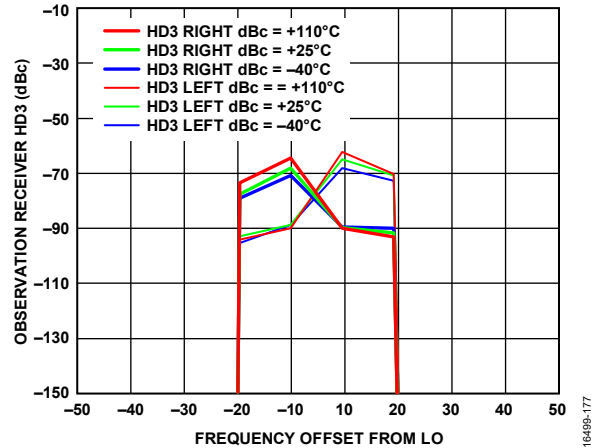


Figure 74. Observation Receiver HD3 vs. Frequency Offset from LO, Tone Level = -21 dBm at Attenuation = 0 dB, LO = 75 MHz

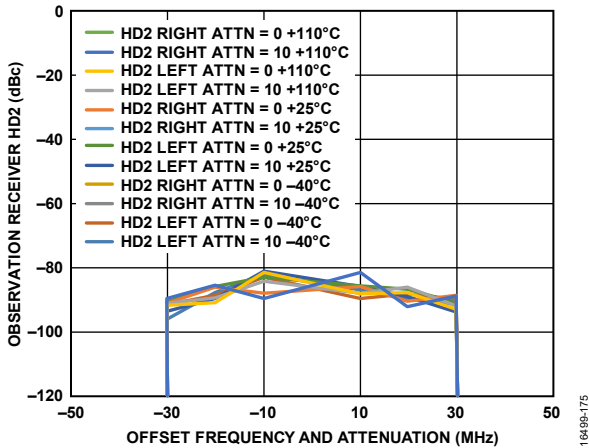


Figure 72. Observation Receiver HD2 vs. Offset Frequency and Attenuation, LO = 75 MHz, Tone Level = -21 dBm Plus Attenuation

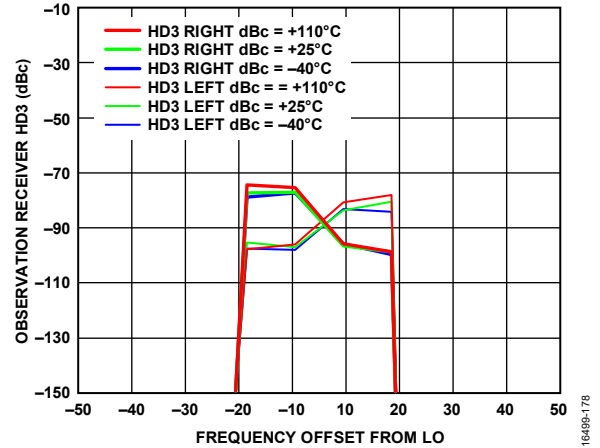


Figure 75. Observation Receiver HD3 vs. Frequency Offset from LO, Tone Level = -22 dBm at Attenuation = 0 dB, LO = 300 MHz

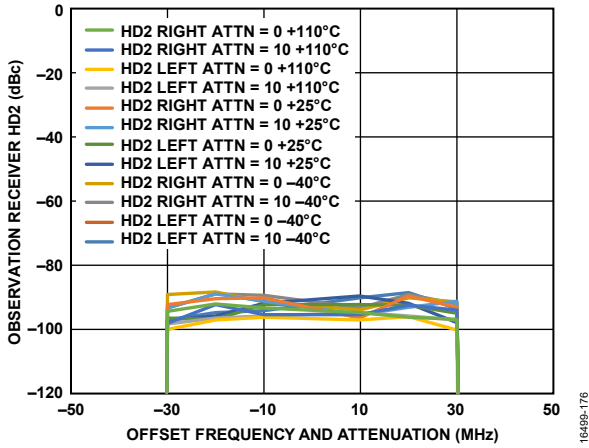


Figure 73. Observation Receiver HD2 vs. Offset Frequency and Attenuation, LO = 300 MHz, Tone Level = -22 dBm Plus Attenuation

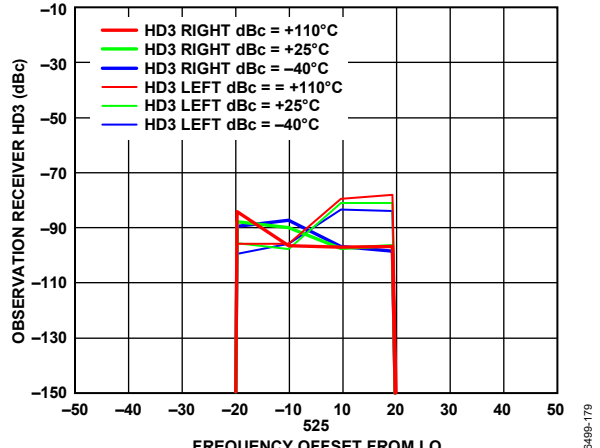


Figure 76. Observation Receiver HD3 vs. Frequency Offset from LO, Tone Level = -22 dBm at Attenuation = 0 dB, LO = 525 MHz

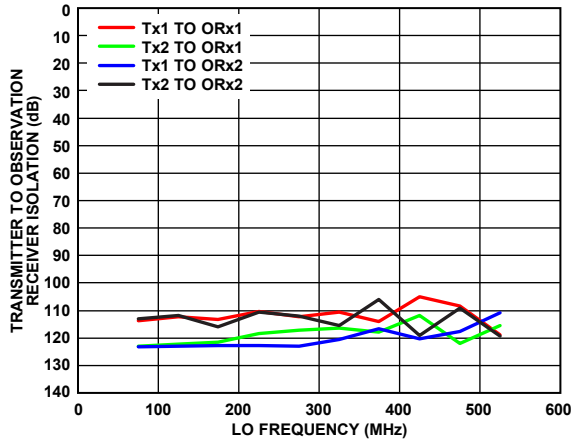


Figure 77. Transmitter to Observation Receiver Isolation vs. LO Frequency, Temperature = 25°C

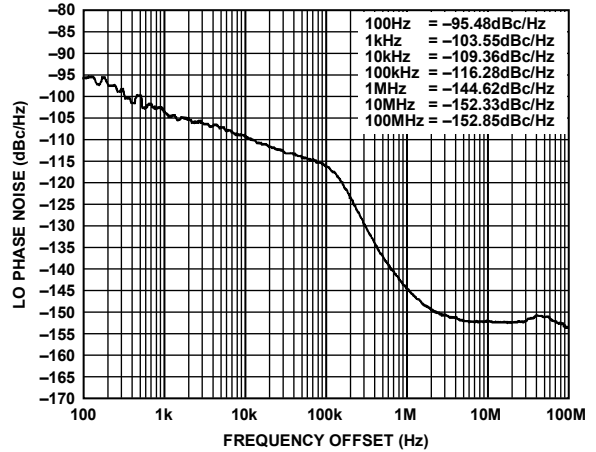


Figure 80. LO Phase Noise vs. Frequency Offset, LO = 525 MHz, PLL Loop Bandwidth = 50 kHz

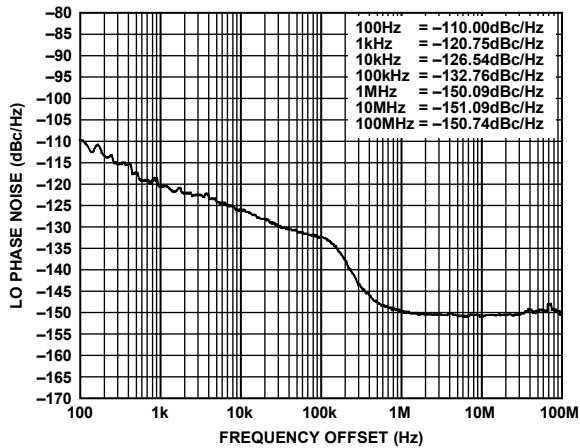


Figure 78. LO Phase Noise vs. Frequency Offset, LO = 75 MHz, PLL Loop Bandwidth = 50 kHz

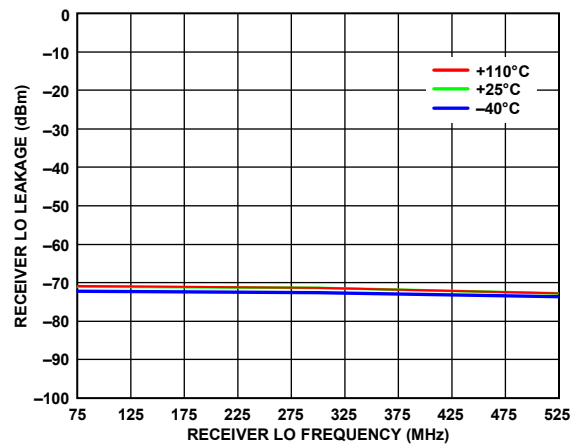


Figure 81. Receiver LO Leakage vs. Receiver LO Frequency = 75 MHz, 300 MHz, and 525 MHz, Receiver Attenuation = 0 dB, RF Bandwidth = 50 MHz, Sample Rate = 61.44 MSPS

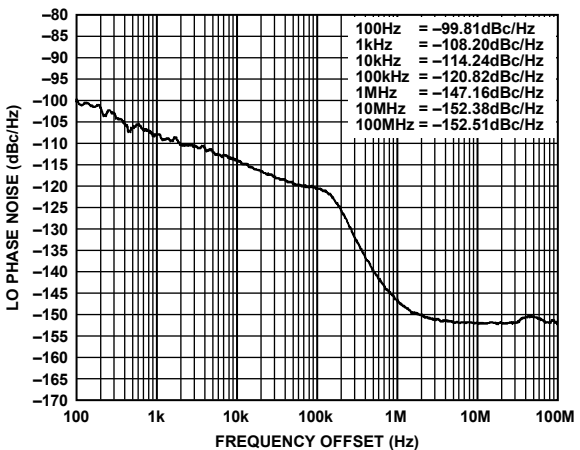


Figure 79. LO Phase Noise vs. Frequency Offset, LO = 300 MHz, PLL Loop Bandwidth = 50 kHz

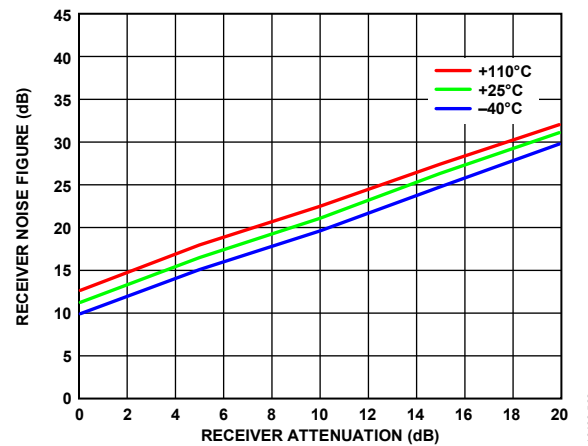


Figure 82. Receiver Noise Figure vs. Receiver Attenuation, LO = 75 MHz, RF Bandwidth = 50 MHz, Sample Rate = 61.44 MSPS, Integration Bandwidth = 1 MHz to 25 MHz

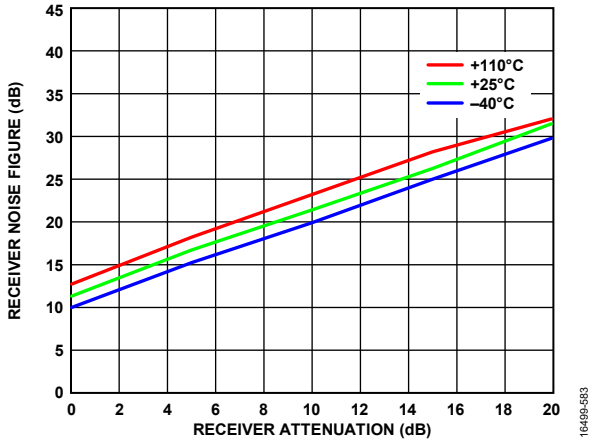


Figure 83. Receiver Noise Figure vs. Receiver Attenuation, LO = 300 MHz, RF Bandwidth = 50 MHz, Sample Rate = 61.44 MSPS, Integration Bandwidth = 1 MHz to 25 MHz

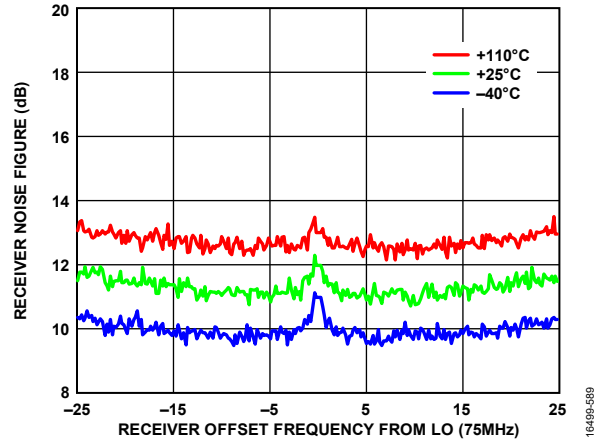


Figure 86. Receiver Noise Figure vs. Receiver Offset Frequency from LO, Integration Bandwidth = 200 kHz, LO = 75 MHz

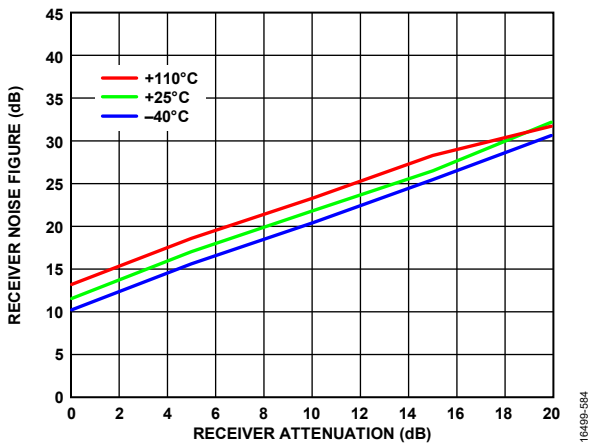


Figure 84. Receiver Noise Figure vs. Receiver Attenuation, LO = 525 MHz, RF Bandwidth = 50 MHz, Sample Rate = 61.44 MSPS, Integration Bandwidth = 1 MHz to 25 MHz

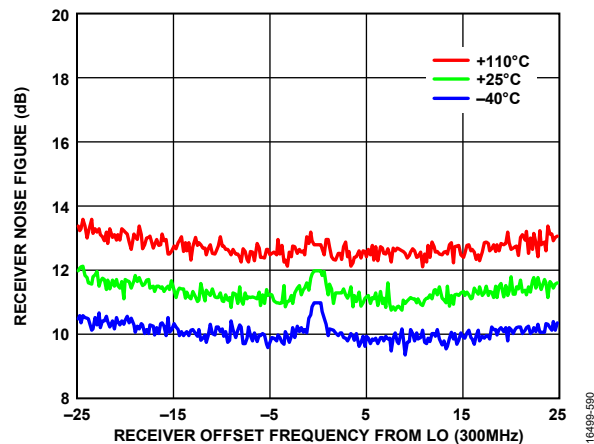


Figure 87. Receiver Noise Figure vs. Receiver Offset Frequency from LO, Integration Bandwidth = 200 kHz, LO = 300 MHz

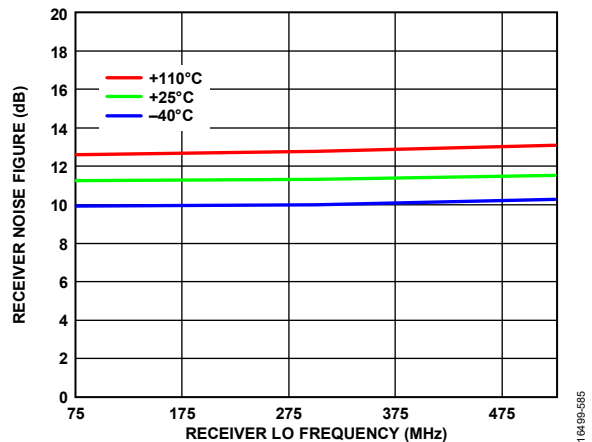


Figure 85. Receiver Noise Figure vs. Receiver LO Frequency, Receiver Attenuation = 0 dB, RF Bandwidth = 50 MHz, Sample Rate = 61.44 MSPS, Integration Bandwidth = ±25 MHz

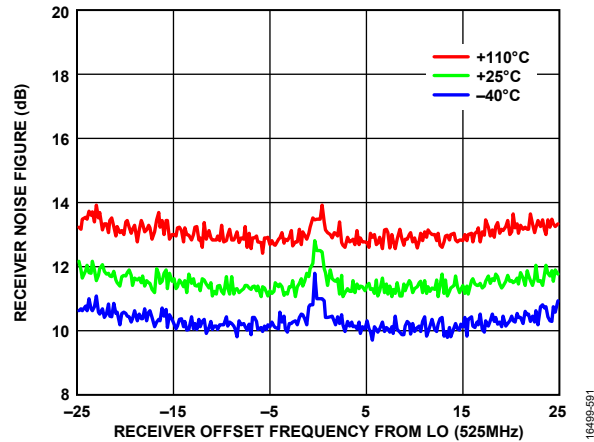


Figure 88. Receiver Noise Figure vs. Receiver Offset Frequency from LO, Integration Bandwidth = 200 kHz, LO = 525 MHz

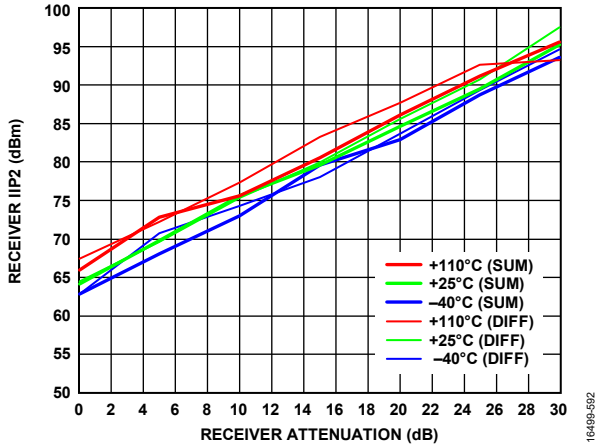


Figure 89. Receiver IIP2 vs. Receiver Attenuation, LO = 75 MHz, Tones Placed at 82.5 MHz and 83.5 MHz, -23.5 dBm Plus Attenuation

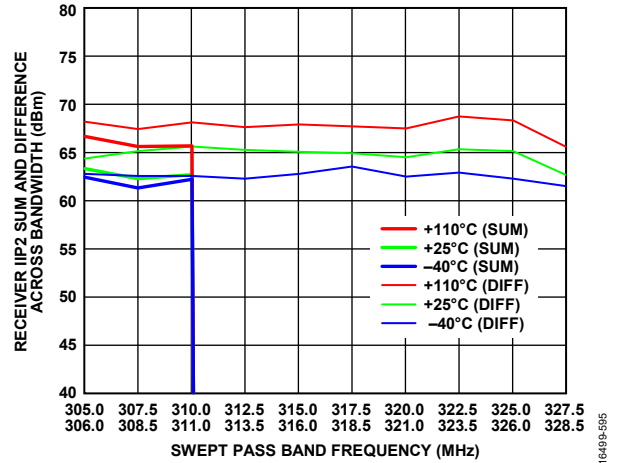


Figure 92. Receiver IIP2 Sum and Difference Across Bandwidth vs. Swept Pass Band Frequency, Receiver Attenuation = 0 dB, LO = 300 MHz, 10 Tone Pairs, -23.5 dBm Each

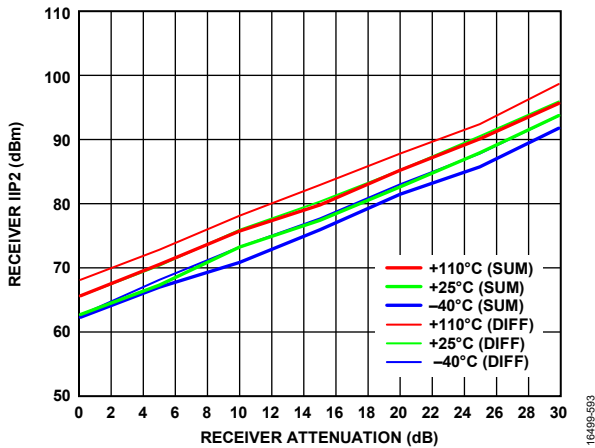


Figure 90. Receiver IIP2 vs. Receiver Attenuation, LO = 300 MHz, Tones Placed at 310 MHz and 311 MHz, -23.5 dBm Plus Attenuation

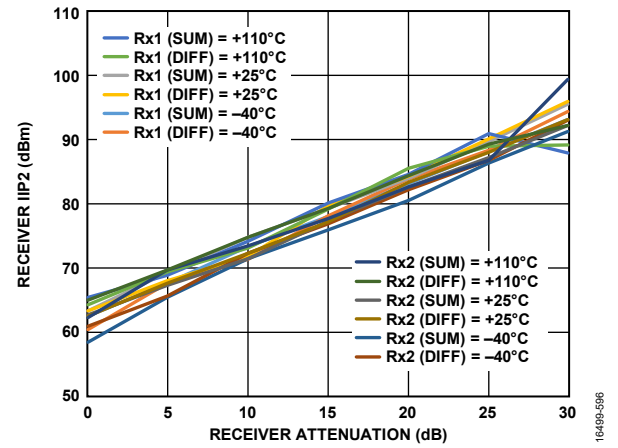


Figure 93. Receiver IIP2 vs. Receiver Attenuation, LO = 75 MHz, Tones Placed at 77 MHz and 97 MHz, -23.5 dBm Plus Attenuation

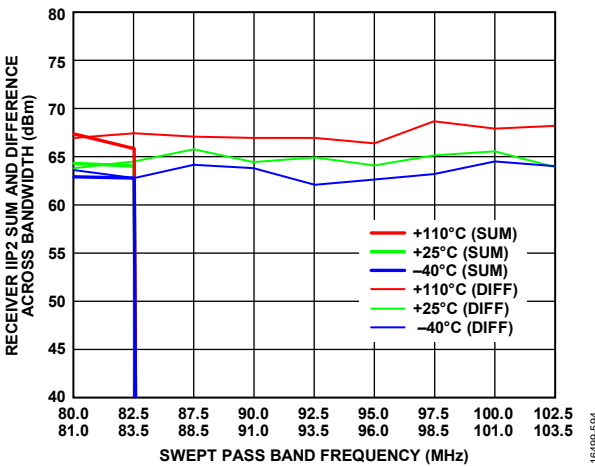


Figure 91. Receiver IIP2 Sum and Difference Across Bandwidth vs. Swept Pass Band Frequency, Receiver Attenuation = 0 dB, LO = 75 MHz, 10 Tone Pairs, -23.5 dBm Each

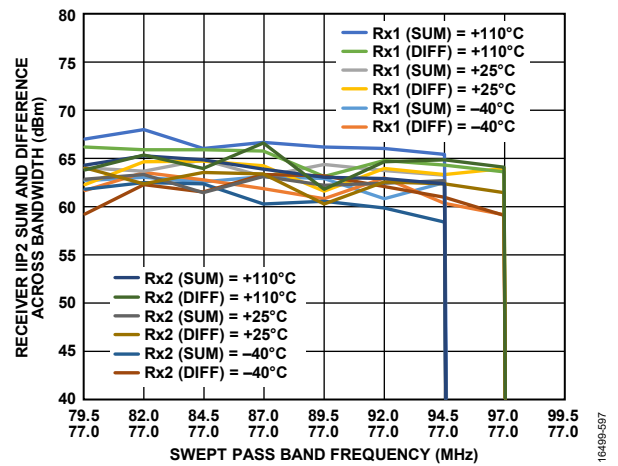


Figure 94. Receiver IIP2 Sum and Difference Across Bandwidth vs. Swept Pass Band Frequency, Receiver Attenuation = 0 dB, LO = 75 MHz, Tone 1 = 77 MHz, Tone 2 Swept, -23.5 dBm Each

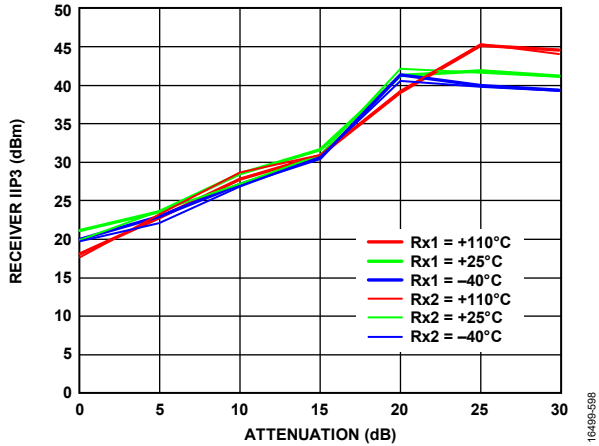


Figure 95. Receiver IIP3 vs. Attenuation, LO = 300 MHz, Tone 1 = 325 MHz, Tone 2 = 326 MHz, -21 dBm Plus Attenuation

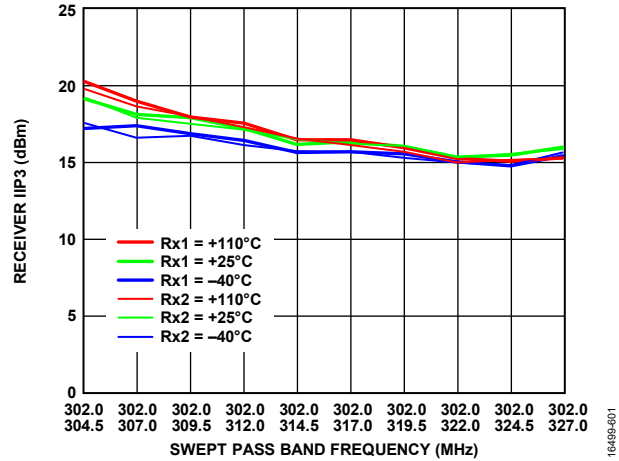


Figure 98. Receiver IIP3 vs. Swept Pass Band Frequency, Receiver Attenuation = 0 dB, LO = 300 MHz, Tone 1 = 302 MHz, Tone 2 = Swept Across Pass Band, -19 dBm Each

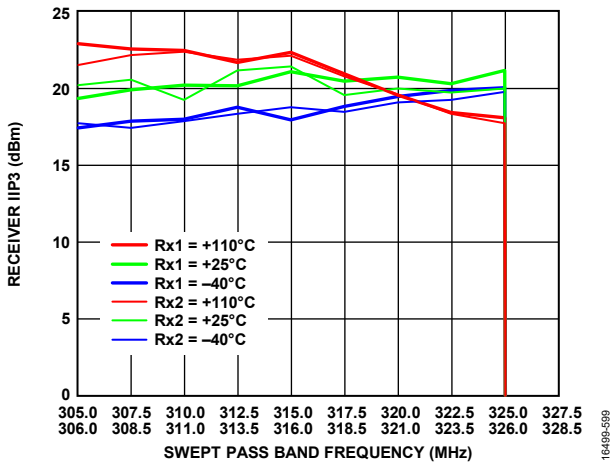


Figure 96. Receiver IIP3 vs. Swept Pass Band Frequency, Receiver Attenuation = 0 dB, LO = 300 MHz, Tone 2 = Tone 1 + 1 MHz, -21 dBm Each

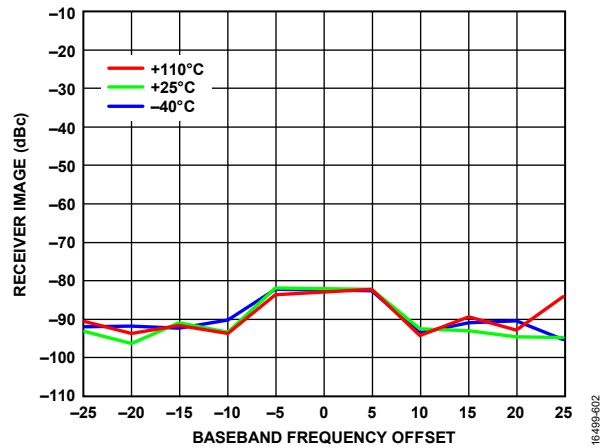


Figure 99. Receiver Image vs. Baseband Frequency Offset, Attenuation = 0 dB, RF Bandwidth = 50 MHz, Tracking Calibration Active, Sample Rate = 61.44 MSPS, LO = 75 MHz

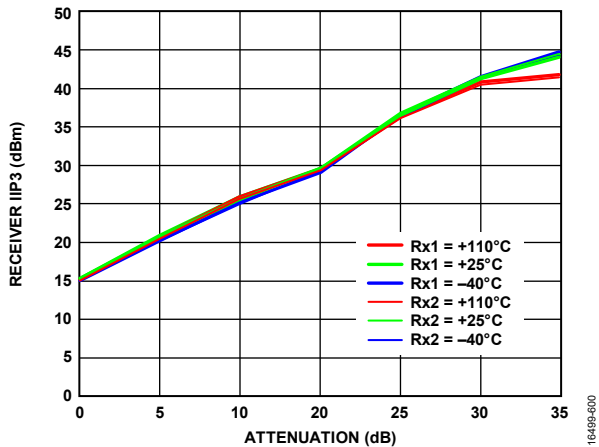


Figure 97. Receiver IIP3 vs. Attenuation, LO = 300 MHz, Tone 1 = 302 MHz, Tone 2 = 322 MHz, -19 dBm Plus Attenuation

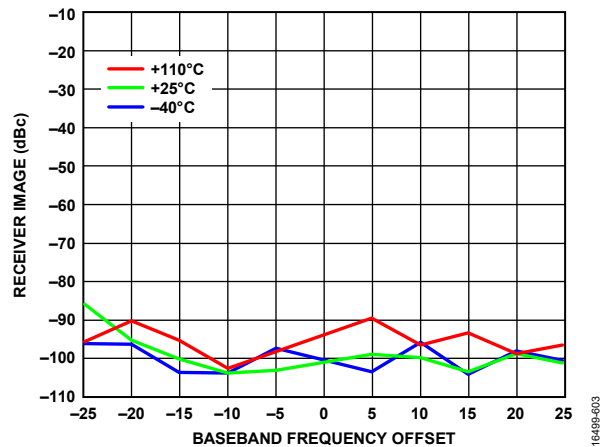


Figure 100. Receiver Image vs. Baseband Frequency Offset, Attenuation = 0 dB, RF Bandwidth = 50 MHz, Tracking Calibration Active, Sample Rate = 61.44 MSPS, LO = 300 MHz

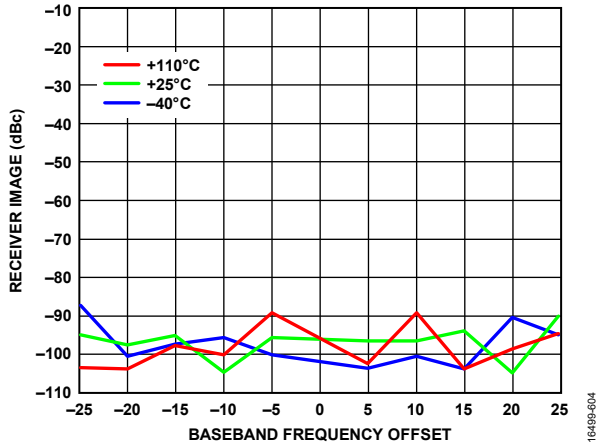


Figure 101. Receiver Image vs. Baseband Frequency Offset, Attenuation = 0 dB, RF Bandwidth = 50 MHz, Tracking Calibration Active, Sample Rate = 61.44 MSPS, LO = 525 MHz

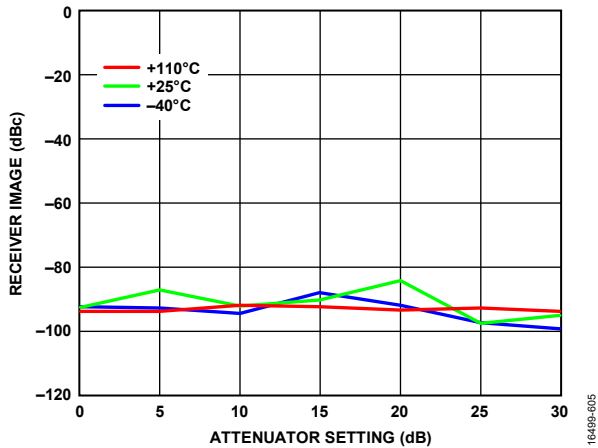


Figure 102. Receiver Image vs. Attenuator Setting, RF Bandwidth = 25 MHz, Tracking Calibration Active, Sample Rate = 61.44 MSPS, LO = 75 MHz, Baseband Frequency = 25 MHz

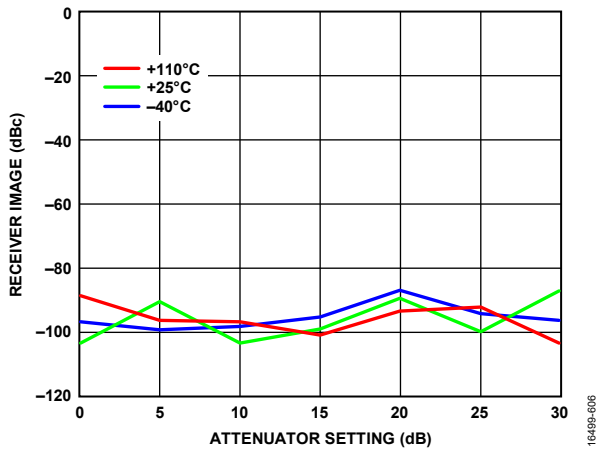


Figure 103. Receiver Image vs. Attenuator Setting, RF Bandwidth = 25 MHz, Tracking Calibration Active, Sample Rate = 61.44 MSPS, LO = 325 MHz, Baseband Frequency = 25 MHz

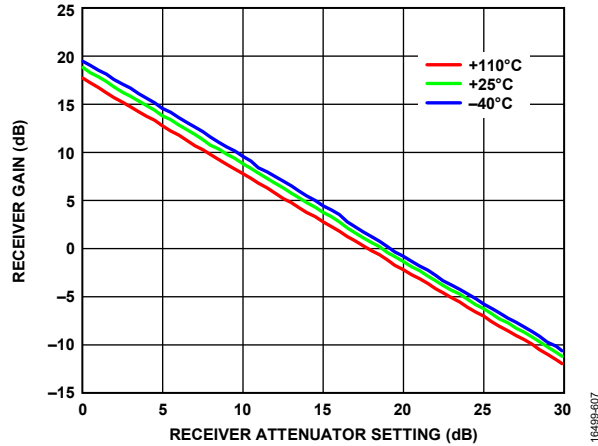


Figure 104. Receiver Gain vs. Receiver Attenuator Setting, RF Bandwidth = 50 MHz, Sample Rate = 61.44 MSPS, LO = 75 MHz

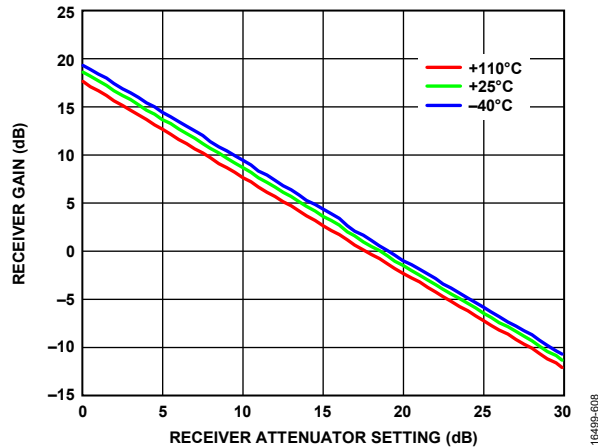


Figure 105. Receiver Gain vs. Receiver Attenuator Setting, RF Bandwidth = 50 MHz, Sample Rate = 61.44 MSPS, LO = 325 MHz

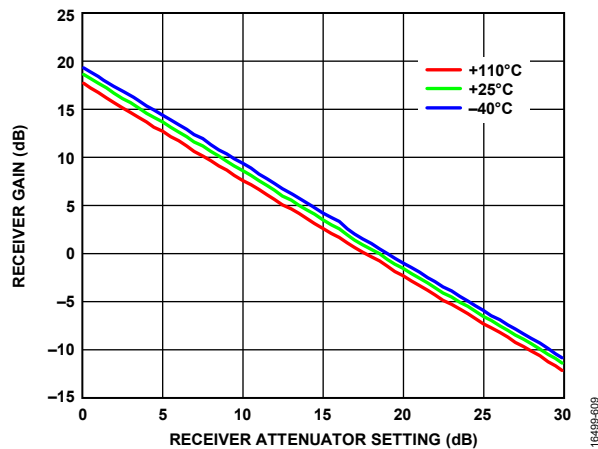


Figure 106. Receiver Gain vs. Receiver Attenuator Setting, RF Bandwidth = 50 MHz, Sample Rate = 61.44 MSPS, LO = 525 MHz

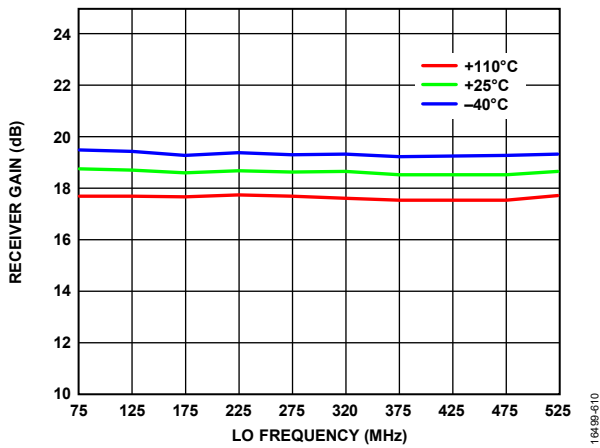


Figure 107. Receiver Gain vs. LO Frequency, RF Bandwidth = 50 MHz, Sample Rate = 61.44 MSPS

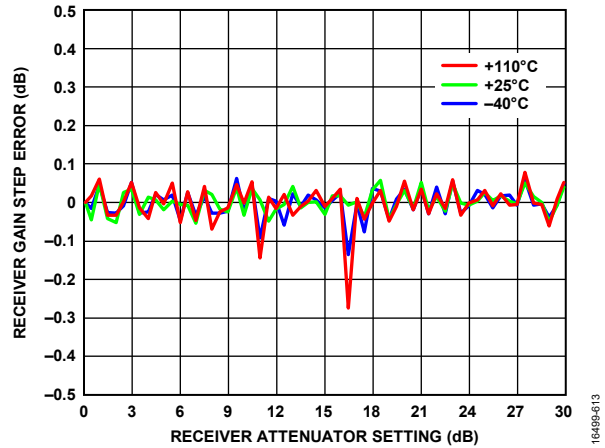


Figure 110. Receiver Gain Step Error vs. Receiver Attenuator Setting, LO = 525 MHz

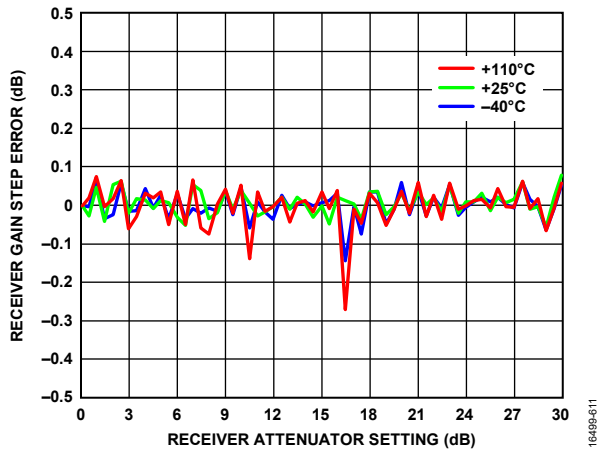


Figure 108. Receiver Gain Step Error vs. Receiver Attenuator Setting, LO = 75 MHz

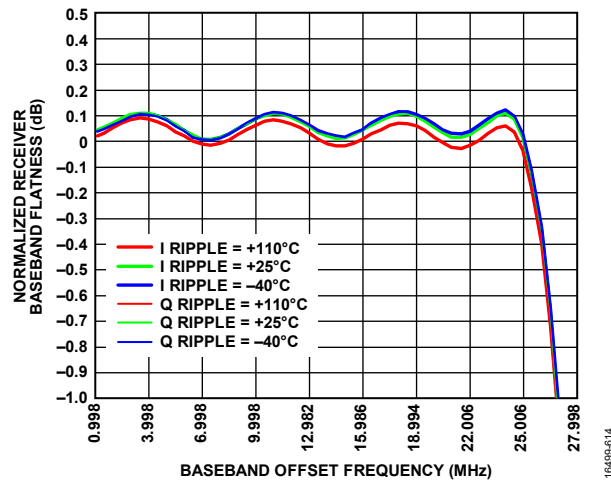


Figure 111. Normalized Receiver Baseband Flatness vs. Baseband Offset Frequency, LO = 75 MHz

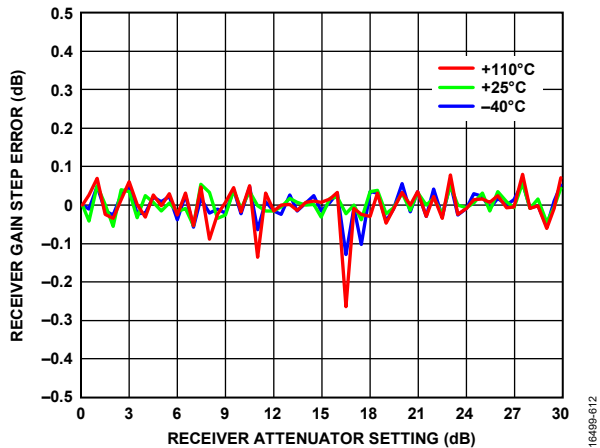


Figure 109. Receiver Gain Step Error vs. Receiver Attenuator Setting, LO = 325 MHz

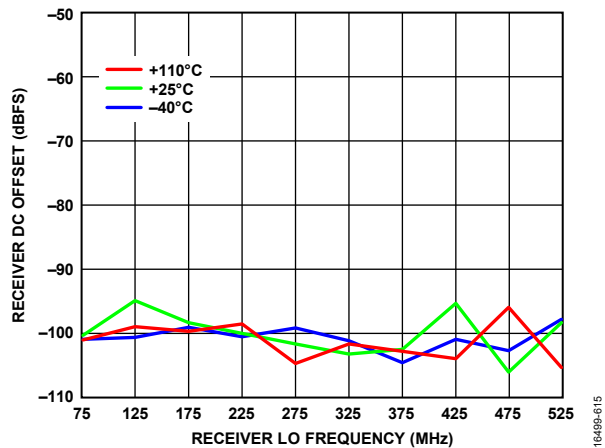


Figure 112. Receiver DC Offset vs. Receiver LO Frequency



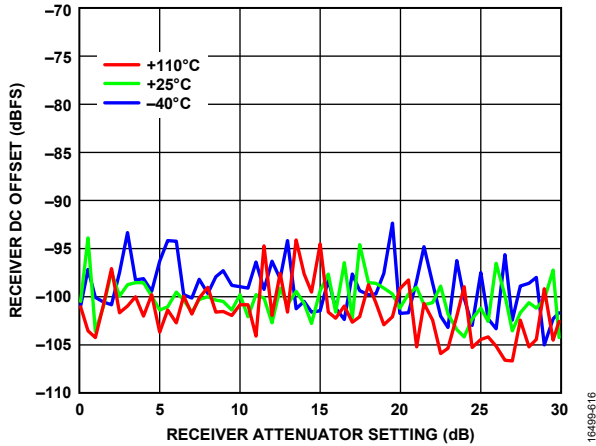


Figure 113. Receiver DC Offset vs. Receiver Attenuator Setting, LO = 75 MHz

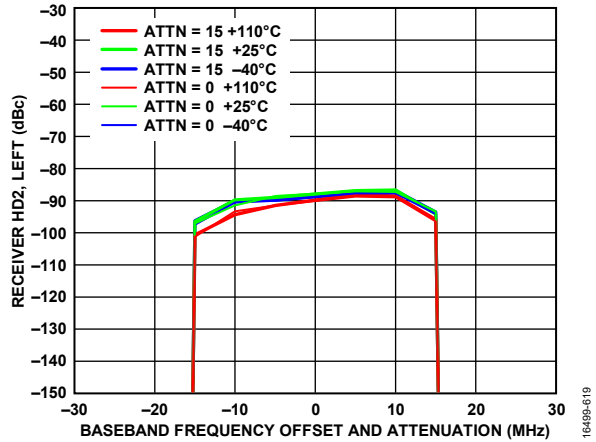


Figure 116. Receiver HD2 Left vs. Baseband Frequency Offset and Attenuation, Tone Level = -21 dBm at Attenuation = 0 dB, X-Axis is Baseband Frequency Offset of Fundamental Tone, Not Frequency of HD2 Product (HD2 Product Is 2 x Baseband Frequency), HD2 Canceller Disabled, LO = 300 MHz

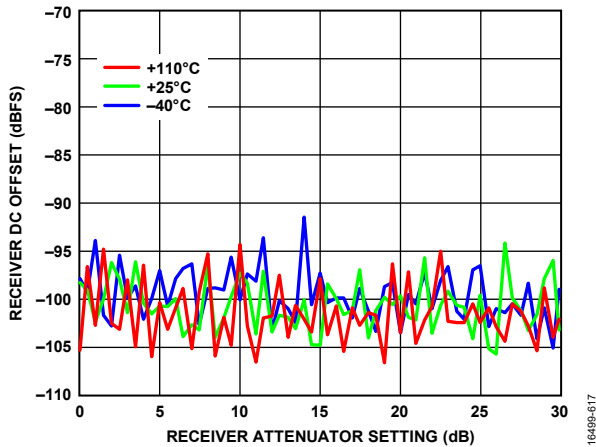


Figure 114. Receiver DC Offset vs. Receiver Attenuator Setting, LO = 525 MHz

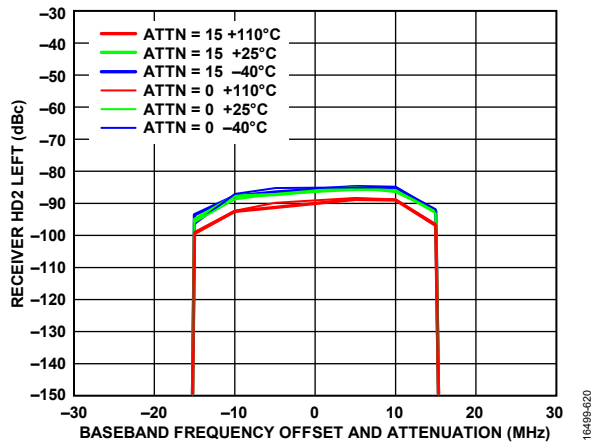


Figure 117. Receiver HD2 Left vs. Baseband Frequency Offset and Attenuation, Tone Level = -21 dBm at Attenuation = 0 dB, X-Axis is Baseband Frequency Offset of Fundamental Tone, Not Frequency of HD2 Product (HD2 Product Is 2 x Baseband Frequency), HD2 Canceller Disabled, LO = 525 MHz

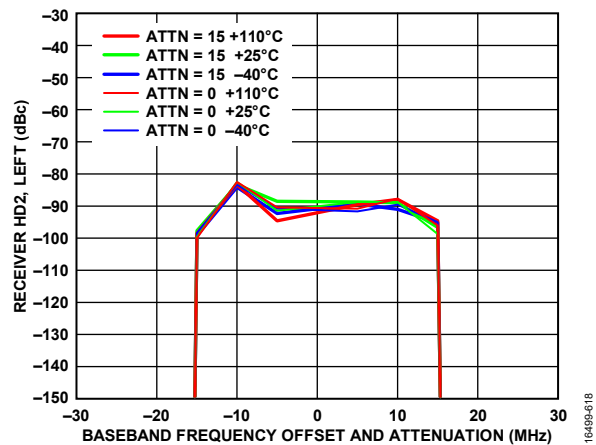


Figure 115. Receiver HD2, Left vs. Baseband Frequency Offset and Attenuation, Tone Level = -21 dBm at Attenuation = 0 dB, X-Axis is Baseband Frequency Offset of Fundamental Tone, Not Frequency of HD2 Product (HD2 Product is 2 x Baseband Frequency), HD2 Canceller Disabled, LO = 75 MHz

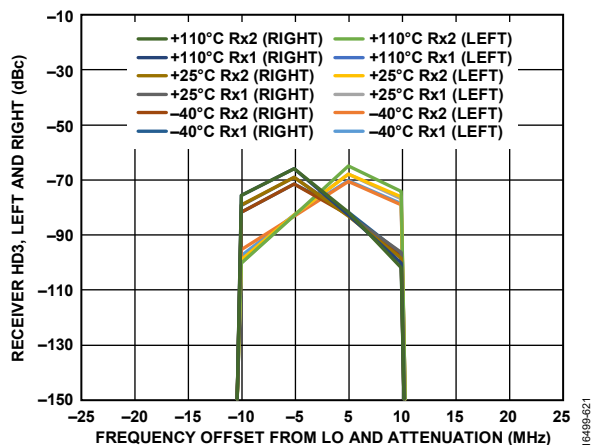


Figure 118. Receiver HD3, Left and Right vs. Frequency Offset from LO and Attenuation, Tone Level = -16 dBm at Attenuation = 0 dB, LO = 75 MHz

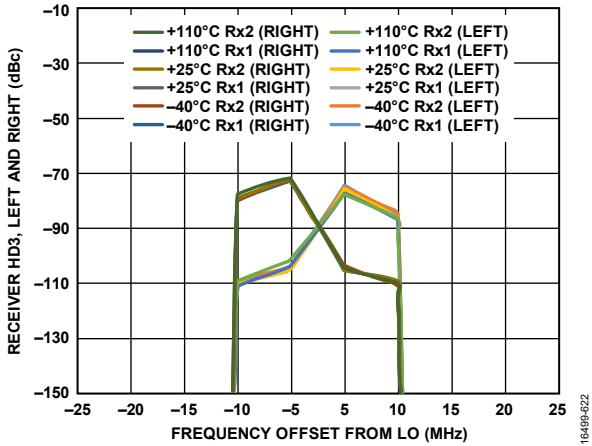


Figure 119. Receiver HD3, Left and Right vs. Frequency Offset from LO, Tone Level = -17 dBm at Attenuation = 0 dB, LO = 300 MHz

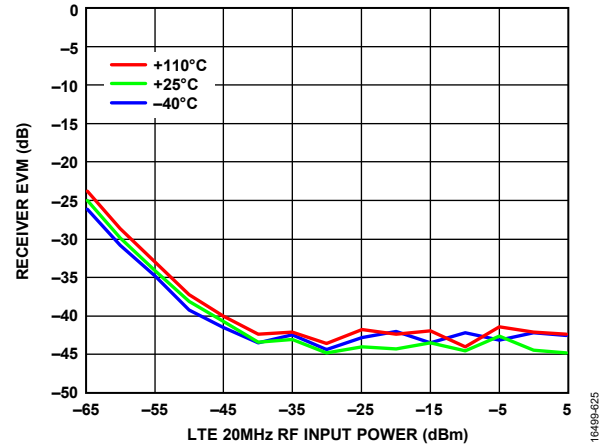


Figure 122. Receiver EVM vs. LTE 20 MHz RF Input Power, LTE 20 MHz RF Signal, LO = 300 MHz, Default AGC Settings

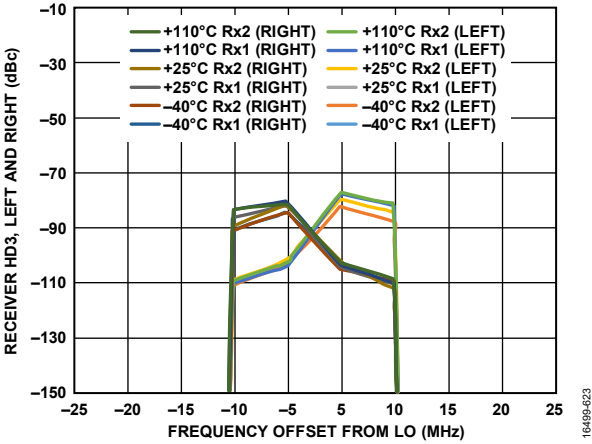


Figure 120. Receiver HD3, Left and Right vs. Frequency Offset from LO, Tone Level = -17 dBm at Attenuation = 0 dB, LO = 525 MHz

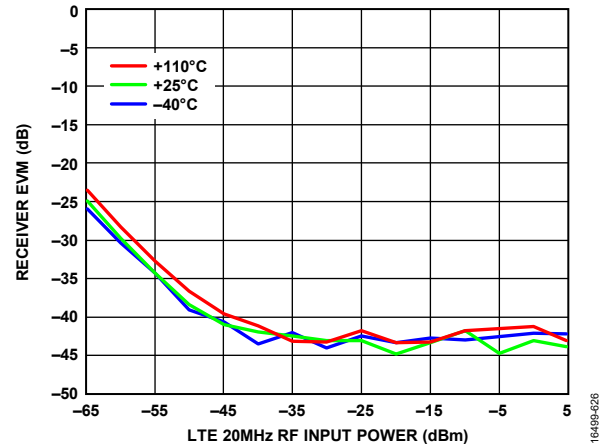


Figure 123. Receiver EVM vs. LTE 20 MHz RF Input Power, LTE 20 MHz RF Signal, LO = 525 MHz, Default AGC Settings

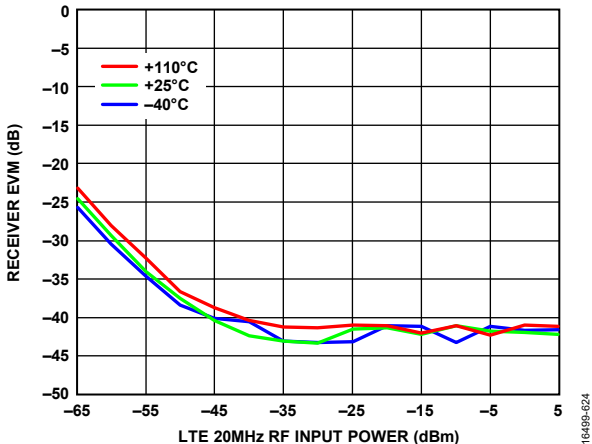


Figure 121. Receiver EVM vs. LTE 20 MHz RF Input Power, LTE 20 MHz RF Signal, LO = 75 MHz, Default AGC Settings

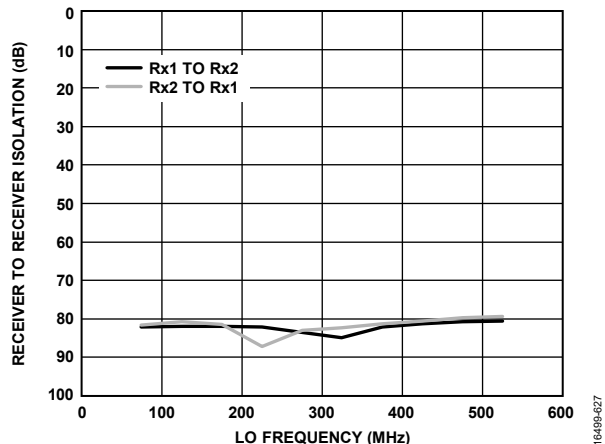


Figure 124. Receiver to Receiver Isolation vs. LO Frequency, Baseband Frequency = 10 MHz

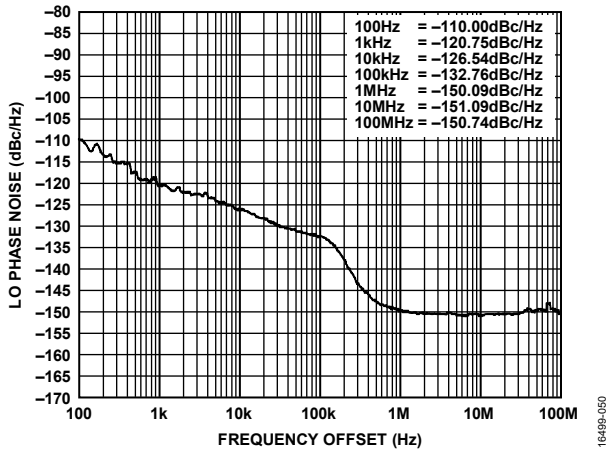


Figure 125. LO Phase Noise vs. Frequency Offset, LO = 75 MHz, PLL Loop Bandwidth = 50 kHz

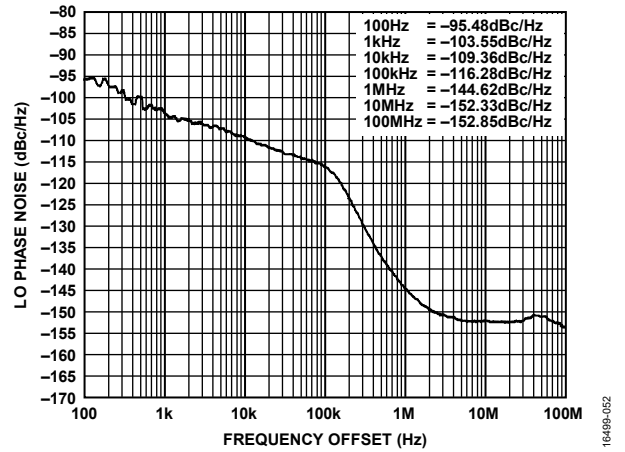


Figure 127. LO Phase Noise vs. Frequency Offset, LO = 525 MHz, PLL Loop Bandwidth = 50 kHz

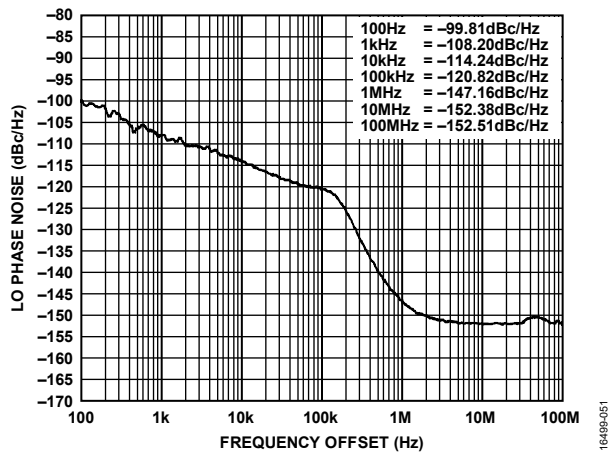


Figure 126. LO Phase Noise vs. Frequency Offset, LO = 300 MHz, PLL Loop Bandwidth = 50 kHz

650 MHz TO 3000 MHz BAND

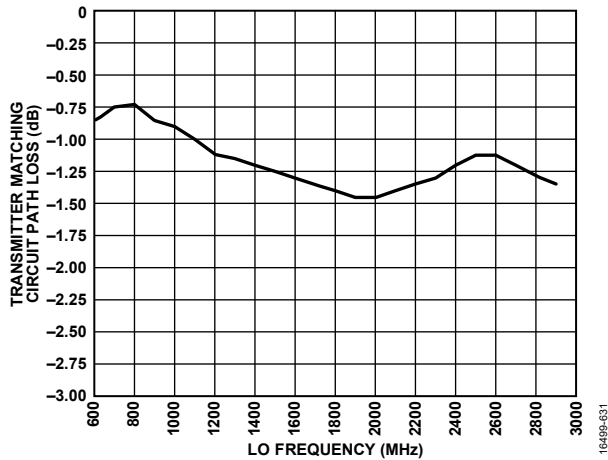


Figure 128. Transmitter Matching Circuit Path Loss vs. LO Frequency, Can be Used for De-Embedding Performance Data

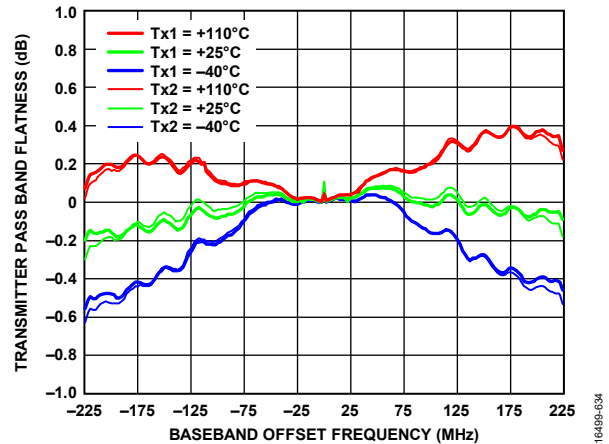


Figure 131. Transmitter Pass Band Flatness vs. Baseband Offset Frequency, LO = 2600 MHz

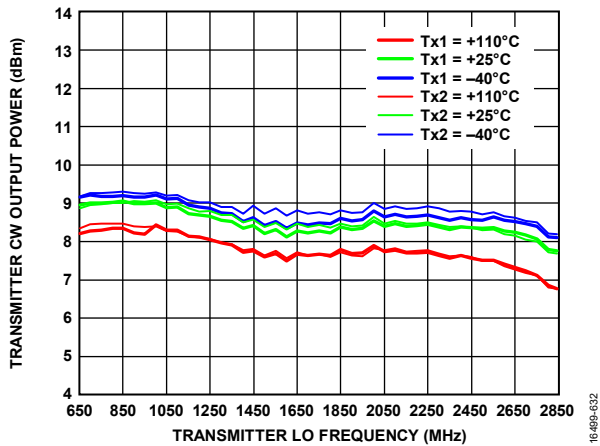


Figure 129. Transmitter CW Output Power vs. Transmitter LO Frequency, Transmitter QEC and External LO Leakage Active, Transmitter in 200 MHz/450 MHz Bandwidth Mode, IQ Rate = 491.52 MHz, 0 dB Attenuation, Not De-Embedded

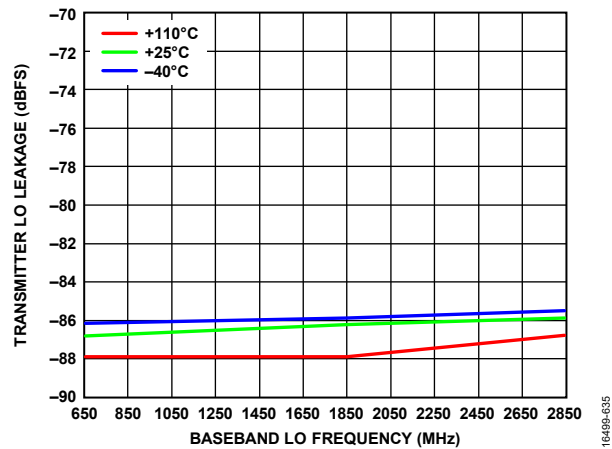


Figure 132. Transmitter LO Leakage vs. Baseband LO Frequency, Transmitter Attenuation = 0 dB

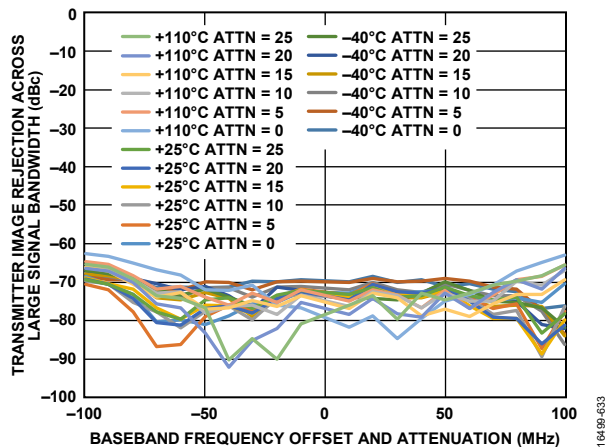


Figure 130. Transmitter Image Rejection Across Large Signal Bandwidth vs. Baseband Frequency Offset and Attenuation, QEC Trained with Three Tones Placed at 10 MHz, 50 MHz, and 100 MHz (Tracking On), Total Combined Power = -6 dBFS, Correction Then Frozen (Tracking Turned Off), CW Tone Swept Across Large Signal Bandwidth

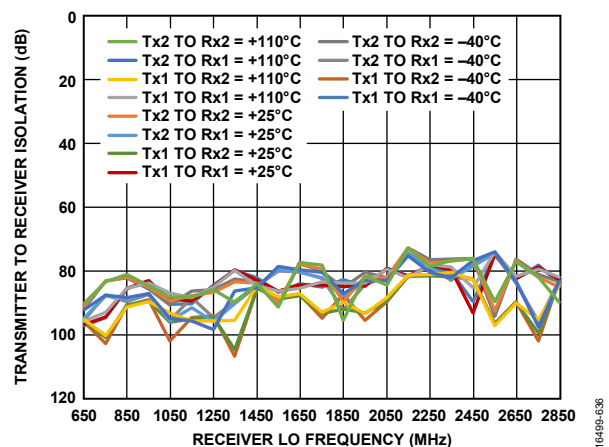


Figure 133. Transmitter to Receiver Isolation vs. Receiver LO Frequency

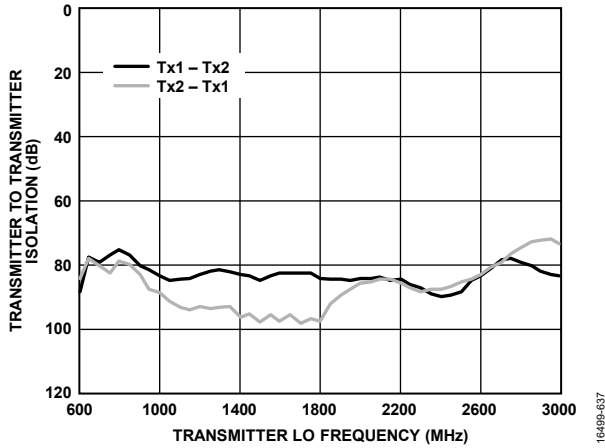


Figure 134. Transmitter to Transmitter Isolation vs. Transmitter LO Frequency, Temperature = 25°C

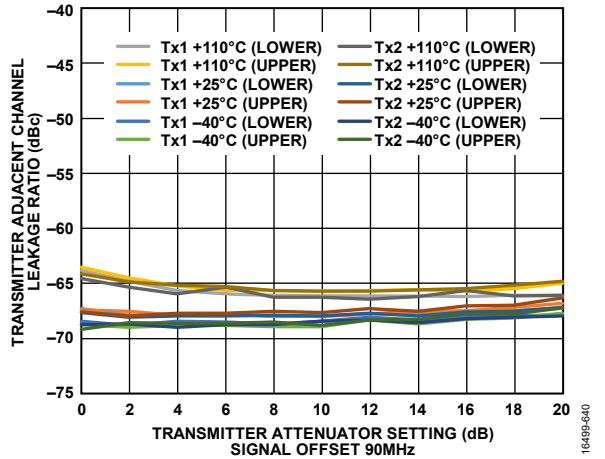


Figure 137. Transmitter Adjacent Channel Leakage Ratio vs. Transmitter Attenuator Setting, Signal Offset = 90 MHz, LO = 1850 MHz, LTE20 MHz, PAR = 12 dB, Upper Side and Lower Side

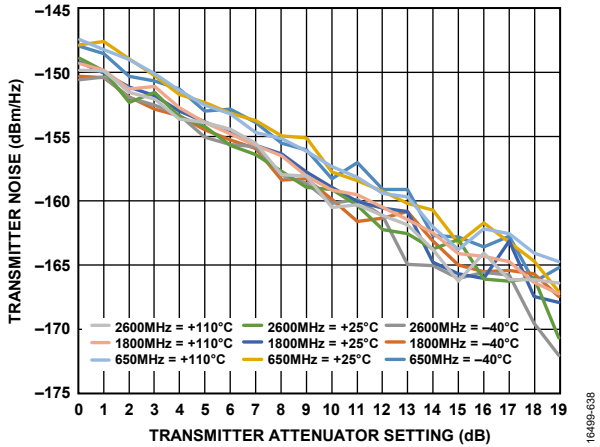


Figure 135. Transmitter Noise vs. Transmitter Attenuator Setting,

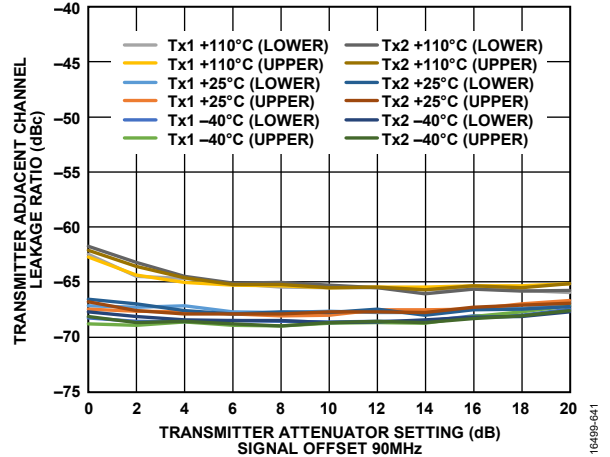


Figure 138. Transmitter Adjacent Channel Leakage Ratio vs. Transmitter Attenuator Setting, Signal Offset = 90 MHz, LO = 2850 MHz, LTE20 MHz, PAR = 12 dB, Upper Side and Lower Side

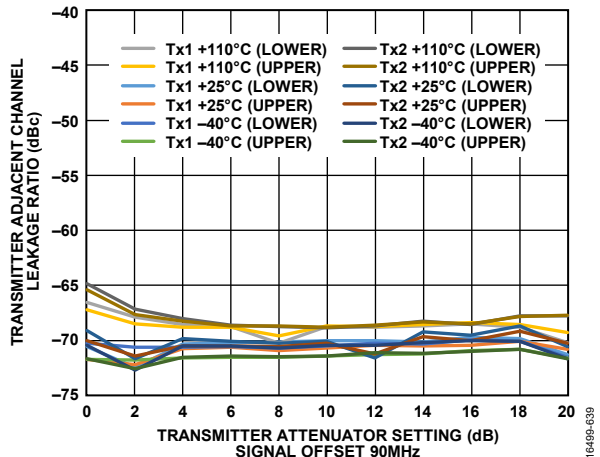


Figure 136. Transmitter Adjacent Channel Leakage Ratio vs. Transmitter Attenuator Setting, Signal Offset 90 MHz, LO = 650 MHz, LTE20 PAR = 12 dB, Upper Side and Lower Side

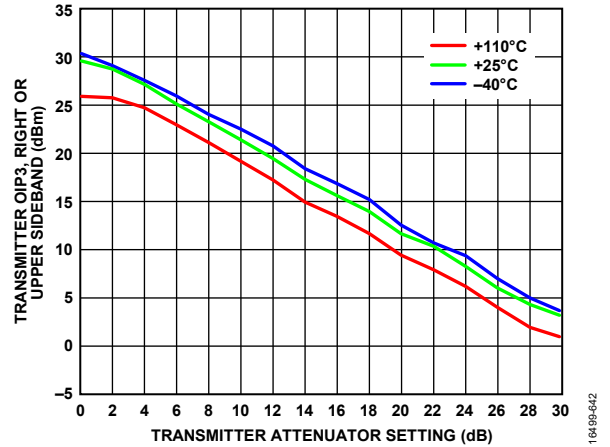


Figure 139. Transmitter OIP3, Right or Upper Sideband vs. Transmitter Attenuator Setting, LO = 850 MHz, 15 dB Digital Backoff per Tone

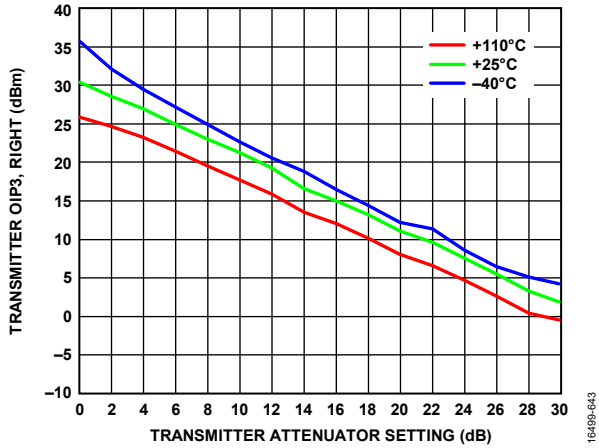


Figure 140. Transmitter OIP3, Right vs. Transmitter Attenuator Setting, LO = 1850 MHz, 15 dB Digital Backoff per Tone

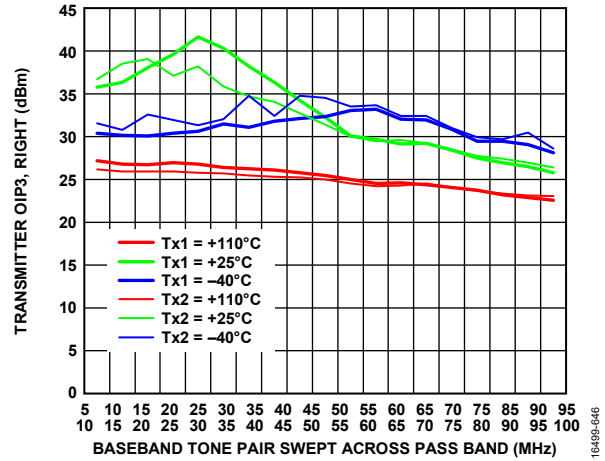


Figure 143. Transmitter OIP3, Right vs. Baseband Tone Pair Swept Across Pass Band, LO = 1850 MHz, 15 dB Digital Backoff per Tone

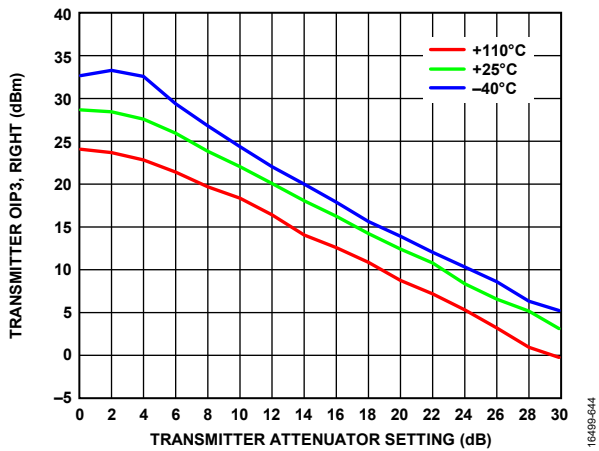


Figure 141. Transmitter OIP3, Right vs. Transmitter Attenuator Setting, LO = 2650 MHz, 15 dB Digital Backoff per Tone

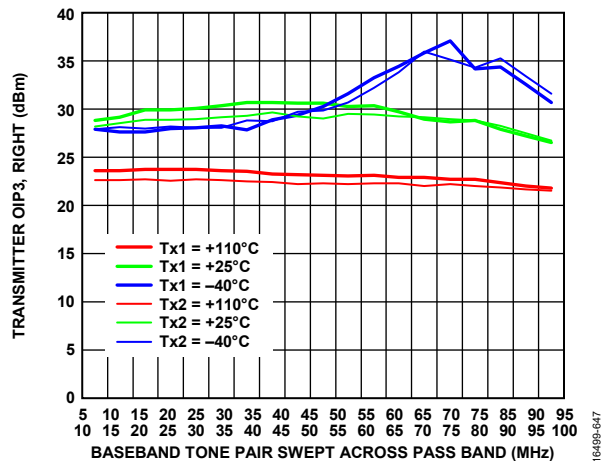


Figure 144. Transmitter OIP3, Right vs. Baseband Tone Pair Swept Across Pass Band, LO = 2850 MHz, 15 dB Digital Backoff per Tone

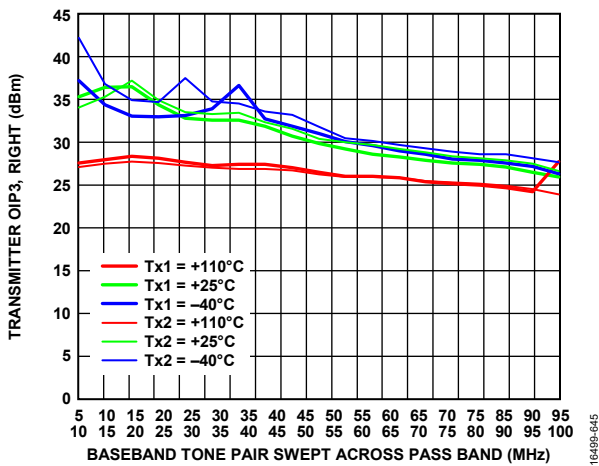


Figure 142. Transmitter OIP3, Right vs. Baseband Tone Pair Swept Across Pass Band, LO = 850 MHz, 15 dB Digital Backoff per Tone

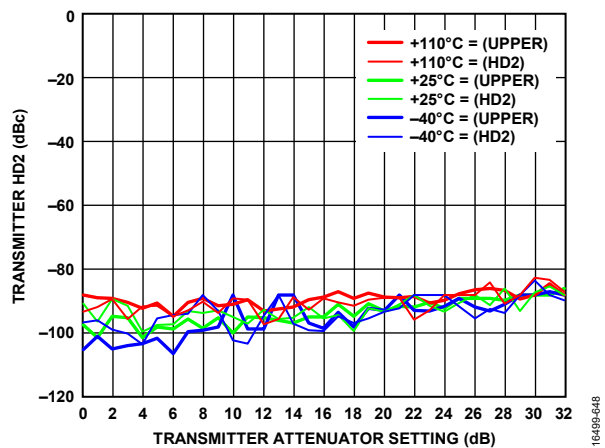


Figure 145. Transmitter HD2 vs. Transmitter Attenuator Setting, Baseband Frequency = 10 MHz, LO = 1850 MHz, Digital Backoff = 15 dB

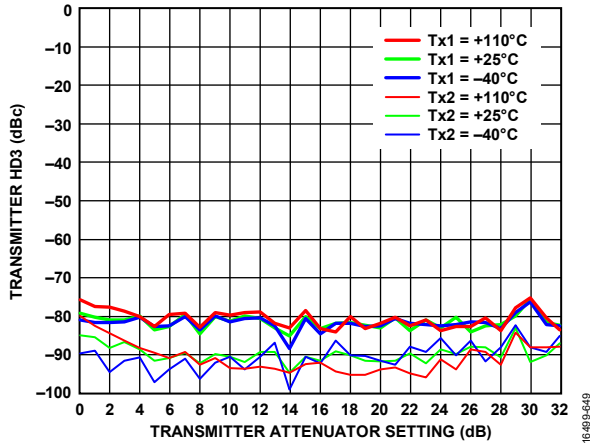


Figure 146. Transmitter HD3 vs. Transmitter Attenuator Setting, LO = 650 MHz, Digital Backoff = 15 dB

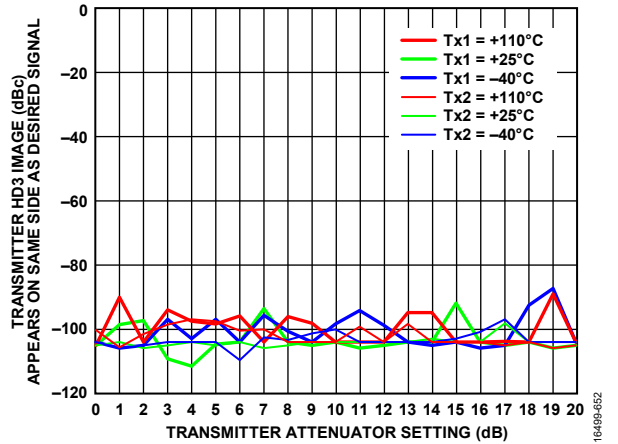


Figure 149. Transmitter HD3 Image Appears on Same Sideband as Desired Signal vs. Transmitter Attenuator Setting, LO = 1850 MHz Digital Backoff = 15 dB

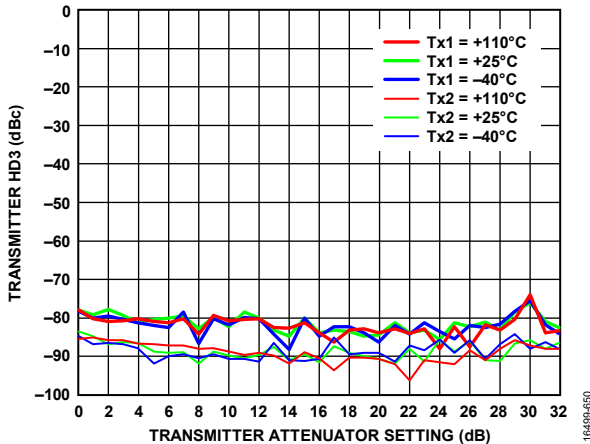


Figure 147. Transmitter HD3 vs. Transmitter Attenuator Setting, LO = 1850 MHz, Digital Backoff = 15 dB

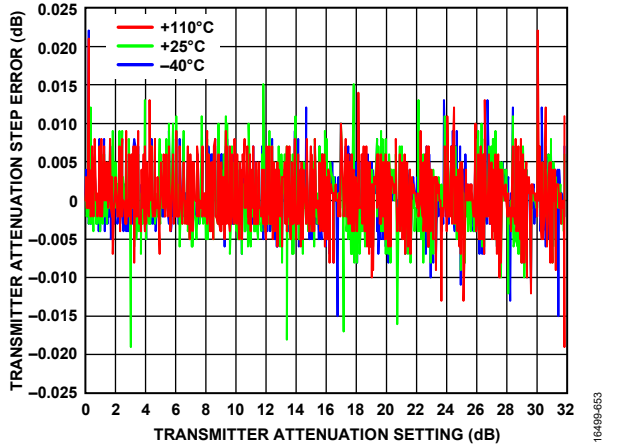


Figure 150. Transmitter Attenuation Step Error vs. Transmitter Attenuator Setting, LO = 650 MHz

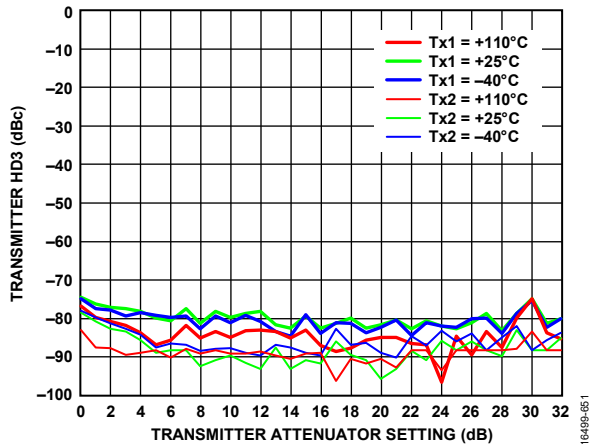


Figure 148. Transmitter HD3 vs. Transmitter Attenuator Setting, LO = 2850 MHz, Digital Backoff = 15 dB

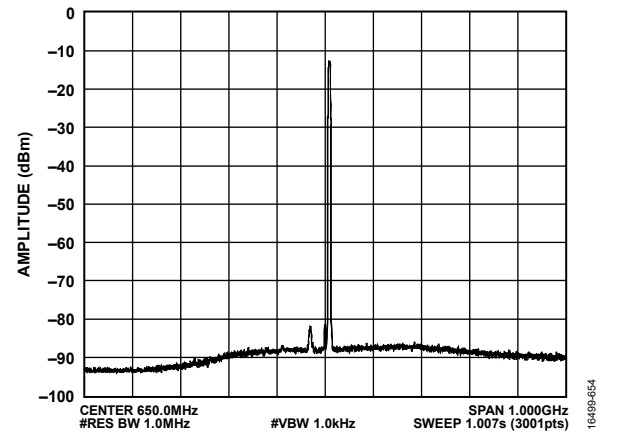


Figure 151. Amplitude vs. Frequency, Transmitter Output Spurious, Transmitter 1 = 650 MHz, LTE = 5 MHz, Offset = 10 MHz, RMS = -12 dBFS, Temperature = 25°C

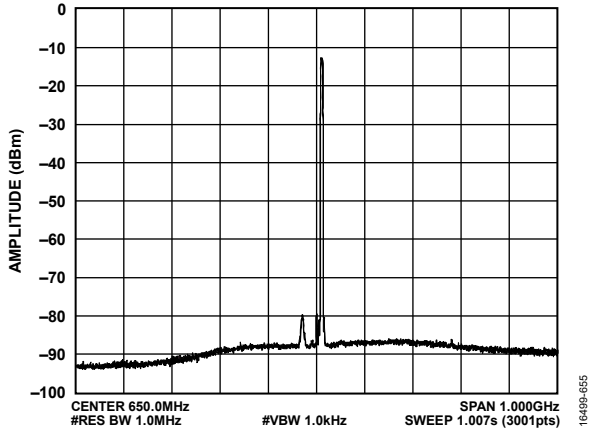


Figure 152. Amplitude vs. Frequency, Transmitter Output Spurious, Transmitter 2 = 650 MHz, LTE = 5 MHz, Offset = 10 MHz, RMS = -12 dBFS, Temperature = 25°C

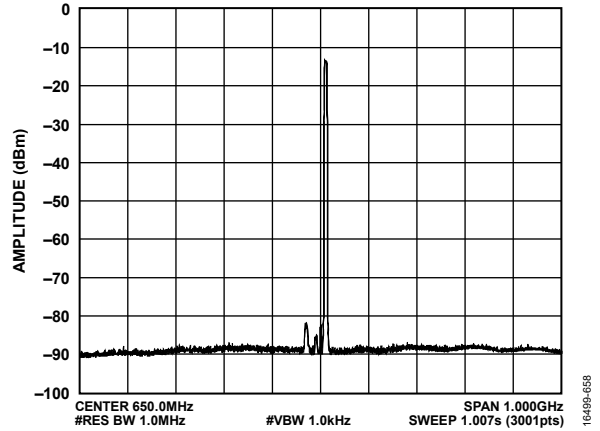


Figure 155. Amplitude vs. Frequency, Transmitter Output Spurious, Transmitter 1 = 2850 MHz, LTE = 5 MHz, Offset = 10 MHz, RMS = -12 dBFS, Temperature = 25°C

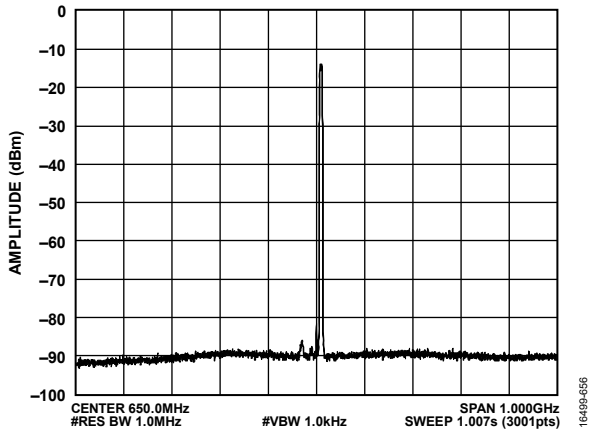


Figure 153. Amplitude vs. Frequency, Transmitter Output Spurious, Transmitter 1 = 1850 MHz, LTE = 5 MHz, Offset = 10 MHz, RMS = -12 dBFS, Temperature = 25°C

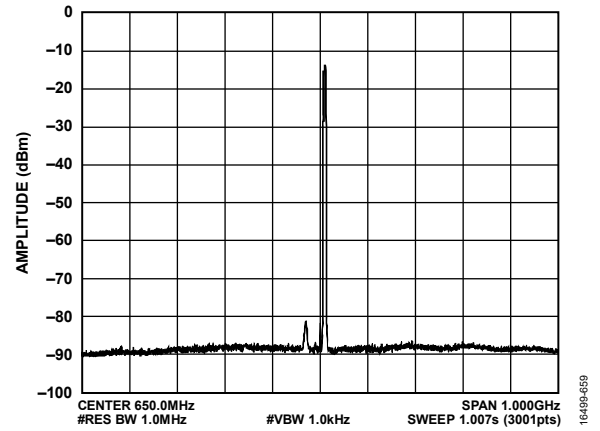


Figure 156. Amplitude vs. Frequency, Transmitter Output Spurious, Transmitter 2 = 2850 MHz, LTE = 5 MHz, Offset = 10 MHz, RMS = -12 dBFS, Temperature = 25°C

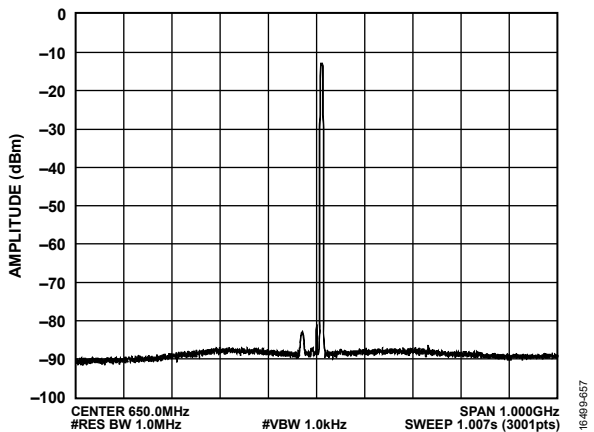


Figure 154. Amplitude vs. Frequency, Transmitter Output Spurious, Transmitter 2 = 1850 MHz, LTE = 5 MHz, Offset = 10 MHz, RMS = -12 dBFS, Temperature = 25°C

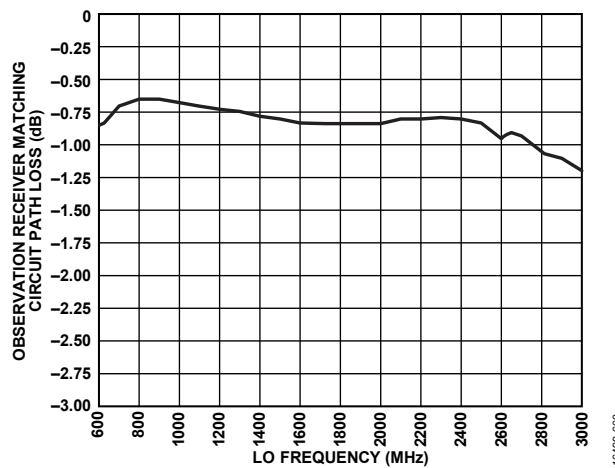


Figure 157. Observation Receiver Matching Circuit Path Loss vs. LO Frequency, Can Be Used for De-Embedding Performance Data



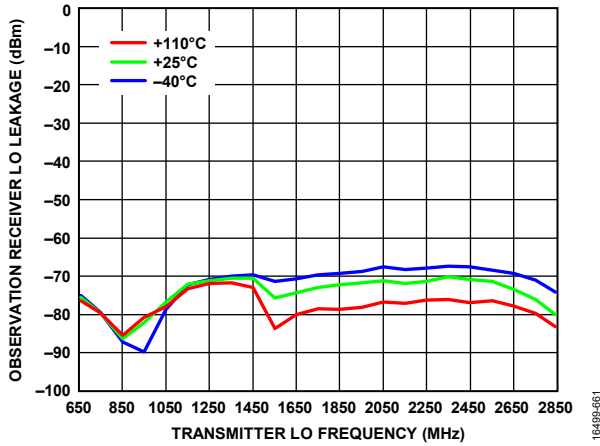


Figure 158. Observation Receiver LO Leakage vs. Transmitter LO Frequency,

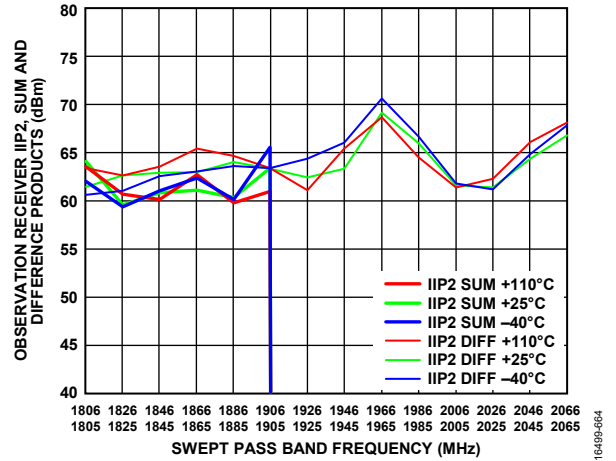


Figure 161. Observation Receiver IIP2, Sum and Difference Products vs. Swept Pass Band Frequency, LO = 1800 MHz, Attenuation = 0 dB

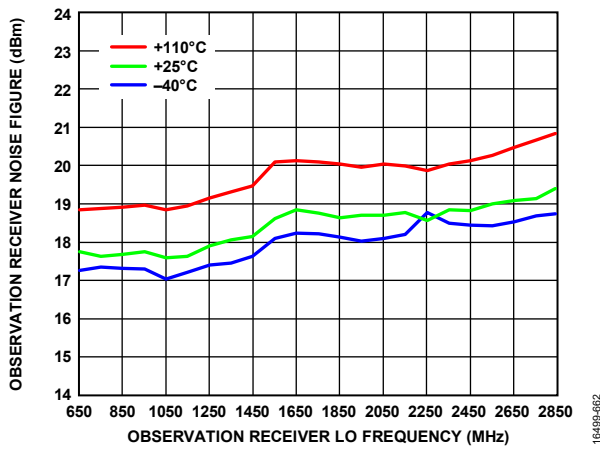


Figure 159. Observation Receiver Noise Figure vs. Observation Receiver LO Frequency, Total Nyquist Integration Bandwidth

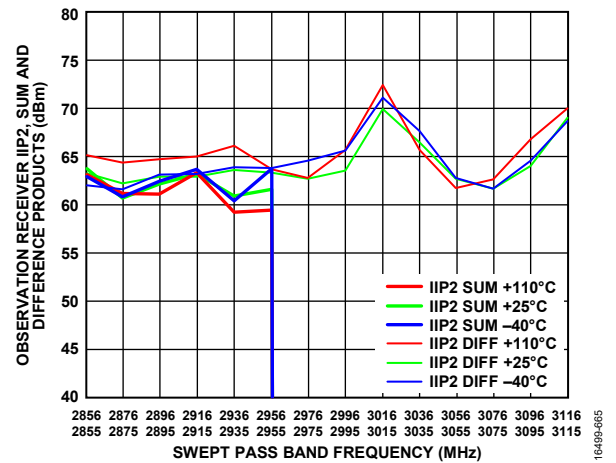


Figure 162. Observation Receiver IIP2, Sum and Difference Products vs. Swept Pass Band Frequency, LO = 2850 MHz, Attenuation = 0 dB

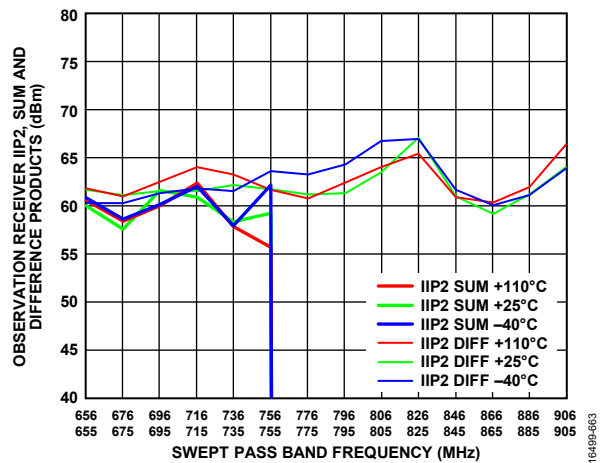


Figure 160. Observation Receiver IIP2, Sum and Difference Products vs. Swept Pass Band Frequency, LO = 650 MHz, Attenuation = 0 dB

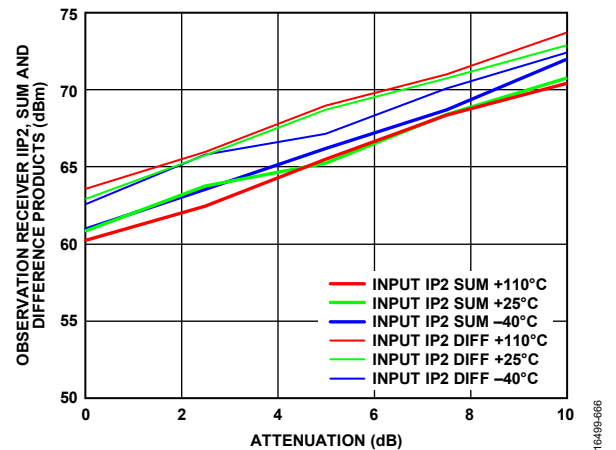


Figure 163. Observation Receiver IIP2, Sum and Difference Products vs. Attenuation, Tone 1 = 1845 MHz, Tone 2 = 1846 MHz at -19 dBm Plus Attenuation, LO = 1800 MHz

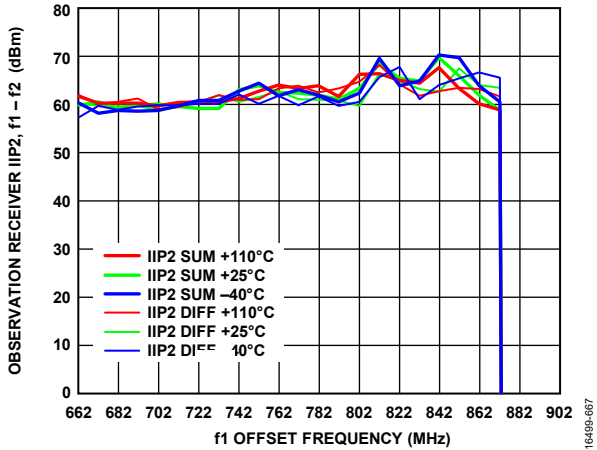


Figure 164. Observation Receiver IIP2,  $f_1 - f_2$  vs.  $f_1$  Offset Frequency, LO = 650 MHz, Tone 1 = 652 MHz, Tone 2 = Swept at -19 dBm Each, Attenuation = 0 dB

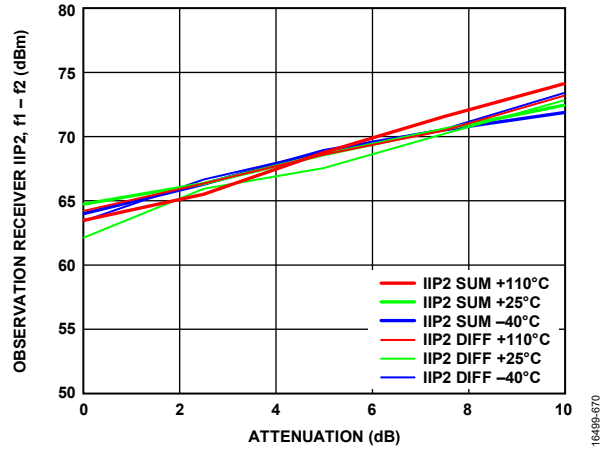


Figure 167. Observation Receiver IIP2,  $f_1 - f_2$  vs. Attenuation, LO = 1800 MHz, Tone 1 = 1802 MHz, Tone 2 = 1902 MHz at -19 dBm Plus Attenuation

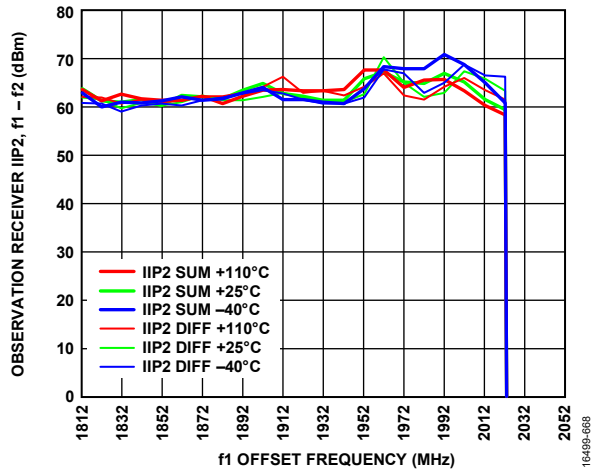


Figure 165. Observation Receiver IIP2,  $f_1 - f_2$  vs.  $f_1$  Offset Frequency, LO = 1800 MHz, Tone 1 = 1802 MHz, Tone 2 = Swept at -19 dBm Each, Attenuation = 0 dB

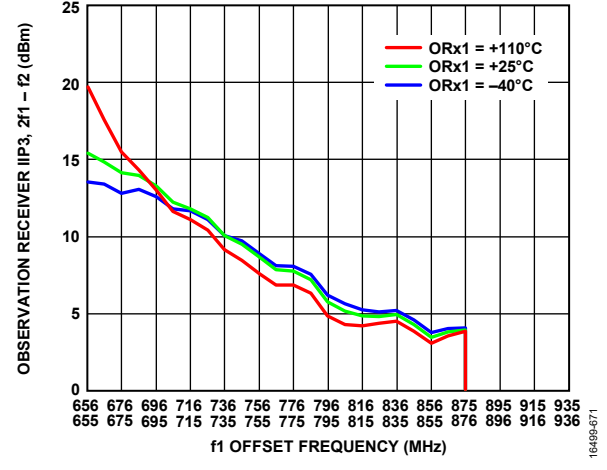


Figure 168. Observation Receiver IIP3,  $2f_1 - f_2$  vs.  $f_1$  Offset Frequency, LO = 650 MHz, Attenuation = 0 dB, Tones Separated by 1 MHz Swept Across Pass Band at -19 dBm Each

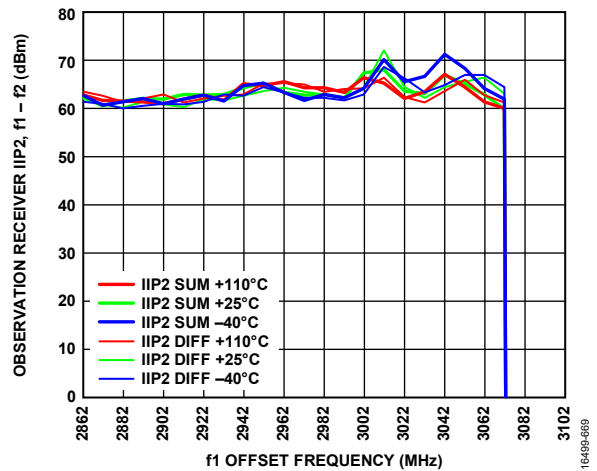


Figure 166. Observation Receiver IIP2,  $f_1 - f_2$  vs.  $f_1$  Offset Frequency, LO = 2850 MHz, Tone 1 = 2852 MHz, Tone 2 = Swept at -19 dBm Each, Attenuation = 0 dB

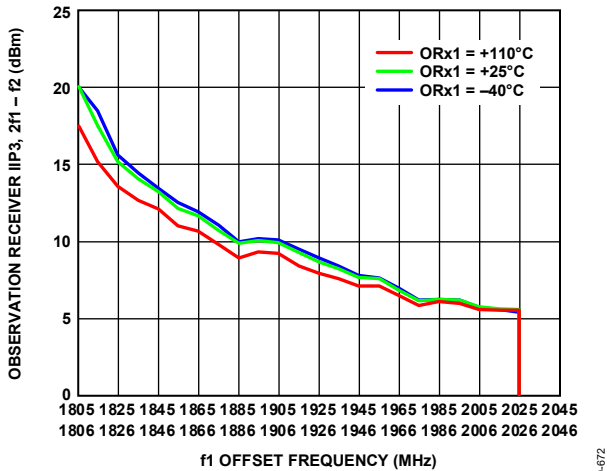


Figure 169. Observation Receiver IIP3,  $2f_1 - f_2$  vs.  $f_1$  Offset Frequency, LO = 1800 MHz, Attenuation = 0 dB, Tones Separated by 1 MHz Swept Across Pass Band at -19 dBm Each

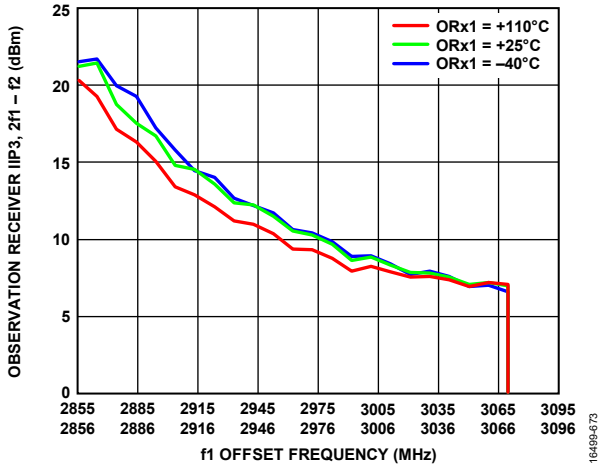


Figure 170. Observation Receiver IIP3, 2f1 – f2 vs. f1 Offset Frequency, LO = 2850 MHz, Attenuation = 0 dB, Tones Separated by 1 MHz Swept Across Pass Band at –19 dBm Each

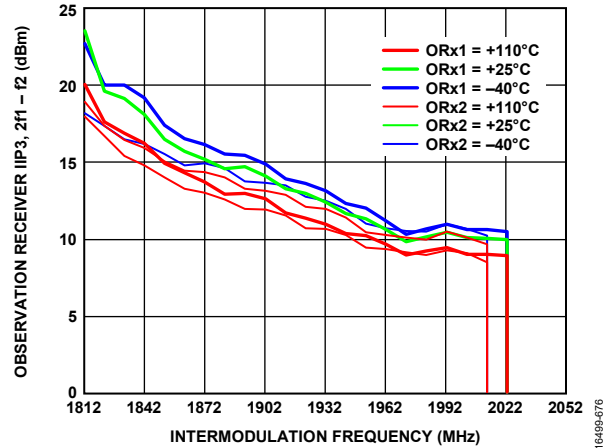


Figure 173. Observation Receiver IIP3, 2f1 – f2 vs. Intermodulation Frequency, LO = 1800 MHz, Tone 1 = 1802 MHz, Tone 2 = Swept at –19 dBm Each

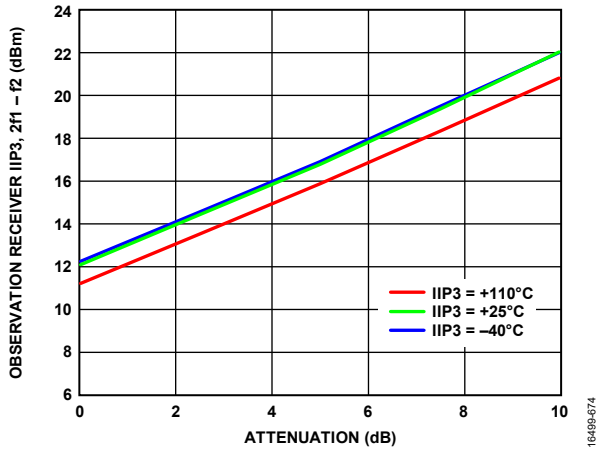


Figure 171. Observation Receiver IIP3, 2f1 – f2 vs. Attenuation, LO = 1800 MHz, Tone 1 = 1895 MHz, Tone 2 = 1896 MHz at –19 dBm Plus Attenuation

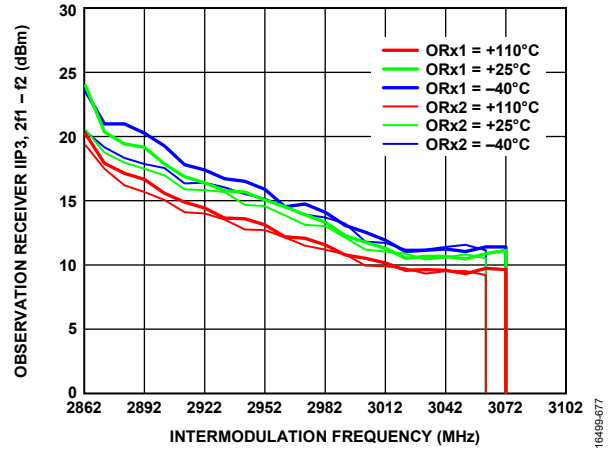


Figure 174. Observation Receiver IIP3, 2f1 – f2 vs. Intermodulation Frequency, LO = 2850 MHz, Tone 1 = 2852 MHz, Tone 2 = Swept at –19 dBm Each

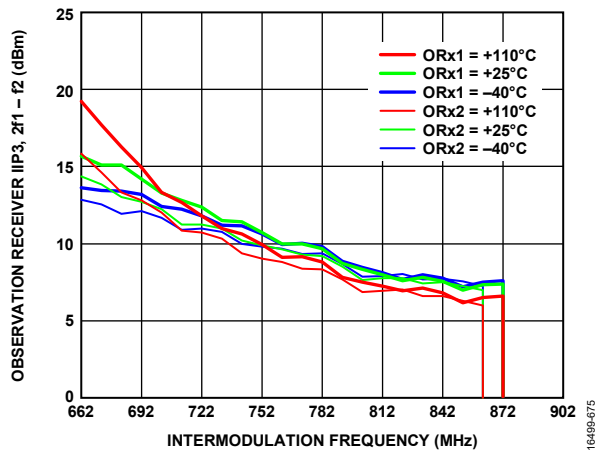


Figure 172. Observation Receiver IIP3, 2f1 – f2 vs. Intermodulation Frequency, LO = 650 MHz, Tone 1 = 652 MHz, Tone 2 = Swept at –19 dBm Each

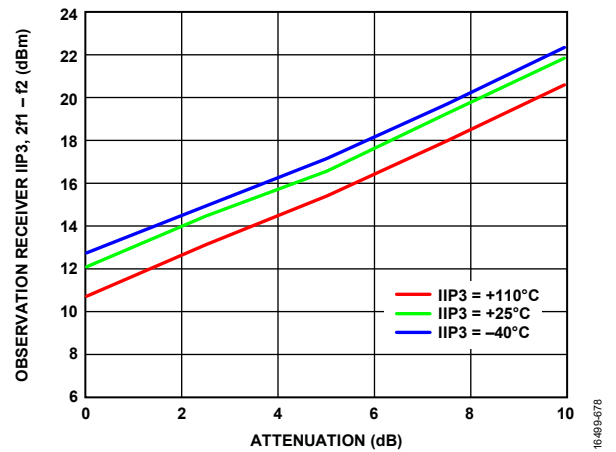


Figure 175. Observation Receiver IIP3, 2f1 – f2 vs. Attenuation, LO = 1800 MHz, Tone 1 = 1802 MHz, Tone 2 = 1922 MHz at –19 dBm Plus Attenuation

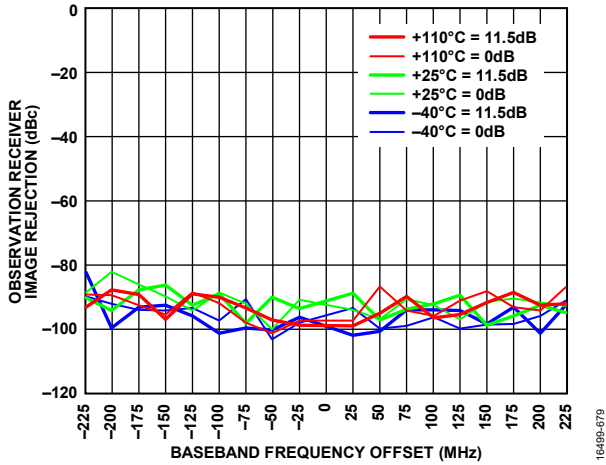


Figure 176. Observation Receiver Image Rejection vs. Baseband Frequency Offset, CW Signal Swept Across the Pass Band, LO = 650 MHz

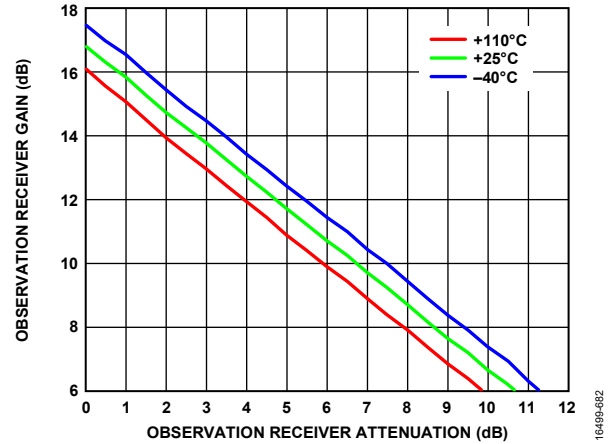


Figure 179. Observation Receiver Gain vs. Observation Receiver Attenuation, LO = 650 MHz

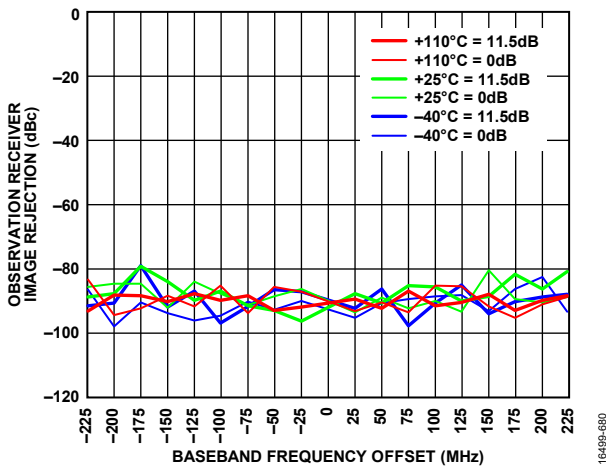


Figure 177. Observation Receiver Image Rejection vs. Baseband Frequency Offset, CW Signal Swept Across the Pass Band, LO = 1850 MHz

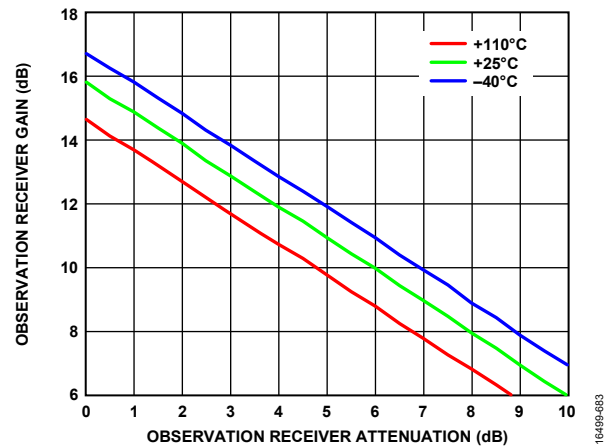


Figure 180. Observation Receiver Gain vs. Observation Receiver Attenuation, LO = 1800 MHz

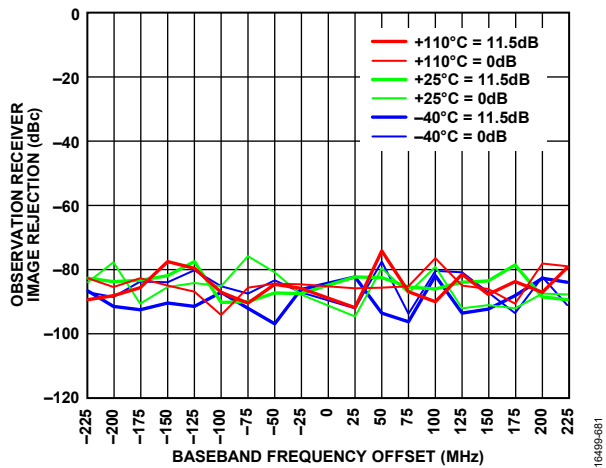


Figure 178. Observation Receiver Image Rejection vs. Baseband Frequency Offset, CW Signal Swept Across the Pass Band, LO = 2850 MHz

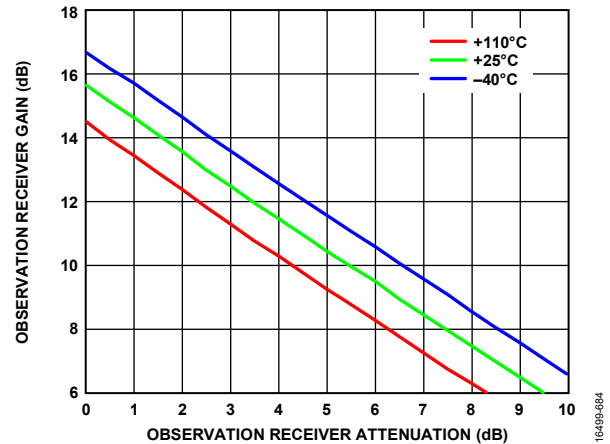


Figure 181. Observation Receiver Gain vs. Observation Receiver Attenuation, LO = 2800 MHz

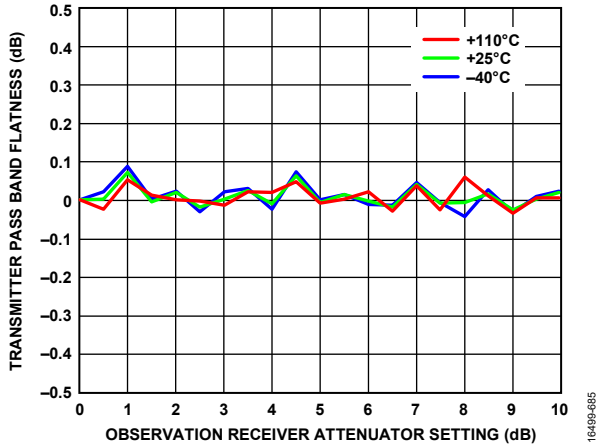


Figure 182. Transmitter Pass Band Flatness vs. Observation Receiver Attenuator Setting, LO = 2600 MHz

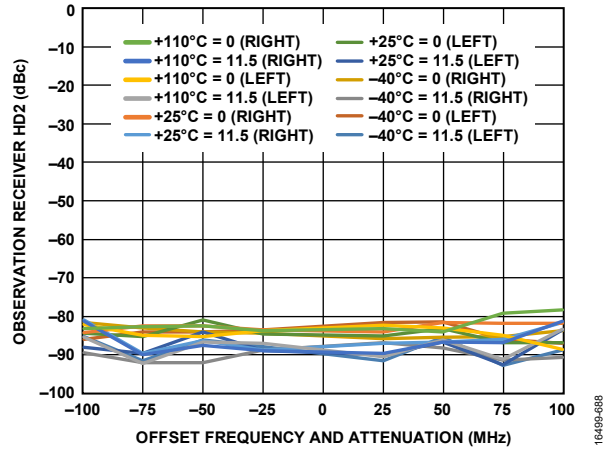


Figure 185. Observation Receiver HD2 vs. Offset Frequency and Attenuation, LO = 650 MHz, Tone Level = -20 dBm at 0 dB Attenuation

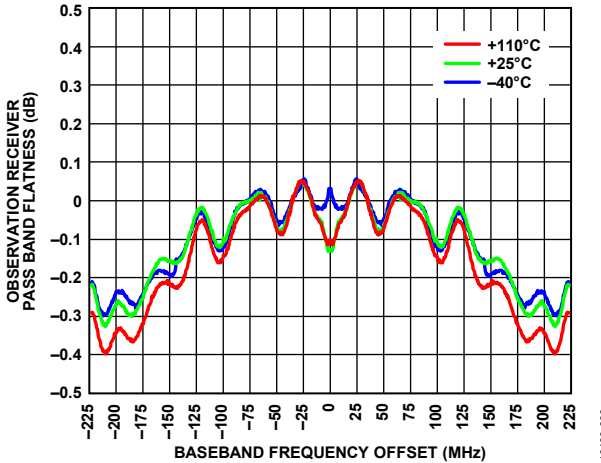


Figure 183. Observation Receiver Pass Band Flatness vs. Baseband Frequency Offset, LO = 1800 MHz

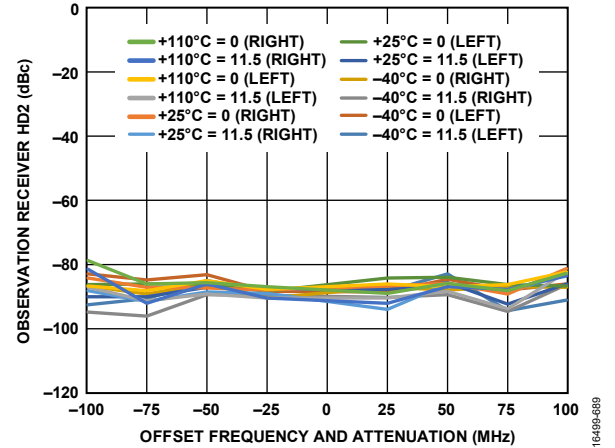


Figure 186. Observation Receiver HD2 vs. Offset Frequency and Attenuation, LO = 1850 MHz, Tone Level = -20 dBm at 0 dB Attenuation

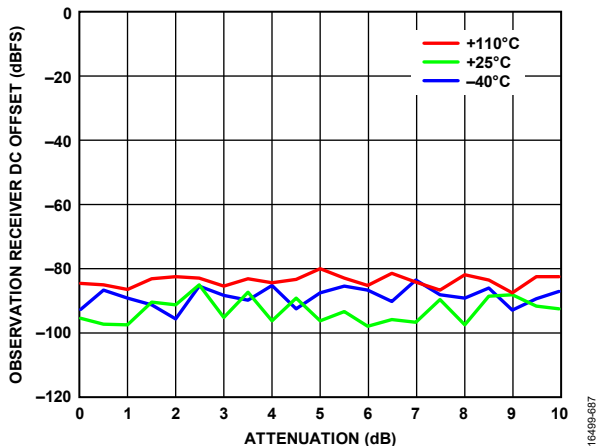


Figure 184. Observation Receiver DC Offset vs. Attenuation, LO = 1850 MHz

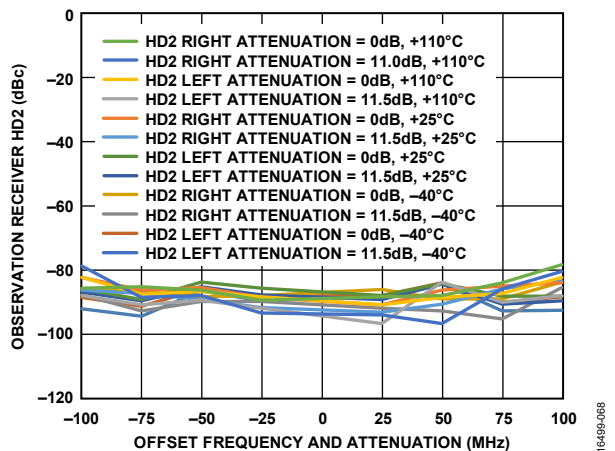


Figure 187. Observation Receiver HD2 vs. Offset Frequency and Attenuation, LO = 2850 MHz, Tone Level = -20 dBm at 0 dB Attenuation

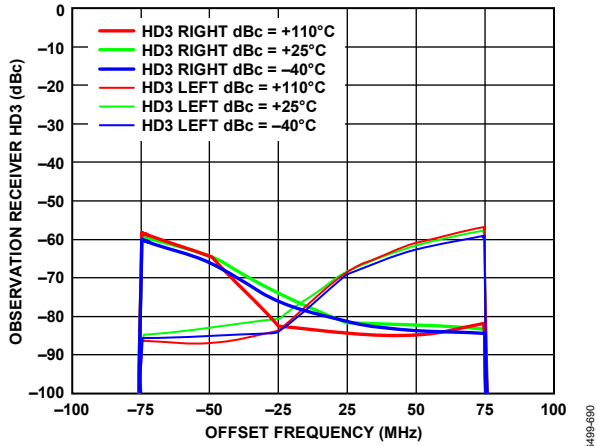


Figure 188. Observation Receiver HD3 vs. Offset Frequency, LO = 650 MHz, Tone Level = -20 dBm at 0 dB Attenuation

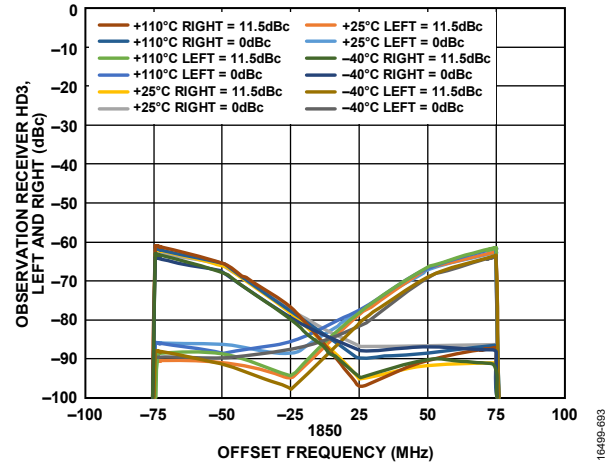


Figure 191. Observation Receiver HD3, Left and Right vs. Offset Frequency, LO = 1850 MHz, Observation Receiver Attenuation = 0 dB and 11.5 dB

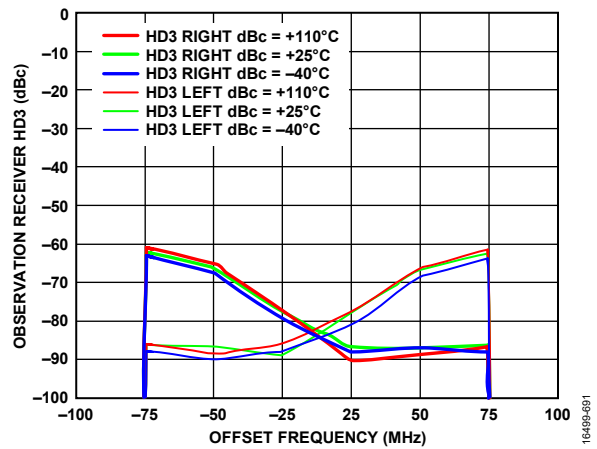


Figure 189. Observation Receiver HD3 vs. Offset Frequency, LO = 1850 MHz, Tone Level = -20 dBm at 0 dB Attenuation

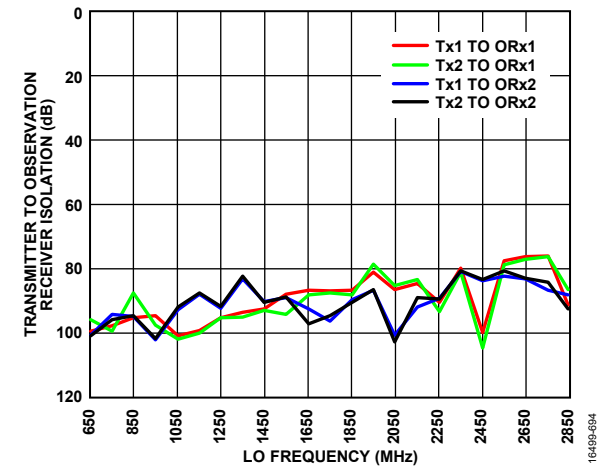


Figure 192. Transmitter to Observation Receiver Isolation vs. LO Frequency, Temperature = 25°C

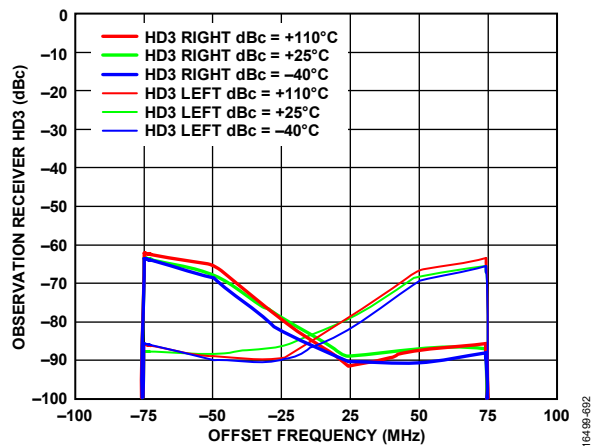


Figure 190. Observation Receiver HD3 vs. Offset Frequency, LO = 2850 MHz, Tone Level = -20 dBm at 0 dB Attenuation

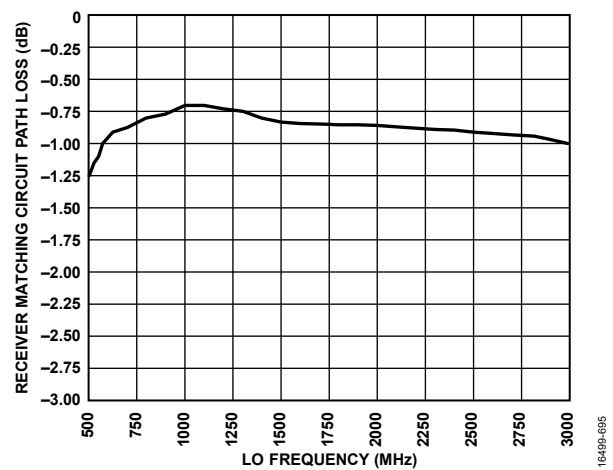


Figure 193. Receiver Matching Circuit Path Loss vs. LO Frequency, Can be Used for De-Embedding Performance Data

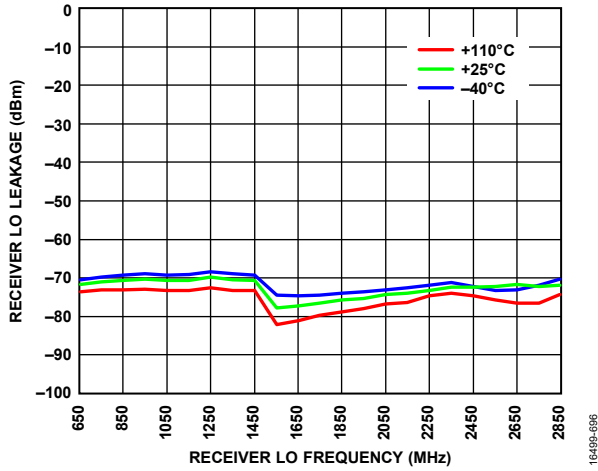


Figure 194. Receiver LO Leakage vs. Receiver LO Frequency, Receiver Attenuation = 0 dB, RF Bandwidth = 200 MHz, Sample Rate = 245.76 MSPS

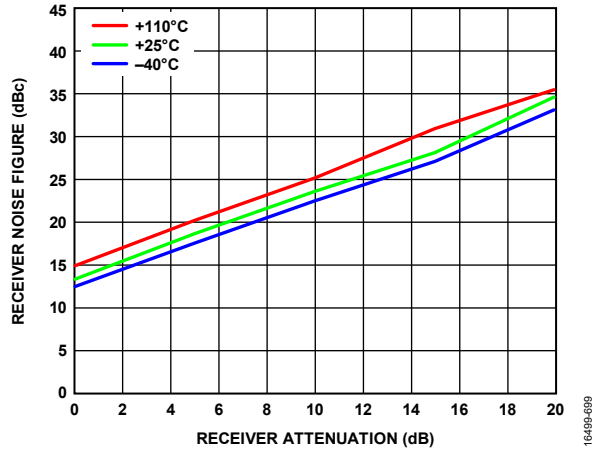


Figure 197. Receiver Noise Figure vs. Receiver Attenuation, LO = 2850 MHz, Receiver Bandwidth = 200 MHz Bandwidth, Sample Rate = 245.76 MSPS, Integration Bandwidth = 500 kHz to 100 MHz

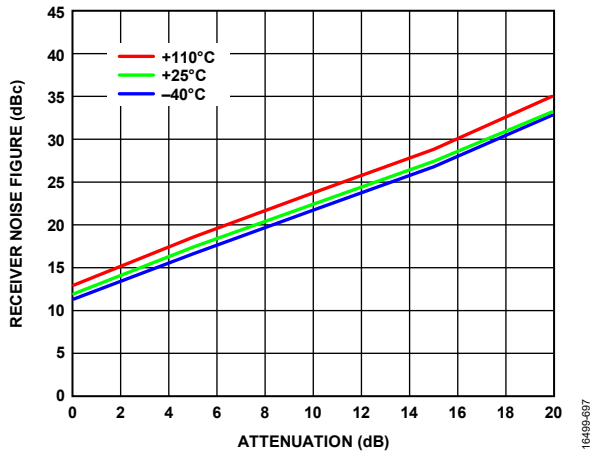


Figure 195. Receiver Noise Figure vs. Attenuation, LO = 650 MHz, Receiver Bandwidth = 200 MHz Bandwidth, Sample Rate = 245.76 MSPS, Integration Bandwidth = 500 kHz to 100 MHz

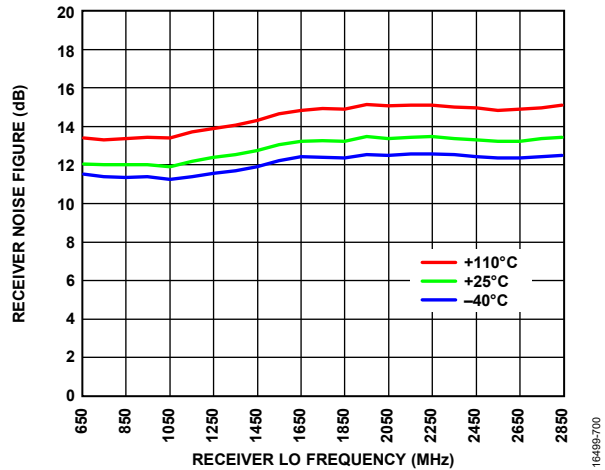


Figure 198. Receiver Noise Figure vs. Receiver LO Frequency, Receiver Attenuation = 0 dB, RF Bandwidth = 200 MHz, Sample Rate = 245.76 MSPS, Integration Bandwidth =  $\pm 100$  MHz

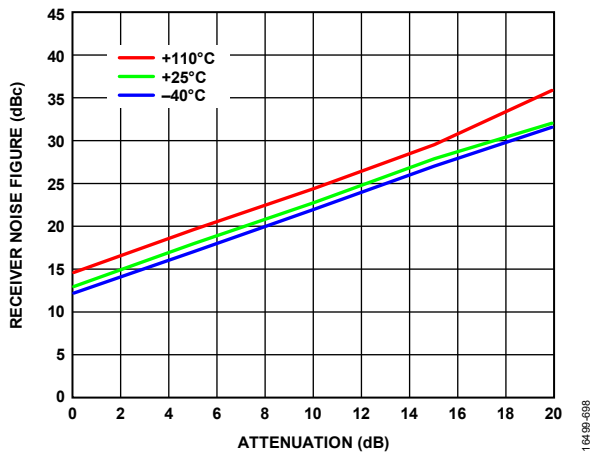


Figure 196. Receiver Noise Figure vs. Attenuation, LO = 1850 MHz, Receiver Bandwidth = 200 MHz Bandwidth, Sample Rate = 245.76 MSPS, Integration Bandwidth = 500 kHz to 100 MHz

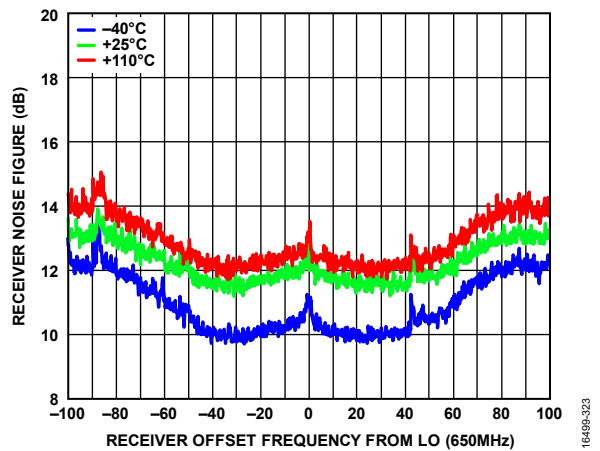


Figure 199. Receiver Noise Figure vs. Receiver Offset Frequency from LO, LO = 650 MHz

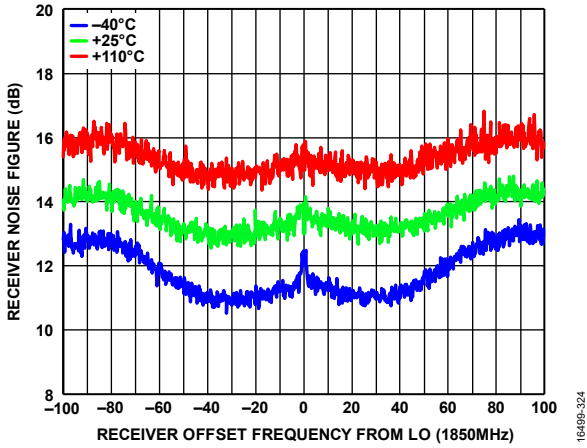


Figure 200. Receiver Noise Figure vs. Receiver Offset Frequency from LO, LO = 1850 MHz

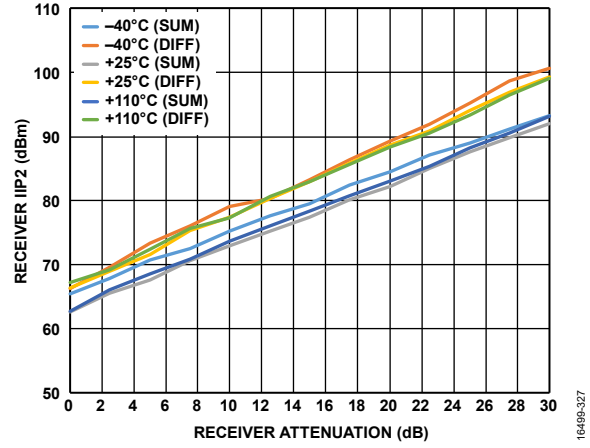


Figure 203. Receiver IIP2 vs. Receiver Attenuation, LO = 1800 MHz, Tones Placed at 1845 MHz and 1846 MHz, -21 dBm Each at Attenuation = 0 dB

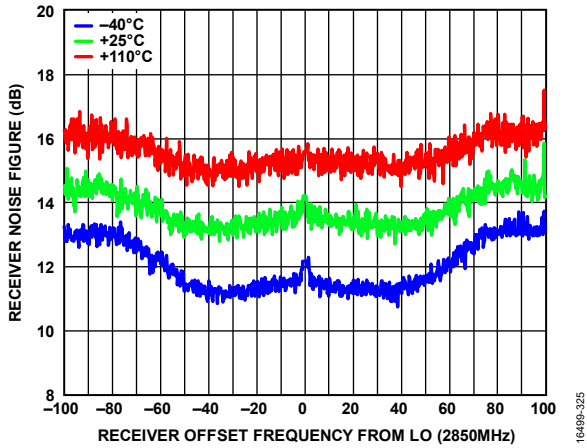


Figure 201. Receiver Noise Figure vs. Receiver Offset Frequency from LO, LO = 2850 MHz

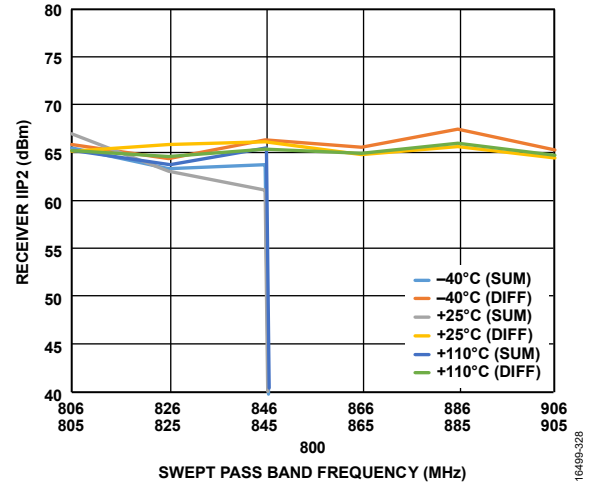


Figure 204. Receiver IIP2 Sum and Difference Across Bandwidth vs Swept Pass Band Frequency, LO = 800 MHz

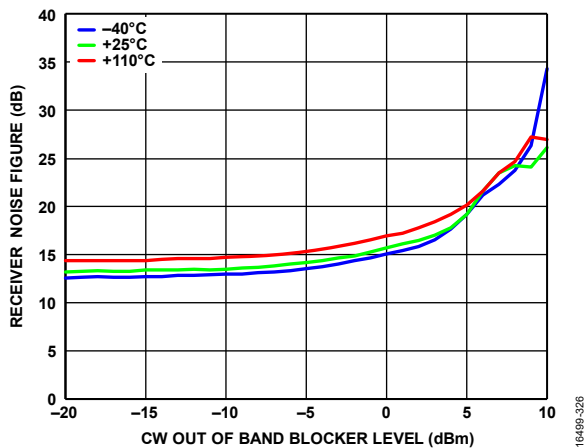


Figure 202. Receiver Noise Figure vs. CW Out of Band Blocker Level, Receiver LO = 1685 MHz, Blocker = 2085 MHz

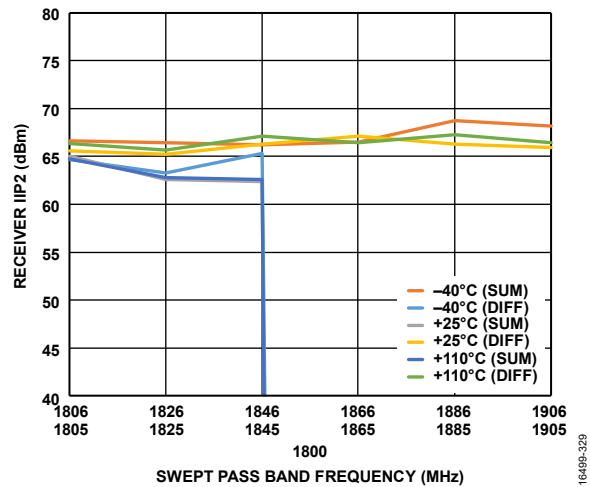


Figure 205. Receiver IIP2 Sum and Difference Across Bandwidth vs Swept Pass Band Frequency, LO = 1800 MHz



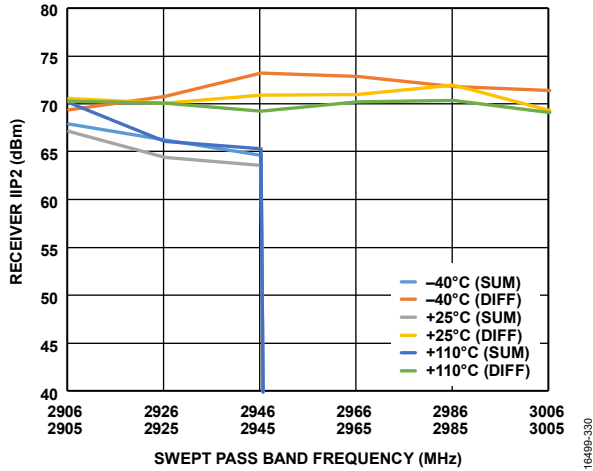


Figure 206. Receiver IIP2 Sum and Difference Across Bandwidth vs Swept Pass Band Frequency, LO = 2900 MHz

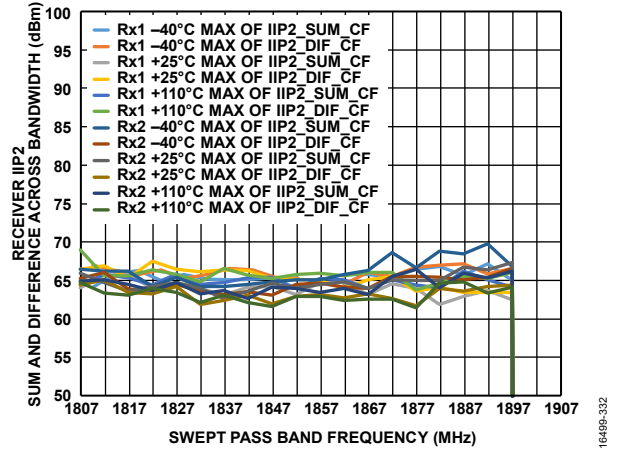


Figure 209. Receiver IIP2 Sum and Difference Across Bandwidth vs. Swept Pass Band Frequency, Receiver Attenuation = 0 dB, LO = 1800 MHz, Tone 1 = 1802 MHz, Tone 2 = Swept, -21 dBm Each

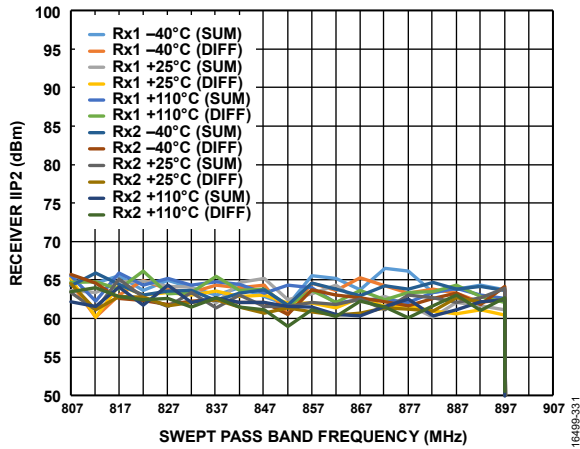


Figure 207. Receiver IIP2 vs. Swept Pass Band Frequency, LO = 1800 MHz, Tones Placed at 1802 MHz and 1892 MHz, -21 dBm Each at Attenuation = 0 dB

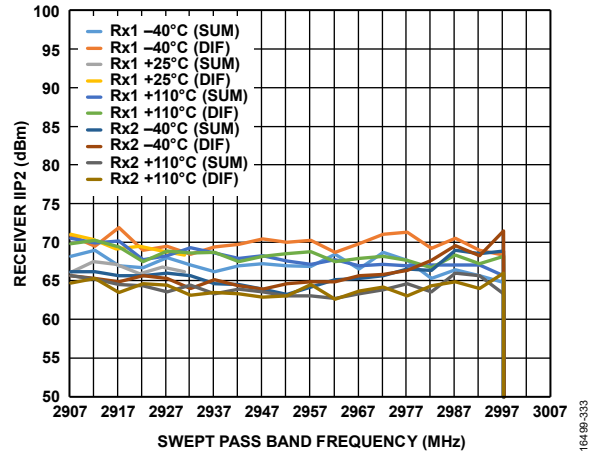


Figure 210. Receiver IIP2 Sum and Difference Across Bandwidth vs. Swept Pass Band Frequency, Receiver Attenuation = 0 dB, LO = 2900 MHz, Tone 1 = 2902 MHz, Tone 2 = Swept, -21 dBm Each

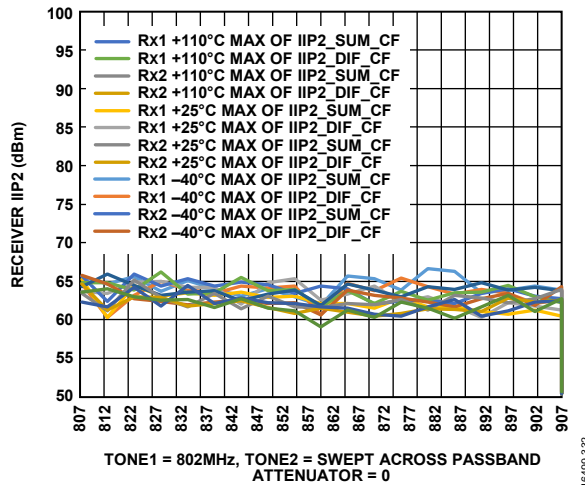


Figure 208. Receiver IIP2 Sum and Difference Across Bandwidth vs. Swept Pass Band Frequency, Receiver Attenuation = 0 dB, LO = 800 MHz, Tone 1 = 802 MHz, Tone 2 Swept, -21 dBm Each

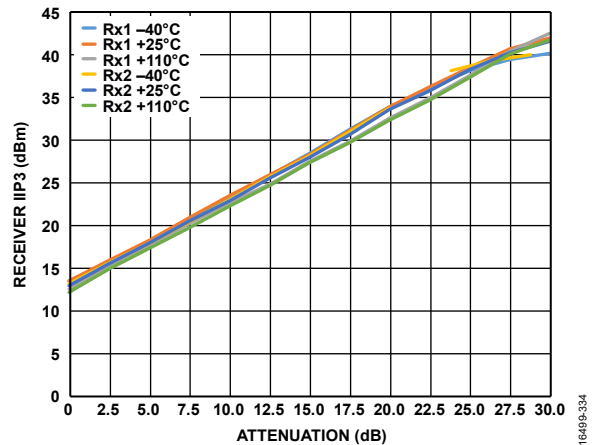


Figure 211. Receiver IIP3 vs. Attenuation, LO = 1800 MHz, Tone 1 = 1890 MHz, Tone 2 = 1891 MHz, -21 dBm Each at Attenuation = 0 dB

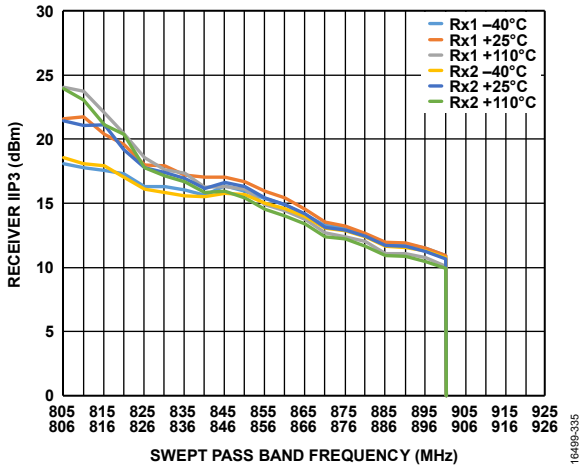


Figure 212. Receiver IIP3 vs. Swept Pass Band Frequency, Receiver Attenuation = 0 dB, LO = 800 MHz, Tone 2 = Tone 1 + 1 MHz, -21 dBm Each, Swept Across Pass Band

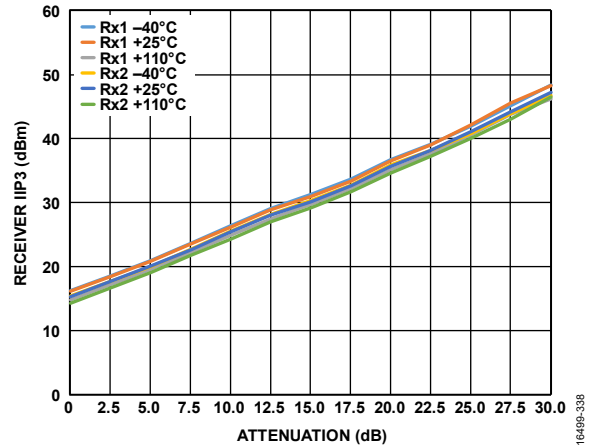


Figure 215. Receiver IIP3 vs. Attenuation, LO = 1800 MHz, Tone 1 = 1802 MHz, Tone 2 = 1892 MHz, -21 dBm Each at Attenuation = 0 dB

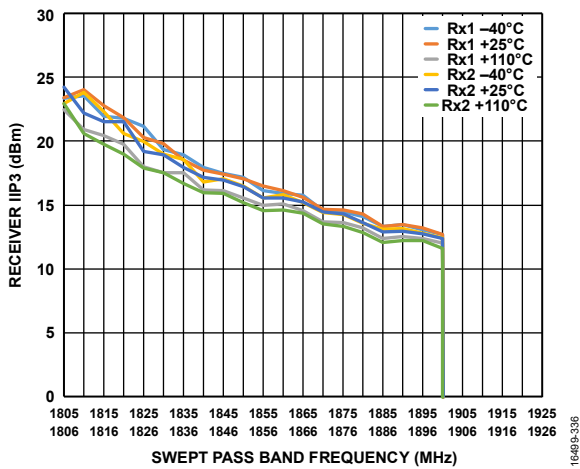


Figure 213. Receiver IIP3 vs. Swept Pass Band Frequency, Receiver Attenuation = 0 dB, LO = 1800 MHz, Tone 2 = Tone 1 + 1 MHz, -21 dBm Each, Swept Across Pass Band

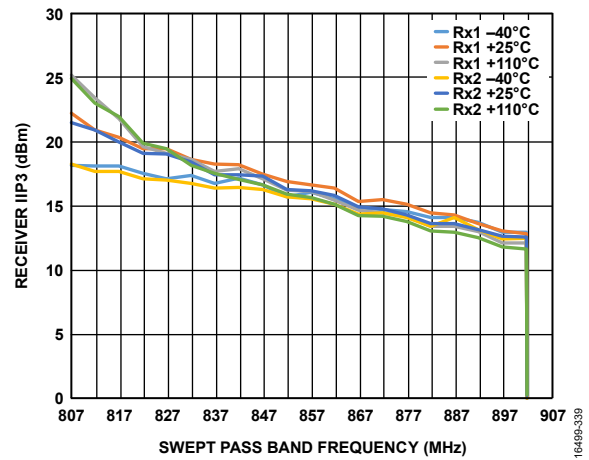


Figure 216. Receiver IIP3 vs. Swept Pass Band Frequency, Receiver Attenuation = 0 dB, LO = 800 MHz, Tone 1 = 802 MHz, Tone 2 = Swept Across Pass Band, -21 dBm Each

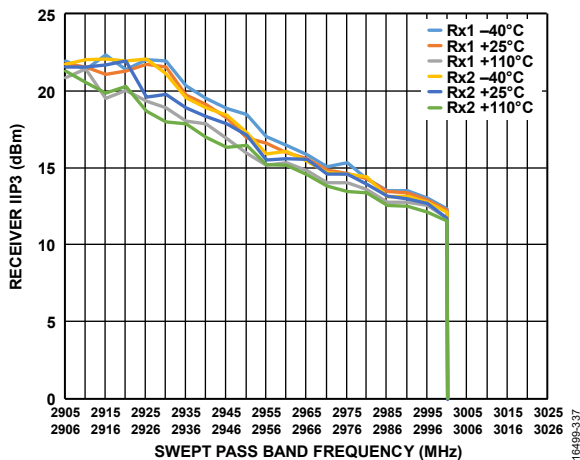


Figure 214. Receiver IIP3 vs. Swept Pass Band Frequency, Receiver Attenuation = 0 dB, LO = 2900 MHz, Tone 2 = Tone 1 + 1 MHz, -21 dBm Each, Swept Across Pass Band

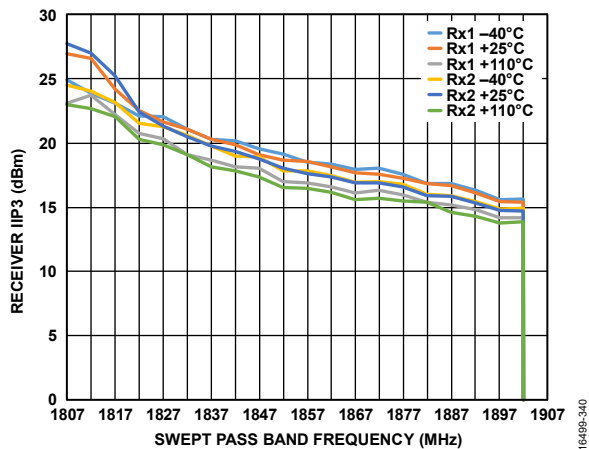


Figure 217. Receiver IIP3 vs. Swept Pass Band Frequency, Receiver Attenuation = 0 dB, LO = 1800 MHz, Tone 1 = 1802 MHz, Tone 2 = Swept Across Pass Band, -21 dBm Each

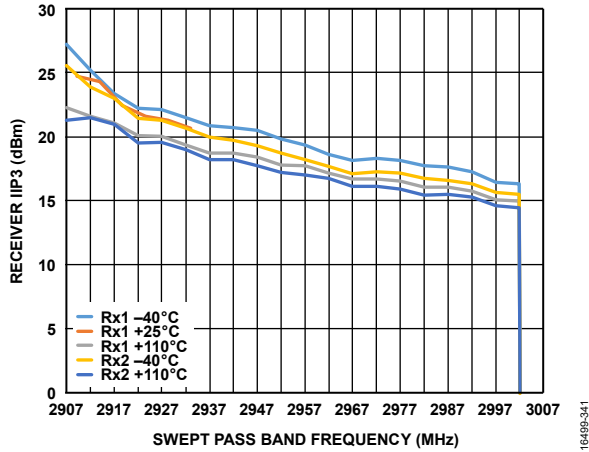


Figure 218. Receiver IIP3 vs. Swept Pass Band Frequency, Receiver Attenuation = 0 dB, LO = 2900 MHz, Tone 1 = 2902 MHz, Tone 2 = Swept Across Pass Band, -21 dBm Each

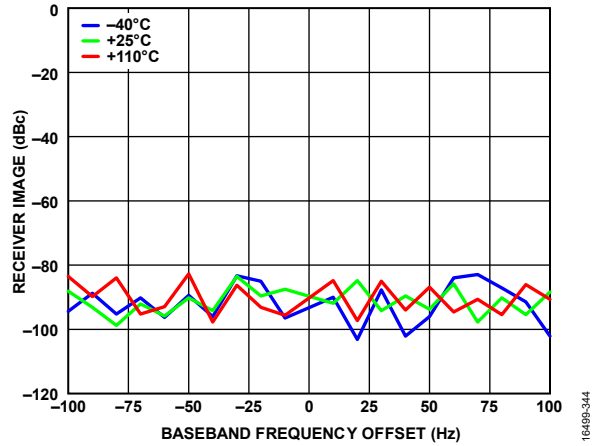


Figure 221. Receiver Image vs. Baseband Frequency Offset, Attenuation = 0 dB, RF Bandwidth = 200 MHz, Tracking Calibration Active, Sample Rate = 245.76 MSPS, LO = 2850 MHz

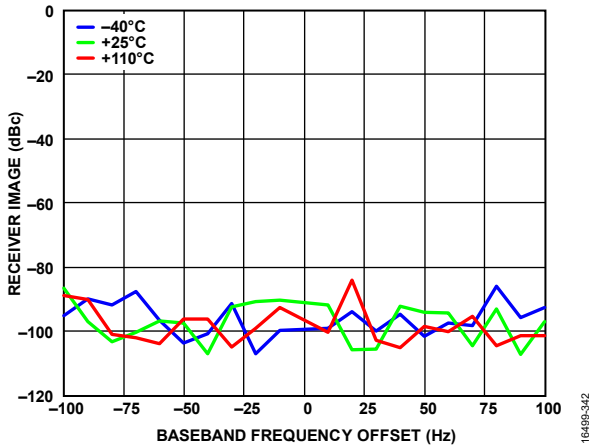


Figure 219. Receiver Image vs. Baseband Frequency Offset, Attenuation = 0 dB, RF Bandwidth = 200 MHz, Tracking Calibration Active, Sample Rate = 245.76 MSPS, LO = 650 MHz

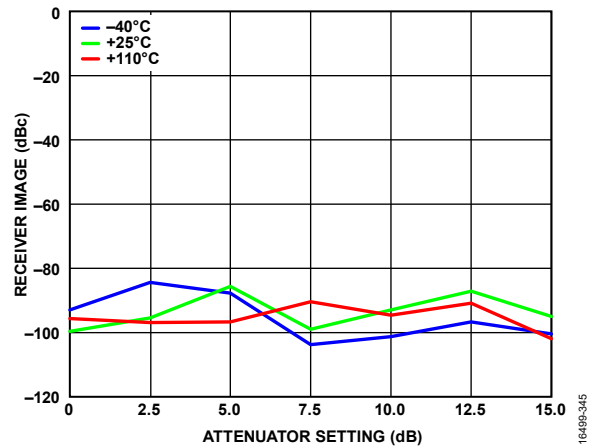


Figure 222. Receiver Image vs. Attenuator Setting, RF Bandwidth = 200 MHz, Tracking Calibration Active, Sample Rate = 245.76 MSPS, LO = 1850 MHz

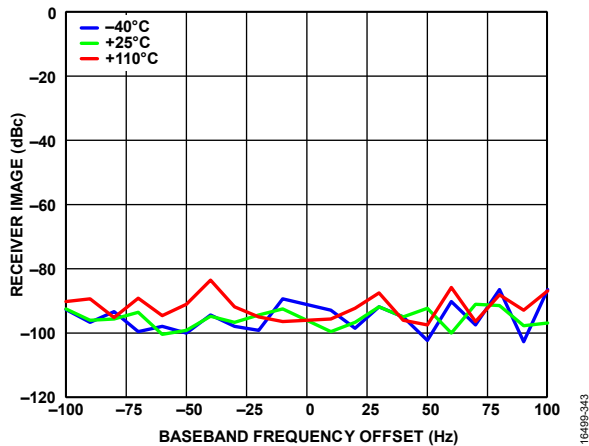


Figure 220. Receiver Image vs. Baseband Frequency Offset, Attenuation = 0 dB, RF Bandwidth = 200 MHz, Tracking Calibration Active, Sample Rate = 245.76 MSPS, LO = 1850 MHz

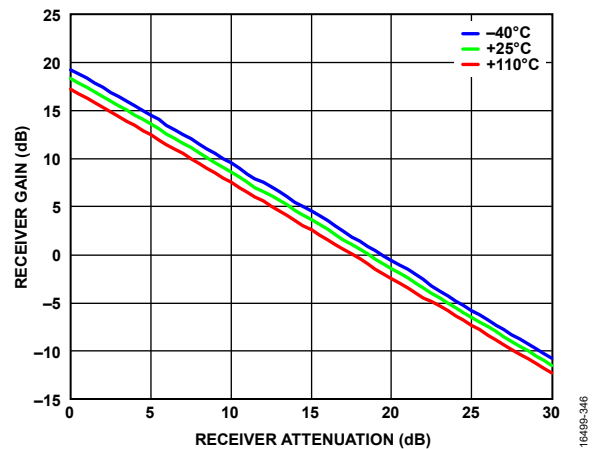


Figure 223. Receiver Gain vs. Receiver Attenuation, RF Bandwidth = 20 MHz, Sample Rate = 245.76 MSPS, LO = 1850 MHz

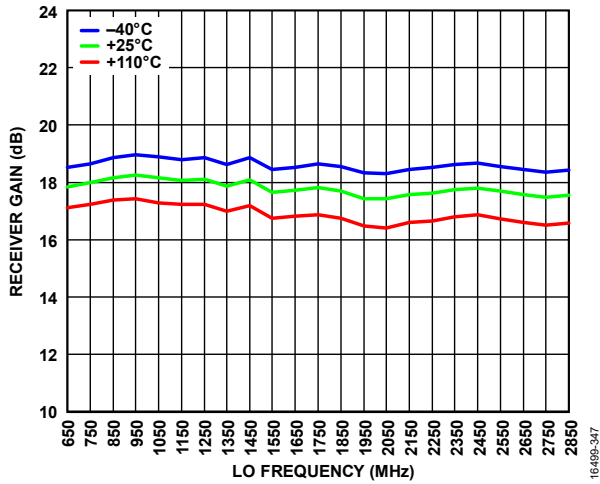


Figure 224. Receiver Gain vs. LO Frequency, RF Bandwidth = 20 MHz, Sample Rate = 245.76 MSPS

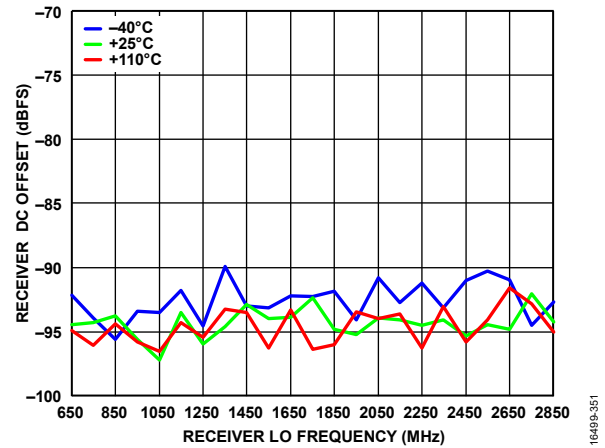


Figure 227. Receiver DC Offset vs. Receiver LO Frequency

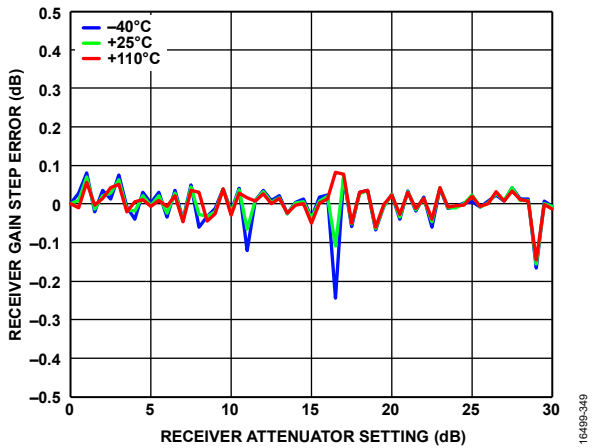


Figure 225. Receiver Gain Step Error vs. Receiver Attenuator Setting over Temperature

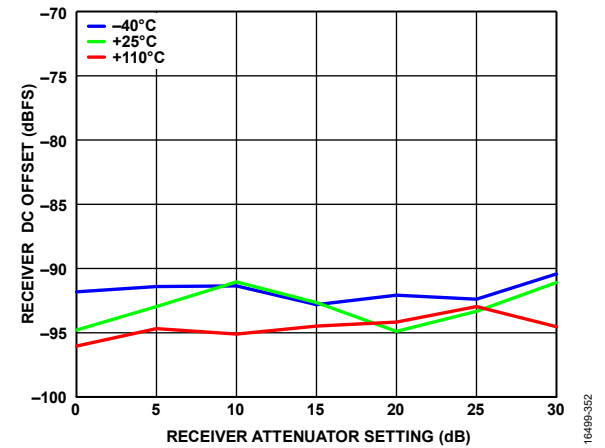


Figure 228. Receiver DC Offset vs. Receiver Attenuator Setting, LO = 1850 MHz

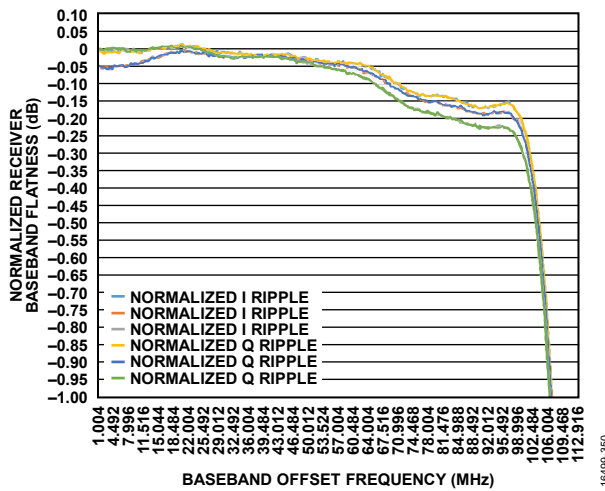


Figure 226. Normalized Receiver Baseband Flatness vs. Baseband Offset Frequency, LO = 2600 MHz

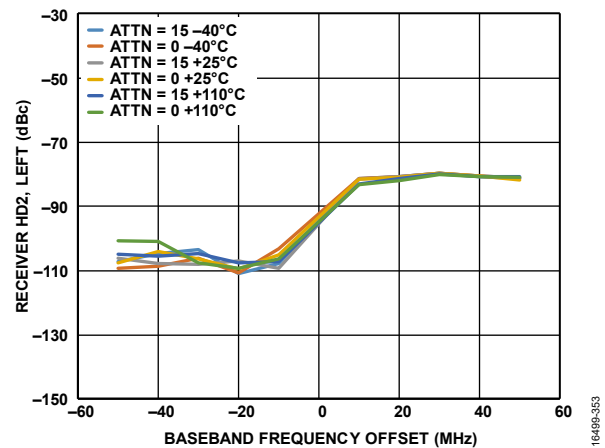


Figure 229. Receiver HD2, Left vs. Baseband Frequency Offset and Attenuation, Tone Level = -15 dBm at Attenuation = 0, HD2 Correction Configured for Low-Side Optimization, X-Axis = Baseband Frequency Offset of Fundamental Tone, Not the Frequency of the HD2 Product (HD2 Product = 2 × Baseband Frequency), LO = 650 MHz

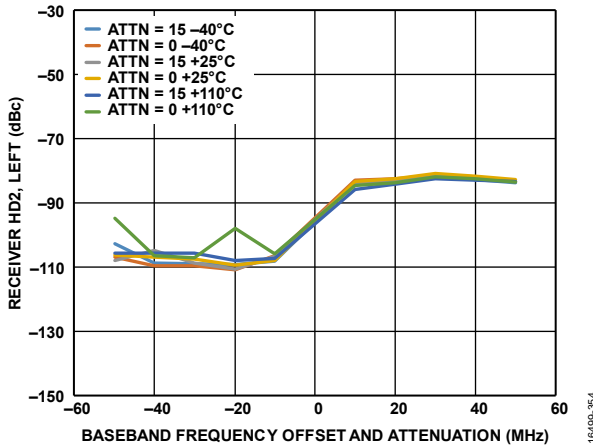


Figure 230. Receiver HD2, Left vs. Baseband Frequency Offset and Attenuation, Tone Level = -15 dBm at Attenuation = 0, HD2 Correction Configured for Low-Side Optimization, X-Axis = Baseband Frequency Offset of the Fundamental Tone, Not the Frequency of the HD2 Product (HD2 Product = 2 × the Baseband Frequency), LO = 1850 MHz

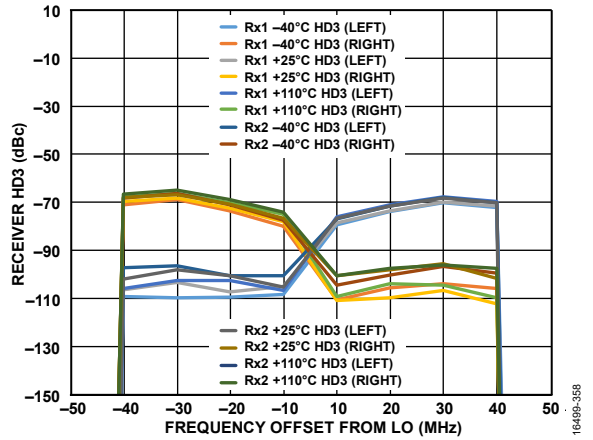


Figure 233. Receiver HD3 vs. Frequency Offset from LO, Tone Level = -15 dBm at Attenuation = 0, LO = 2850 MHz

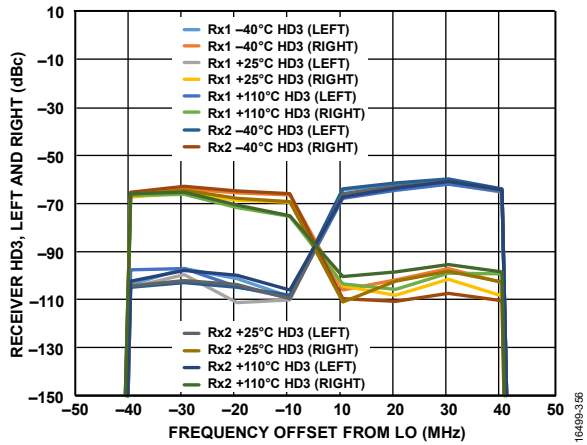


Figure 231. Receiver HD3, Left and Right vs. Frequency Offset from LO, Tone Level = -15 dBm at Attenuation = 0, LO = 650 MHz

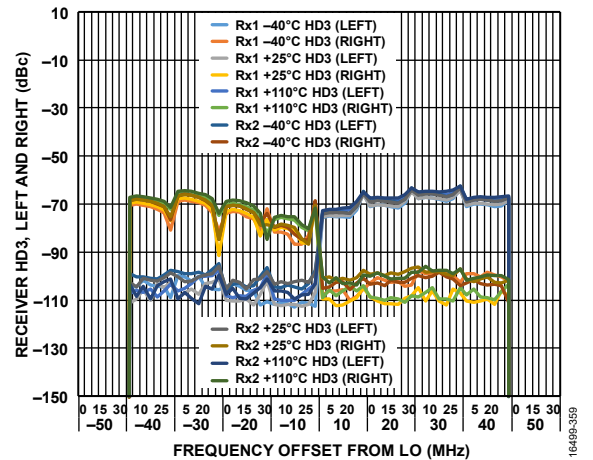


Figure 234. Receiver HD3, Left and Right vs. Frequency Offset from LO, Baseband Tone Held Constant, Tone Level Increased 1 for 1 as Attenuator is Swept from 0 dB to 30 dB, HD3 Right (High-Side): Tone on Same Side as HD3 Product, HD3 Left (Low-Side): Tone on Opposite Side as HD3 Product, CW Signal, LO = 1850 MHz, Tone Level = -15 dBm at Attenuation = 0 dB

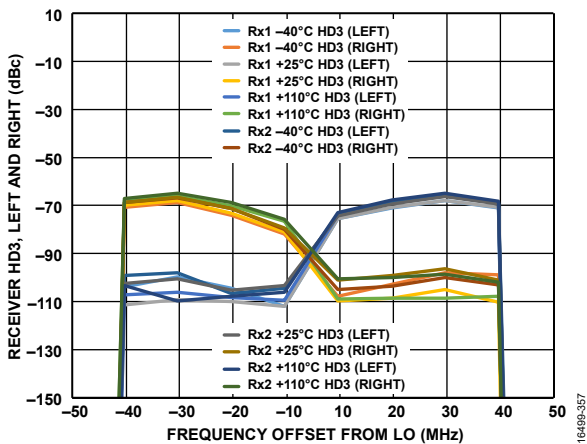


Figure 232. Receiver HD3, Left and Right vs. Frequency Offset from LO, Tone Level = -15 dBm at Attenuation = 0, LO = 1850 MHz

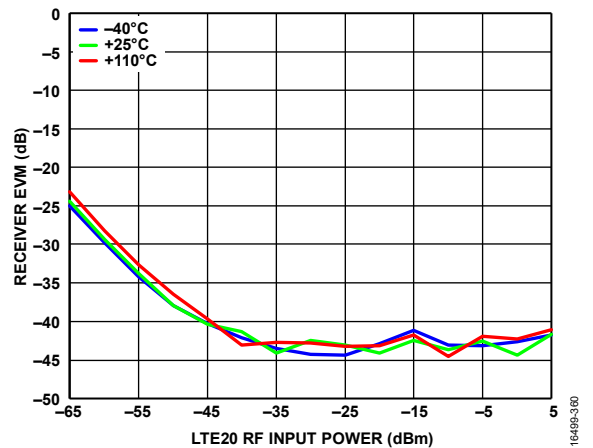


Figure 235. Receiver EVM vs. LTE20 RF Input Power, LTE = 20 MHz RF Signal, LO = 600 MHz

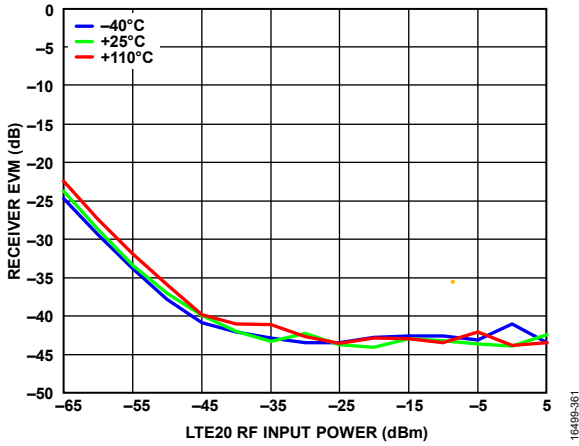


Figure 236. Receiver EVM vs. LTE20 RF Input Power, LTE = 20 MHz RF Signal, LO = 1800 MHz

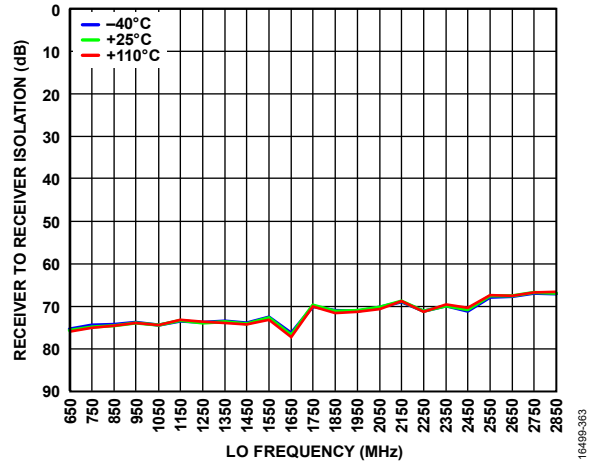


Figure 238. Receiver to Receiver Isolation vs. LO Frequency

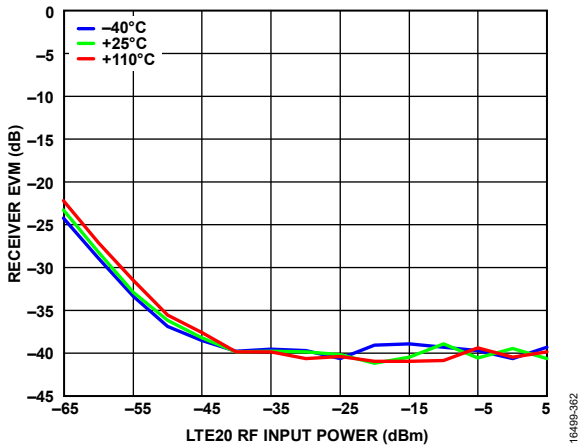


Figure 237. Receiver EVM vs. LTE20 RF Input Power, LTE = 20 MHz RF Signal, LO = 2700 MHz

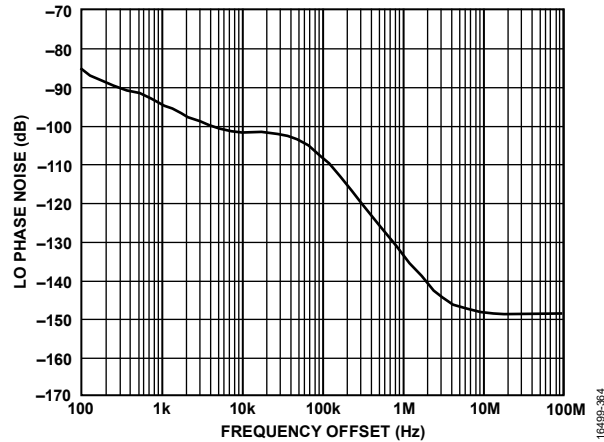


Figure 239. LO Phase Noise vs. Frequency Offset, LO = 1900 MHz, RMS Phase Error Integrated from 2 kHz to 18 MHz, Spectrum Analyzer Limits Far Out Noise

3400 MHz TO 4800 MHz BAND

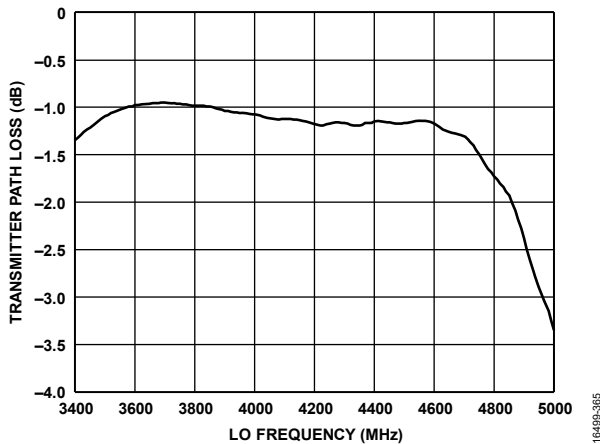


Figure 240. Transmitter Path Loss vs. LO Frequency (Simulation), Can Be Used for De-Embedding Performance Data

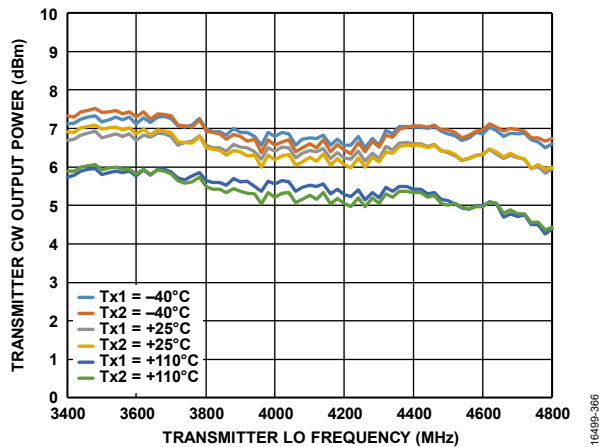


Figure 241. Transmitter CW Output Power vs. Transmitter LO Frequency, Transmitter QEC and External LO Leakage Active, Transmitter in 200 MHz/450 MHz Bandwidth Mode, IQ Rate = 491.52 MHz, Attenuation = 0 dB, Not De-Embedded

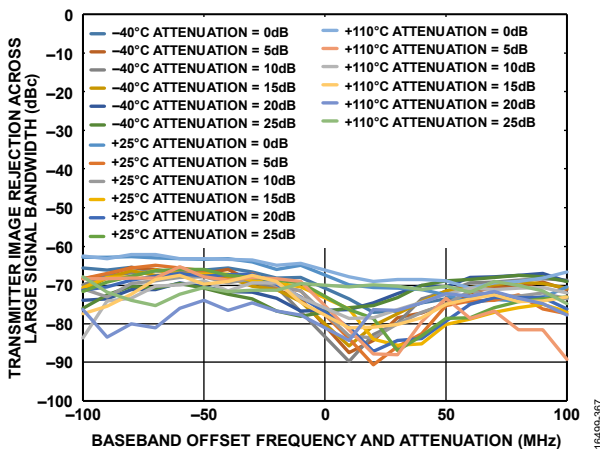


Figure 242. Transmitter Image Rejection Across Large Signal Bandwidth vs. Baseband Offset Frequency and Attenuation, QEC Trained with Three Tones Placed at 10 MHz, 50 MHz, and 100 MHz (Tracking On), Total Combined Power = -6 dBFS, Correction Then Frozen (Tracking Turned Off), CW Tone Swept Across Large Signal Bandwidth, LO = 3700 MHz

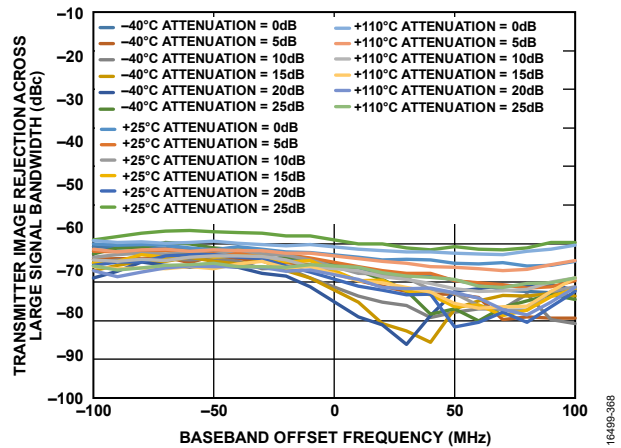


Figure 243. Transmitter Image Rejection Across Large Signal Bandwidth vs. Baseband Offset Frequency and Attenuation, QEC Trained with Three Tones (Tracking On), Total Combined Power = -6 dBFS, Correction Then Frozen (Tracking Turned Off), CW Tone Swept Across Large Signal Bandwidth, LO = 4600 MHz

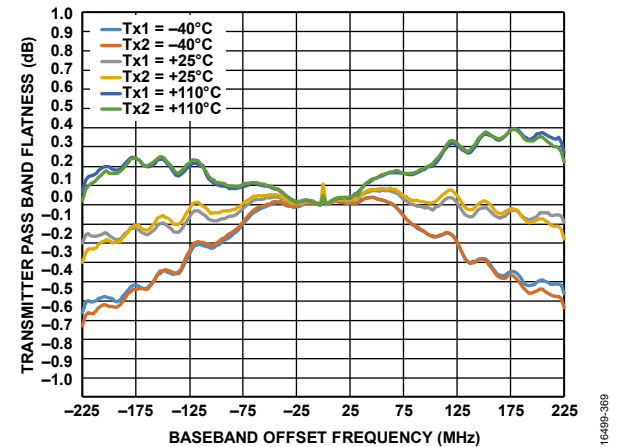


Figure 244. Transmitter Pass Band Flatness vs. Baseband Offset Frequency, Off Chip Match Response De-Embedded, LO = 3600 MHz

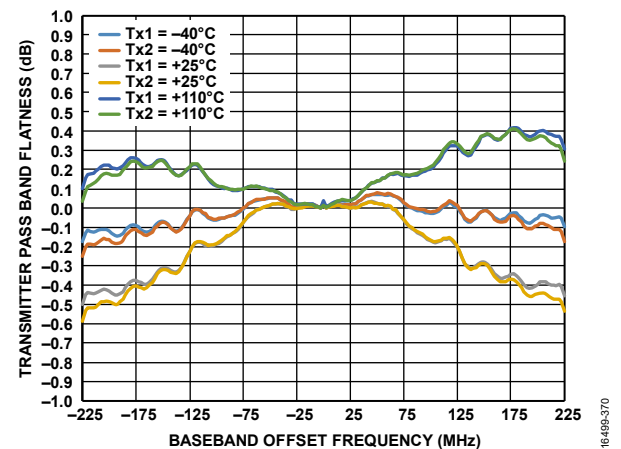


Figure 245. Transmitter Pass Band Flatness vs. Baseband Offset Frequency, Off Chip Match Response De-Embedded, LO = 4600 MHz

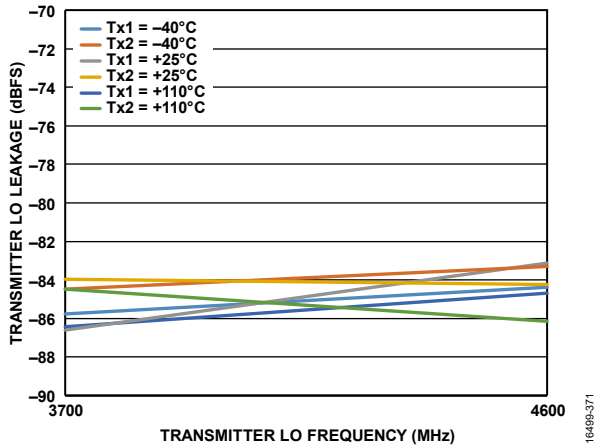


Figure 246. Transmitter LO Leakage vs. Transmitter LO Frequency, Transmitter Attenuation = 0 dB

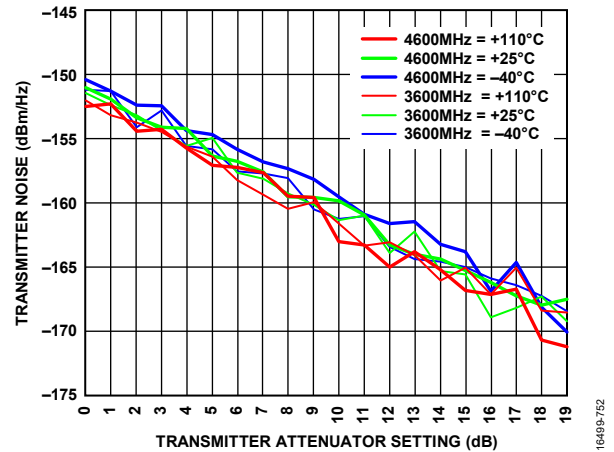


Figure 249. Transmitter Noise vs. Transmitter Attenuator Setting

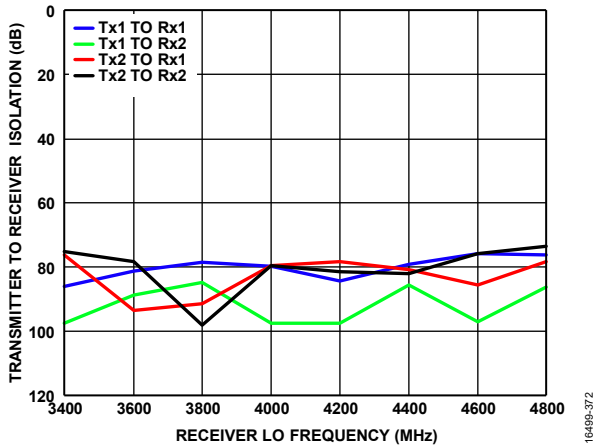


Figure 247. Transmitter to Receiver Isolation vs. Receiver LO Frequency, Temperature = -40°C, +25°C, and +110°C

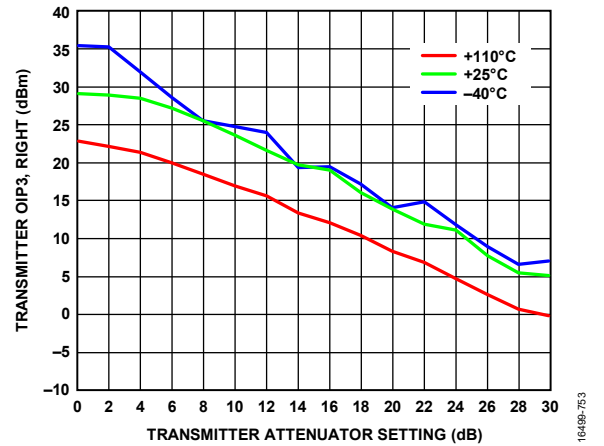


Figure 250. Transmitter OIP3, Right vs. Transmitter Attenuator Setting, LO = 3600 MHz, Total RMS Power = -12 dBFS

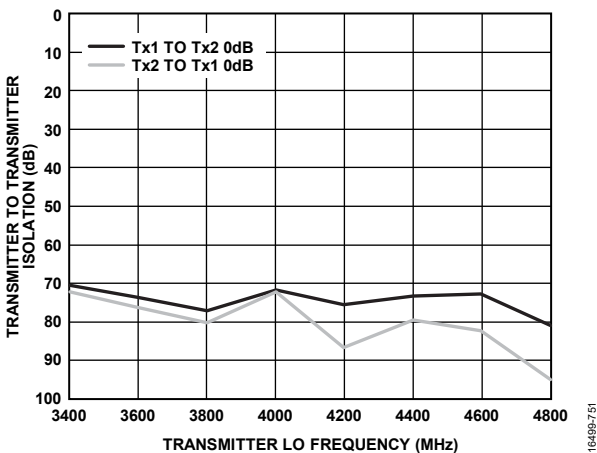


Figure 248. Transmitter to Transmitter Isolation vs. Transmitter LO Frequency, Temperature = 25°C

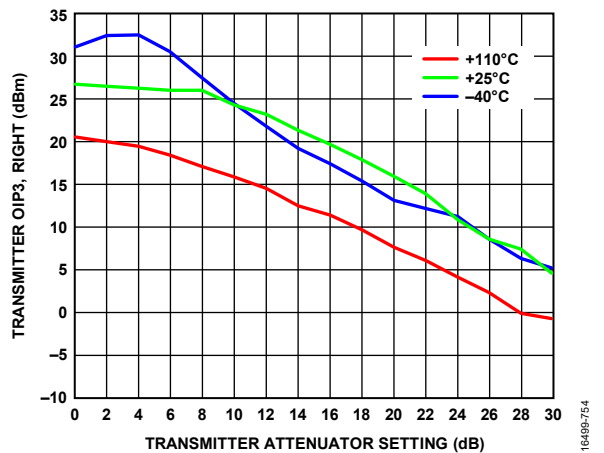


Figure 251. Transmitter OIP3, Right vs. Transmitter Attenuator Setting, LO = 4600 MHz, Total RMS Power = -12 dBFS



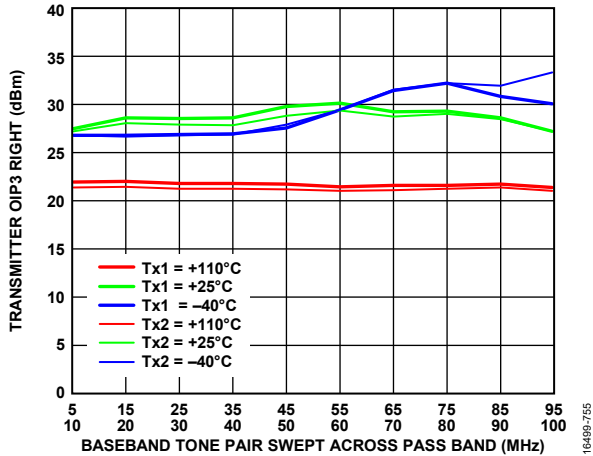


Figure 252. Transmitter OIP3 Right vs. Baseband Tone Pair Swept Across Pass Band, LO = 3600 MHz, Total RMS Power = -12 dBFS

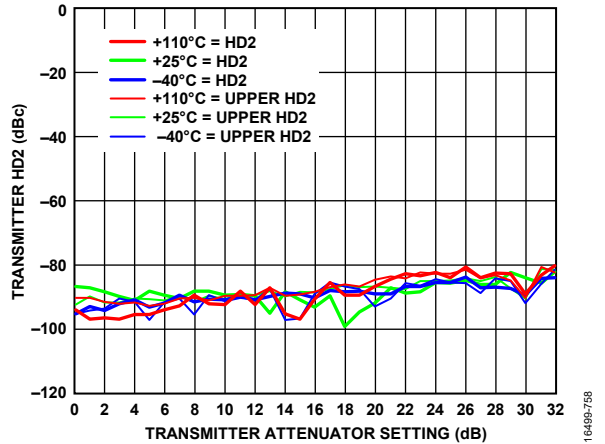


Figure 255. Transmitter HD2 vs. Transmitter Attenuator Setting, Baseband Frequency = 10 MHz, LO = 4600 MHz, CW = -15 dBFS

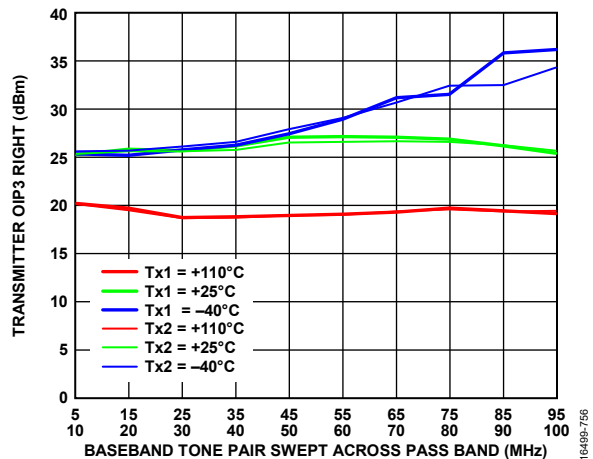


Figure 253. Transmitter OIP3 Right vs. Baseband Tone Pair Swept Across Pass Band, LO = 4600 MHz, Total RMS Power = -12 dBFS

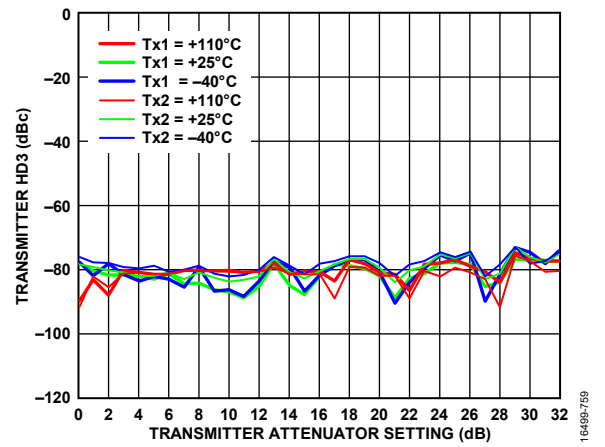


Figure 256. Transmitter HD3 vs. Transmitter Attenuator Setting, LO = 3600 MHz, CW = -15 dBFS, Baseband Frequency = 10 MHz

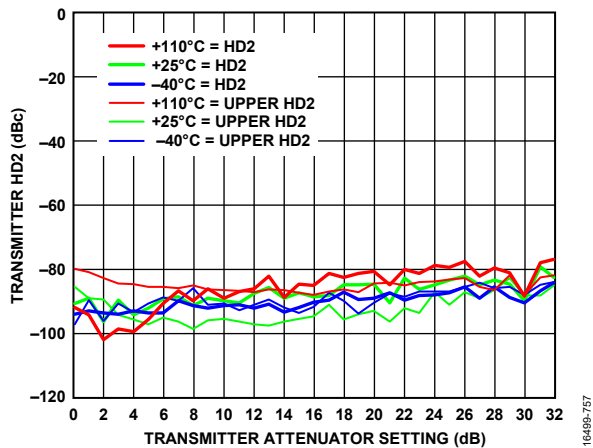


Figure 254. Transmitter HD2 vs. Transmitter Attenuator Setting, Baseband Frequency = 10 MHz, LO = 3600 MHz, CW = -15 dBFS

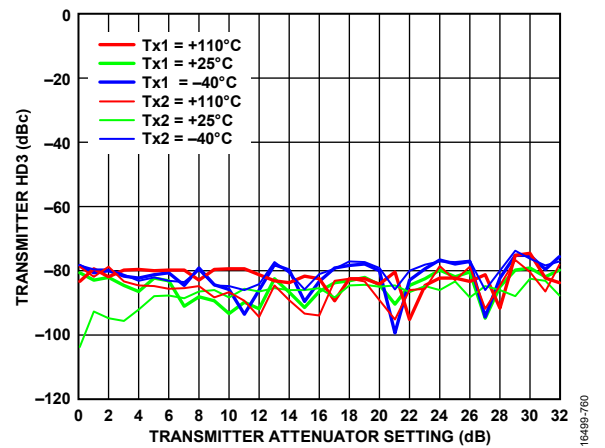


Figure 257. Transmitter HD3 vs. Transmitter Attenuator Setting, LO = 4600 MHz, CW = -15 dBFS, Baseband Frequency = 10 MHz

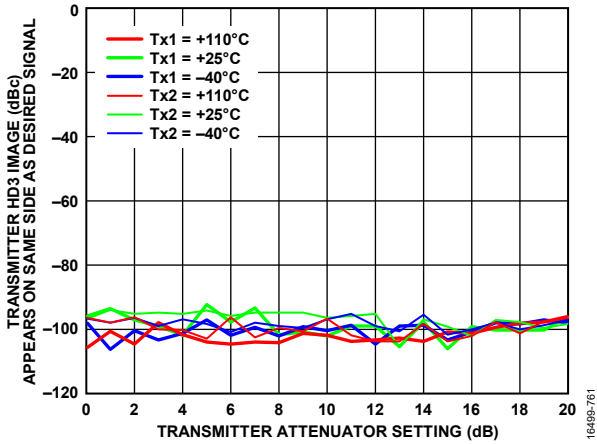


Figure 258. Transmitter HD3 Image Appears on Same Side as Desired Signal vs. Transmitter Attenuator Setting, LO = 3600 MHz, CW = -15 dBFS

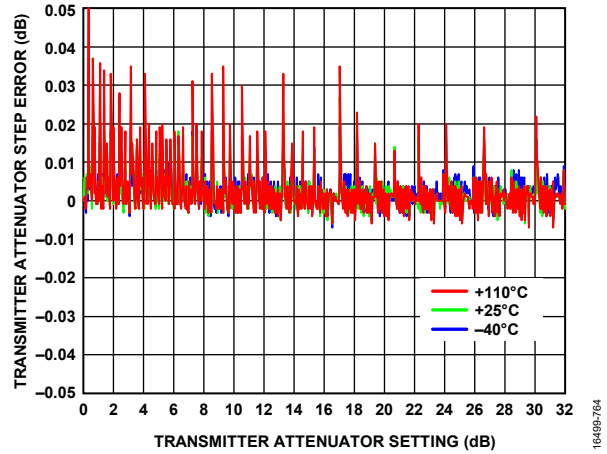


Figure 261. Transmitter Attenuator Step Error vs. Transmitter Attenuator Setting, LO = 4600 MHz

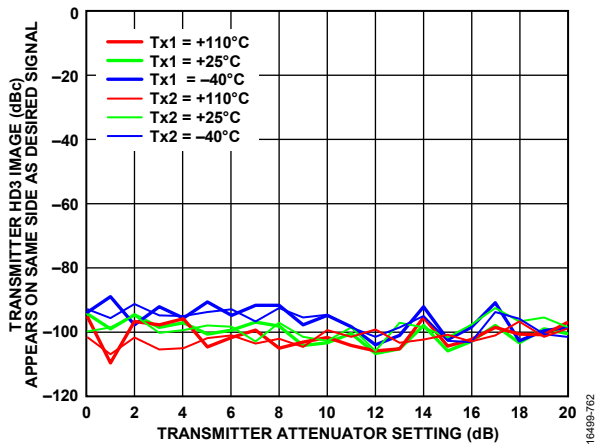


Figure 259. Transmitter HD3 Image Appears on Same Side as Desired Signal vs. Transmitter Attenuator Setting, LO = 4600 MHz, CW = -15 dBFS

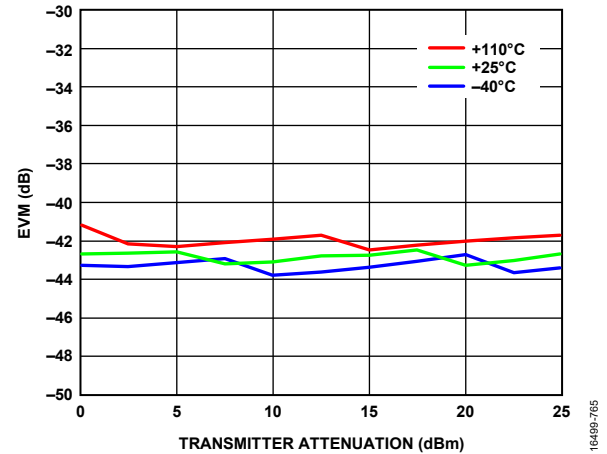


Figure 262. EVM vs. Transmitter Attenuation, LTE = 20 MHz Signal Centered on DC, LO = 3600 MHz

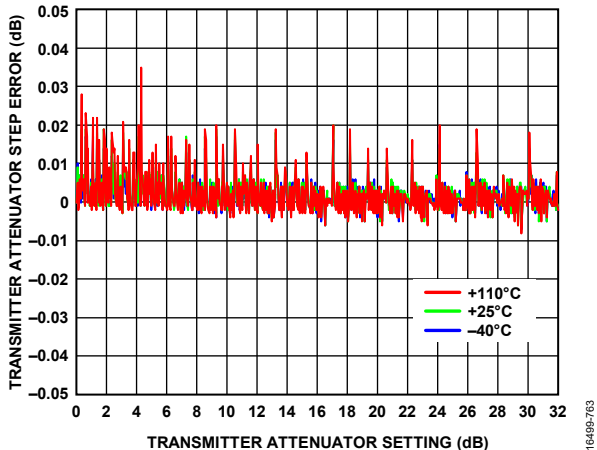


Figure 260. Transmitter Attenuator Step Error vs. Transmitter Attenuator Setting, LO = 3600 MHz

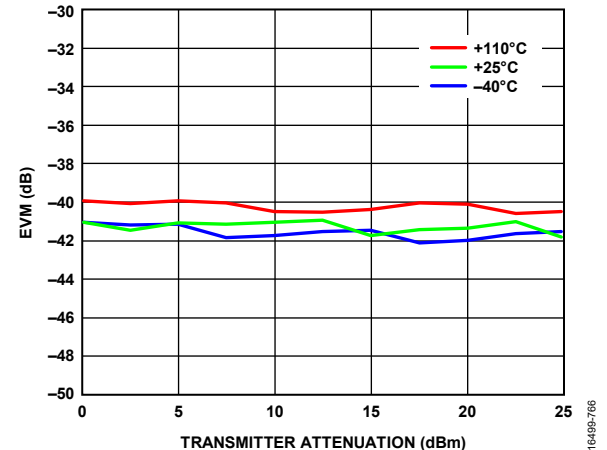


Figure 263. EVM vs. Transmitter Attenuation, LTE = 20 MHz Signal Centered on DC, LO = 4600 MHz

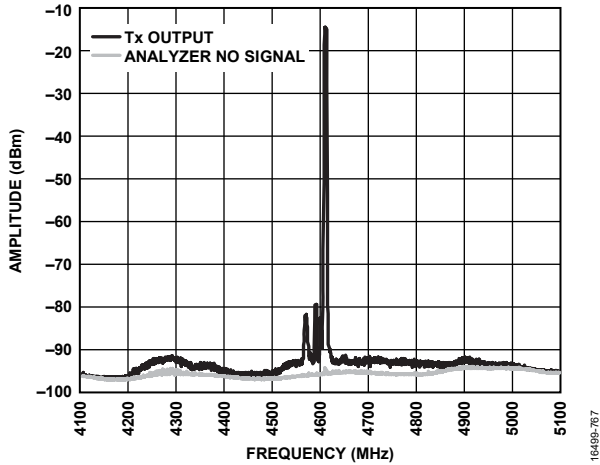


Figure 264. Amplitude vs. Frequency, Transmitter Output Spurious, Transmitter 1 = 4600 MHz, LTE = 5 MHz, Offset = 10 MHz, RMS Ripple in Noise Floor Due to Spectrum Analyzer = -12 dBFS, Temperature = 25°C

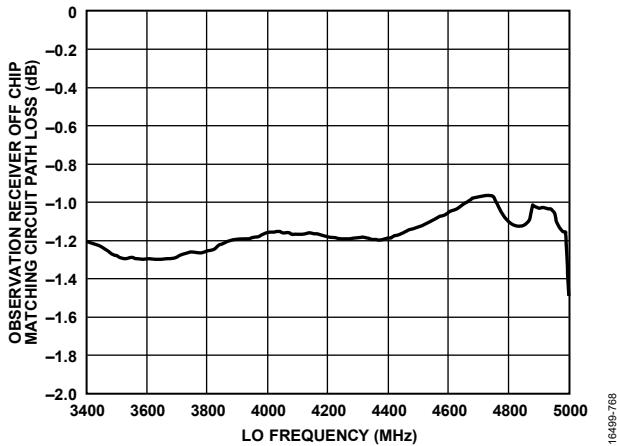


Figure 265. Observation Receiver Off Chip Matching Circuit Path Loss vs. LO Frequency, Simulation, Can be Used for De-Embedding Performance Data

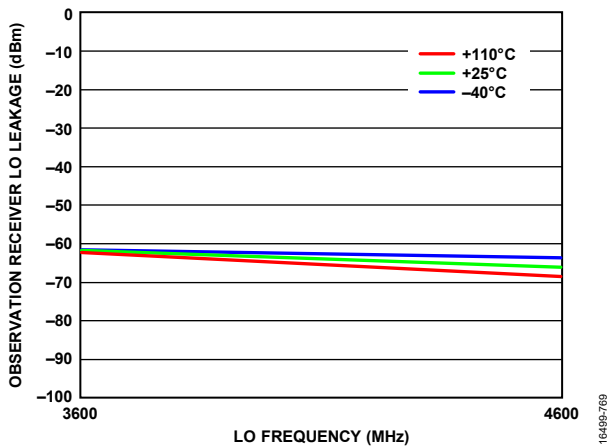


Figure 266. Observation Receiver LO Leakage vs. LO Frequency, from 3600 MHz to 4600 MHz

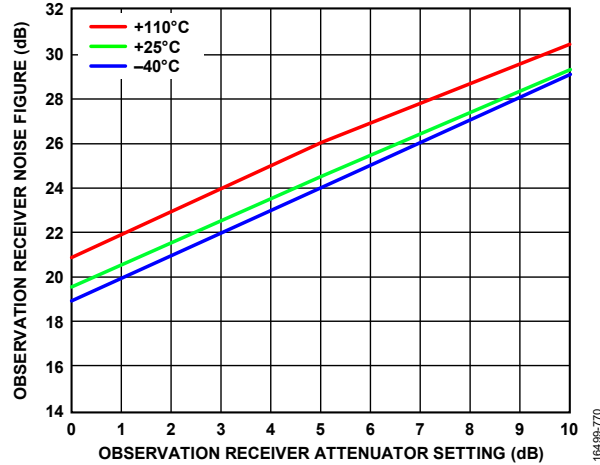


Figure 267. Observation Receiver Noise Figure vs. Observation Receiver Attenuator Setting, LO = 3600 MHz, Total Nyquist Integration Bandwidth

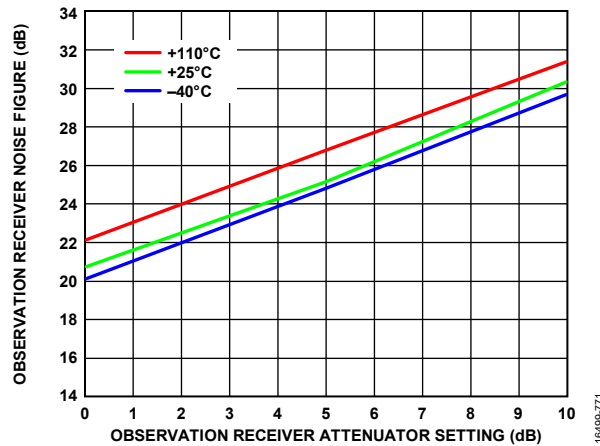


Figure 268. Observation Receiver Noise Figure vs. Observation Receiver Attenuator Setting, LO = 4600 MHz, Total Nyquist Integration Bandwidth

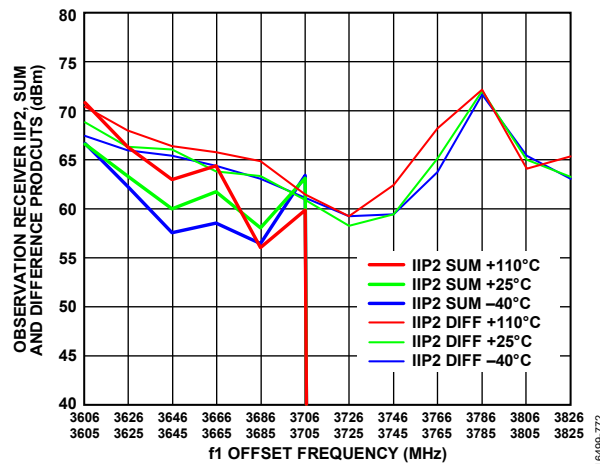


Figure 269. Observation Receiver IIP2, Sum and Difference Products vs. f1 Offset Frequency, Tones Separated by 1 MHz Swept Across Pass Band at -22 dBm Each, LO = 3600 MHz, Attenuation = 0 dB

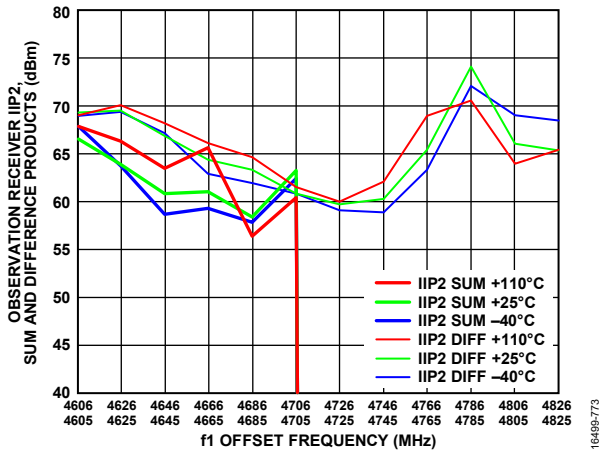


Figure 270. Observation Receiver IIP2, Sum and Difference Products vs. f1 Offset Frequency, Tones Separated by 1 MHz Swept Across Pass Band at -22 dBm Each, 4600 MHz, Attenuation = 0 dB

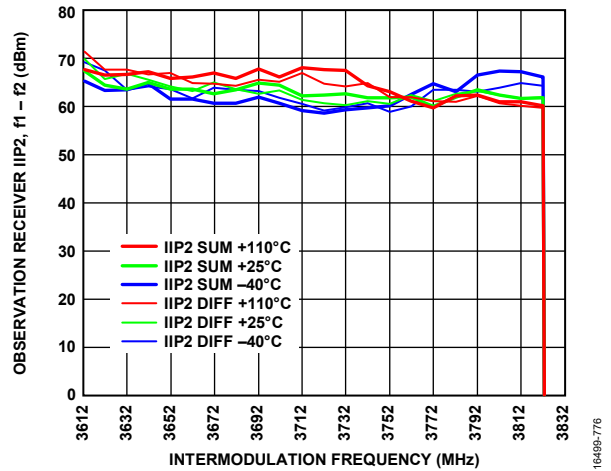


Figure 273. Observation Receiver IIP2, f1 - f2 vs. Intermodulation Frequency, LO = 3600 MHz, Tone 1 = 3602 MHz, Tone 2 Swept, -22 dBm Each, Attenuation = 0 dB

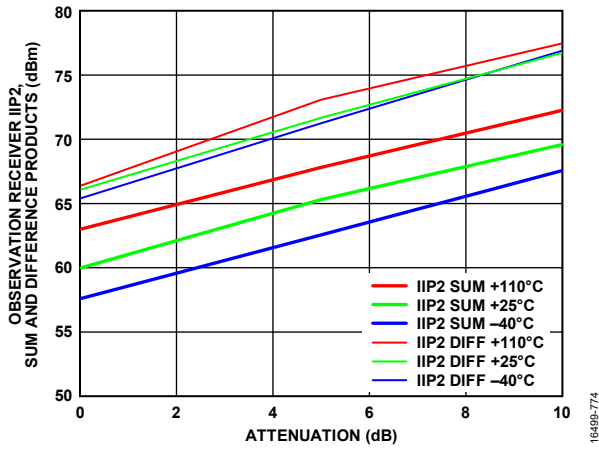


Figure 271. Observation Receiver IIP2, Sum and Difference Products vs. Attenuation, LO = 3600 MHz, Tone 1 = 3645 MHz, Tone 2 = 3646 MHz at -22 dBm Plus Attenuation

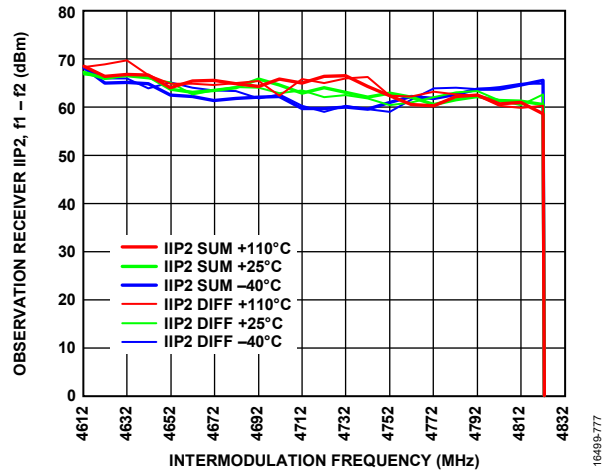


Figure 274. Observation Receiver IIP2, f1 - f2 vs. Intermodulation Frequency, LO = 4600 MHz, Tone 1 = 4602 MHz, Tone 2 Swept, -22 dBm Each, Attenuation = 0 dB

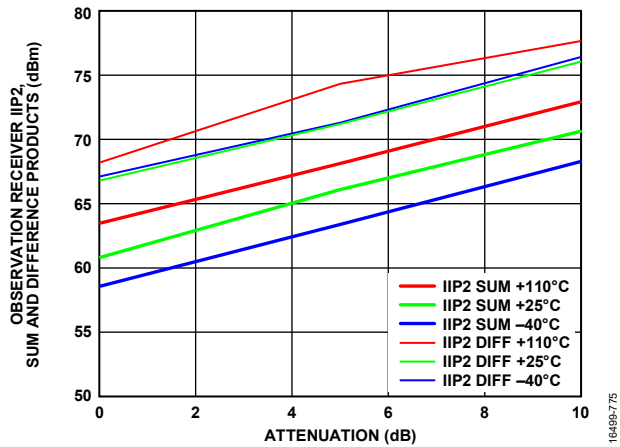


Figure 272. Observation Receiver IIP2, Sum and Difference Products vs. Attenuation, LO = 4600 MHz, Tone 1 = 4645 MHz, Tone 2 = 4646 MHz at -22 dBm Plus Attenuation

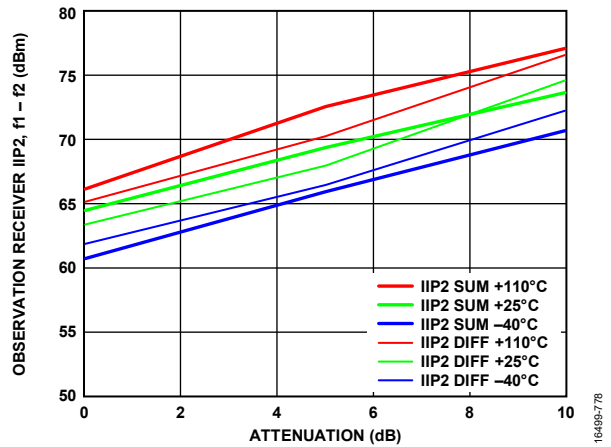


Figure 275. Observation Receiver IIP2, f1 - f2 vs. Attenuation, LO = 3600 MHz, Tone 1 = 3602 MHz, Tone 2 = 3702 MHz at -22 dBm Plus Attenuation

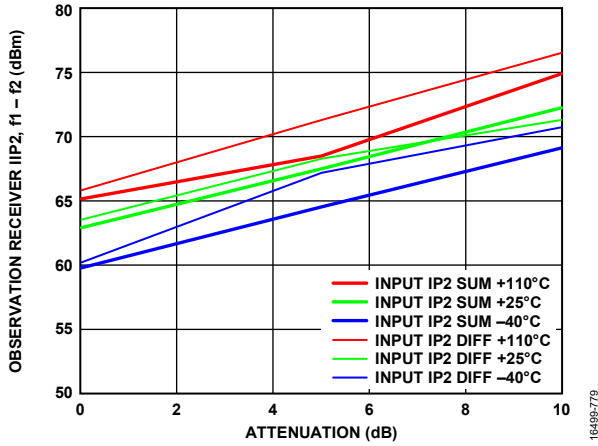


Figure 276. Observation Receiver IIP2,  $f_1 - f_2$  vs. Attenuation, LO = 4600 MHz, Tone 1 = 4602 MHz, Tone 2 = 4612 MHz at -22 dBm Plus Attenuation

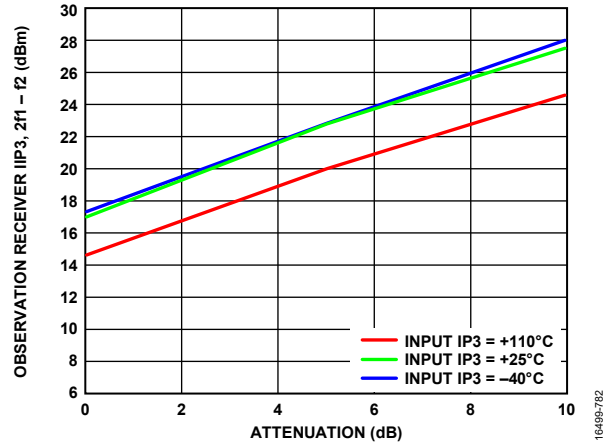


Figure 279. Observation Receiver IIP3,  $2f_1 - f_2$  vs. Attenuation, LO = 3600 MHz, Tone 1 = 3695 MHz, Tone 2 = 3696 MHz at -22 dBm Plus Attenuation

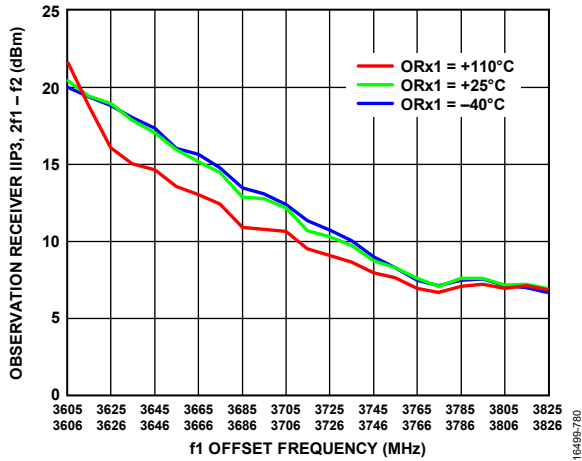


Figure 277. Observation Receiver IIP3,  $2f_1 - f_2$  vs.  $f_1$  Offset Frequency, LO = 3600 MHz, Attenuation = 0 dB, Tones Separated by 1 MHz Swept Across Pass Band at -22 dBm Each

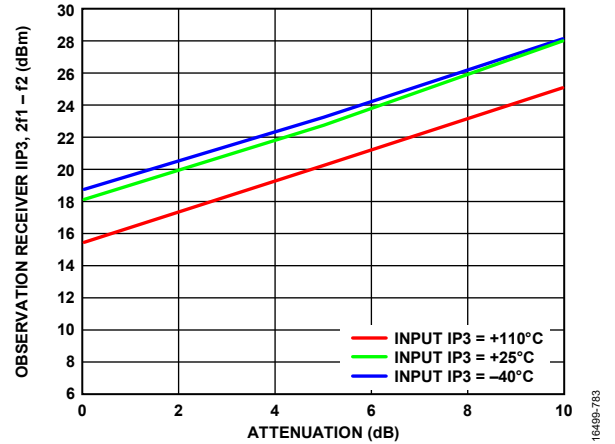


Figure 280. Observation Receiver IIP3,  $2f_1 - f_2$  vs. Attenuation, LO = 4600 MHz, Tone 1 = 4695 MHz, Tone 2 = 4696 MHz at -22 dBm Plus Attenuation

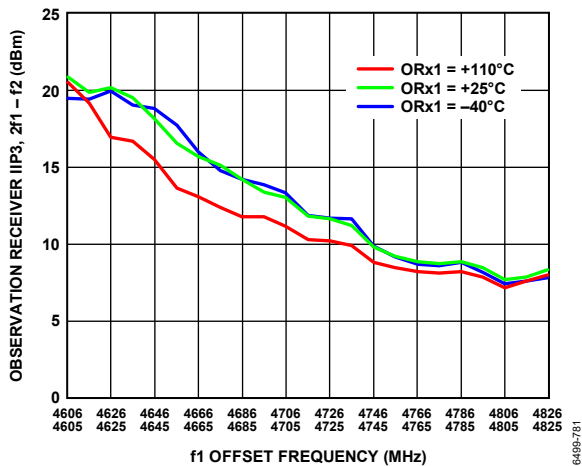


Figure 278. Observation Receiver IIP3,  $2f_1 - f_2$  vs.  $f_1$  Offset Frequency, LO = 4600 MHz, Attenuation = 0 dB, Tones Separated by 1 MHz Swept Across Pass Band at -22 dBm Each

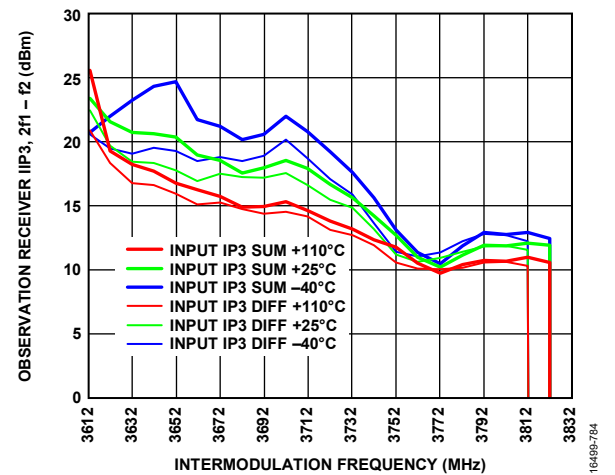


Figure 281. Observation Receiver IIP3,  $2f_1 - f_2$  vs. Intermodulation Frequency, LO = 3600 MHz, Tone 1 = 3602 MHz, Tone 2 = Swept, -22 dBm Each

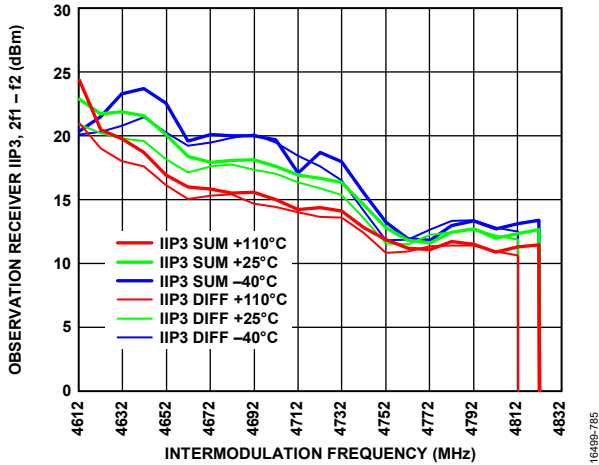


Figure 282. Observation Receiver IIP3, 2f1 - f2 vs. Intermodulation Frequency, LO = 4600 MHz, Tone 1 = 4602 MHz, Tone 2 = Swept, -22 dBm Each

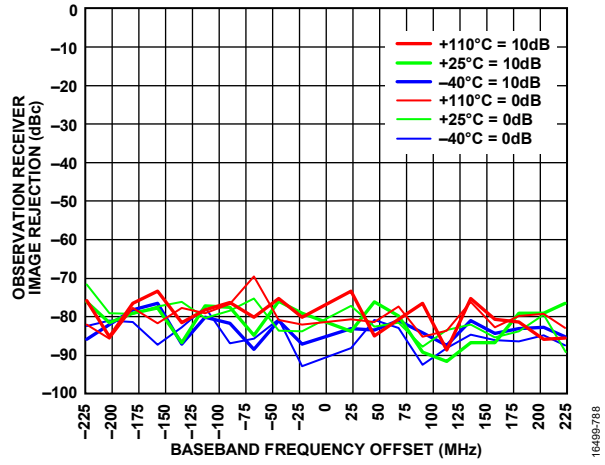


Figure 285. Observation Receiver Image Rejection vs. Baseband Frequency Offset, CW Signal Swept Across the Band, LO = 3600 MHz

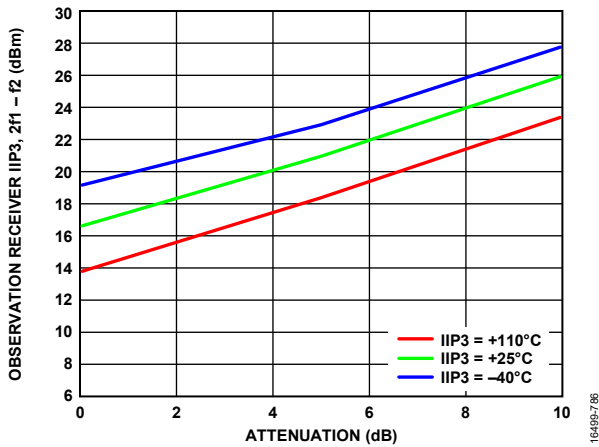


Figure 283. Observation Receiver IIP3, 2f1 - f2 vs. Attenuation, LO = 3600 MHz, Tone 1 = 3602 MHz, Tone 2 = 3722 MHz, -22 dBm Each Plus Attenuation

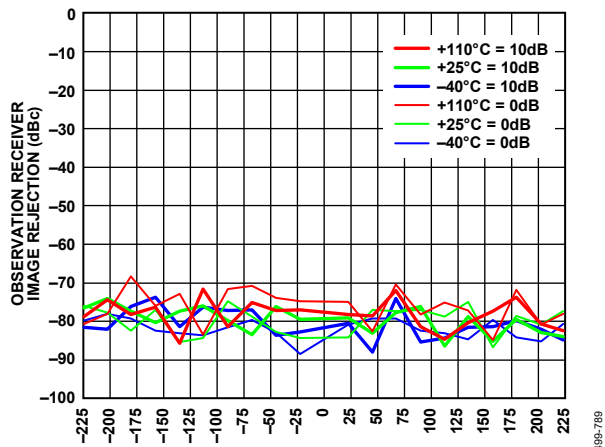


Figure 286. Observation Receiver Image Rejection vs. Baseband Frequency Offset, CW Signal Swept Across the Band, LO = 4600 MHz

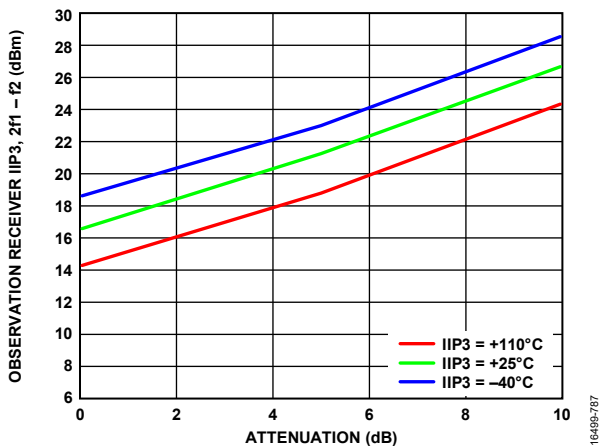


Figure 284. Observation Receiver IIP3, 2f1 - f2 vs. Attenuation, LO = 4600 MHz, Tone 1 = 4602 MHz, Tone 2 = 4722 MHz at -22 dBm Plus Attenuation Each

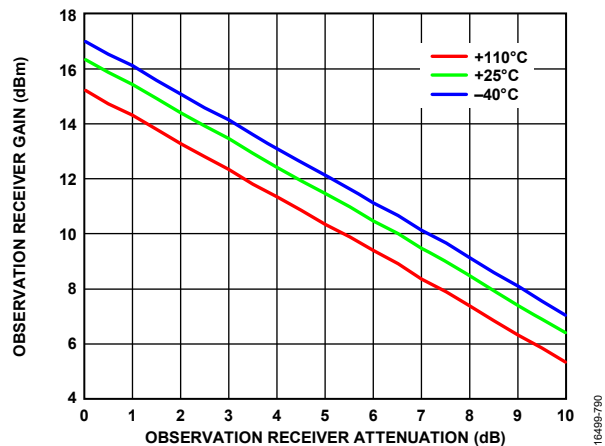


Figure 287. Observation Receiver Gain vs. Observation Receiver Attenuation, LO = 3600 MHz

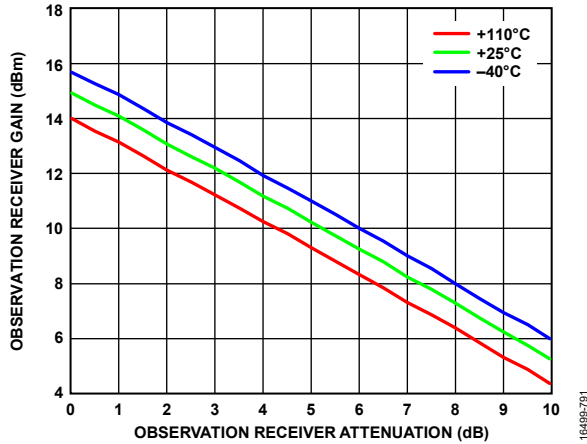


Figure 288. Observation Receiver Gain vs. Observation Receiver Attenuation, LO = 4600 MHz

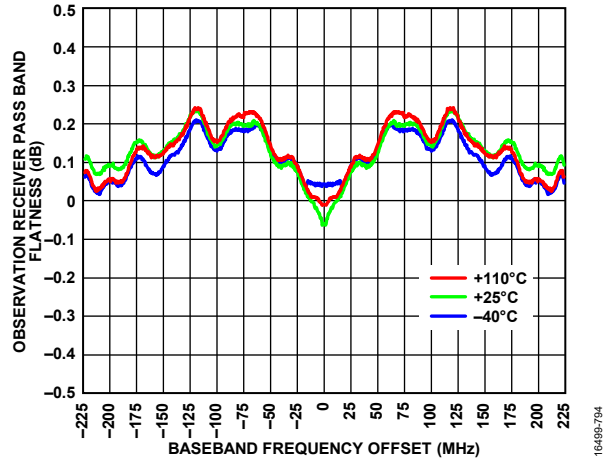


Figure 291. Observation Receiver Pass Band Flatness vs. Baseband Frequency Offset, LO = 3600 MHz

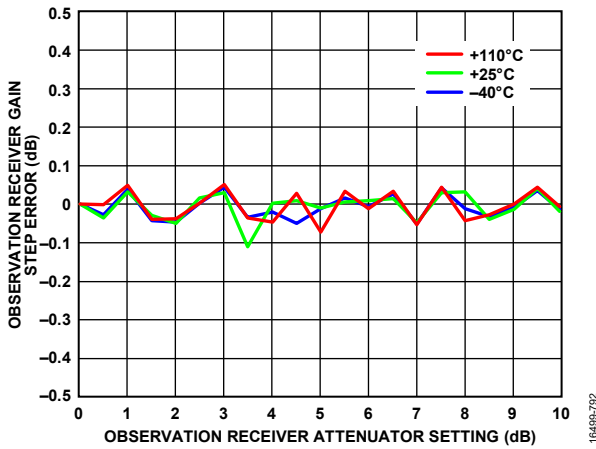


Figure 289. Observation Receiver Gain Step Error vs. Observation Receiver Attenuator Setting, LO = 3600 MHz

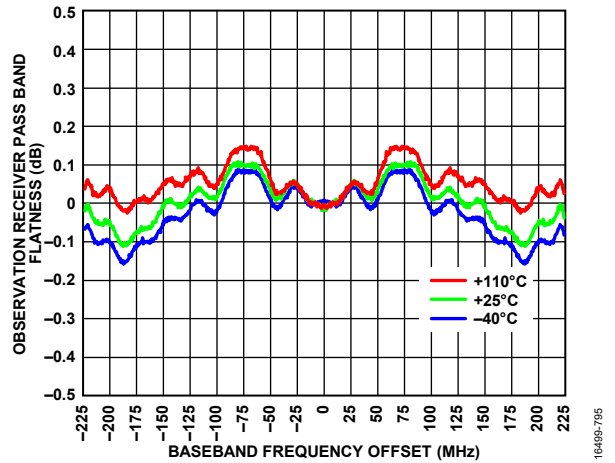


Figure 292. Observation Receiver Pass Band Flatness vs. Baseband Frequency Offset, LO = 4600 MHz

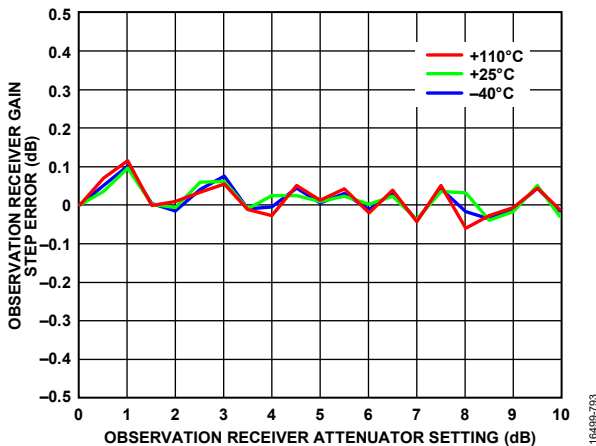


Figure 290. Observation Receiver Gain Step Error vs. Observation Receiver Attenuator Setting, LO = 4600 MHz

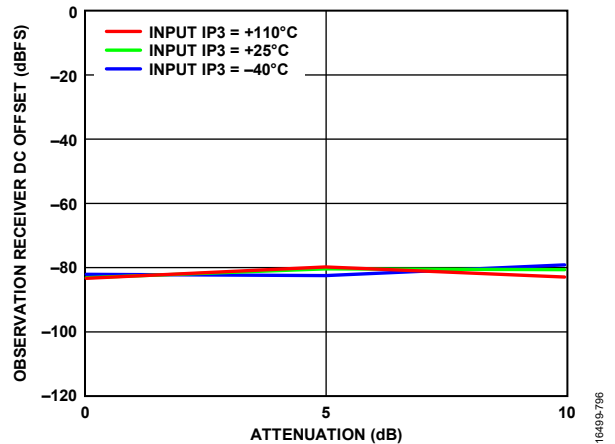


Figure 293. Observation Receiver DC Offset vs. Attenuation, LO = 3600 MHz

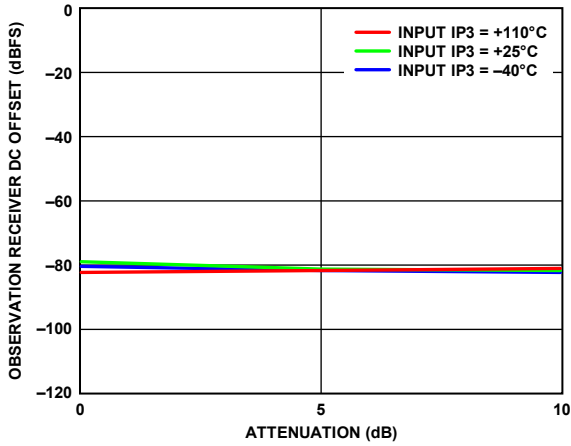


Figure 294. Observation Receiver DC Offset vs. Attenuation, LO = 4600 MHz

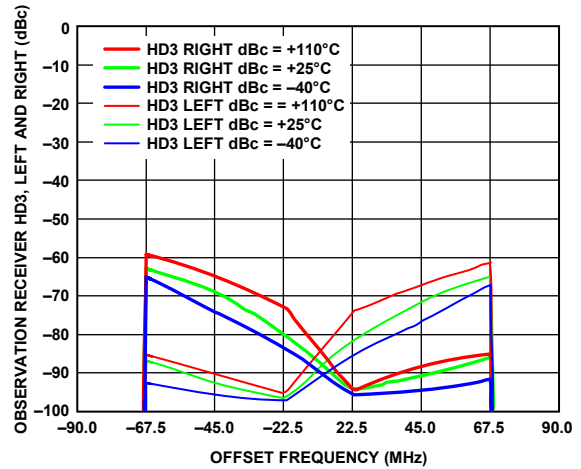


Figure 297. Observation Receiver HD3, Left and Right vs. Offset Frequency, LO = 3600 MHz, Tone Level = -20 dBm

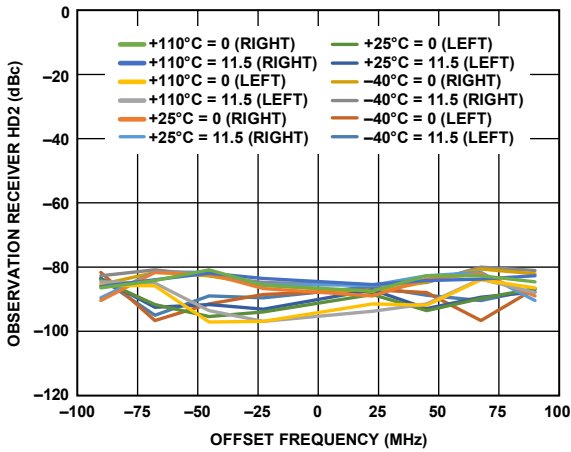


Figure 295. Observation Receiver HD2 vs. Offset Frequency, LO = 3600 MHz, Tone Level = -20 dBm Plus Attenuation

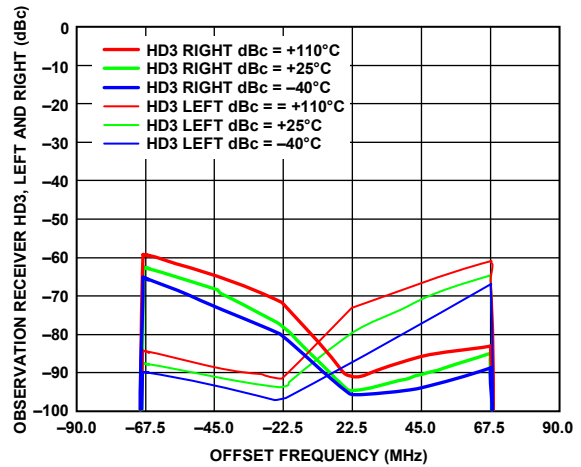


Figure 298. Observation Receiver HD3, Left and Right vs. Offset Frequency, LO = 4600 MHz, Tone Level = -20 dBm

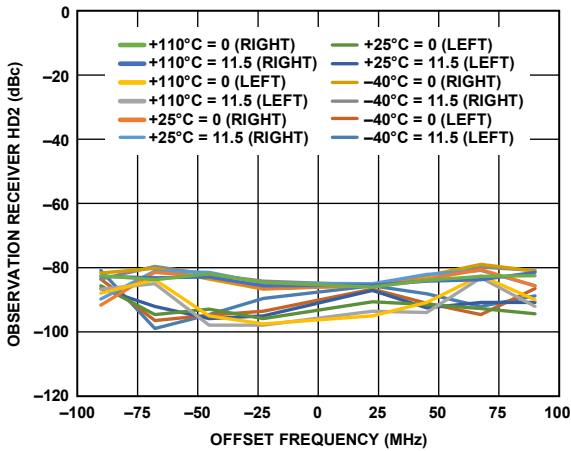


Figure 296. Observation Receiver HD2 vs. Offset Frequency, LO = 4600 MHz, Tone Level = -20 dBm Plus Attenuation

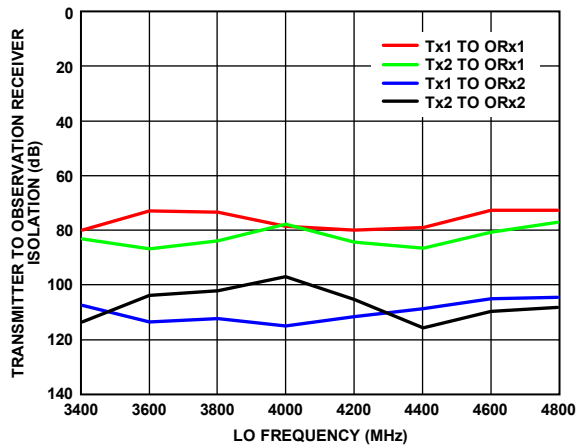


Figure 299. Transmitter to Observation Receiver Isolation vs. LO Frequency, Temperature = 25°C



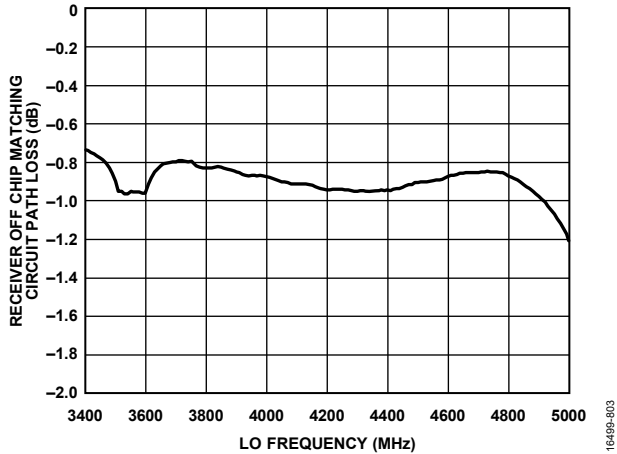


Figure 300. Receiver Off Chip Matching Circuit Path Loss vs. LO Frequency, (Simulation), Can Be Used for De-Embedding Performance Data

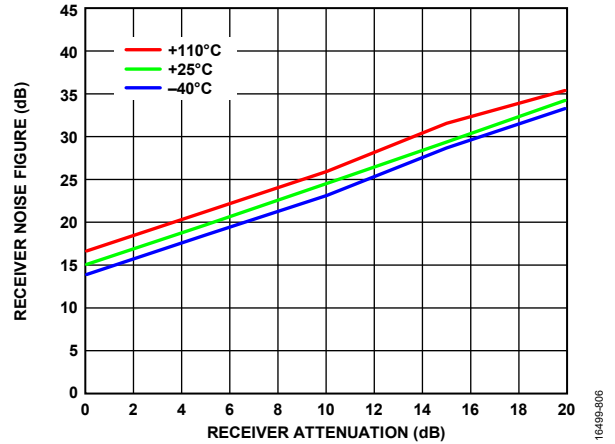


Figure 303. Receiver Noise Figure vs. Receiver Attenuation, LO = 4600 MHz, Bandwidth = 200 MHz, Sample Rate = 245.76 MSPS, Integration Bandwidth = 500 kHz to 100 MHz

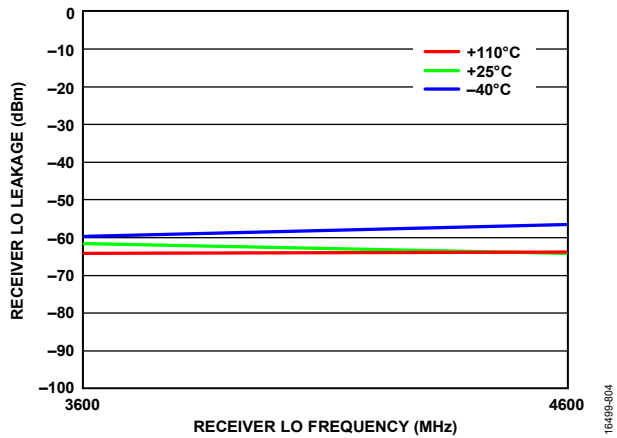


Figure 301. Receiver LO Leakage vs. Receiver LO Frequency, Receiver Attenuation = 0 dB, RF Bandwidth = 200 MHz, Sample Rate = 245.76 MSPS

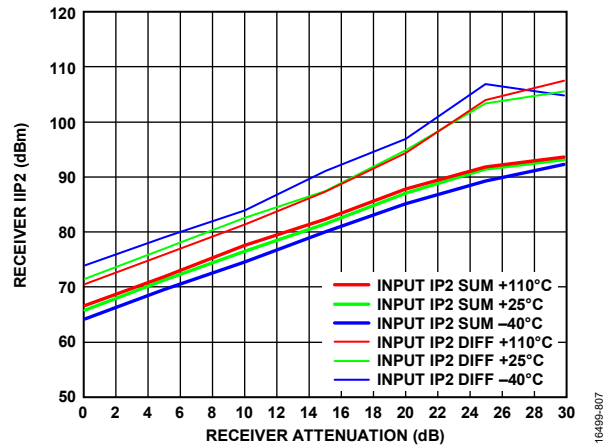


Figure 304. Receiver IIP2 vs. Receiver Attenuation, LO = 3600 MHz, Tones Placed at 3645 MHz and 3646 MHz, -21 dBm Plus Attenuation

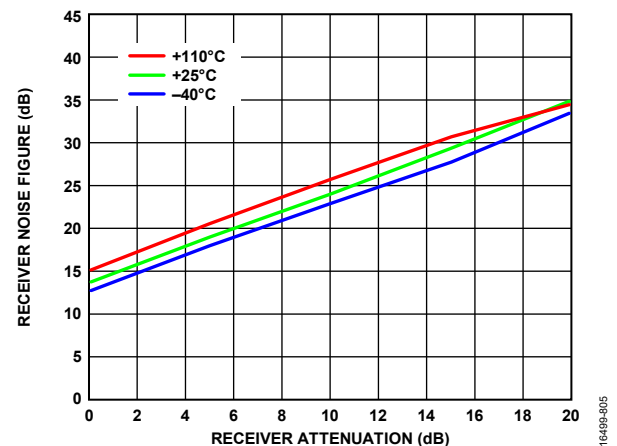


Figure 302. Receiver Noise Figure vs. Receiver Attenuation, LO = 3600 MHz, Receiver Bandwidth = 200 MHz, Sample Rate = 245.76 MSPS, Integration Bandwidth = 500 kHz to 100 MHz

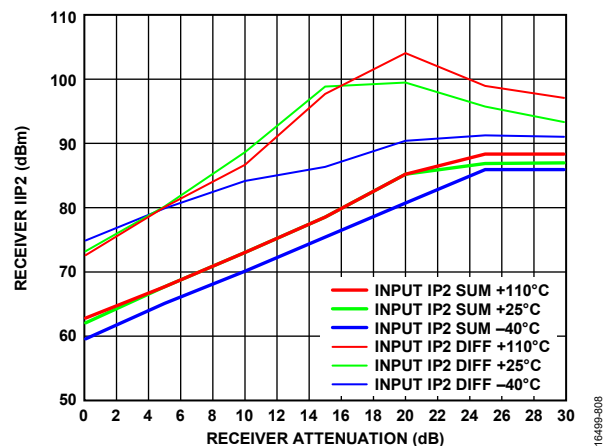


Figure 305. Receiver IIP2 vs. Receiver Attenuation, LO = 4600 MHz, Tones Placed at 4645 MHz and 4646 MHz, -21 dBm Plus Attenuation

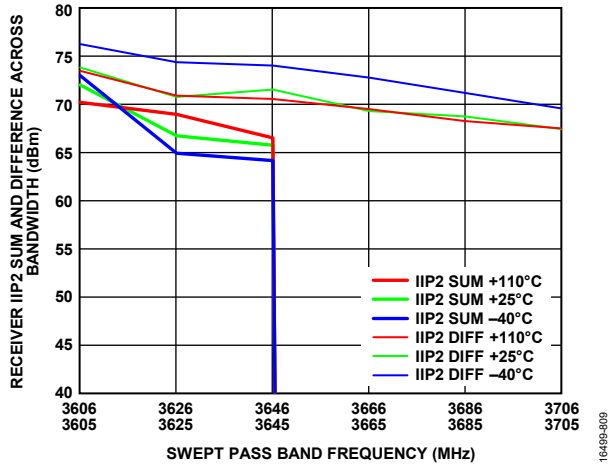


Figure 306. Receiver IIP2 Sum and Difference Across Bandwidth vs. Swept Pass Band Frequency, Receiver Attenuation = 0 dB, LO = 3600 MHz, Six Tone Pairs, -21 dBm Each Plus Attenuation

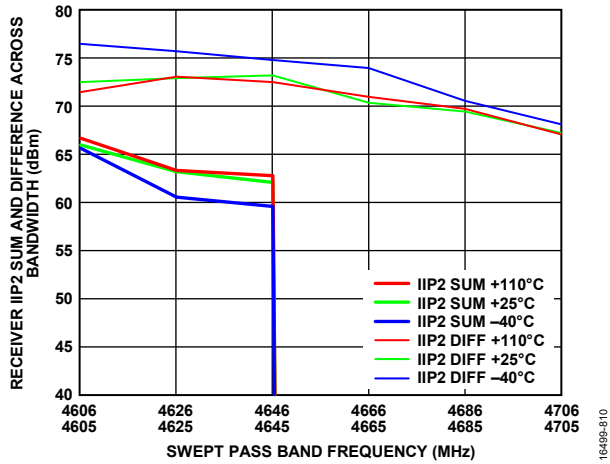


Figure 307. Receiver IIP2 Sum and Difference Across Bandwidth vs. Swept Pass Band Frequency, Receiver Attenuation = 0 dB, LO = 4600 MHz, Six Tone Pairs, -21 dBm Each

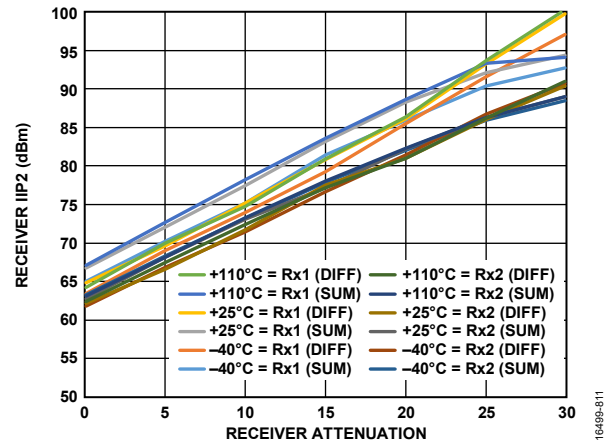


Figure 308. Receiver IIP2 vs. Receiver Attenuation, LO = 3600 MHz, Tones Placed at 3602 MHz and 3692 MHz, -21 dBm Plus Attenuation

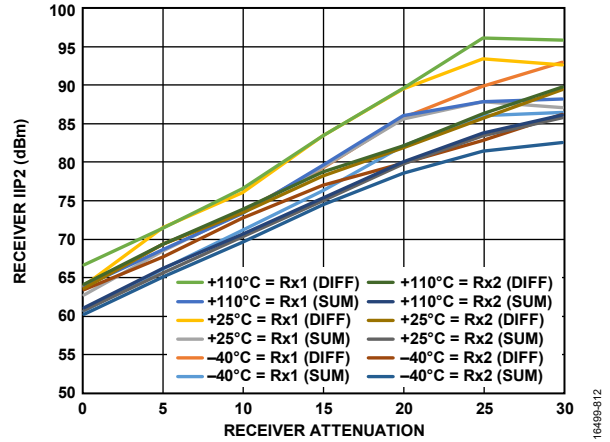


Figure 309. Receiver IIP2 vs. Receiver Attenuation, LO = 4600 MHz, Tones Placed at 4602 MHz and 4692 MHz, -21 dBm Plus Attenuation

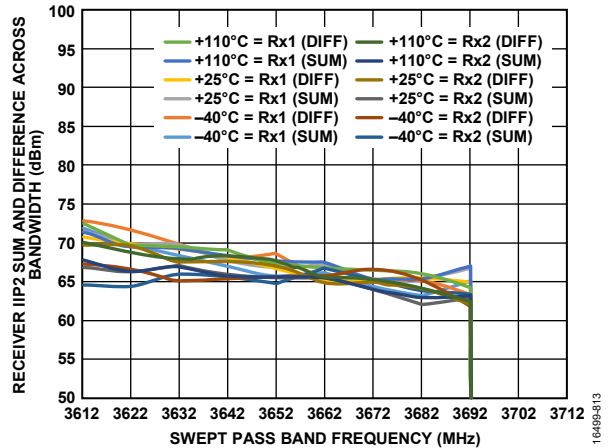


Figure 310. Receiver IIP2 Sum and Difference Across Bandwidth vs. Swept Pass Band Frequency, Receiver Attenuation = 0 dB, LO = 3600 MHz, Tone 1 = 3602 MHz, Tone 2 = Swept, -21 dBm Each

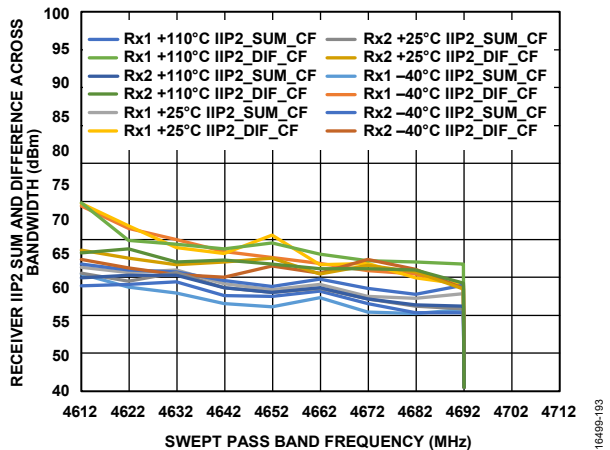


Figure 311. Receiver IIP2 Sum and Difference Across Bandwidth vs. Swept Pass Band Frequency, Receiver Attenuation = 0 dB, LO = 4600 MHz, Tone 1 = 4602 MHz, Tone 2 = Swept, -21 dBm Each

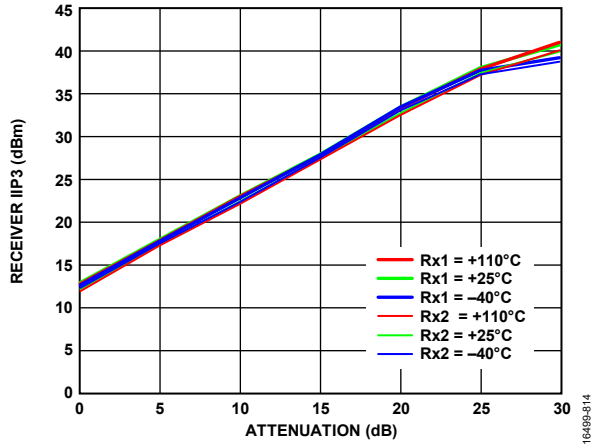


Figure 312. Receiver IIP3 vs. Attenuation, LO = 3600 MHz, Tone 1 = 3695 MHz, Tone 2 = 3696 MHz, -21 dBm Plus Attenuation

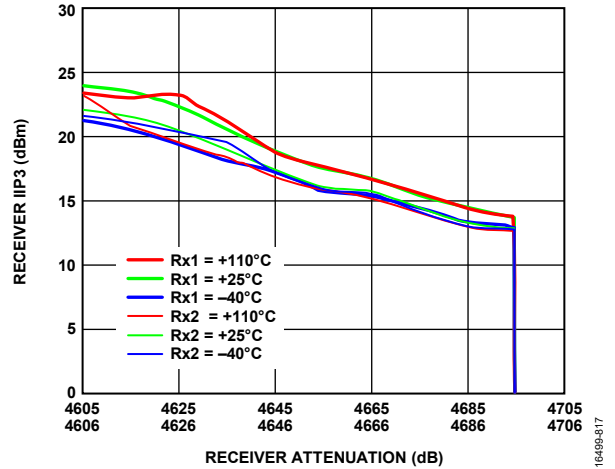


Figure 315. Receiver IIP3 vs. Receiver Attenuation, Receiver Attenuation = 0 dB, LO = 4600 MHz, Tone 2 = Tone 1 + 1 MHz, -21 dBm Each, Swept Across Pass Band

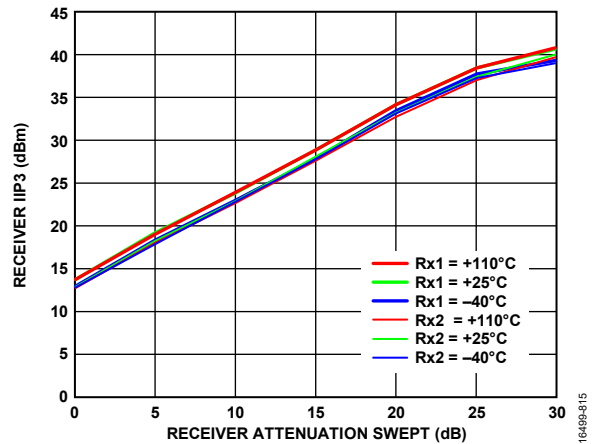


Figure 313. Receiver IIP3 vs. Receiver Attenuation Swept, LO = 4600 MHz, Tone 1 = 4695 MHz, Tone 2 = 4696 MHz, -21 dBm Plus Attenuation

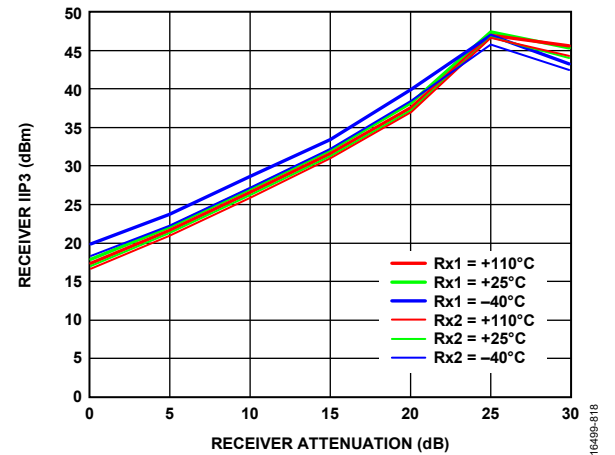


Figure 316. Receiver IIP3 vs. Receiver Attenuation, LO = 3600 MHz, Tone 1 = 3602 MHz, Tone 2 = 3692 MHz, -21 dBm Plus Attenuation

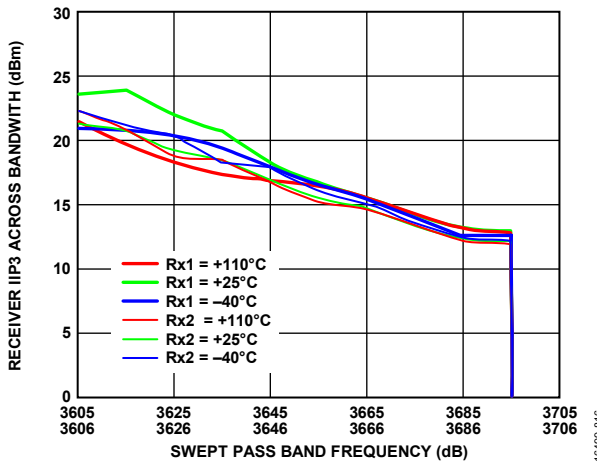


Figure 314. Receiver IIP3 Across Bandwidth vs. Swept Pass Band Frequency, Receiver Attenuation = 0 dB, LO = 3600 MHz, Tone 2 = Tone 1 + 1 MHz, -21 dBm Each, Swept Across Pass Band

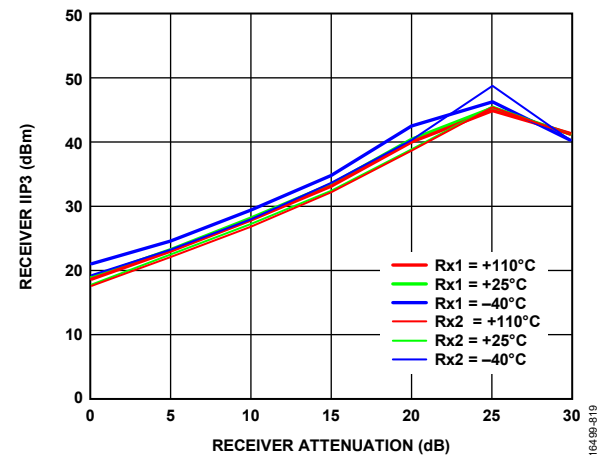


Figure 317. Receiver IIP3 vs. Receiver Attenuation, LO = 4600 MHz, Tone 1 = 4602 MHz, Tone 2 = 4692 MHz, -21 dBm Plus Attenuation

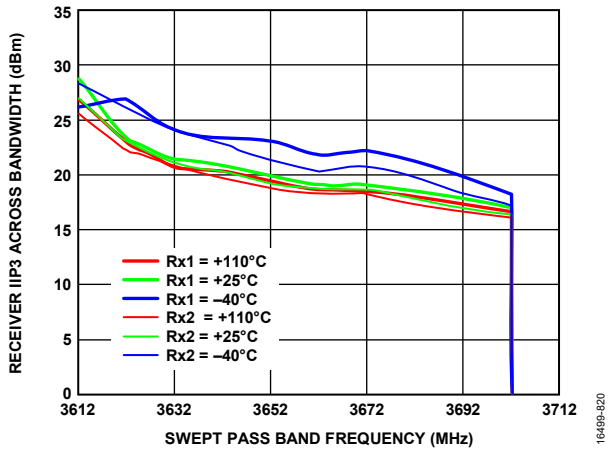


Figure 318. Receiver IIP3 Across Bandwidth vs. Swept Pass Band Frequency, Receiver Attenuation = 0 dB, LO = 3600 MHz, Tone 1 = 3602 MHz, Tone 2 = Swept Across Pass Band, -21 dBm Each

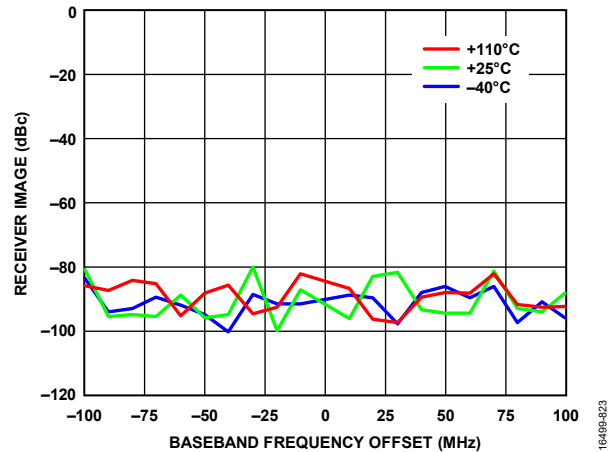


Figure 321. Receiver Image vs. Baseband Frequency Offset, Attenuation = 0 dB, RF Bandwidth = 200 MHz, Tracking Calibration Active, Sample Rate = 245.76 MSPS, LO = 4600 MHz

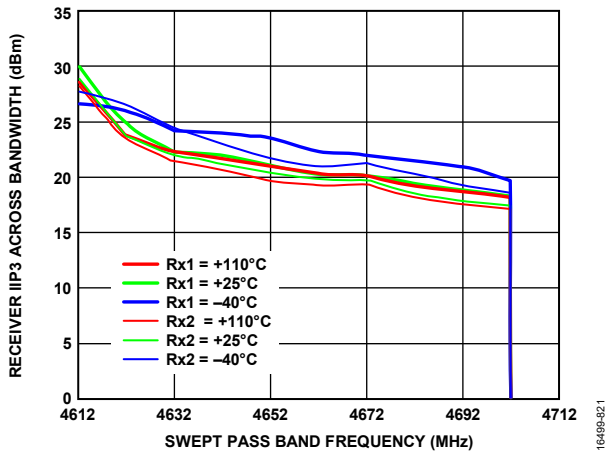


Figure 319. Receiver IIP3 Across Bandwidth vs. Swept Pass Band Frequency, Receiver Attenuation = 0 dB, LO = 4600 MHz, Tone 1 = 4602 MHz, Tone 2 = Swept Across Pass Band, -21 dBm Each

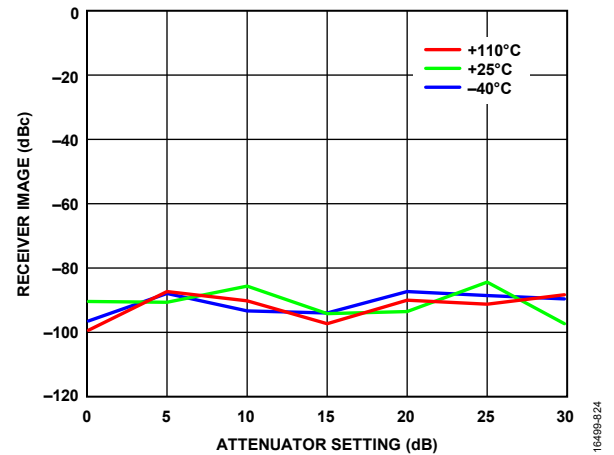


Figure 322. Receiver Image vs. Attenuator Setting, RF Bandwidth = 200 MHz, Tracking Calibration Active, Sample Rate = 245.76 MSPS, LO = 3600 MHz, Baseband Frequency = 10 MHz

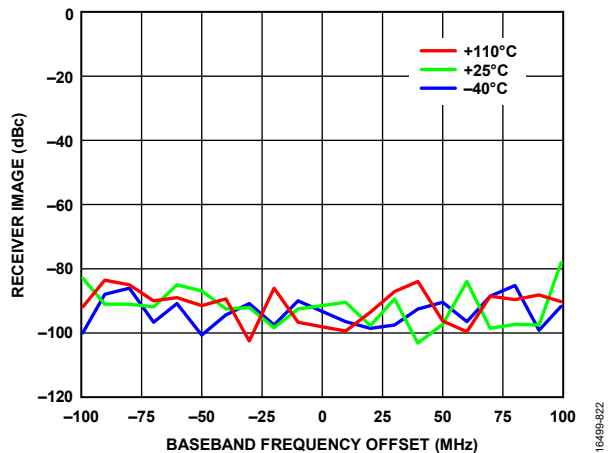


Figure 320. Receiver Image vs. Baseband Frequency Offset, Attenuation = 0 dB, RF Bandwidth = 200 MHz, Tracking Calibration Active, Sample Rate = 245.76 MSPS, LO = 3600 MHz

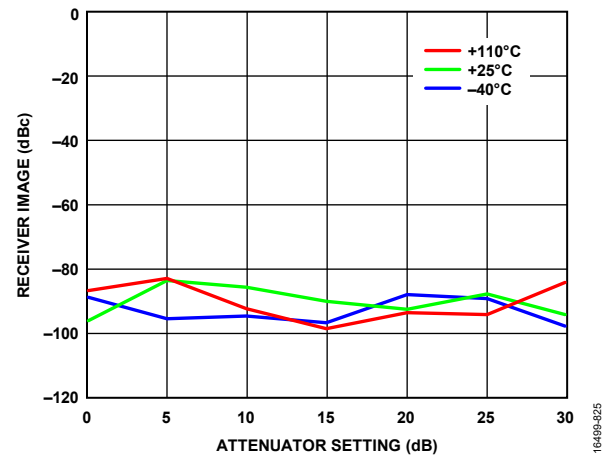


Figure 323. Receiver Image vs. Attenuator Setting, RF Bandwidth = 200 MHz, Tracking Calibration Active, Sample Rate = 245.76 MSPS, LO = 4600 MHz, Baseband Frequency = 10 MHz

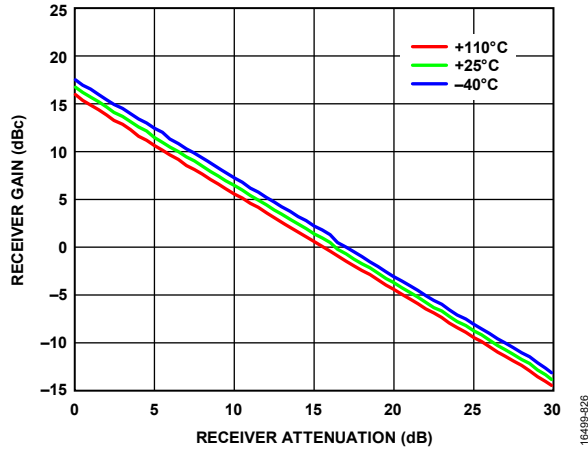


Figure 324. Receiver Gain vs. Receiver Attenuation, RF Bandwidth = 20 MHz, Sample Rate = 245.76 MSPS, LO = 3600 MHz

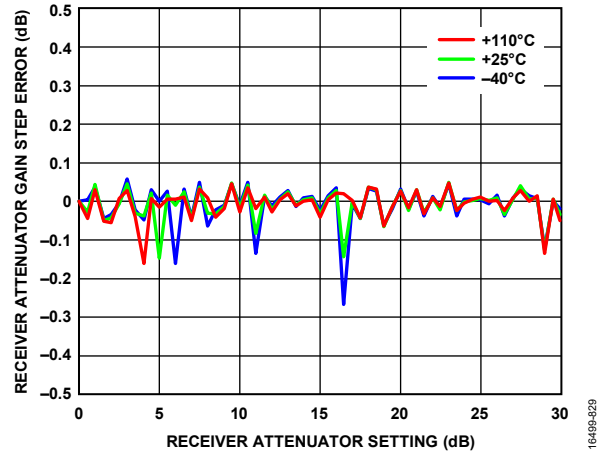


Figure 327. Receiver Attenuator Gain Step Error vs. Receiver Attenuator Setting, LO = 3600 MHz

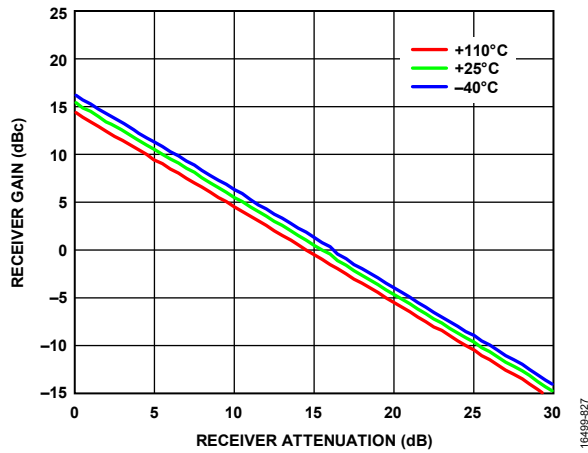


Figure 325. Receiver Gain vs. Receiver Attenuation, RF Bandwidth = 20 MHz, Sample Rate = 245.76 MSPS, LO = 4600 MHz

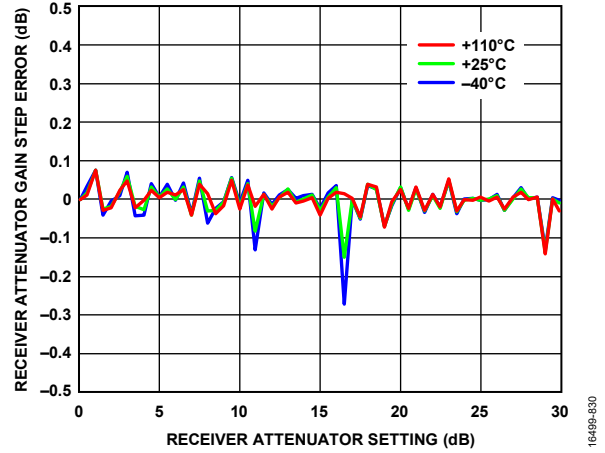


Figure 328. Receiver Attenuator Gain Step Error vs. Receiver Attenuator Setting, LO = 4600 MHz

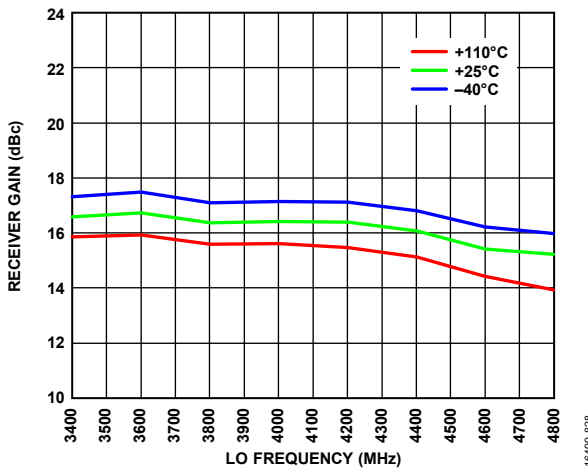


Figure 326. Receiver Gain vs. LO Frequency, RF Bandwidth = 200 MHz, Sample Rate = 245.76 MSPS

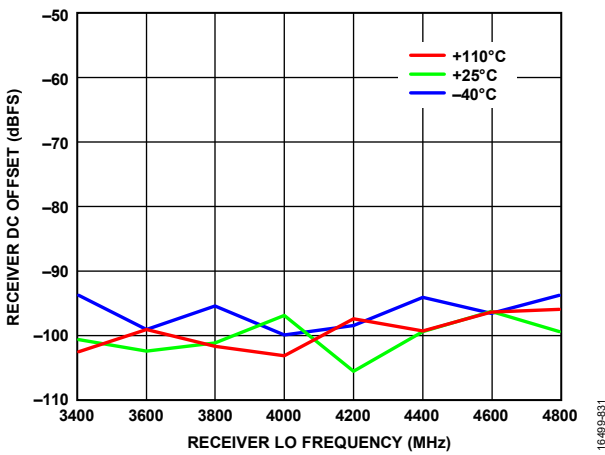


Figure 329. Receiver DC Offset vs. Receiver LO Frequency

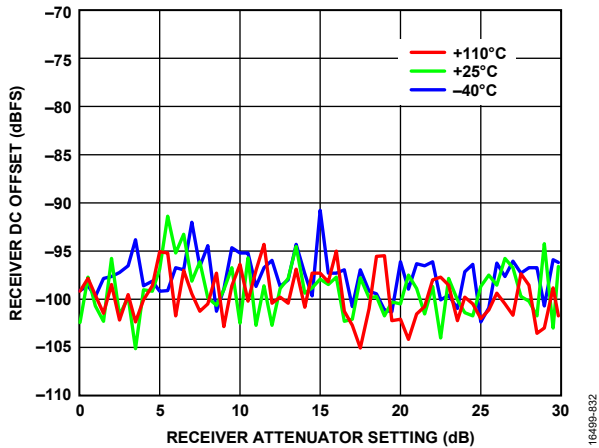


Figure 330. Receiver DC Offset vs. Receiver Attenuator Setting, LO = 3600 MHz

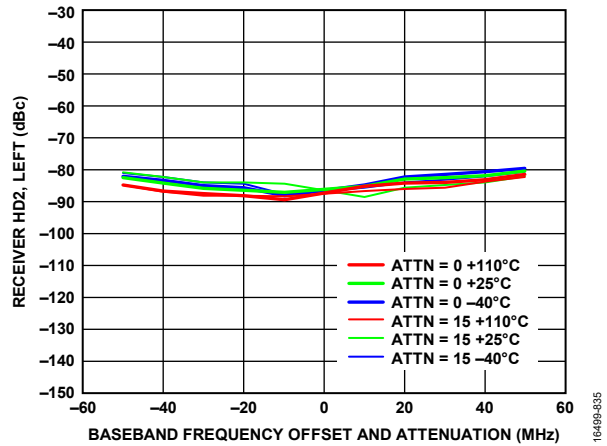


Figure 333. Receiver HD2, Left vs. Baseband Frequency Offset and Attenuation, Tone Level = -15 dBm at Attenuation = 0, X-Axis = Baseband Frequency Offset of the Fundamental Tone, Not the Frequency of the HD2 Product (HD2 Product = 2 x the Baseband Frequency), HD2 Canceller Disabled, LO = 4600 MHz

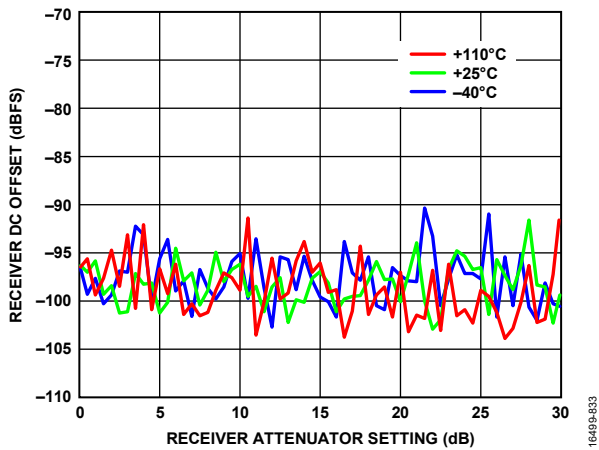


Figure 331. Receiver DC Offset vs. Receiver Attenuator Setting, LO = 4600 MHz

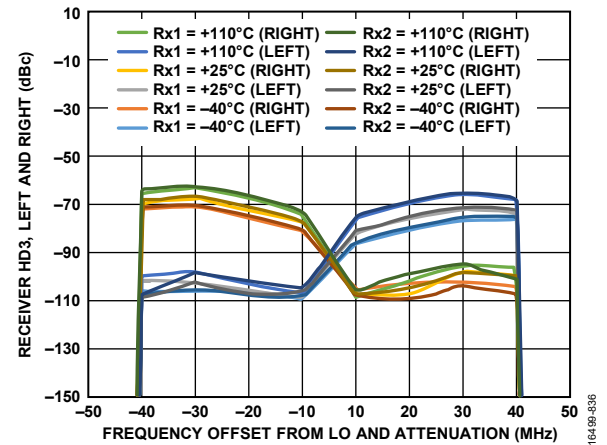


Figure 334. Receiver HD3, Left and Right vs. Frequency Offset from LO and Attenuation, Tone Level = -15 dBm at Attenuation = 0 dB, LO = 3600 MHz

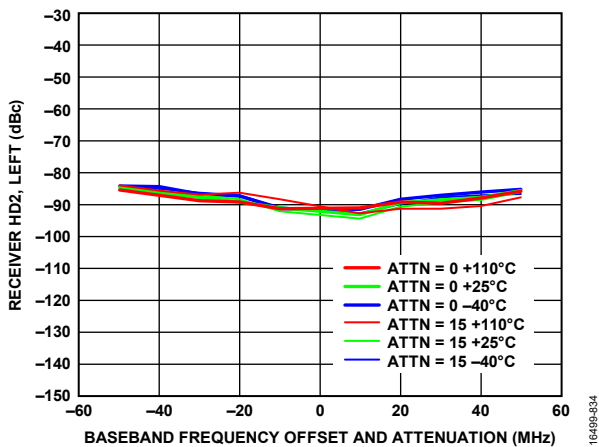


Figure 332. Receiver HD2, Left vs. Baseband Frequency Offset and Attenuation, Tone Level = -15 dBm at Attenuation = 0, X-Axis = Baseband Frequency Offset of the Fundamental Tone, Not the Frequency of the HD2 Product (HD2 Product = 2 x the Baseband Frequency), HD2 Canceller Disabled, LO = 3600 MHz

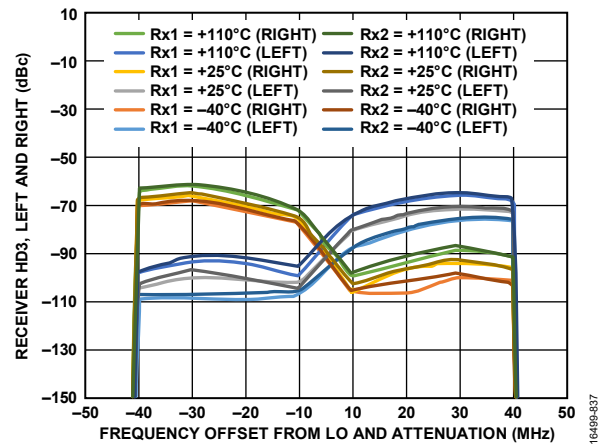


Figure 335. Receiver HD3, Left and Right vs. Frequency Offset from LO and Attenuation, Tone Level = -15 dBm at Attenuation = 0 dB, LO = 4600 MHz

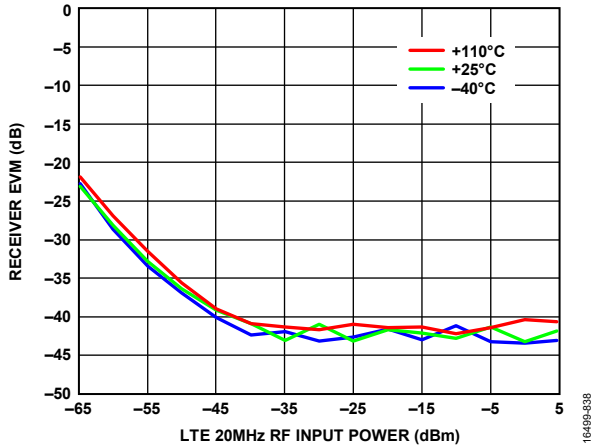


Figure 336. Receiver EVM vs. LTE = 20 MHz RF Input Power, RF Signal = LTE 20 MHz, LO = 3600 MHz, Default AGC Settings

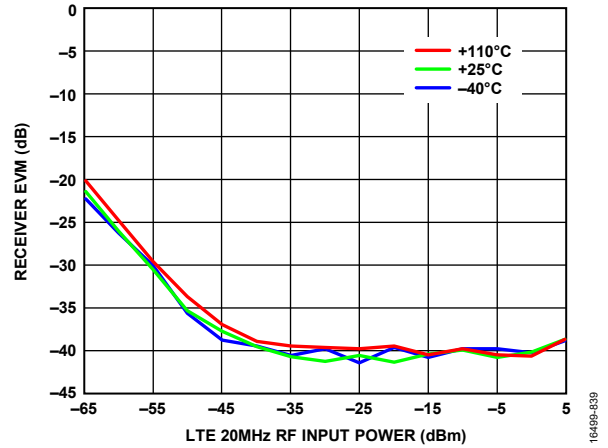


Figure 338. Receiver EVM vs. LTE = 20 MHz RF Input Power, RF Signal = LTE 20 MHz, LO = 4600 MHz, Default AGC Settings

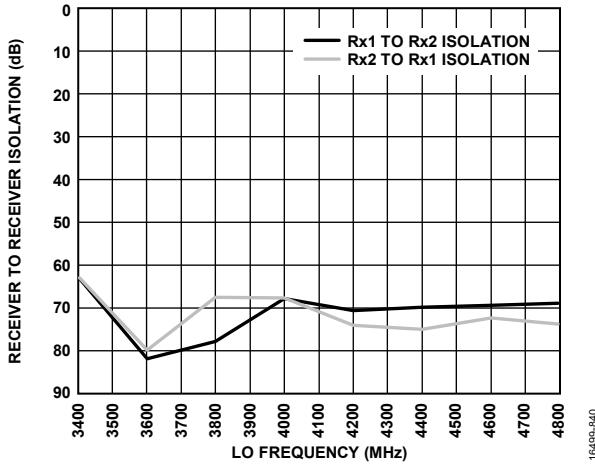


Figure 337. Receiver to Receiver Isolation vs. LO Frequency

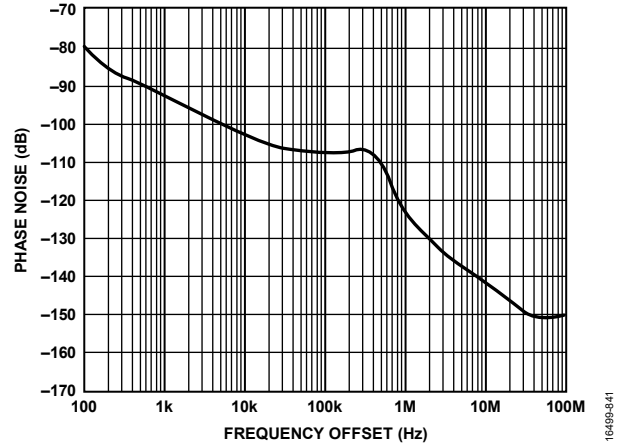


Figure 339. Phase Noise vs. Frequency Offset, LO = 3800 MHz, RMS Phase Error Integrated from 2 kHz to 18 MHz, PLL Loop Bandwidth = 300 kHz, Spectrum Analyzer Limits Far Out Noise

5100 MHz TO 5900 MHz BAND

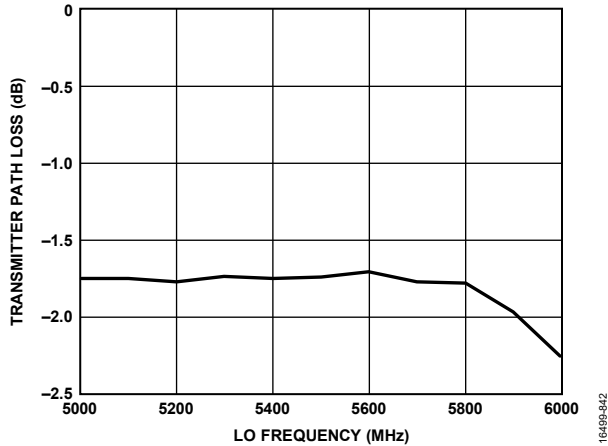


Figure 340. Transmitter Path Loss vs. LO Frequency (Simulation), Useful for De-Embedding Performance Data

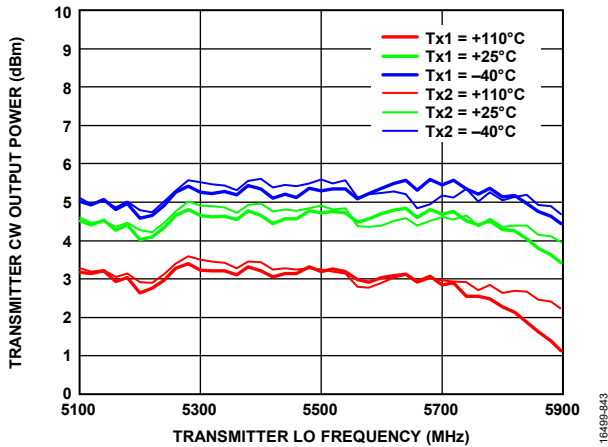


Figure 341. Transmitter CW Output Power vs. Transmitter LO Frequency, Transmitter QEC, and External LO Leakage Active, Bandwidth Mode = 200 MHz/450 MHz, IQ Rate = 491.52 MHz, Attenuation = 0 dB, Not De-Embedded

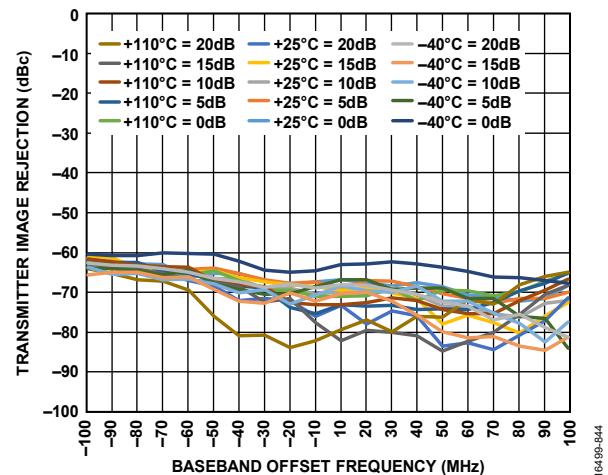


Figure 342. Transmitter Image Rejection vs. Baseband Offset Frequency, QEC Trained with Three Tones Placed at 10 MHz, 50 MHz, and 100 MHz (Tracking On), Total Combined Power = -6 dBFS, Correction then Frozen (Tracking Turned Off), CW Tone Swept Across Large Signal Bandwidth, LO = 5100 MHz

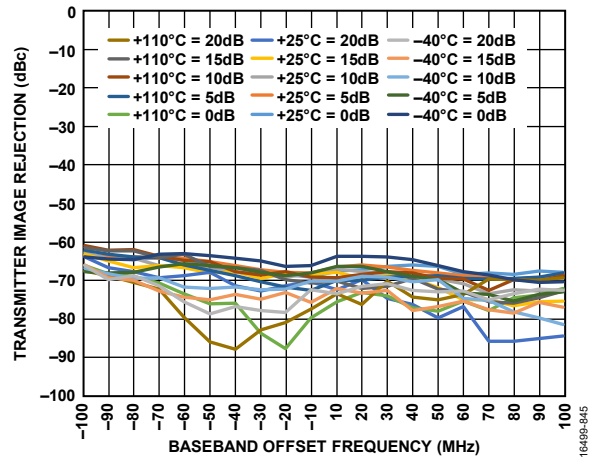


Figure 343. Transmitter Image Rejection vs. Baseband Offset Frequency, QEC Trained with Three Tones Placed at 10 MHz, 50 MHz, and 100 MHz (Tracking On), Total Combined Power = -6 dBFS, Correction then Frozen (Tracking Turned Off), CW Tone Swept Across Large Signal Bandwidth, LO = 5500 MHz

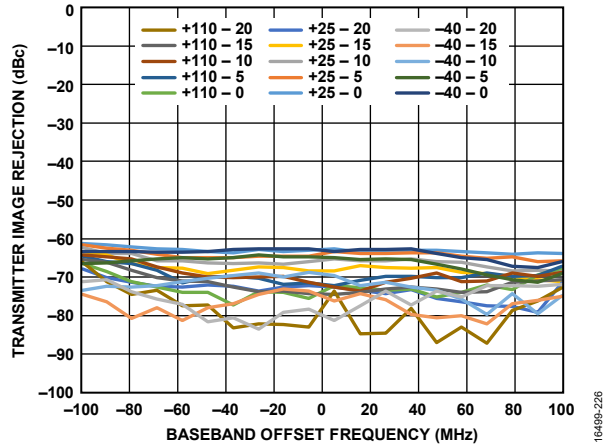


Figure 344. Transmitter Image Rejection vs. Baseband Offset Frequency, QEC Trained with Three Tones Placed at 10 MHz, 50 MHz, and 100 MHz (Tracking On), Total Combined Power = -6 dBFS, Correction then Frozen (Tracking Turned Off), CW Tone Swept Across Large Signal Bandwidth, LO = 5900 MHz

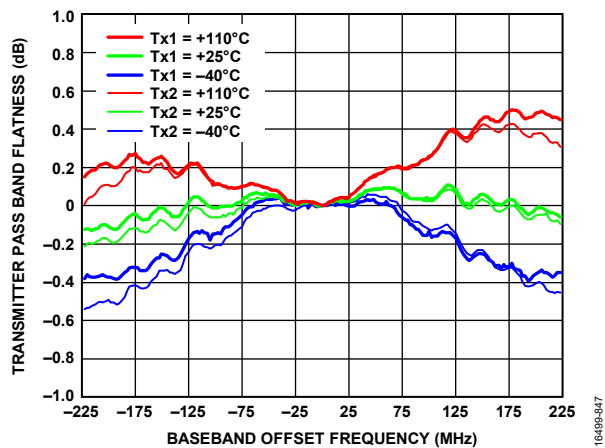


Figure 345. Transmitter Pass Band Flatness vs. Baseband Offset Frequency, Off Chip Match Response De-Embedded, LO = 5700 MHz, Measurements Performed with Device Calibrated at 25°C



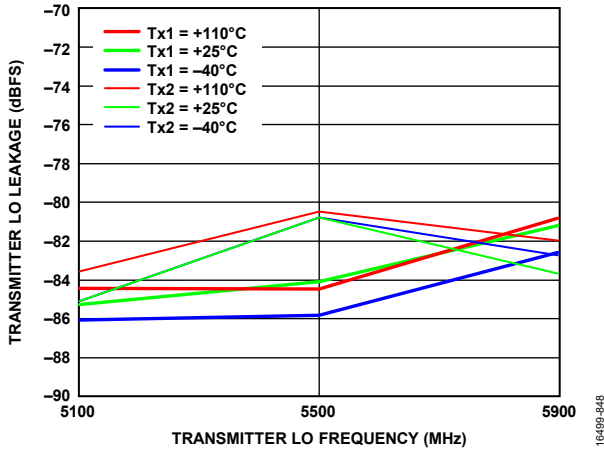


Figure 346. Transmitter LO Leakage vs. Transmitter LO Frequency, Transmitter Attenuation = 0 dB

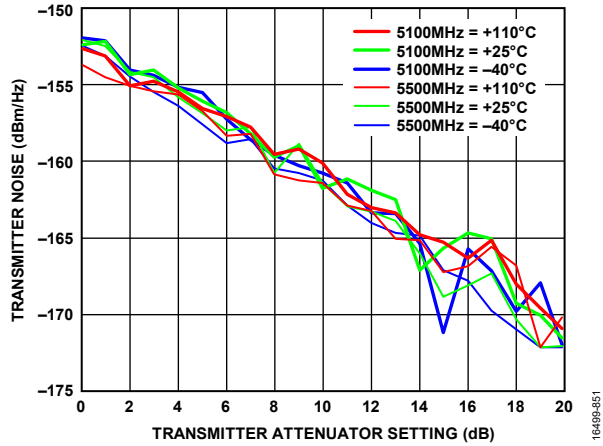


Figure 349. Transmitter Noise vs. Transmitter Attenuator Setting

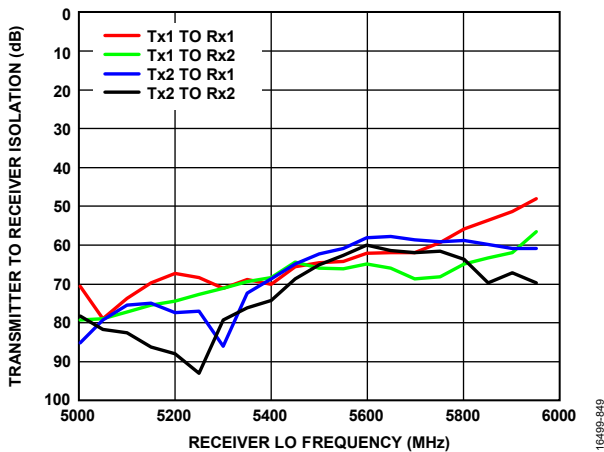


Figure 347. Transmitter to Receiver Isolation vs. Receiver LO Frequency, Temperature = 25°C

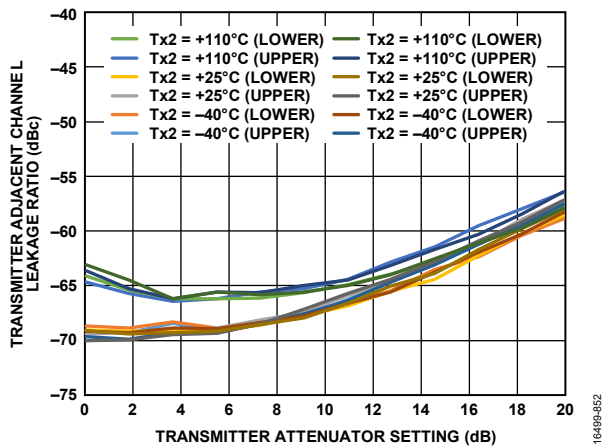


Figure 350. Transmitter Adjacent Channel Leakage Ratio vs. Transmitter Attenuator Setting, LO = 5100 MHz, LTE = 20 MHz, PAR = 12 dB, DAC Boost Normal, Upper Side and Lower Side, Decreasing ACLR at Higher Attenuation Due to Spectrum Analyzer Noise Floor

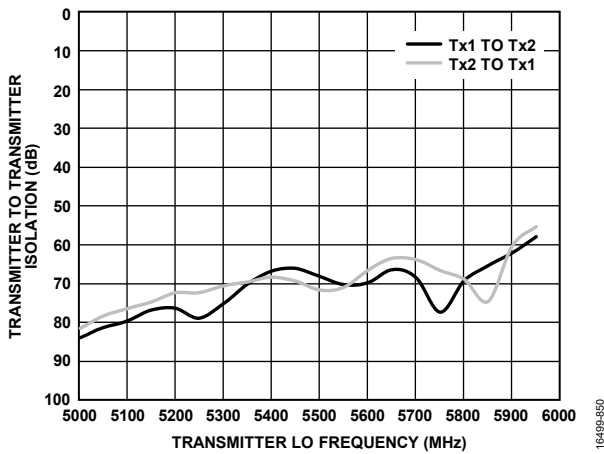


Figure 348. Transmitter to Transmitter Isolation vs. Transmitter LO Frequency, Temperature = 25°C

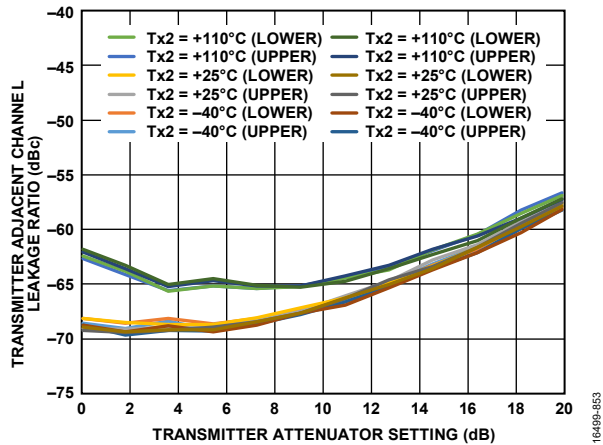


Figure 351. Transmitter Adjacent Channel Leakage Ratio vs. Transmitter Attenuator Setting, LO = 5500 MHz, LTE = 20 MHz, PAR = 12 dB, DAC Boost Normal, Upper Side and Lower Side, Decreasing ACLR at Higher Attenuation Due to Spectrum Analyzer Noise Floor

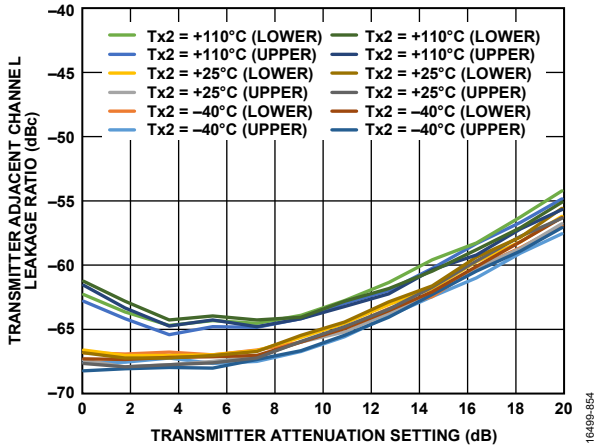


Figure 352. Transmitter Adjacent Channel Leakage Ratio vs. Transmitter Attenuator Setting, LO = 5900 MHz, LTE = 20 MHz, PAR = 12 dB, DAC Boost Normal, Upper Side and Lower Side, Decreasing ACLR at Higher Attenuation Due to Spectrum Analyzer Noise Floor

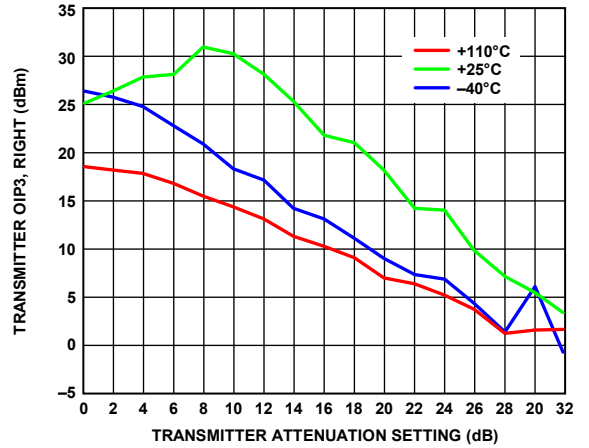


Figure 355. Transmitter OIP3, Right vs. Transmitter Attenuator Setting, LO = 5800 MHz, Total RMS Power = -12 dBFS

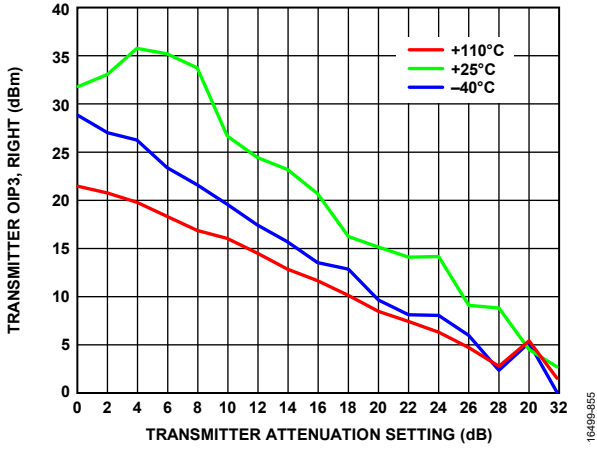


Figure 353. Transmitter OIP3, Right vs. Transmitter Attenuator Setting, LO = 5100 MHz, Total RMS Power = -12 dBFS

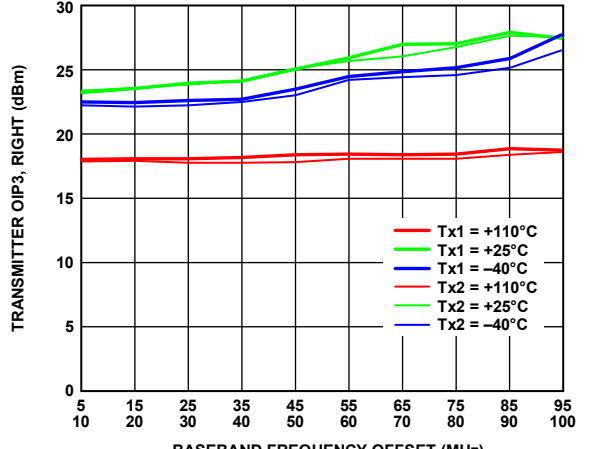


Figure 356. Transmitter OIP3, Right vs. Baseband Frequency Offset, LO = 5100 MHz, Total RMS Power = -12 dBFS Power, Transmitter Attenuation = 4 dB

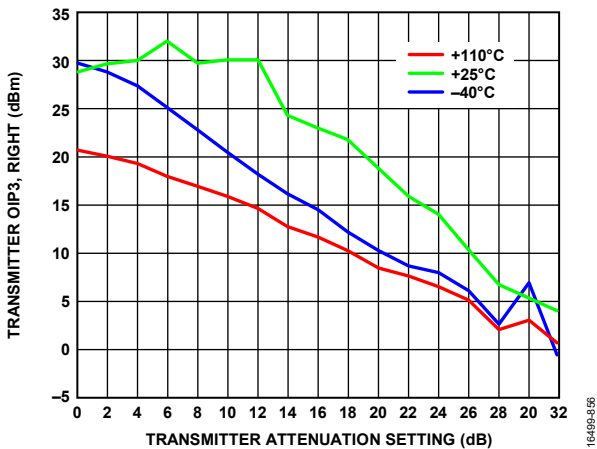


Figure 354. Transmitter OIP3, Right vs. Transmitter Attenuator Setting, LO = 5500 MHz, Total RMS Power = -12 dBFS

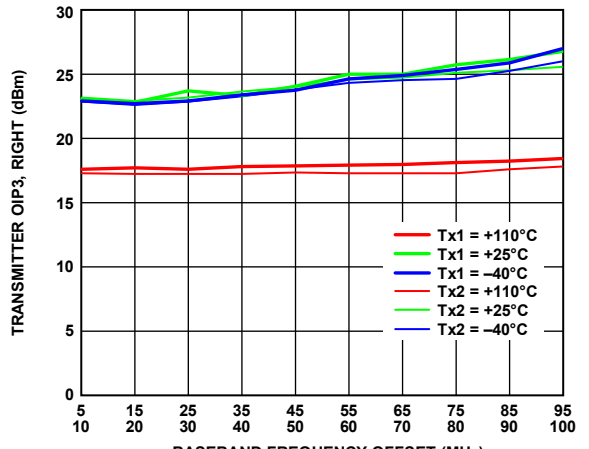


Figure 357. Transmitter OIP3, Right vs. Baseband Frequency Offset, LO = 5500 MHz, Total RMS Power = -12 dBFS, Transmitter Attenuation = 4 dB

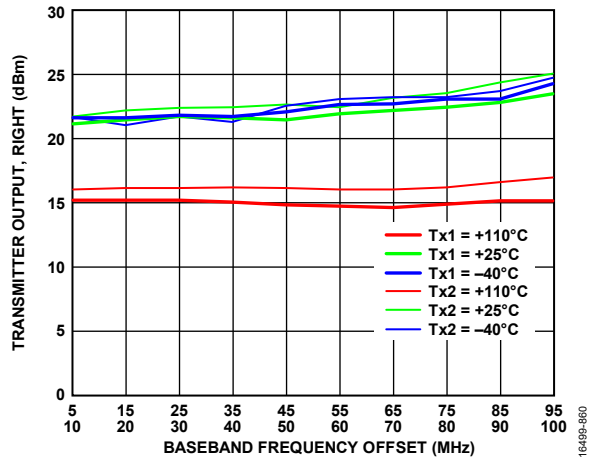


Figure 358. Transmitter Output, Right vs. Baseband Frequency Offset, LO = 5900 MHz, Total RMS Power = -12 dBFS, Transmitter Attenuation = 4 dB

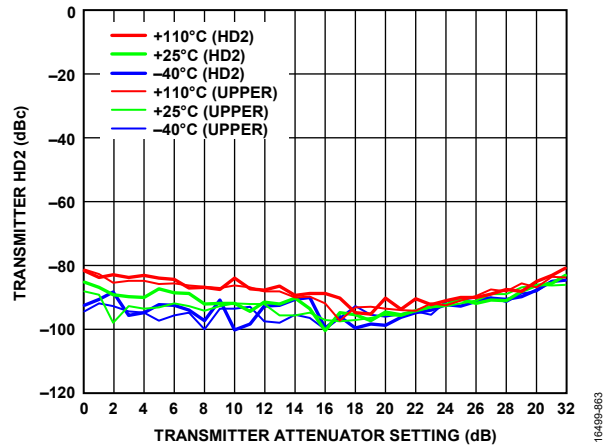


Figure 361. Transmitter HD2 vs. Transmitter Attenuator Setting, Baseband Frequency = 10 MHz, LO = 5900 MHz, CW = -15 dBFS

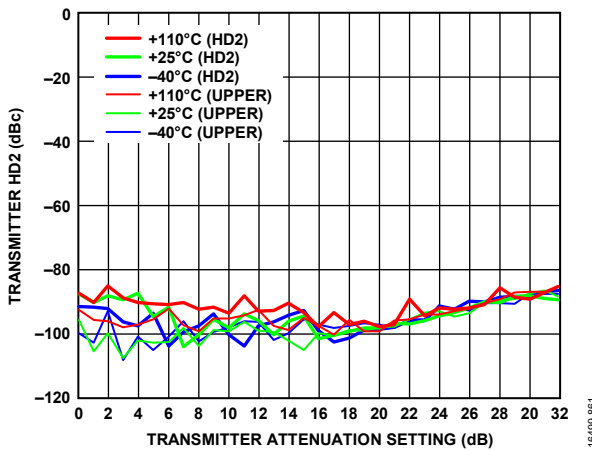


Figure 359. Transmitter HD2 vs. Transmitter Attenuation Setting, Baseband Frequency = 10 MHz, LO = 5100 MHz, CW = -15 dBFS

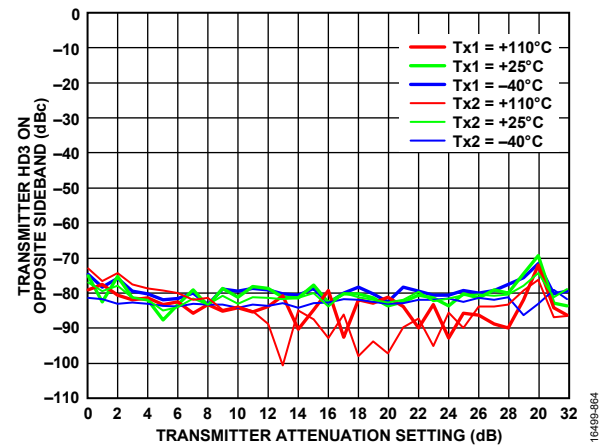


Figure 362. Transmitter HD3 on Opposite Sideband vs. Transmitter Attenuator Setting, LO = 5100 MHz, CW = -15 dBFS, Baseband Frequency = 10 MHz

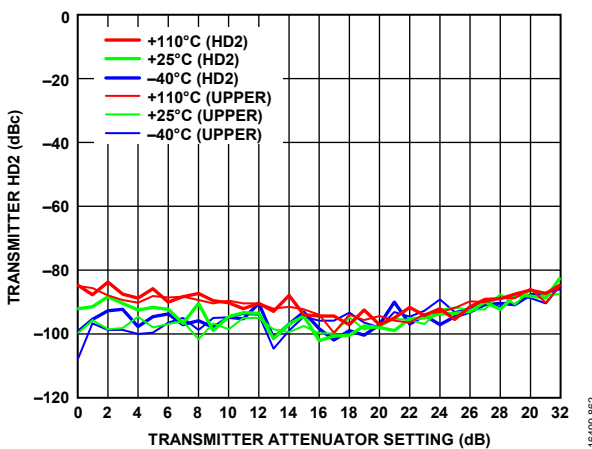


Figure 360. Transmitter HD2 vs. Transmitter Attenuator Setting, Baseband Frequency = 10 MHz, LO = 5500 MHz, CW = -15 dBFS

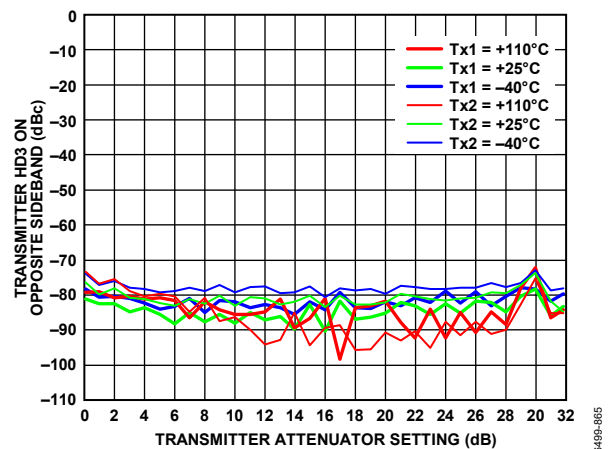


Figure 363. Transmitter HD3 on Opposite Sideband vs. Transmitter Attenuator Setting, LO = 5500 MHz, CW = -15 dBFS, Baseband Frequency = 10 MHz

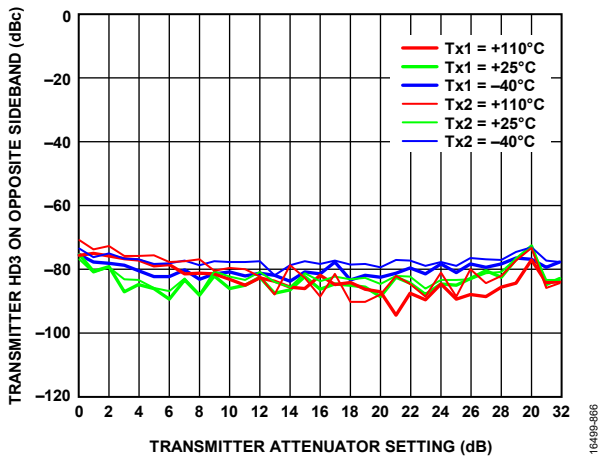


Figure 364. Transmitter HD3 on Opposite Sideband vs. Transmitter Attenuator Setting, LO = 5900 MHz, CW = -15 dBFS, Baseband Frequency = 10 MHz

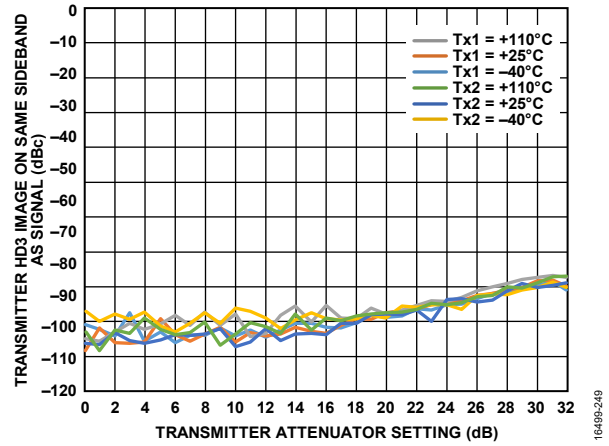


Figure 367. Transmitter HD3 Image on Same Sideband as Signal vs. Transmitter Attenuator Setting, LO = 5900 MHz, CW = -15 dBFS

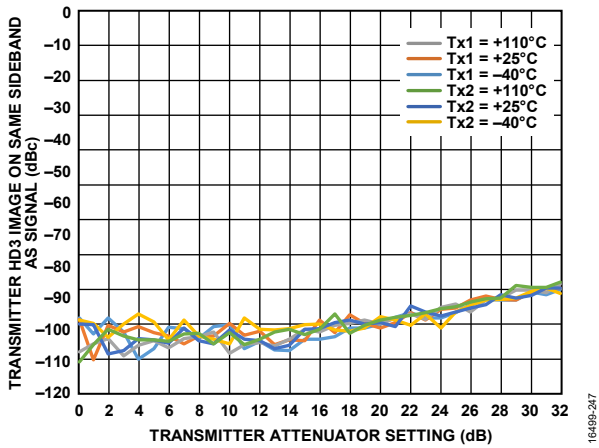


Figure 365. Transmitter HD3 Image on Same Sideband as Signal vs. Transmitter Attenuator Setting, LO = 5100 MHz, CW = -15 dBFS

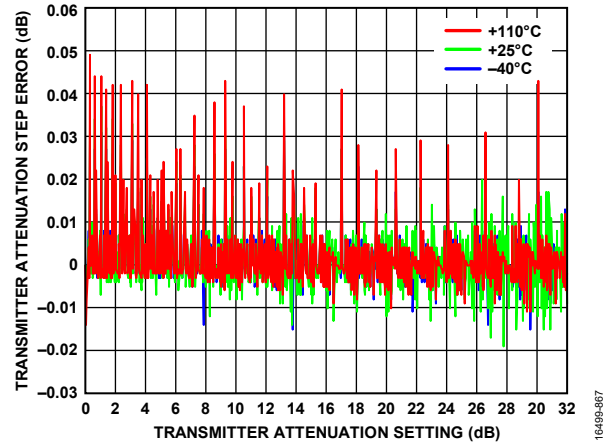


Figure 368. Transmitter Attenuation Step Error vs. Transmitter Attenuator Setting, LO = 5100 MHz

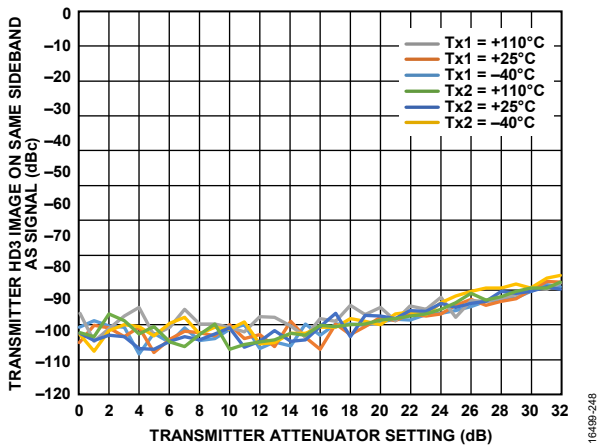


Figure 366. Transmitter HD3 Image on Same Sideband as Signal vs. Transmitter Attenuator Setting, LO = 5500 MHz, CW = -15 dBFS

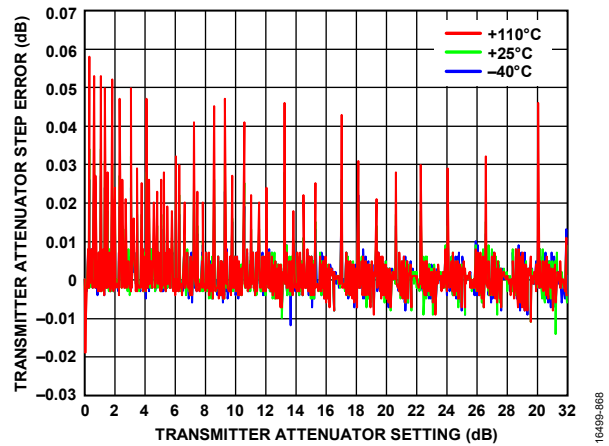


Figure 369. Transmitter Attenuation Step Error vs. Transmitter Attenuator Setting, LO = 5500 MHz

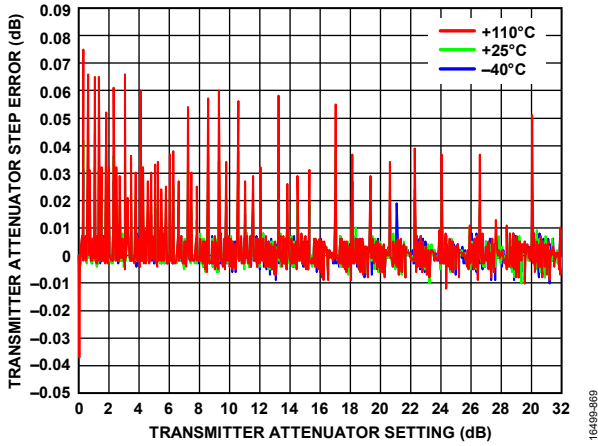


Figure 370. Transmitter Attenuator Step Error vs. Transmitter Attenuator Setting, LO = 5900 MHz

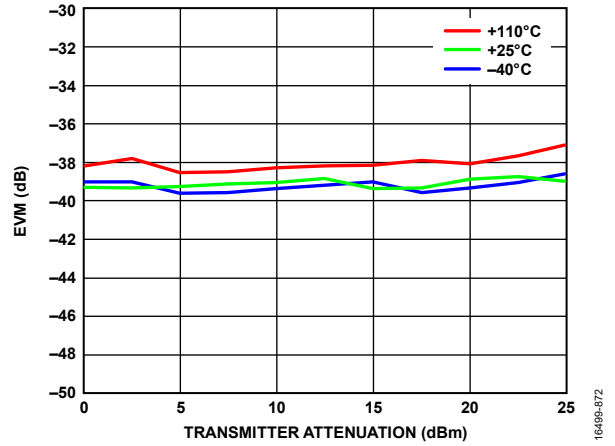


Figure 373. EVM vs. Transmitter Attenuation, LTE Signal = 20 MHz, Centered on DC, LO = 5900 MHz

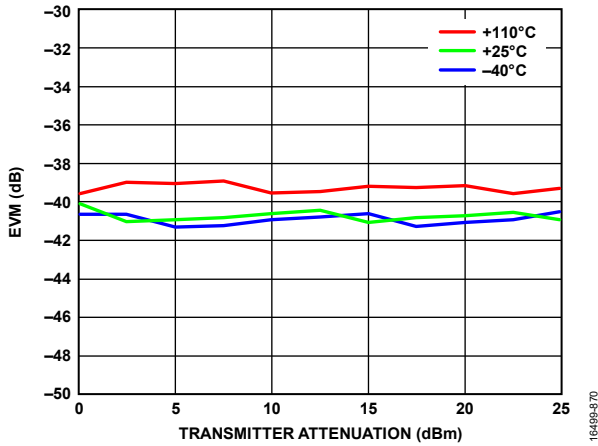


Figure 371. EVM vs. Transmitter Attenuation, LTE Signal = 20 MHz Centered on DC, LO = 5100 MHz

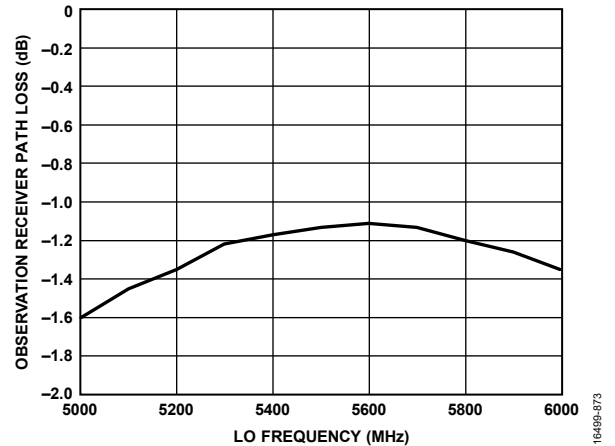


Figure 374. Observation Receiver Path Loss vs. LO Frequency, Can be Used for De-Embedding Performance Data

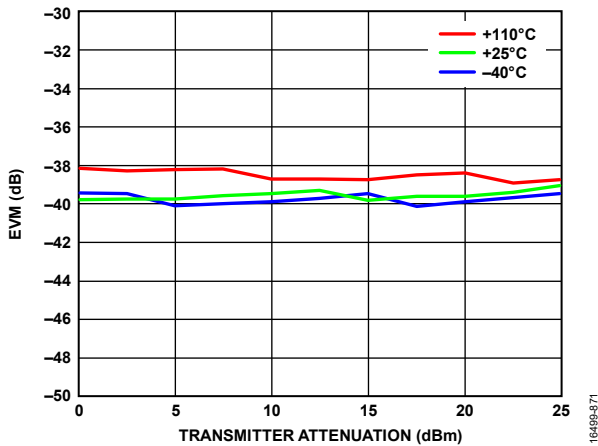


Figure 372. EVM vs. Transmitter Attenuation, LTE Signal = 20 MHz, Centered on DC, LO = 5500 MHz

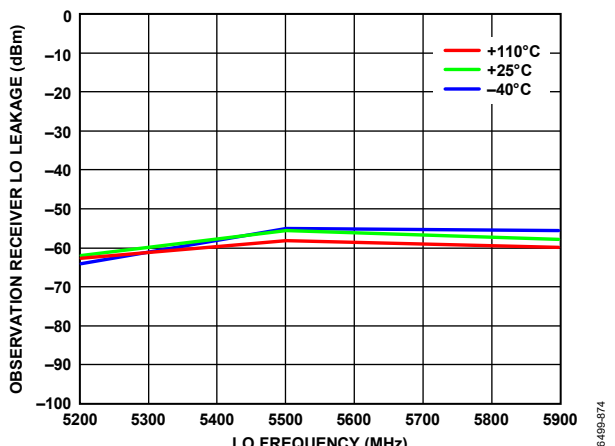


Figure 375. Observation Receiver LO Leakage vs. LO Frequency LO = 5200 MHz, 5500 MHz, and 5900 MHz

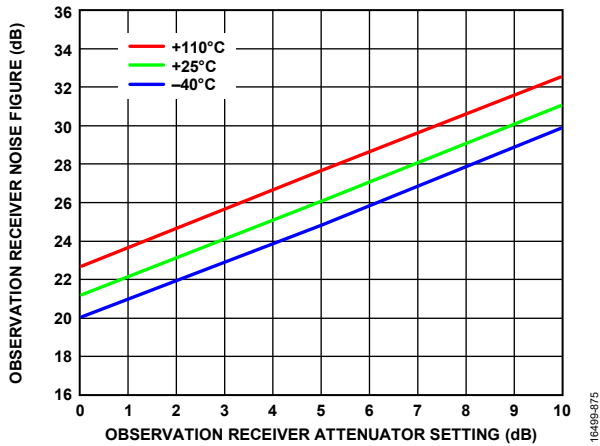


Figure 376. Observation Receiver Noise Figure vs. Observation Receiver Attenuator Setting, 5200 MHz, Total Nyquist Integration Bandwidth

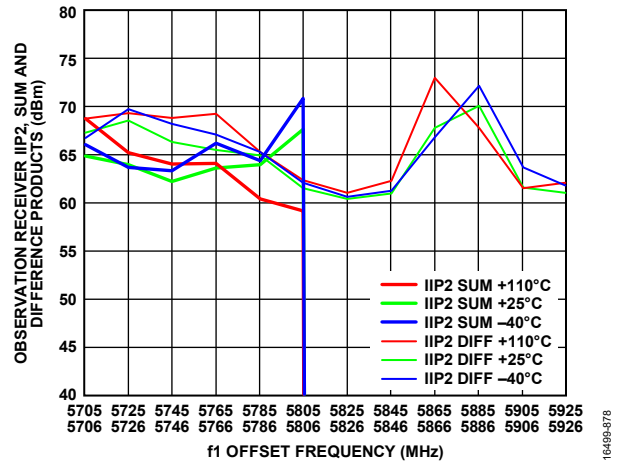


Figure 379. Observation Receiver IIP2, Sum and Difference Products vs. f1 Offset Frequency, Tones Separated by 1 MHz Swept Across Pass Band at -19 dBm Each, LO = 5700 MHz, Attenuation = 0 dB

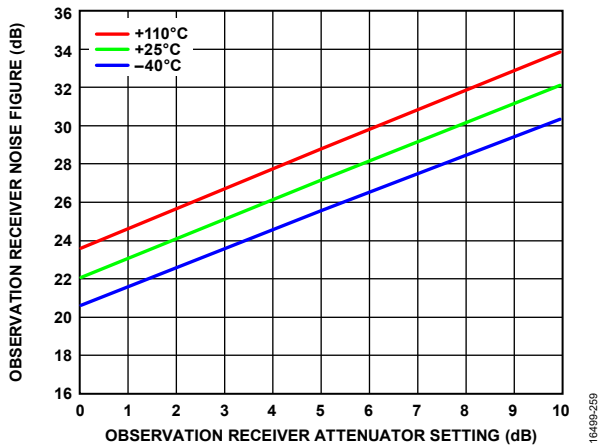


Figure 377. Observation Receiver Noise Figure vs. Observation Receiver Attenuator Setting, LO = 5500 MHz, Total Nyquist Integration Bandwidth

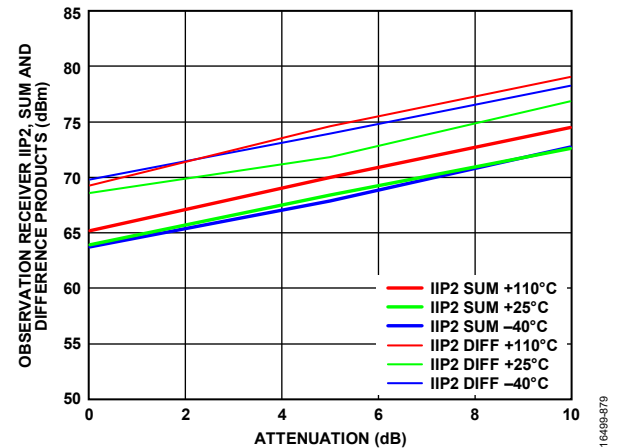


Figure 380. Observation Receiver IIP2, Sum and Difference Products vs. Attenuation, LO = 5700 MHz, Tone 1 = 5725 MHz, Tone 2 = 5726 MHz at -19 dBm Plus Attenuation

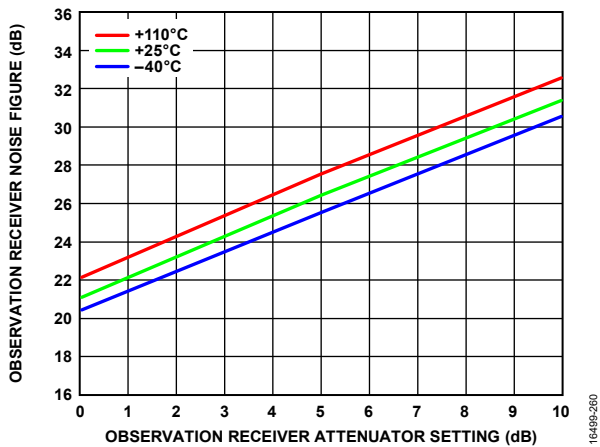


Figure 378. Observation Receiver Noise Figure vs. Observation Receiver Attenuator Setting, LO = 5800 MHz, Total Nyquist Integration Bandwidth

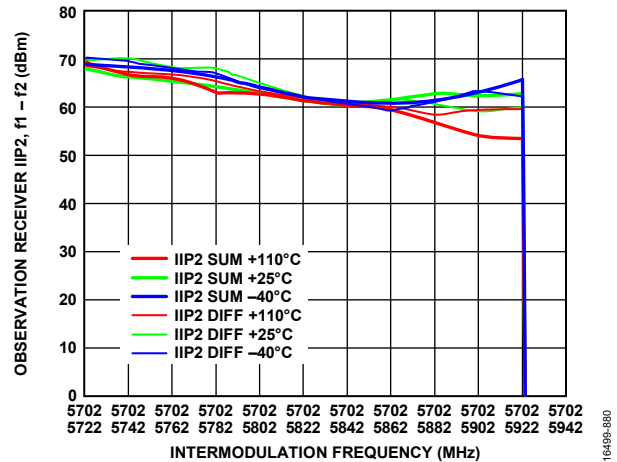


Figure 381. Observation Receiver IIP2, f1 - f2 vs. Intermodulation Frequency, LO = 5700 MHz, Tone 1 = 5702 MHz, Tone 2 = Swept, -19 dBm Each, Attenuation = 0 dB

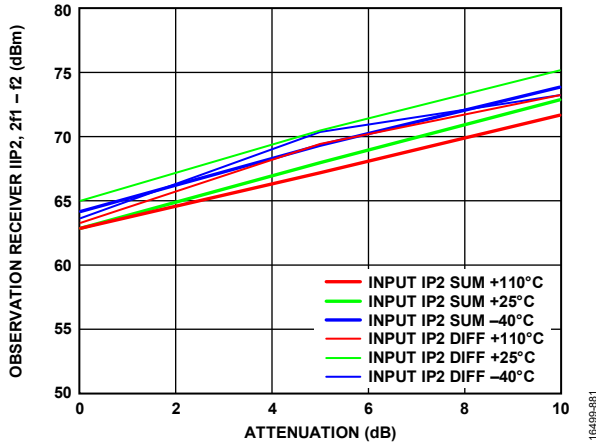


Figure 382. Observation Receiver IIP2, 2f1 - f2 vs. Attenuation, LO = 5700 MHz, Tone 1 = 5702 MHz, Tone 2 = 5802 MHz at -19 dBm Plus Attenuation

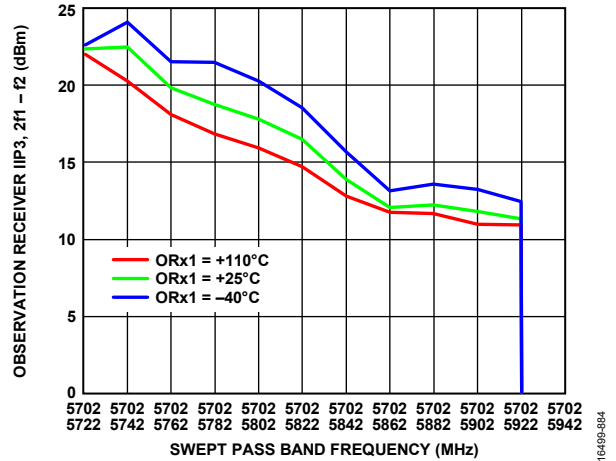


Figure 385. Observation Receiver IIP3, 2f1 - f2 vs. Swept Pass Band Frequency, LO = 5700 MHz, Tone 1 = 5702 MHz, Tone 2 = 5722 MHz at -22 dBm Each Plus Attenuation

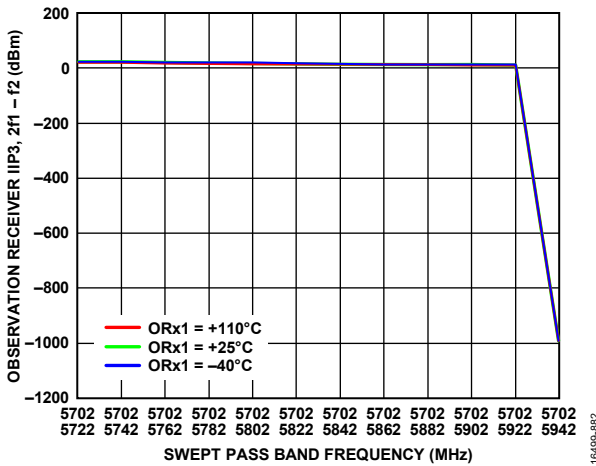


Figure 383. Observation Receiver IIP3, 2f1 - f2 vs. Swept Pass Band Frequency, LO = 5700 MHz, Observer Receiver Attenuation = 0 dB, Tones Separated by 1 MHz Swept Across Pass Band at -19 dBm Each

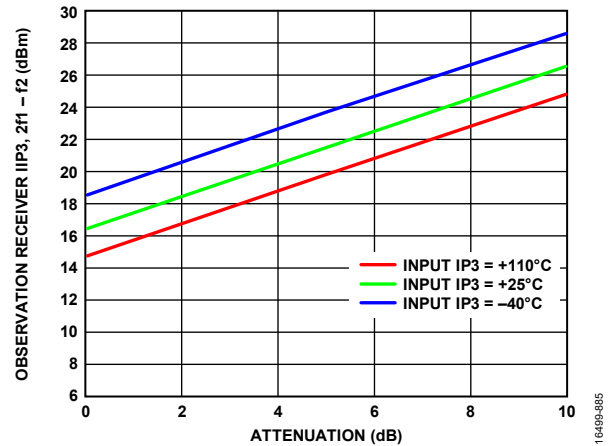


Figure 386. Observation Receiver IIP3, 2f1 - f2 vs. Attenuation, LO = 5700 MHz, Tone 1 = 5702 MHz, Tone 2 = 5822 MHz at -19 dBm Plus Attenuation

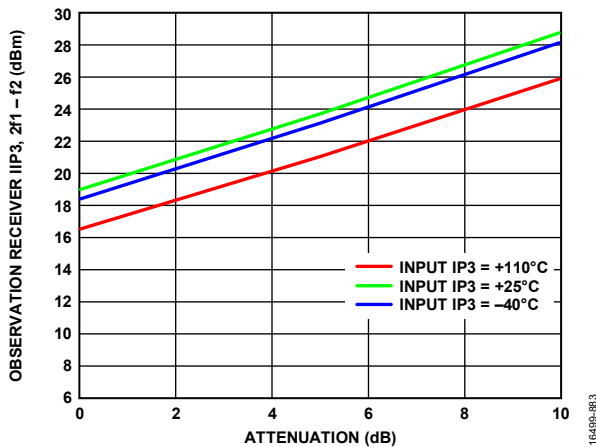


Figure 384. Observation Receiver IIP3, 2f1 - f2 vs. Attenuation, LO = 5700 MHz, Tone 1 = 5745 MHz, Tone 2 = 5746 MHz at -19 dBm Plus Attenuation

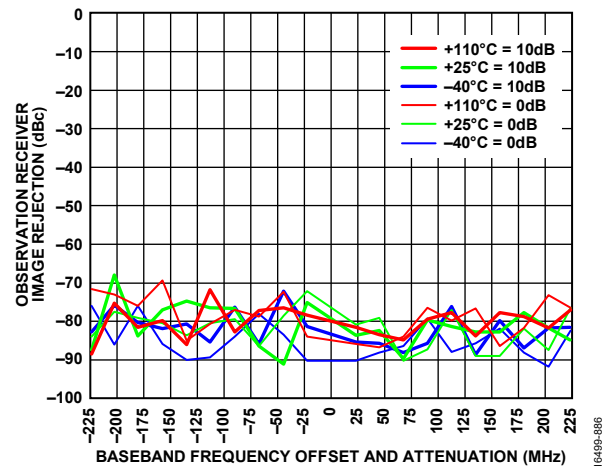


Figure 387. Observation Receiver Image Rejection vs. Baseband Frequency Offset and Attenuation, CW Signal Swept Across the Pass Band, LO = 5200 MHz

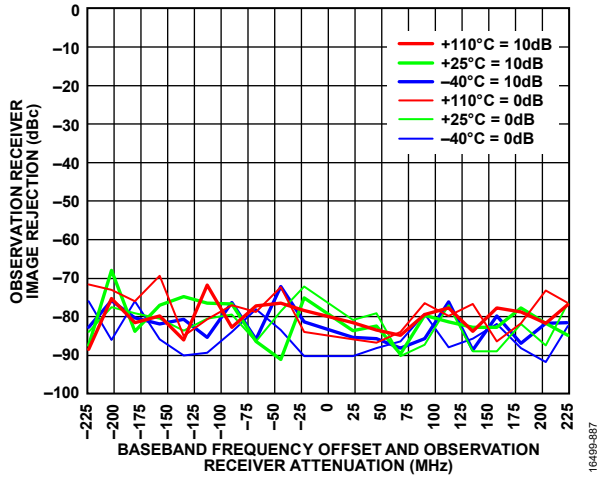


Figure 388. Observation Receiver Image Rejection vs. Baseband Frequency Offset and Observation Receiver Attenuation, CW Signal Swept Across the Pass Band, LO = 5700 MHz

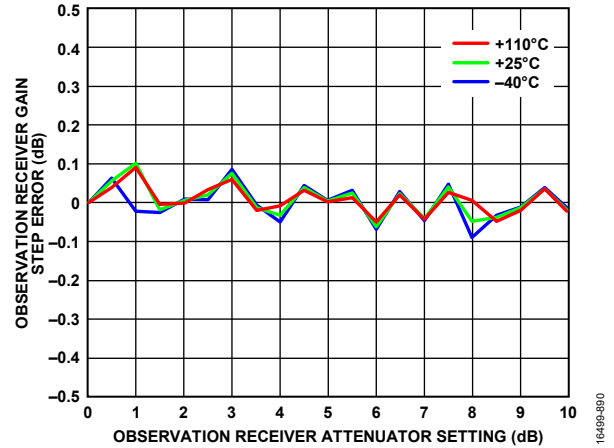


Figure 391. Observation Receiver Gain Step Error vs. Observation Receiver Attenuator Setting, LO = 5200 MHz

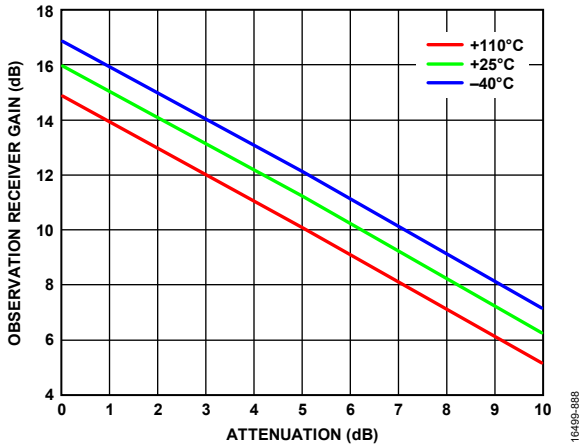


Figure 389. Observation Receiver Gain vs. Attenuation, LO = 5200 MHz

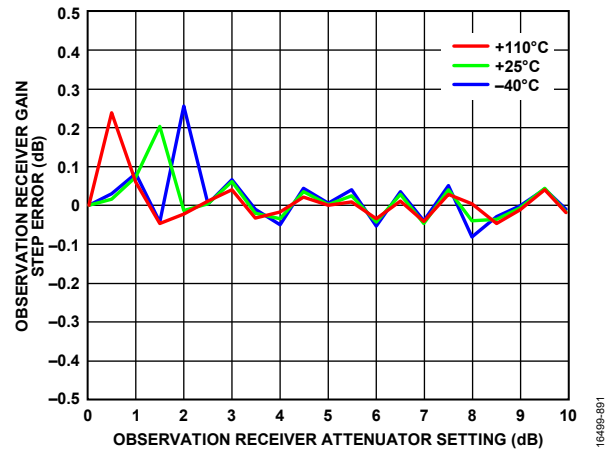


Figure 392. Observation Receiver Gain Step Error vs. Observation Receiver Attenuator Setting, LO = 5600 MHz

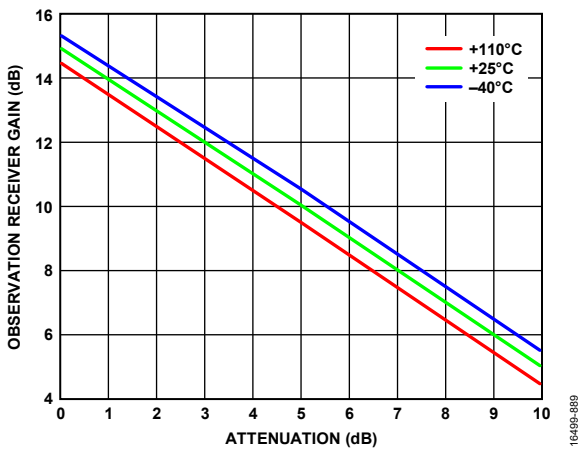


Figure 390. Observation Receiver Gain vs. Attenuation, LO = 5700 MHz

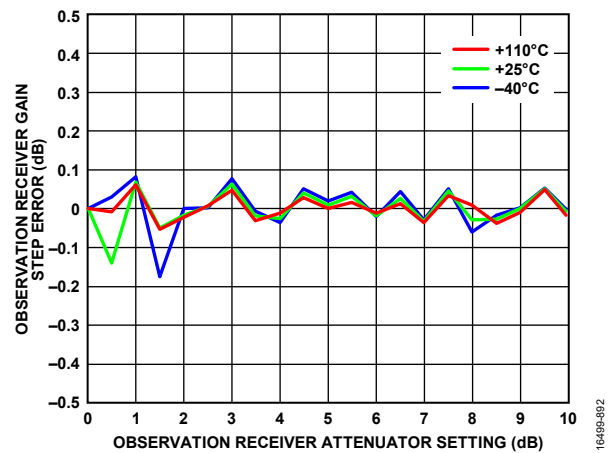


Figure 393. Observation Receiver Gain Step Error vs. Observation Receiver Attenuator Setting, LO = 5600 MHz



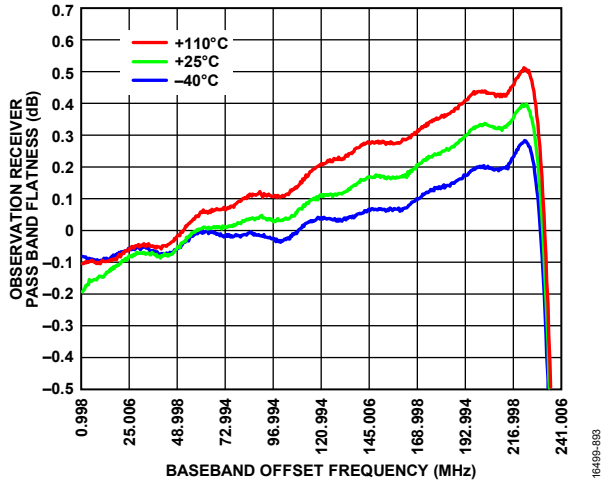


Figure 394. Observation Receiver Pass Band Flatness vs. Baseband Offset Frequency, LO = 5700 MHz

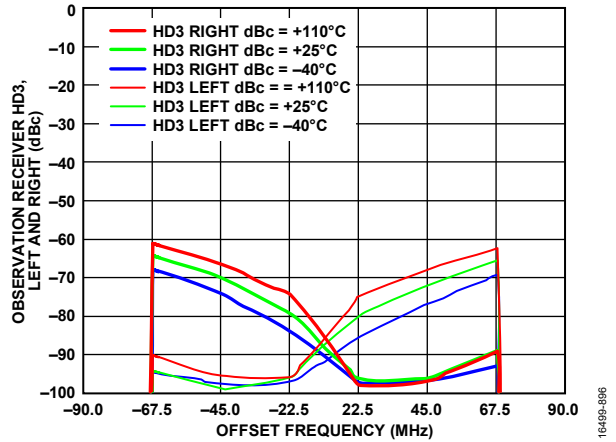


Figure 397. Observation Receiver HD3, Left and Right vs. Offset Frequency, LO = 5200 MHz, Tone Level = -20 dBm

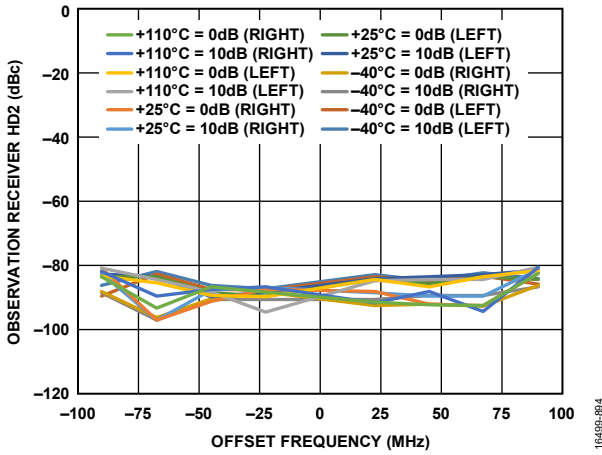


Figure 395. Observation Receiver HD2 vs. Offset Frequency, LO = 5200 MHz, Tone Level = -20 dBm Plus Attenuation

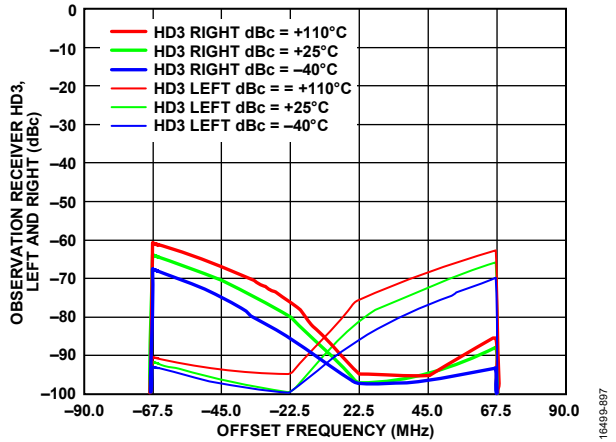


Figure 398. Observation Receiver HD3, Left and Right vs. Offset Frequency, LO = 5700 MHz, Tone Level = -20 dBm

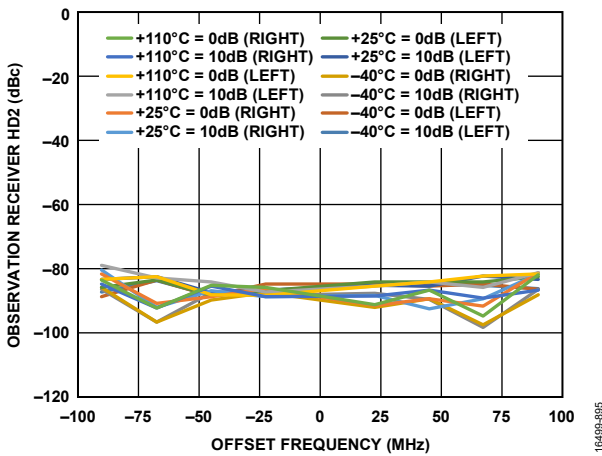


Figure 396. Observation Receiver HD2 vs. Offset Frequency, LO = 5700 MHz, Tone Level = -20 dBm Plus Attenuation

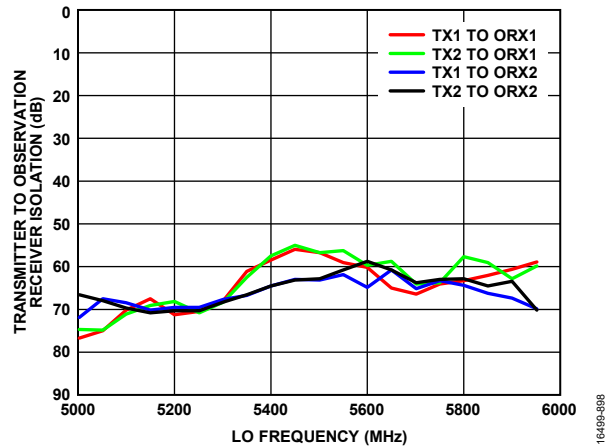


Figure 399. Transmitter to Observation Receiver Isolation vs. LO Frequency, Temperature = 25°C

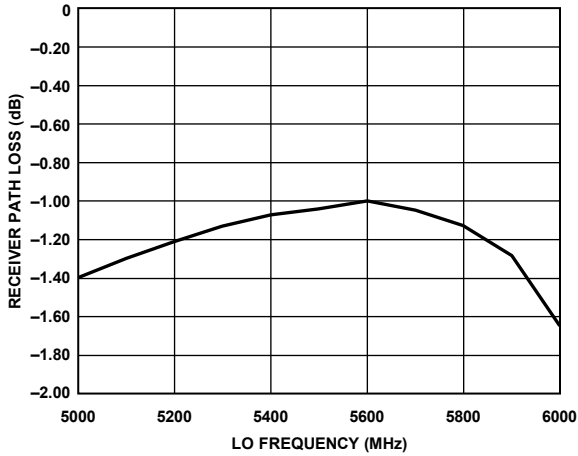


Figure 400. Receiver Path Loss vs. LO Frequency, Can Be Used for De-Embedding Performance Data

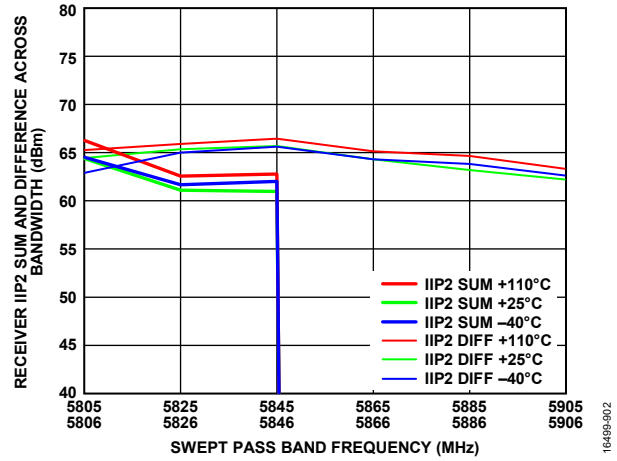


Figure 403. Receiver IIP2 Sum and Difference Across Bandwidth vs. Swept Pass Band Frequency, Receiver Attenuation = 0 dB, LO = 5800 MHz, Six Tone Pairs, -21 dBm Plus Attenuation Each

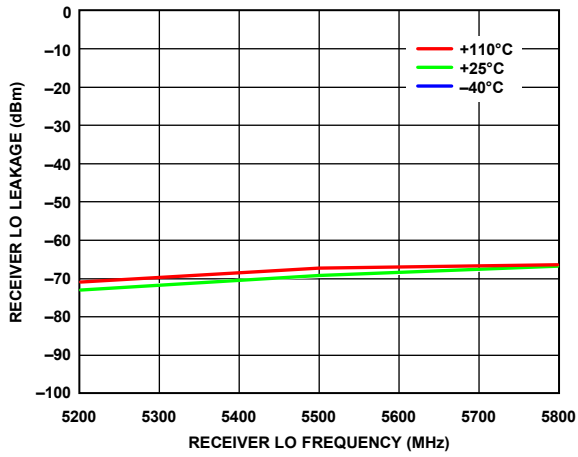


Figure 401. Receiver LO Leakage vs. Receiver LO Frequency, LO = 5200 MHz, 5500 MHz, and 5800 MHz, Receiver Attenuation = 0 dB, RF Bandwidth = 200 MHz, Sample Rate = 245.76 MSPS

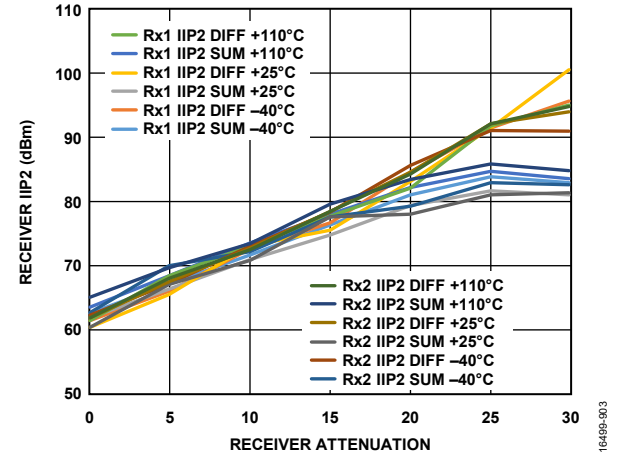


Figure 404. Receiver IIP2 vs. Receiver Attenuation, LO = 5800 MHz, Tones Placed at 5802 MHz and 5892 MHz, -21 dBm Plus Attenuation

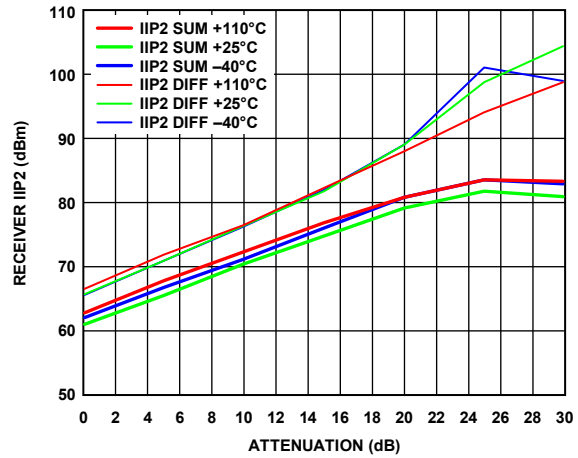


Figure 402. Receiver IIP2 vs. Attenuation, LO = 5800 MHz LO, Tones Placed at 5845 MHz and 5846 MHz, -21 dBm Plus Attenuation

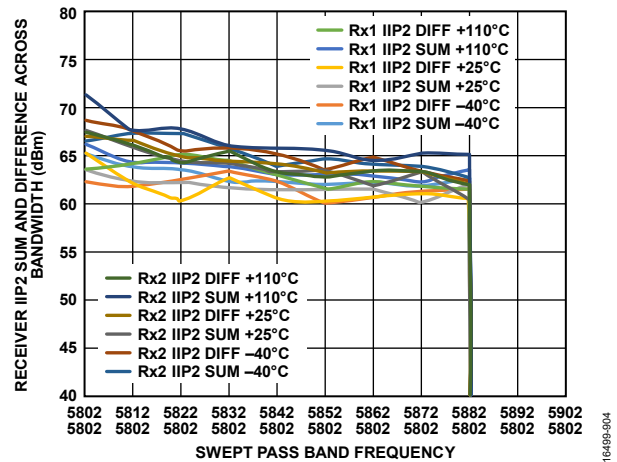


Figure 405. Receiver IIP2 Sum and Difference Across Bandwidth vs. Swept Pass Band Frequency, Receiver Attenuation = 0 dB, LO = 5800 MHz, Tone 1 = 5802 MHz, Tone 2 Swept, -21 dBm Each

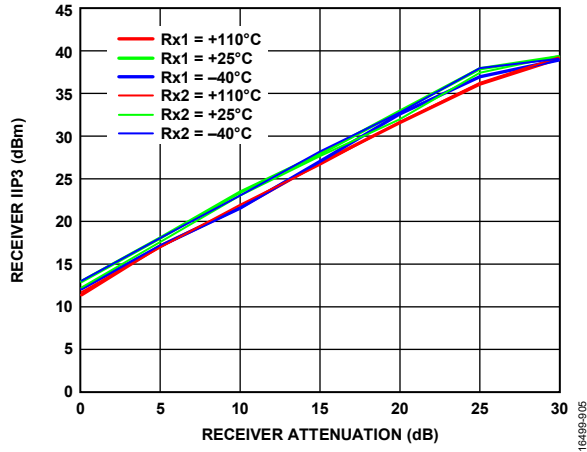


Figure 406. Receiver IIP3 vs. Receiver Attenuation, LO = 5800 MHz, Tone 1 = 5895 MHz, Tone 2 = 5896 MHz, -21 dBm Plus Attenuation

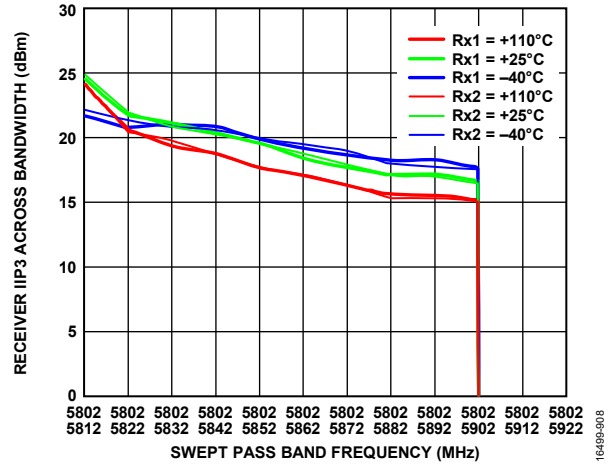


Figure 409. Receiver IIP3 Across Bandwidth vs. Swept Pass Band Frequency, Receiver Attenuation = 0 dB, LO = 5800 MHz, Tone 1 = 5802 MHz, Tone 2 Swept Across Pass Band, -21 dBm Each

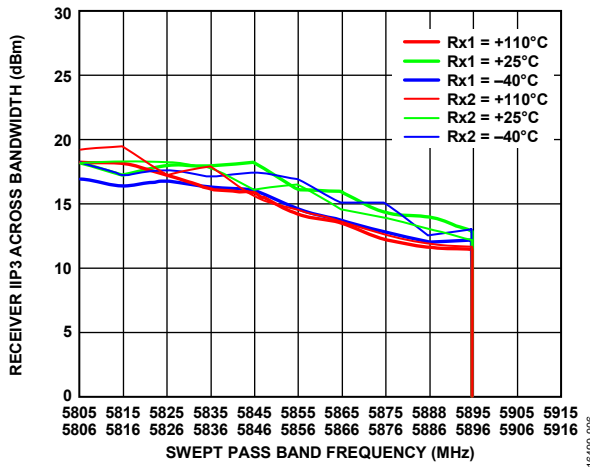


Figure 407. Receiver IIP3 Across Bandwidth vs. Swept Pass Band Frequency, Receiver Attenuation = 0 dB, LO = 5800 MHz, Tone 2 = Tone 1 + 1 MHz, -21 dBm each, Swept Across Pass Band

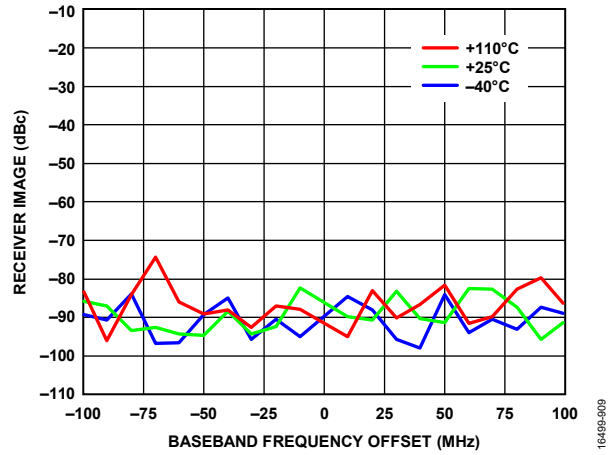


Figure 410. Receiver Image vs. Baseband Frequency Offset, Attenuation = 0 dB, RF Bandwidth = 200 MHz, Tracking Calibration Active, Sample Rate = 245.76 MSPS, LO = 5200 MHz

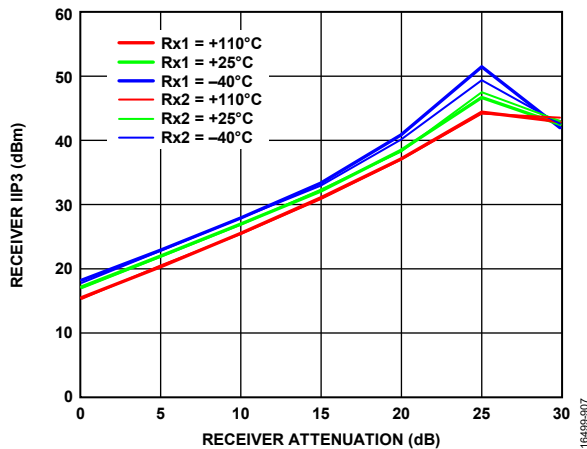


Figure 408. Receiver IIP3 vs. Receiver Attenuation, LO = 5800 MHz, Tone 1 = 5802 MHz, Tone 2 = 5892 MHz, -21 dBm Plus Attenuation

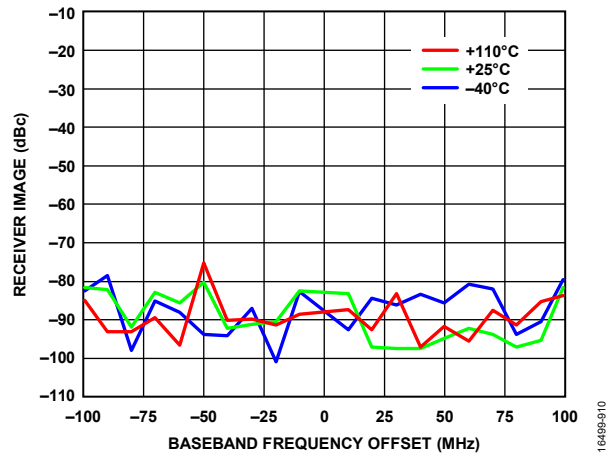


Figure 411. Receiver Image vs. Baseband Frequency Offset, Attenuation = 0 dB, RF Bandwidth = 200 MHz, Tracking Calibration Active, Sample Rate = 245.76 MSPS, LO = 5900 MHz

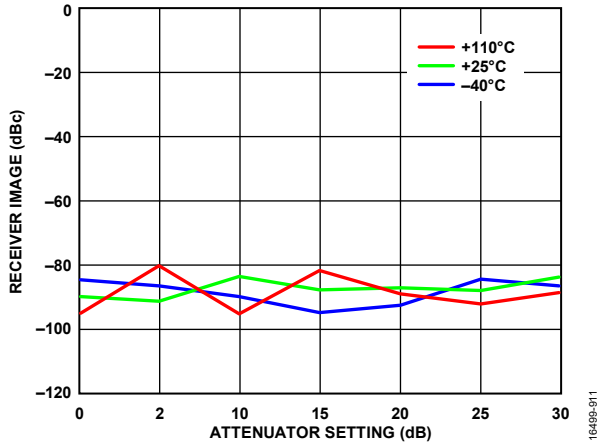


Figure 412. Receiver Image vs. Attenuator Setting, RF Bandwidth = 200 MHz, Tracking Calibration Active, Sample Rate = 245.76 MSPS, LO = 5200 MHz, Baseband Frequency = 10 MHz

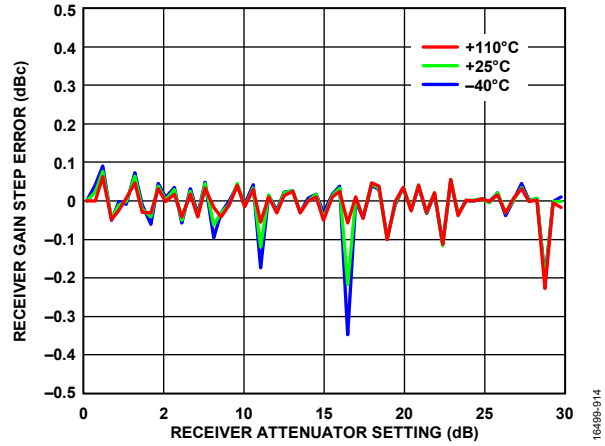


Figure 415. Receiver Gain Step Error vs. Receiver Attenuator Setting, LO = 5600 MHz

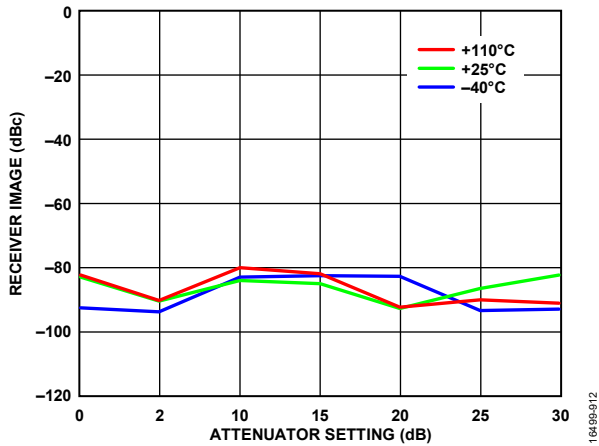


Figure 413. Receiver Image vs. Attenuator Setting, RF Bandwidth = 200 MHz, Tracking Calibration Active, Sample Rate = 245.76 MSPS, LO = 5900 MHz, Baseband Frequency = 10 MHz

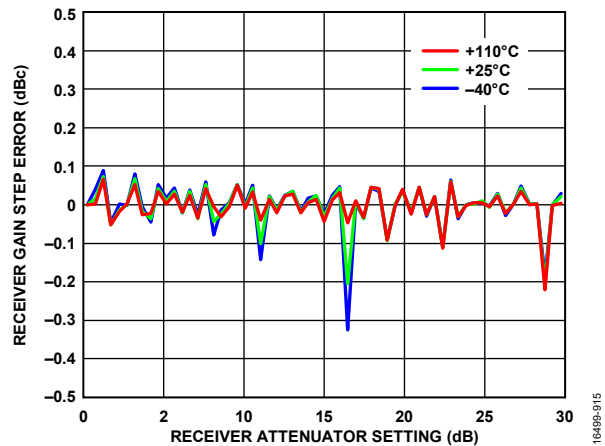


Figure 416. Receiver Gain Step Error vs. Receiver Attenuator Setting, LO = 6000 MHz

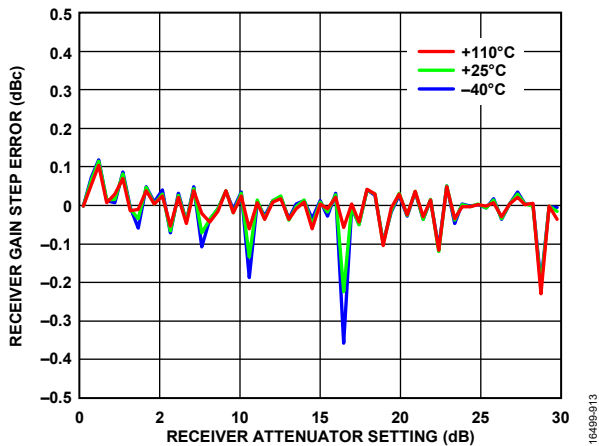


Figure 414. Receiver Gain Step Error vs. Receiver Attenuator Setting, LO = 5200 MHz

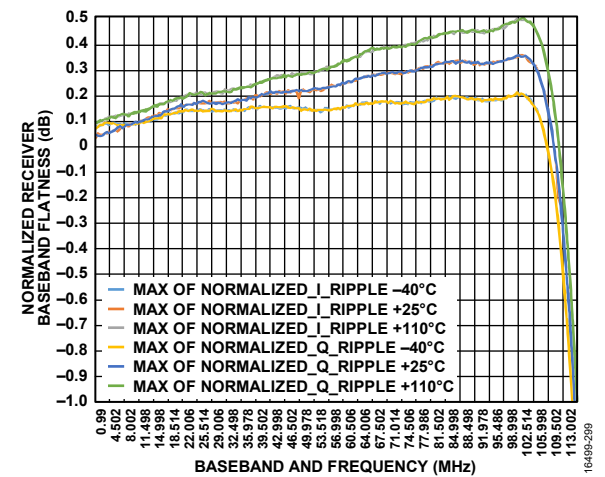


Figure 417. Normalized Receiver Baseband Flatness vs. Baseband and Frequency (Receiver Flatness)

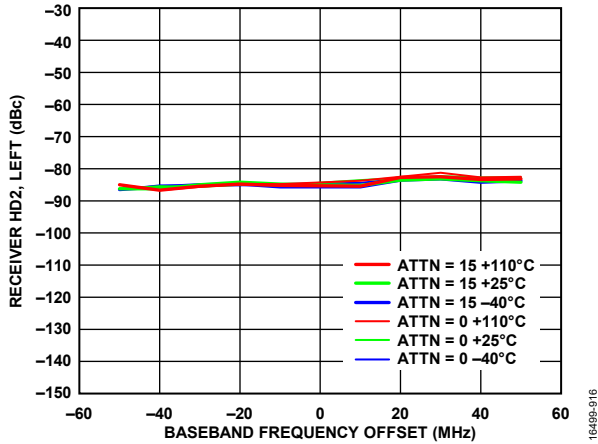


Figure 418. Receiver HD2, Left vs. Baseband Frequency Offset, Tone Level = -15 dBm at Attenuation = 0 dB, X-Axis = Baseband Frequency Offset of the Fundamental Tone, Not the Frequency of the HD2 Product (HD2 Product = 2 × the Baseband Frequency), HD2 Canceller Disabled, LO = 5200 MHz

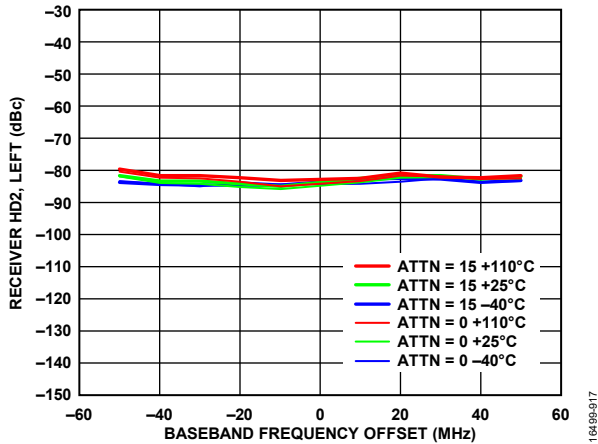


Figure 419. Receiver HD2, Left vs. Baseband Frequency Offset, Tone Level = -15 dBm at Attenuation = 0 dB, X-Axis = Baseband Frequency Offset of the Fundamental Tone, Not the Frequency of the HD2 Product (HD2 Product = 2 × the Baseband Frequency), HD2 Canceller Disabled, LO = 5900 MHz

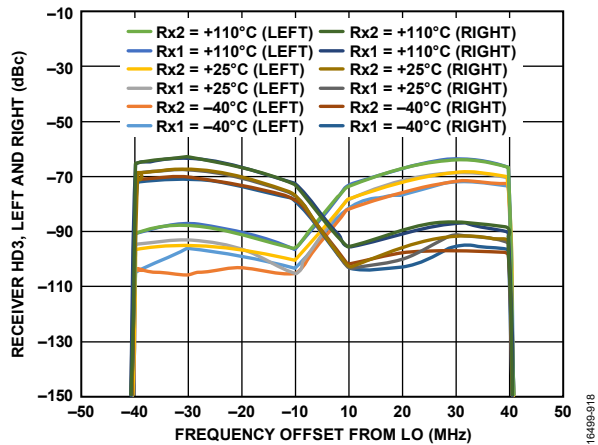


Figure 420. Receiver HD3, Left and Right vs. Frequency Offset from LO, Tone Level = -15 dBm at Attenuation = 0 dB, LO = 5200 MHz

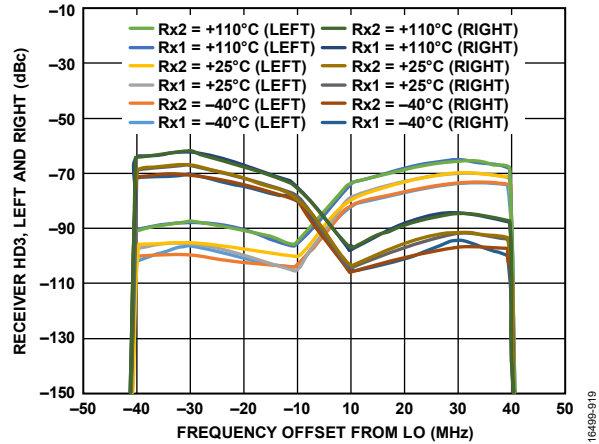


Figure 421. Receiver HD3, Left and Right vs. Frequency Offset from LO, Tone Level = -15 dBm at Attenuation = 0 dB, LO = 5900 MHz

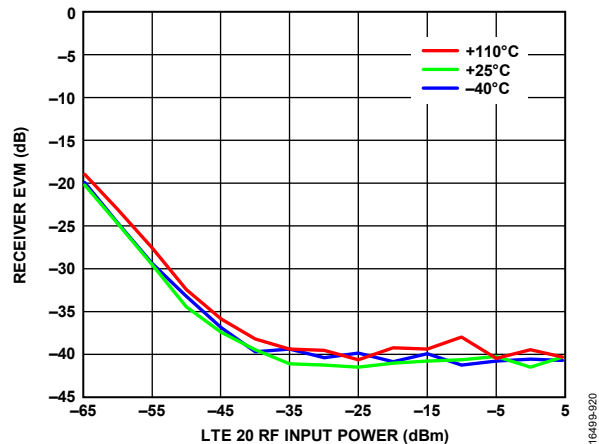


Figure 422. Receiver EVM vs. LTE20 RF Input Power, LO = 5200 MHz, Default AGC Settings

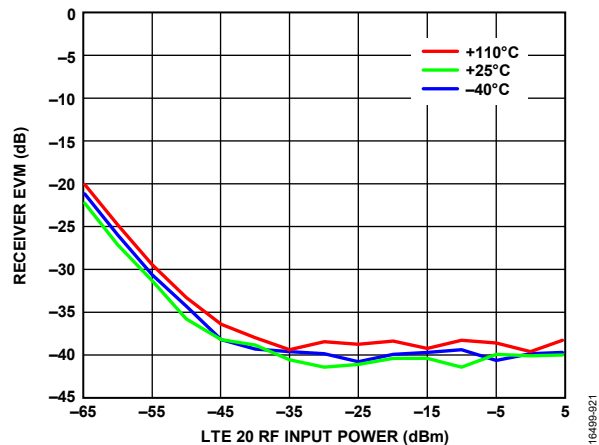


Figure 423. Receiver EVM vs. LTE20 RF Input Power, LO = 5500 MHz, Default AGC Settings

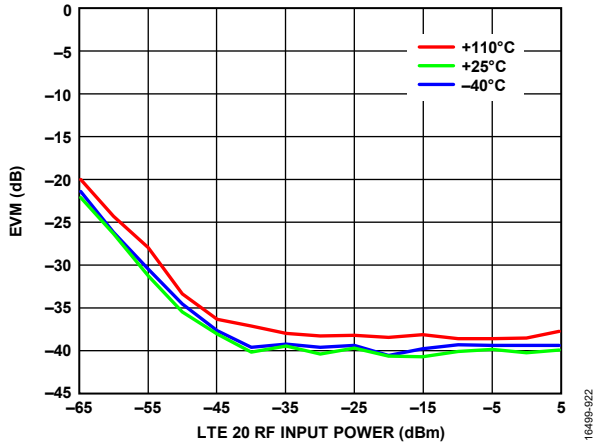


Figure 424. EVM vs. LTE20 RF Input Power, LO = 5800 MHz, Default AGC Settings

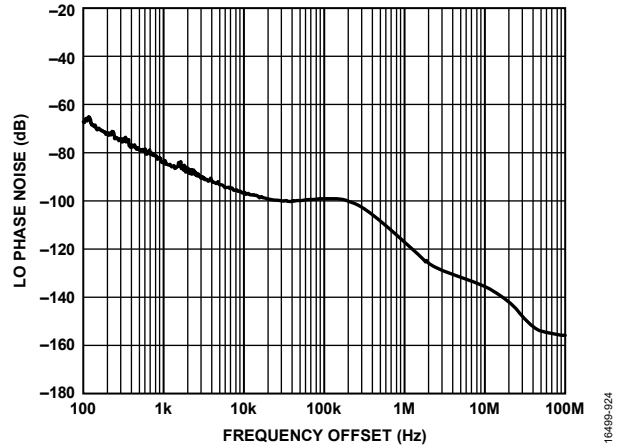


Figure 426. LO Phase Noise vs. Frequency Offset, LO = 5900 MHz, RMS Phase Error Integrated from 2 kHz to 18 MHz, PLL Loop Bandwidth > 300 kHz, Spectrum Analyzer Limits Far Out Noise

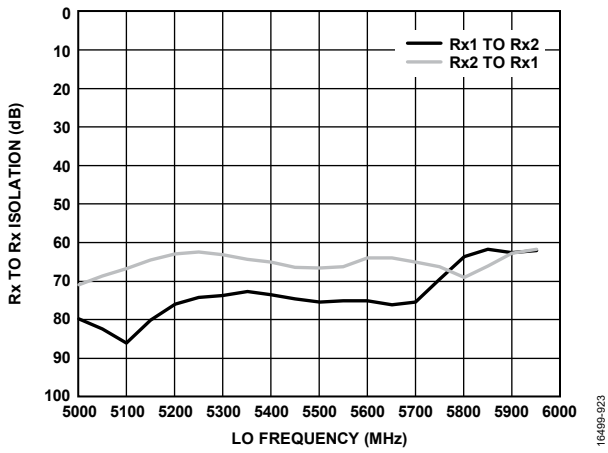


Figure 425. Receiver to Receiver Isolation vs. LO Frequency

TRANSMITTER OUTPUT IMPEDANCE

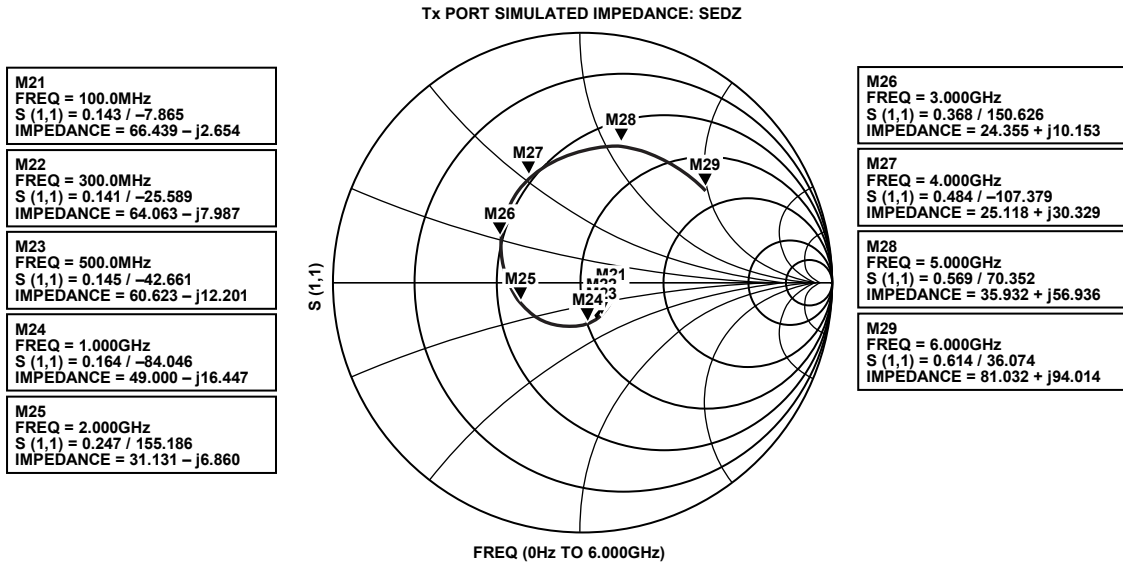


Figure 427. Transmitter Output Impedance Series Equivalent Differential Impedance (SEDZ)

OBSERVATION RECEIVER INPUT IMPEDANCE

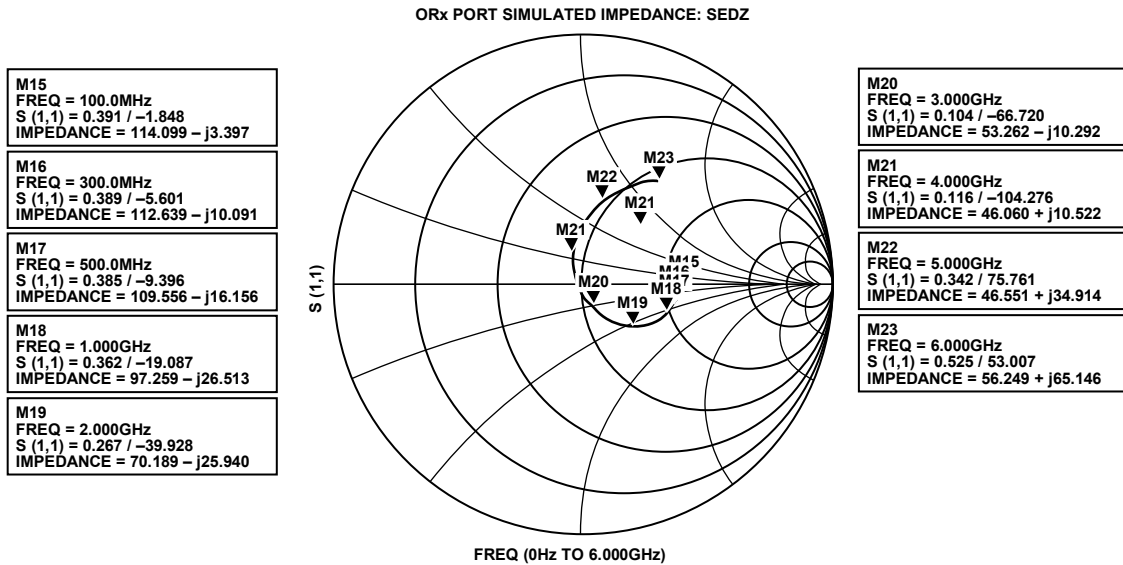
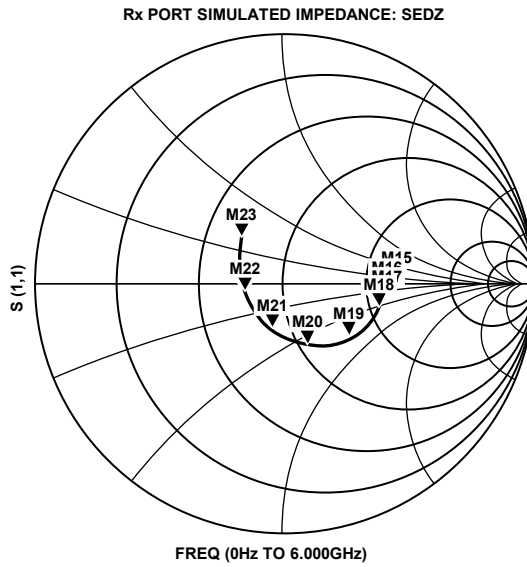


Figure 428. Observation Receiver Input Impedance SEDZ

RECEIVER INPUT IMPEDANCE

|   |
|---|
| <b>M15</b><br>FREQ = 100.0MHz<br>S (1,1) = 0.390 / -1.819<br>IMPEDANCE = 113.933 - j3.331   |
| <b>M16</b><br>FREQ = 300.0MHz<br>S (1,1) = 0.390 / -5.495<br>IMPEDANCE = 112.803 - j9.931   |
| <b>M17</b><br>FREQ = 500.0MHz<br>S (1,1) = 0.388 / -9.198<br>IMPEDANCE = 110.398 - j16.107  |
| <b>M18</b><br>FREQ = 1.000GHz<br>S (1,1) = 0.377 / -18.643<br>IMPEDANCE = 100.377 - j28.250 |
| <b>M19</b><br>FREQ = 2.000GHz<br>S (1,1) = 0.336 / -39.123<br>IMPEDANCE = 74.966 - j35.800  |



|   |
|---|
| <b>M20</b><br>FREQ = 3.000GHz<br>S (1,1) = 0.267 / -64.650<br>IMPEDANCE = 55.102 - j28.685  |
| <b>M21</b><br>FREQ = 4.000GHz<br>S (1,1) = 0.186 / -104.336<br>IMPEDANCE = 42.821 - j16.026 |
| <b>M22</b><br>FREQ = 5.000GHz<br>S (1,1) = 0.164 / -173.106<br>IMPEDANCE = 35.977 - j1.455  |
| <b>M23</b><br>FREQ = 6.000GHz<br>S (1,1) = 0.266 / 130.063<br>IMPEDANCE = 32.890 + j14.399  |

Figure 429. Receiver Input Impedance SEDZ

16499-004



## TERMINOLOGY

### Large Signal Bandwidth

Large signal bandwidth, otherwise known as instantaneous bandwidth or signal bandwidth, is the bandwidth over which there are large signals. For example, for Band 42 LTE, the large signal bandwidth is 200 MHz.

### Occupied Bandwidth

Occupied bandwidth is the total bandwidth of the active signals. For example, three 20 MHz carriers have a 60 MHz occupied bandwidth, regardless of where the carriers are placed within the large signal bandwidth.

### Synthesis Bandwidth

Synthesis bandwidth is the bandwidth over which digital predistortion (DPD) linearization is transmitted. Synthesis bandwidth is the 1 dB bandwidth of the transmitter. The power density of the signal outside the occupied bandwidth is assumed to be 25 dB below the signal in the occupied bandwidth, which also assumes that the unlinearized power amplifier (PA) achieves 25 dB ACLR.

### Observation Bandwidth

Observation bandwidth is the 1 dB bandwidth of the observation receiver. With the observation receiver sharing the transmitter LO, the observation receiver senses similar power densities, such as those in the occupied bandwidth and synthesis bandwidth of the transmitter.

### Backoff

Backoff is the difference (in dB) between full scale and the rms signal power.

### $P_{\text{HIGH}}$

$P_{\text{HIGH}}$  is the largest signal that can be applied without overloading the ADC for the receiver or observation receiver input. This input level results in slightly less than full scale at the digital output because of the nature of the continuous time  $\Sigma$ - $\Delta$  ADCs, which, for example, exhibit a soft overload in contrast to the hard clipping of pipeline ADCs.

## THEORY OF OPERATION

The ADRV9009 is a highly integrated RF transmitter subsystem capable of configuration for a wide range of applications. The device integrates all RF, mixed-signal, and digital blocks necessary to provide all transmitter traffic and DPD observation receiver functions in a single device. Programmability allows the transmitter to be adapted for use in many TDD systems and 3G/4G/5G cellular standards. The ADRV9009 contains four high speed serial interface links for the transmitter chain, and two high speed links each for the receiver and observation receiver chains. The links are JESD204B, Subclass 1 compliant. The two receiver lanes can be reused for the observation receiver, providing a low pin count and a reliable data interface to field programmable gate arrays (FPGAs) or integrated baseband solutions.

The ADRV9009 also provides tracking correction of dc offset QEC errors and transmitter LO leakage to maintain high performance under varying temperatures and input signal conditions. The device also includes test modes that allow system designers to debug designs during prototyping and to optimize radio configurations.

### TRANSMITTER

The ADRV9009 transmitter section consists of two identical and independently controlled channels that provide all digital processing, mixed-signal, and RF blocks necessary to implement a direct conversion system while sharing a common frequency synthesizer. The digital data from the JESD204B lanes pass through a fully programmable, 128-tap FIR filter with variable interpolation rates. The FIR output is sent to a series of interpolation filters that provide additional filtering and interpolation prior to reaching the DAC. Each 14-bit DAC has an adjustable sample rate.

When converted to baseband analog signals, the inphase (I) and quadrature (Q) signals are filtered to remove sampling artifacts and are fed to the upconversion mixers. Each transmitter chain provides a wide attenuation adjustment range with fine granularity to optimize SNR.

### RECEIVER

The ADRV9009 receiver contains all the blocks necessary to receive RF signals and convert them to digital data usable by a BBP. Each receiver can be configured as a direct conversion system that supports up to a 200 MHz bandwidth. Each receiver contains a programmable attenuator stage, followed by matched I and Q mixers that downconvert received signals to baseband for digitization.

Gain control can be achieved by using the on-chip AGC or by allowing the BBP to make gain adjustments in a manual gain control mode. Performance is optimized by mapping each gain control setting to specific attenuation levels at each adjustable gain block in the receiver signal path. Additionally, each channel contains independent receive signal strength indicator (RSSI) measurement capability, dc offset tracking, and all circuitry necessary for self calibration.

The receivers include ADCs and adjustable sample rates that produce data streams from the received signals. The signals can be conditioned further by a series of decimation filters and a programmable FIR filter with additional decimation settings. The sample rate of each digital filter block is adjustable by changing decimation factors to produce the desired output data rate.

### OBSERVATION RECEIVER

The ADRV9009 contains an independent DPD observation receiver front end with two multiplexed inputs and a common digital back end that is shared with the traffic receiver. This configuration enables an efficient shared receiver and observation receiver mode where the device can support fast switching between receiver and observation receiver mode in TDD applications. The observation receiver shares the common frequency synthesizer with the transmitter.

The observation receiver is a direct conversion system that contains a programmable attenuator stage, followed by matched I and Q mixers, baseband filters, and ADCs.

The continuous time  $\Sigma$ - $\Delta$  ADCs have inherent antialiasing that reduces the RF filtering requirement.

The ADC outputs can be conditioned further by a series of decimation filters and a programmable FIR filter with additional decimation settings. The sample rate of each digital filter block is adjustable by changing decimation factors to produce the desired output data rate.

### CLOCK INPUT

The ADRV9009 requires a differential clock connected to the REF\_CLK\_IN± pins. The frequency of the clock input must be between 10 MHz and 1000 MHz and must have very low phase noise because this signal generates the RF LO and internal sampling clocks.

### SYNTHESIZERS

#### RF PLL

The ADRV9009 contains a fractional-N PLL to generate the RF LO for the signal paths. The PLL incorporates an internal VCO and loop filter, requiring no external components. The LOs on multiple chips can be phase synchronized to support active antenna systems and beamforming applications.

#### Clock PLL

The ADRV9009 contains a PLL synthesizer that generates all the baseband related clock signals and serialization/deserialization (SERDES) clocks. This PLL is programmed based on the data rate and sample rate requirements of the system.

## SPI

The ADRV9009 uses an SPI interface to communicate with the BBP. This interface can be configured as a 4-wire interface with dedicated receiver and transmitter ports, or the interface can be configured as a 3-wire interface with a bidirectional data communications port. This bus allows the BBP to set all device control parameters using a simple address data serial bus protocol.

Write commands follow a 24-bit format. The first five bits set the bus direction and the number of bytes to transfer. The next 11 bits set the address where data is written. The final 8 bits are the data to be transferred to the specific register address.

Read commands follow a similar format with the exception that the first 16 bits are transferred on the SDIO pin and the final eight bits are read from the ADRV9009, either on the SDO pin in 4-wire mode or on the SDIO pin in 3-wire mode.

## JTAG BOUNDARY SCAN

The ADRV9009 provides support for JTAG boundary scan. Five dual function pins are associated with the JTAG interface. Use these pins, listed in Table 5, to access the on-chip test access port. To enable the JTAG functionality, set the GPIO\_3 pin through the GPIO\_0 pin to 1001, and then pull the TEST pin high.

## POWER SUPPLY SEQUENCE

The ADRV9009 requires a specific power-up sequence to avoid undesired power-up currents. In the optimal power-up sequence, the VDDD1P3\_DIG and the VDDA1P3 supplies (VDDA1P3 includes all 1.3 V domains) power up first and at the same time. If these supplies cannot be powered up simultaneously, the VDDD1P3\_DIG supply must power up first. Power up the VDDA\_3P3, VDDA1P8\_BB, VDDA1P8\_TX, VDDA1P3\_DES, and VDDA1P3\_SER supplies after the 1.3 V supplies. The VDD\_INTERFACE supply can be powered up at any time. Note that no device damage occurs if this sequence is not followed. However, failure to follow this sequence may result in higher than expected power-up currents. It is also recommended to toggle the RESET signal after power stabilizes, prior to configuration. The power-down sequence is not critical. If a power-down sequence is followed, remove the VDDD1P3\_DIG supply last to avoid any back biasing of the digital control lines.

## GPIO\_x PINS

The ADRV9009 provides 19, 1.8 V to 2.5 V GPIO signals that can be configured for numerous functions. When configured as outputs, certain pins can provide real-time signal information to the BBP, allowing the BBP to determine observation receiver

performance. A pointer register selects the information that is output to these pins. Signals used for manual gain mode, calibration flags, state machine states, and various observation receiver parameters are among the outputs that can be monitored on these pins. Additionally, certain pins can be configured as inputs and used for various functions, such as setting the observation receiver gain in real time.

Twelve 3.3 V GPIO\_x pins are also included on the device. These pins provide control signals to external components.

## AUXILIARY CONVERTERS

### AUXADC\_x

The ADRV9009 contains an auxiliary ADC that is multiplexed to four input pins (AUXADC\_x). The auxiliary ADC is 12 bits with an input voltage range of 0.05 V to VDDA\_3P3 – 0.05 V. When enabled, the auxiliary ADC is free running. The SPI reads provide the last value latched at the ADC output. The auxiliary ADC can also be multiplexed to a built in, diode-based temperature sensor.

### Auxiliary DAC x

The ADRV9009 contains 10 identical auxiliary DACs (auxiliary DAC x) that can be used for bias or other system functionality. The auxiliary DACs are 10 bits, have an output voltage range of approximately 0.7 V to VDDA\_3P3 – 0.3 V, and have an output drive of 10 mA.

## JESD204B DATA INTERFACE

The digital data interface for the ADRV9009 uses JEDEC JESD204B Subclass 1. The serial interface operates at speeds of up to 12.288 Gbps. The benefits of the JESD204B interface include a reduction in required board area for data interface routing, resulting in smaller total system size. Four high speed serial lanes are provided for the transmitter and four high speed lanes are provided for the observation receiver. The ADRV9009 supports single-lane or dual-lane interfaces as well as fixed and floating point data formats for observation receiver data.

Table 6. Observation Path Interface Rates

| Bandwidth (MHz) | Output Rate (MSPS) | JESD204B         |                 |
|-----------------|--------------------|------------------|-----------------|
|                 |                    | Lane Rate (Mbps) | Number of Lanes |
| 200             | 245.76             | 9830.4           | 1               |
| 200             | 307.2              | 12288            | 1               |
| 250             | 307.2              | 12288            | 1               |
| 450             | 491.52             | 9830.4           | 2               |
| 450             | 491.52             | 4915.2           | 4               |

Table 7. Example Transmitter Interface Rates (Other Input Rates, Bandwidth, and JESD204B Lanes Also Supported)

| Bandwidth (MHz) | Input Rate (MSPS) | Single-Channel Operation  |                          | Dual-Channel Operation    |                          |
|-----------------|-------------------|---------------------------|--------------------------|---------------------------|--------------------------|
|                 |                   | JESD204B Lane Rate (Mbps) | JESD204B Number of Lanes | JESD204B Lane Rate (Mbps) | JESD204B Number of Lanes |
| 200             | 245.76            | 9830.4                    | 1                        | 9830.4                    | 2                        |
| 200             | 307.2             | 12288                     | 1                        | 12288                     | 2                        |
| 250             | 307.2             | 12288                     | 1                        | 12288                     | 2                        |
| 450             | 491.52            | 9830.4                    | 2                        | 9830.4                    | 4                        |

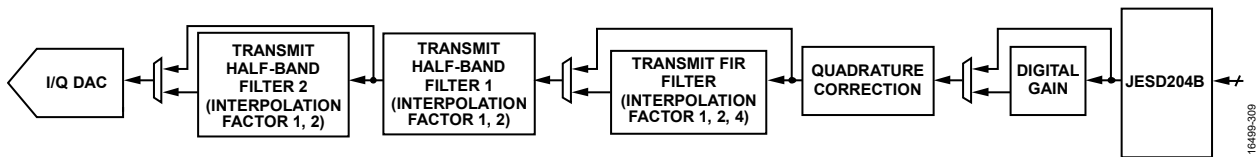


Figure 430. Transmitter Datapath Filter Implementation

Table 8. Example Receiver Interface Rates (Other Output Rates, Bandwidth, and JESD204B Lanes Also Supported)

| Bandwidth (MHz) | Output Rate (MSPS) | Single-Channel Operation  |                          | Dual-Channel Operation    |                          |
|-----------------|--------------------|---------------------------|--------------------------|---------------------------|--------------------------|
|                 |                    | JESD204B Lane Rate (Mbps) | JESD204B Number of Lanes | JESD204B Lane Rate (Mbps) | JESD204B Number of Lanes |
| 80              | 122.88             | 4915.2                    | 1                        | 9830.4                    | 1                        |
| 100             | 153.6              | 6144                      | 1                        | 12288                     | 1                        |
| 100             | 245.76             | 9830.4                    | 1                        | 9830.4                    | 2                        |
| 200             | 245.76             | 9830.4                    | 1                        | 9830.4                    | 2                        |
| 200             | 245.76             | 4915.2                    | 2                        | 4915.2                    | 4                        |

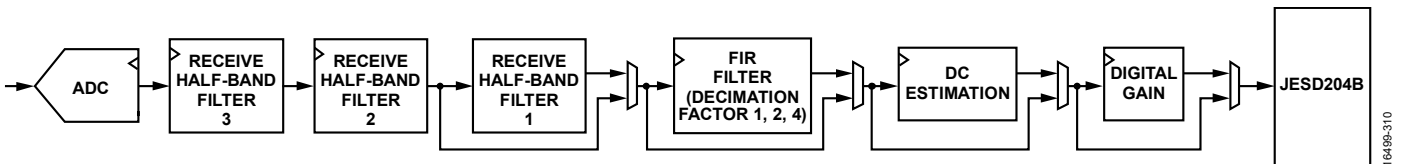


Figure 431. Receiver and Observation Receiver Datapath Filter Implementation

# APPLICATIONS INFORMATION

## PCB LAYOUT AND POWER SUPPLY RECOMMENDATIONS

### Overview

The ADRV9009 device is a highly integrated RF agile transceiver with significant signal conditioning integrated on one chip. Due to the increased complexity of the device and its high pin count, careful PCB layout is important to get the optimal performance. This data sheet provides a checklist of issues to look for and guidelines on how to optimize the PCB to mitigate performance issues. The goal of this data sheet is to help achieve the optimal performance from the ADRV9009 while reducing board layout effort. This data sheet assumes that the user is an experienced analog and RF engineer with an understanding of RF PCB layout and RF transmission lines. This data sheet discusses the following issues and provides guidelines for system designers to achieve the optimal performance for the ADRV9009:

- PCB material and stack up selection
- Fanout and trace space layout guidelines
- Component placement and routing guidelines
- RF and JESD204B transmission line layout
- Isolation techniques used on the [ADRV9009-W/PCBZ](#)
- Power management considerations
- Unused pin instructions

### PCB MATERIAL AND STACKUP SELECTION

Figure 432 shows the PCB stackup used for the [ADRV9009-W/PCBZ](#). Table 9 and Table 10 list the single-ended and differential impedance for the stackup shown in Figure 432. The dielectric material used on the top and the bottom layers is 8 mil Rogers 4003C. The remaining dielectric layers are FR4-370 HR. The board design uses the Rogers laminate for the top layer and bottom layer for the low loss tangent at high frequencies. The ground planes under the Rogers laminate (Layer 2 and Layer 13) are the reference planes for the transmission lines routed on the outer surfaces. These layers are solid copper planes without any splits under the RF traces.

Layer 2 and Layer 13 are crucial to maintaining the RF signal integrity and, ultimately, the ADRV9009 performance. Layer 3 and Layer 12 route power supply domains. To keep the RF section of the ADRV9009 isolated from the fast transients of the digital section, the JESD204B interface lines are routed on Layer 5 and Layer 10. These layers have impedance control set to a 100 Ω differential. The remaining digital lines from the ADRV9009 are routed on Inner Layer 7 and Inner Layer 8. RF traces on the outer layers must be a controlled impedance to get the best performance from the device. The inner layers on this board use 0.5 ounce copper or 1 ounce copper. The outer layers use 1.5 ounce copper so the RF traces are less prone to peeling. Ground planes on this board are full copper floods with no splits except for vias, through-hole components, and isolation structures. The ground planes must route entirely to the edge of the PCB under the Surface-Mount Type A (SMA) connectors to maintain signal launch integrity. Power planes can be pulled back from the board edge to decrease the risk of shorting from the board edge.

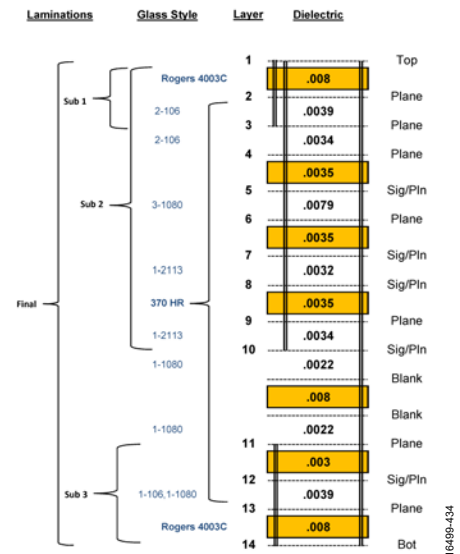


Figure 432. ADRV9009-W/PCBZ Trace Impedance and Stackup

Table 9. ADRV9009-W/PCBZ Single Ended Impedance and Stackup<sup>1</sup>

| Layer | Board Copper % | Starting Copper (oz.) | Finished Copper (oz.) | Single-Ended Impedance | Designed Trace Single-Ended (Inches) | Finished Trace Single-Ended (Inches) | Calculated Impedance (Ω) | Single-Ended Reference Layers |
|-------|----------------|-----------------------|-----------------------|------------------------|--------------------------------------|--------------------------------------|--------------------------|-------------------------------|
| 1     | N/A            | 0.5                   | 1.71                  | 50 Ω ±10%              | 0.0155                               | 0.0135                               | 49.97                    | 2                             |
| 2     | 65             | 1                     | 1                     | N/A                    | N/A                                  | N/A                                  | N/A                      | N/A                           |
| 3     | 50             | 0.5                   | 1                     | N/A                    | N/A                                  | N/A                                  | N/A                      | N/A                           |
| 4     | 65             | 1                     | 1                     | N/A                    | N/A                                  | N/A                                  | N/A                      | N/A                           |
| 5     | 50             | 0.5                   | 0.5                   | 50 Ω ±10%              | 0.0045                               | 0.0042                               | 49.79                    | 4, 6                          |
| 6     | 65             | 1                     | 1                     | N/A                    | N/A                                  | N/A                                  | N/A                      | N/A                           |
| 7     | 50             | 0.5                   | 0.5                   | 50 Ω ±10%              | 0.0049                               | 0.0039                               | 50.05                    | 6, 9                          |
| 8     | 50             | 0.5                   | 0.5                   | 50 Ω ±10%              | 0.0049                               | 0.0039                               | 50.05                    | 6, 9                          |
| 9     | 65             | 1                     | 1                     | N/A                    | N/A                                  | N/A                                  | N/A                      | N/A                           |
| 10    | 50             | 0.5                   | 1                     | 50 Ω ±10%              | 0.0045                               | 0.0039                               | 49.88                    | 9, 11                         |
| 11    | 65             | 0.5                   | 1                     | N/A                    | N/A                                  | N/A                                  | N/A                      | N/A                           |
| 12    | 50             | 1                     | 1                     | N/A                    | N/A                                  | N/A                                  | N/A                      | N/A                           |
| 13    | 65             | 1                     | 1                     | N/A                    | N/A                                  | N/A                                  | N/A                      | N/A                           |
| 14    | N/A            | 0.5                   | 1.64                  | 50 Ω ±10%              | 0.0155                               | 0.0135                               | 49.97                    | 13                            |

<sup>1</sup> N/A means not applicable.

Table 10. ADRV9009-W/PCBZ Differential Impedance and Stackup<sup>1</sup>

| Layer | Differential Impedance | Designed Trace Differential (Inches) | Designed Gap Differential (Inches) | Finished Trace (Inches) | Finished Gap Differential (Inches) | Calculated Impedance (Ω) | Differential Reference Layers |
|-------|------------------------|--------------------------------------|------------------------------------|-------------------------|------------------------------------|--------------------------|-------------------------------|
| 1     | 100 Ω ±10%             | 0.008                                | 0.006                              | 0.007                   | 0.007                              | 99.55                    | 2                             |
|       | 50 Ω ±10%              | 0.0032                               | 0.004                              | 0.0304                  | 0.0056                             | 50.11                    | 2                             |
| 2     | N/A                    | N/A                                  | N/A                                | N/A                     | N/A                                | N/A                      | N/A                           |
| 3     | N/A                    | N/A                                  | N/A                                | N/A                     | N/A                                | N/A                      | N/A                           |
| 4     | N/A                    | N/A                                  | N/A                                | N/A                     | N/A                                | N/A                      | N/A                           |
| 5     | 100 Ω ±10%             | 0.0036                               | 0.0064                             | 0.0034                  | 0.0065                             | 99.95                    | 4, 6                          |
| 6     | N/A                    | N/A                                  | N/A                                | N/A                     | N/A                                | N/A                      | N/A                           |
| 7     | 100 Ω ±10%             | 0.0036                               | 0.0064                             | 0.0034                  | 0.0066                             | 100.51                   | 6, 9                          |
| 8     | 100 Ω ±10%             | 0.0038                               | 0.0062                             | 0.0034                  | 0.0066                             | 100.51                   | 6, 9                          |
| 9     | N/A                    | N/A                                  | N/A                                | N/A                     | N/A                                | N/A                      | N/A                           |
| 10    | 100 Ω ±10%             | 0.0036                               | 0.0064                             | 0.003                   | 0.007                              | 100.80                   | 9, 11                         |
|       | N/A                    | N/A                                  | N/A                                | N/A                     | N/A                                | N/A                      | N/A                           |
|       | N/A                    | N/A                                  | N/A                                | N/A                     | N/A                                | N/A                      | N/A                           |
| 11    | N/A                    | N/A                                  | N/A                                | N/A                     | N/A                                | N/A                      | N/A                           |
| 12    | N/A                    | N/A                                  | N/A                                | N/A                     | N/A                                | N/A                      | N/A                           |
| 13    | 100 Ω ±10%             | 0.008                                | 0.006                              | 0.007                   | 0.007                              | 99.55                    | 13                            |
| 14    | 50 Ω ±10%              | 0.032                                | N/A                                | 0.004                   | N/A                                | 50.11                    | 13                            |

<sup>1</sup> N/A means not applicable.

**FANOUT AND TRACE SPACE GUIDELINES**

The ADRV9009 uses a 196-ball chip scale package ball grid array (CSP\_BGA), 12 mm × 12 mm package. The pitch between the pins is 0.8 mm. This small pitch makes it impractical to route all signals on a single layer. RF pins are placed on the outer edges of the ADRV9009 package. The location of the pins helps route the critical signals without a fanout via. Each digital signal is routed from the CSP\_BGA pad using a 4.5 mil trace. The trace is connected to the CSP\_BGA using a via in the pad structure. The signals are buried in the inner layers of the board for routing to other parts of the system.

The JESD204B interface signals are routed on two signal layers that use impedance control (Layer 5 and Layer 10). The spacing between the CSP\_BGA pads is 17.5 mil. After the signal is on the inner layers, a 3.6 mil trace (50 Ω) connects the JESD204B signal to the FPGA mezzanine card (FMC) connector. The recommended CSP\_BGA land pad size is 15 mil.

Figure 433 shows the fanout scheme of the [ADRV9009-W/PCBZ](#). Like the CSP\_BGA, the [ADRV9009-W/PCBZ](#) uses a via in the pad technique. This routing approach can be used for the ADRV9009 if there are no issues with manufacturing capabilities.

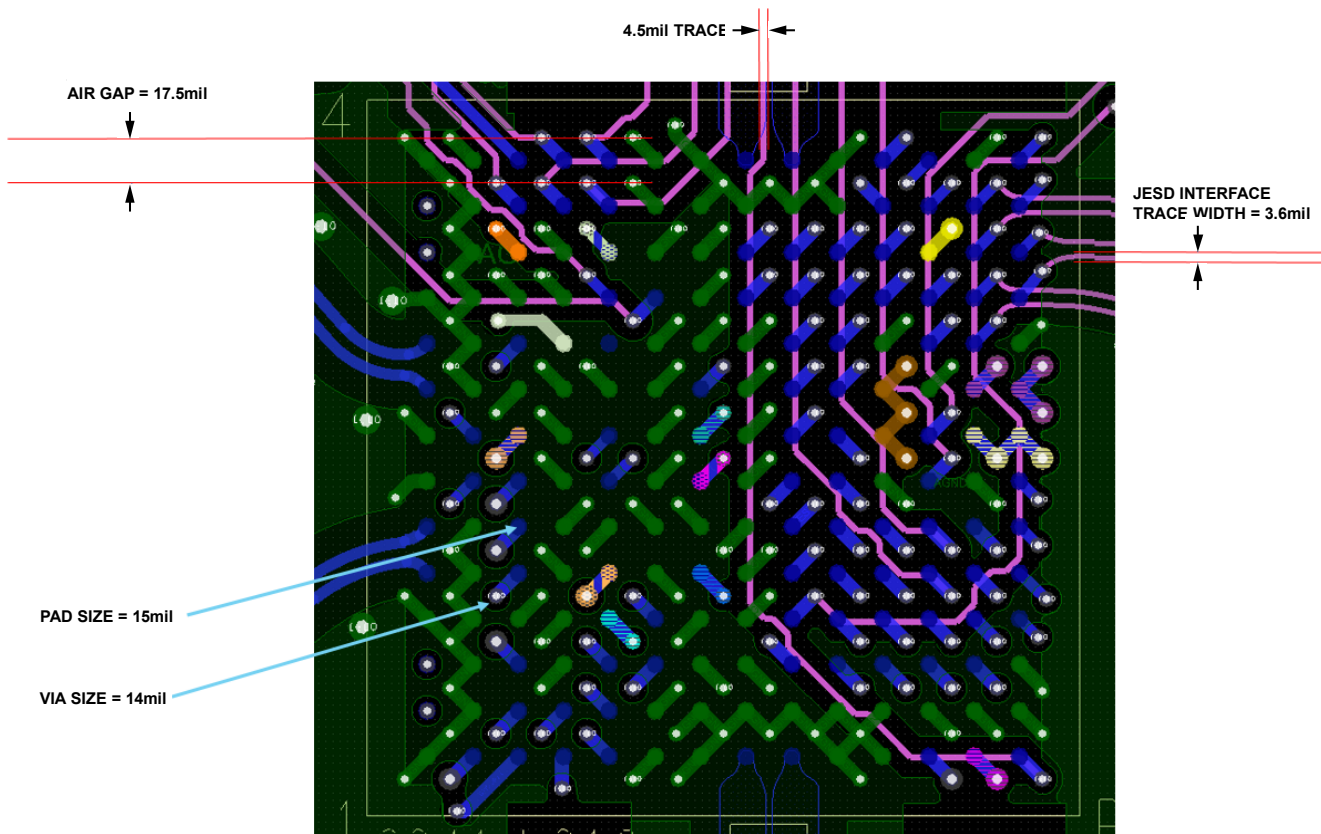


Figure 433. Trace Fanout Scheme on the [ADRV9009-W/PCBZ](#) (PCB Layer Top and Layer 5 Enabled)

16499-435

**COMPONENT PLACEMENT AND ROUTING GUIDELINES**

The ADRV9009 transceiver requires few external components to function, but those that are used require careful placement and routing to optimize performance. This section provides a checklist for properly placing and routing critical signals and components.

**Signals with Highest Routing Priority**

RF lines and JESD204B interface signals are the signals that are most critical and must be routed with the highest priority.

Figure 434 shows the general directions in which each of the signals must be routed so that they can be properly isolated from noisy signals.

The observation receiver and transmitter baluns and the matching circuits affect the overall RF performance of the

ADRV9009 transceiver. Make every effort to optimize the component selection and placement to avoid performance degradation. The RF Routing Guidelines section describes proper matching circuit placement and routing in more detail. Refer to the RF Port Interface Information section for more information.

To achieve the desired level of isolation between RF signal paths, use the technique described in the Isolation Techniques Used on the ADRV9009-W/PCBZ section in customer designs.

Install a 10  $\mu$ F capacitor near the transmitter balun(s) VDDA1P8\_TX dc feed(s) for RF transmitter outputs. The capacitor acts as a reservoir for the transmitter supply current. The Transmitter Balun DC Feed Supplies section discusses more details about the transmitter output power supply configuration.

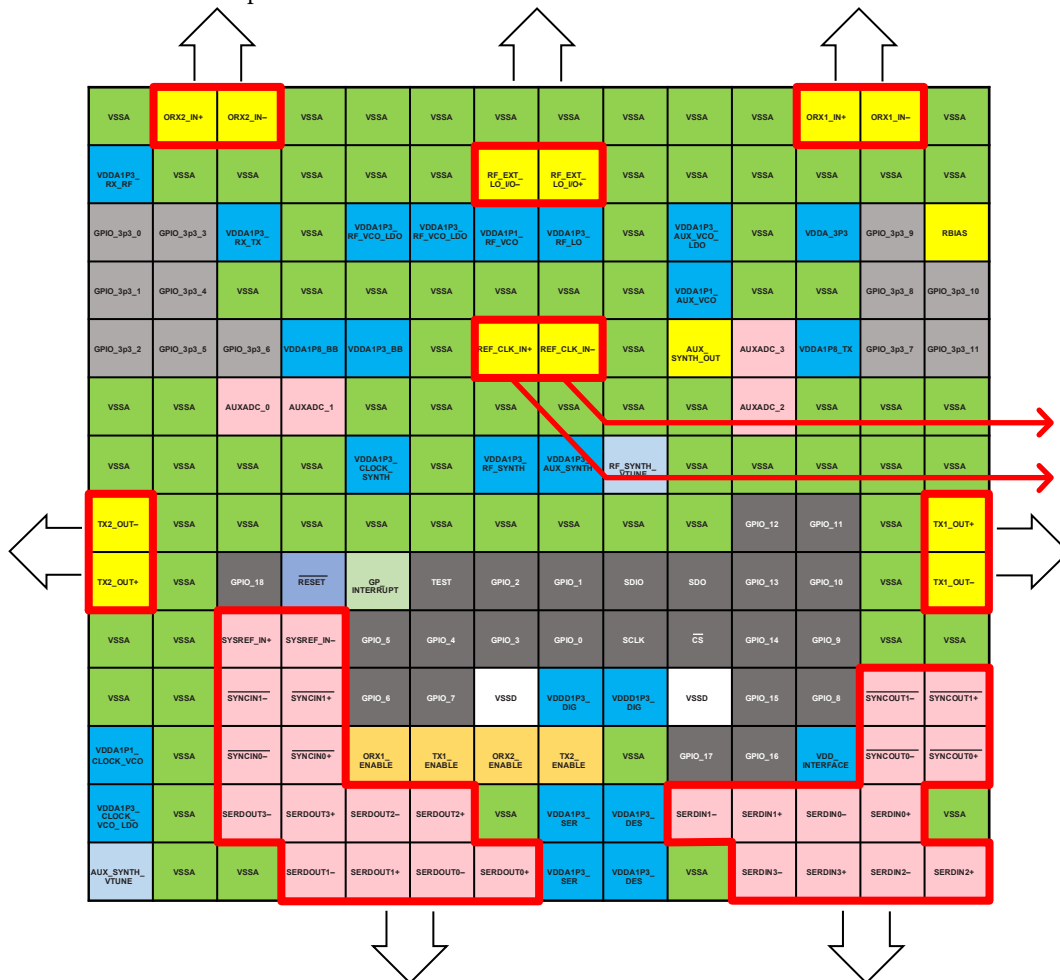


Figure 434. RF Input/Output, REF\_CLK\_IN±, and JESD204B Signal Routing Guidelines

16495-436



Figure 435 shows placement for ac coupling capacitors and a 100  $\Omega$  termination resistor near the REF\_CLK\_IN $\pm$  pins. Shield the traces with ground flooding that is surrounded with vias staggered along the edge of the trace pair. The trace pair creates a shielded channel that shields the reference clock from any interference from other signals. Refer to the [ADRV9009-W/PCBZ](#) layout, including board support files included with the evaluation board software, for exact details.

Route the JESD204B interface at the beginning of the PCB design and with the same priority as the RF signals. The RF Routing Guidelines section outlines recommendations for

JESD204B interface routing. Provide appropriate isolation between interface differential pairs. The Isolation Between JESD204B Lines section provides guidelines for optimizing isolation.

The RF\_EXT\_LO\_I/O- pin (B7) and the RF\_EXT\_LO\_I/O+ pin (B8) on the ADRV9009 are internally dc biased. If an external LO is used, connect the LO via ac coupling capacitors.

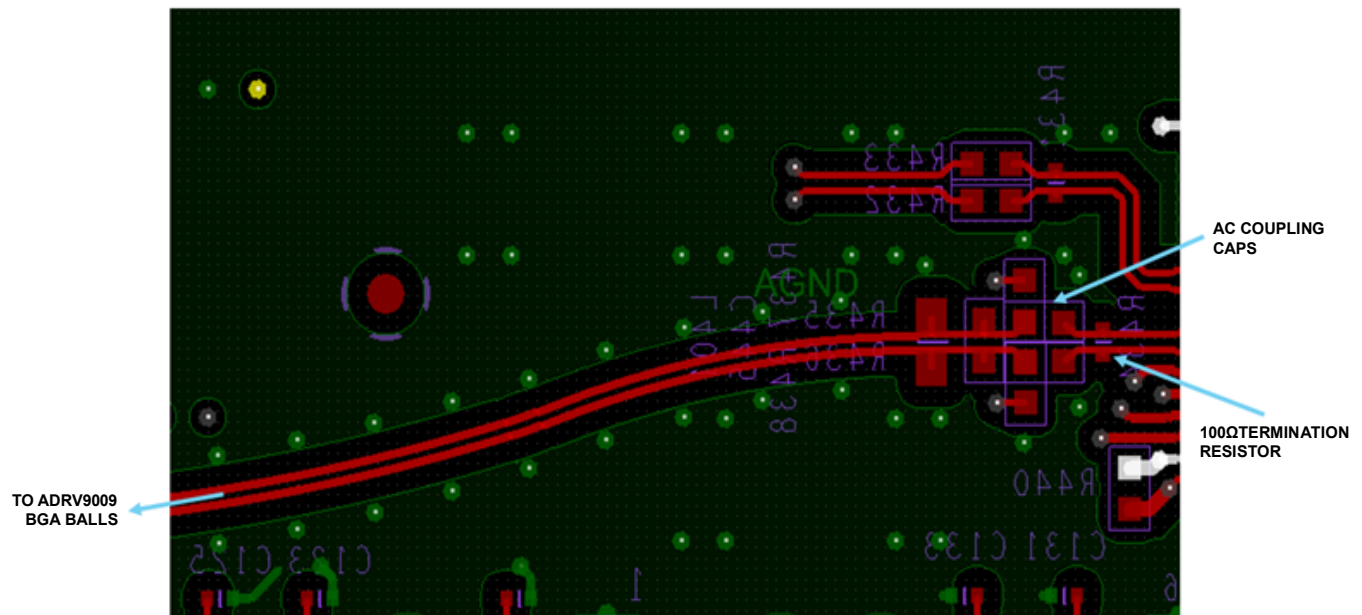


Figure 435. REF\_CLK\_IN $\pm$  Routing Recommendation



Each power supply pin requires a 0.1  $\mu$ F bypass capacitor near the pin at a minimum. Place the ground side of the bypass capacitor in a way so that ground currents flow away from other power pins and the bypass capacitors.

For the domains shown in Figure 437, like the domains powered through a 0  $\Omega$  placeholder resistor or FB, place the 0  $\Omega$  placeholder resistors or FBs further away from the device. Space 0  $\Omega$  placeholder resistors or FBs apart from each other to ensure that the electric fields on the FBs do not influence each other.

Figure 438 shows an example of how the FBs, reservoir capacitors, and decoupling capacitors are placed. It is

recommended to connect an FB between a power plane and the ADRV9009 at a distance away from the device (see Figure 438 for specific distances) The FB and the reservoir capacitor provide stable voltage for the ADRV9009 during operation by isolating the pin or pins that the network is connected to from the power plane. Then, shield that trace with ground and provide power to the power pins on the ADRV9009. Place a 100 nF capacitor near the power supply pin with the ground side of the bypass capacitor placed in a way so that ground currents flow away from other power pins and the bypass capacitors.

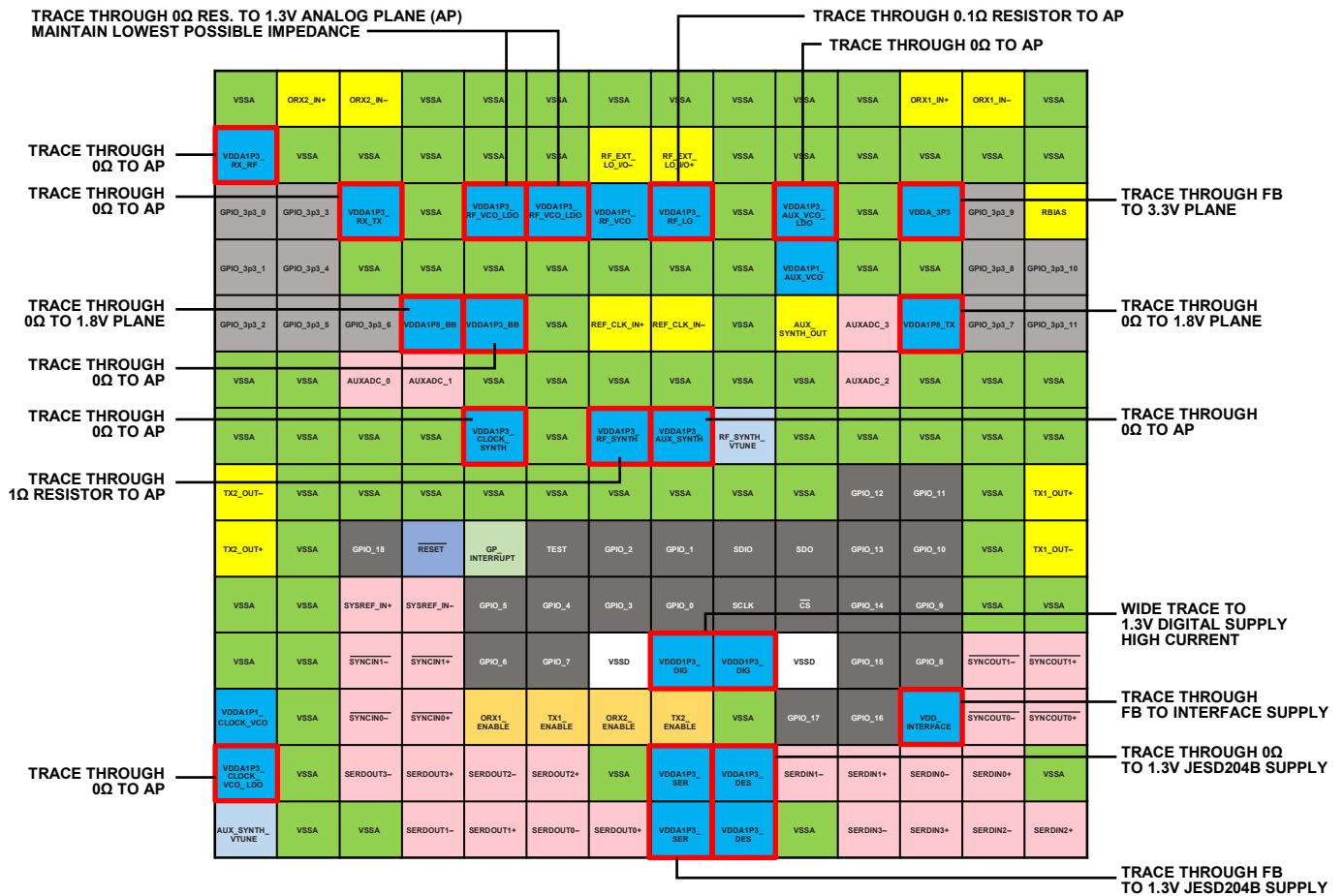


Figure 437. Power Supply Domains Interconnection Guidelines

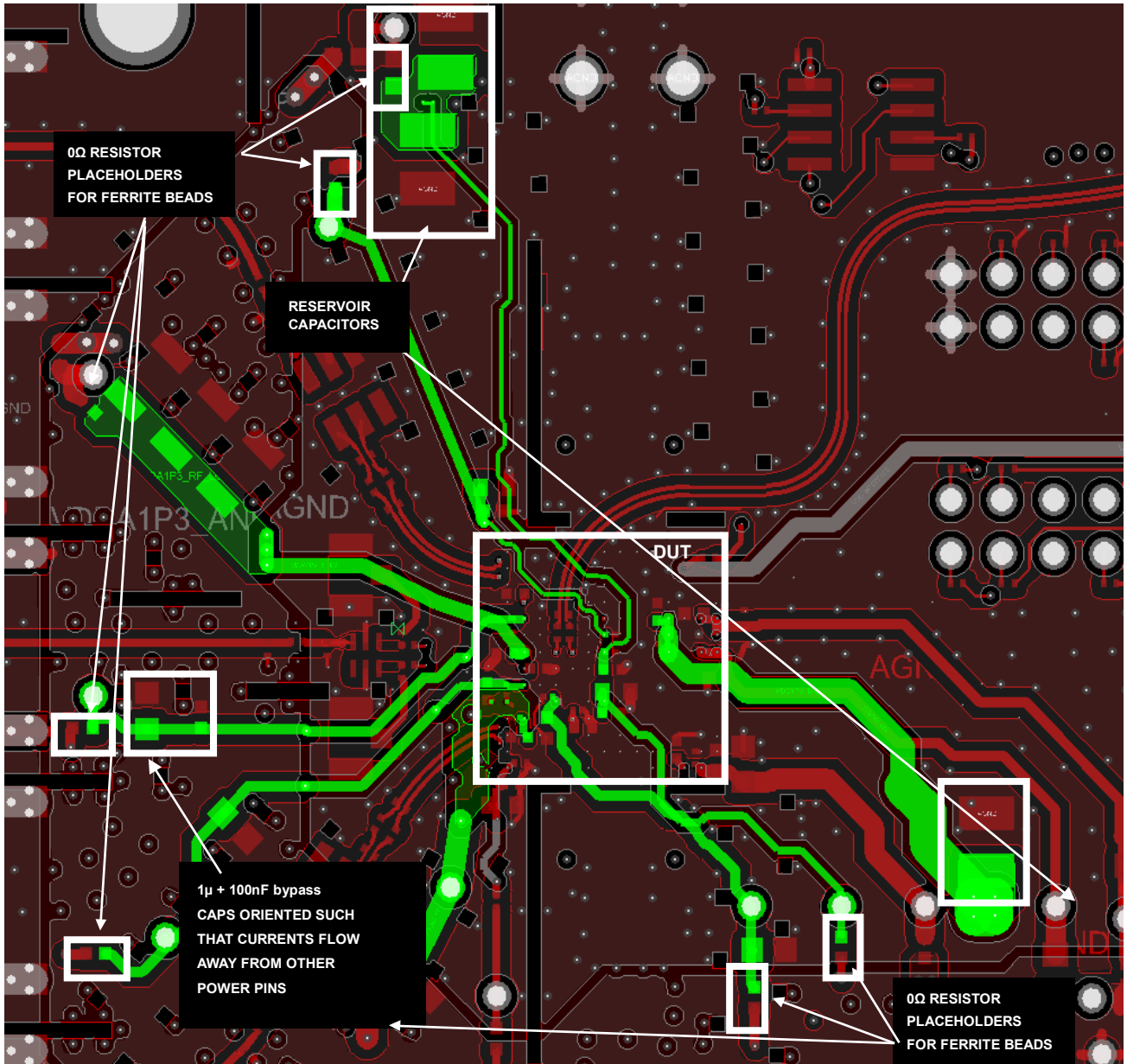


Figure 438. Placement Example of 0Ω Resistor Placeholders for FBs, Reservoir Capacitors, and Bypass Capacitors on the ADRV9009-W/PCBZ (Layer 12 to Power Layer and Bottom Layer)

**Signals with Lowest Routing Priority**

As a last step while designing the PCB layout, route signals shown in Figure 439. The following list outlines the recommended order of signal routing:

1. Use ceramic 1  $\mu$ F bypass capacitors at the VDDA1P1\_RF\_VCO pin, VDDA1P1\_AUX\_VCO pin, and VDDA1P1\_CLOCK\_VCO pin. Place them as close as possible to the ADRV9009 device with the ground side of the bypass capacitor placed in a way so that ground currents flow away from other power pins and the bypass capacitors, if possible.
2. Connect a 14.3 k $\Omega$  resistor to the RBIAS pin (C14). This resistor must have a 1% tolerance.
3. Pull the TEST pin (J6) to ground for normal operation. The device has support for JTAG boundary scan, and this pin is used to access that function. Refer to the JTAG Boundary Scan section for JTAG boundary scan information.
4. Pull the RESET pin (J4) high with a 10 k $\Omega$  resistor to VDD\_INTERFACE for normal operation. To reset the device, drive the RESET pin low.

When routing analog signals, such as GPIO\_3P3\_x/Auxiliary DAC x or AUXADC\_x, it is recommended to route them away from the digital section (Row H through Row P). Do not cross the analog section of the ADRV9009, highlighted by a red dotted line in Figure 439, by any digital signal routing.

When routing digital signals from Row H and below, it is important to route them away from the analog section (Row A through Row G). Do not cross the analog section of the ADRV9009, highlighted by a red dotted line in Figure 439, by any digital signal routing.

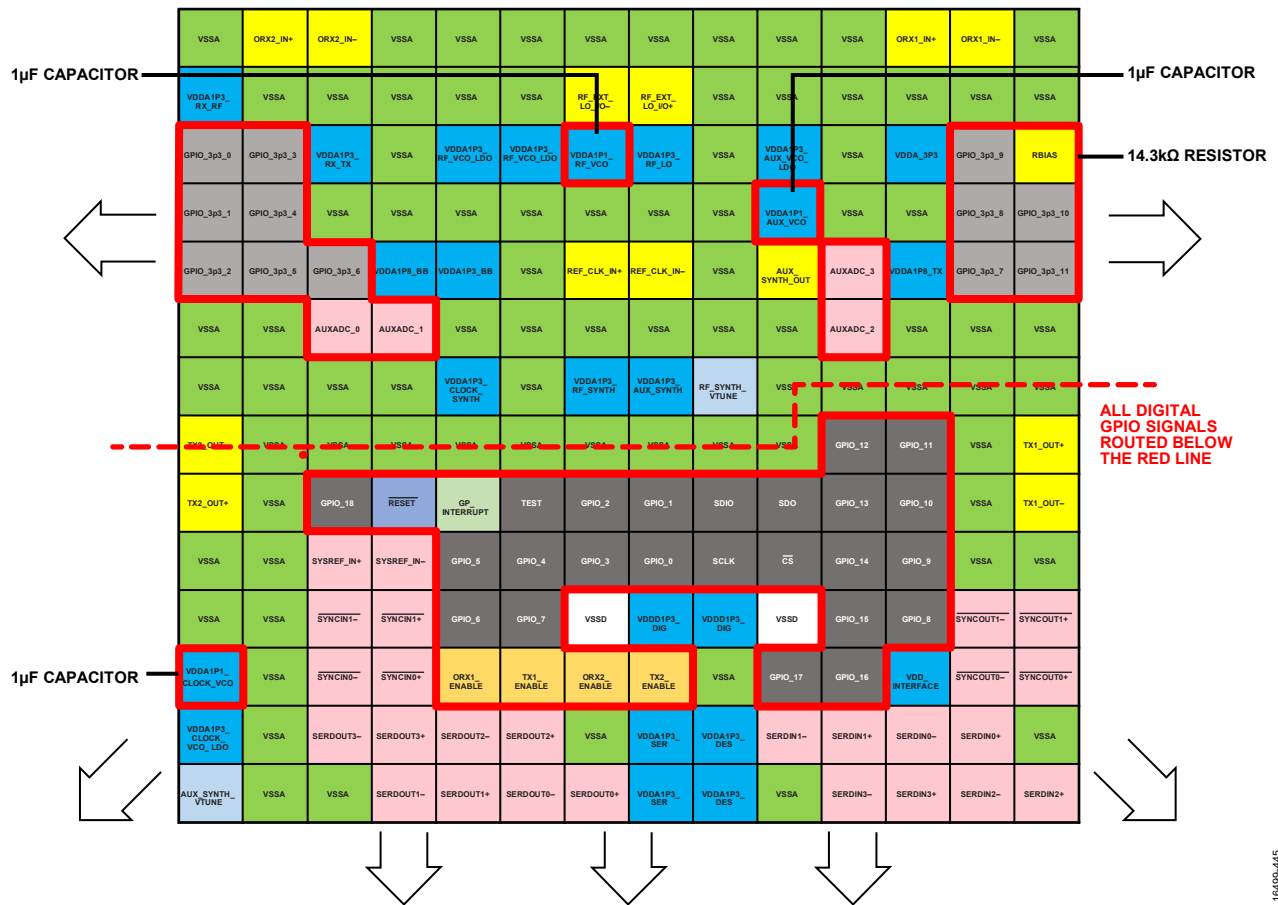


Figure 439. Auxiliary ADC, Analog, and Digital GPIO Signals Routing Guidelines

16499-445

**RF AND JESD204B TRANSMISSION LINE LAYOUT**

**RF Routing Guidelines**

The [ADRV9009-W/PCBZ](#) uses microstrip type lines for receiver, observation receiver, and transmitter RF traces. In general, it is not recommended to use any number of vias to route RF traces unless a direct line route is not possible. Differential lines from the balun to the receiver pins, observation receiver pins, and transmitter pins must be as short as possible. Also, make the length of the single-ended transmission line short to minimize the effects of parasitic coupling. These traces are the most critical when optimizing performance and are, therefore, routed before any other routing. These traces have the highest priority if trade-offs are needed.

Figure 440 and Figure 441 show pi matching networks on the single-ended side of the baluns. The observation receiver front

end is dc biased internally, so the differential side of the balun is ac-coupled. The system designer can optimize the RF performance with a proper selection of the balun, matching components, and ac coupling capacitors. The external LO traces and the REF\_CLK\_IN± traces may require matching components as well to ensure optimal performance.

All the RF signals mentioned previously must have a solid ground reference under each trace. Do not run any of the critical traces over a section of the reference plane that is discontinuous. The ground flood on the reference layer must extend all the way to the edge of the board. This flood length ensures signal integrity for the SMA launch when an edge launch connector is used.

Refer to the RF Port Interface Information section for more information on RF matching recommendations for the device.

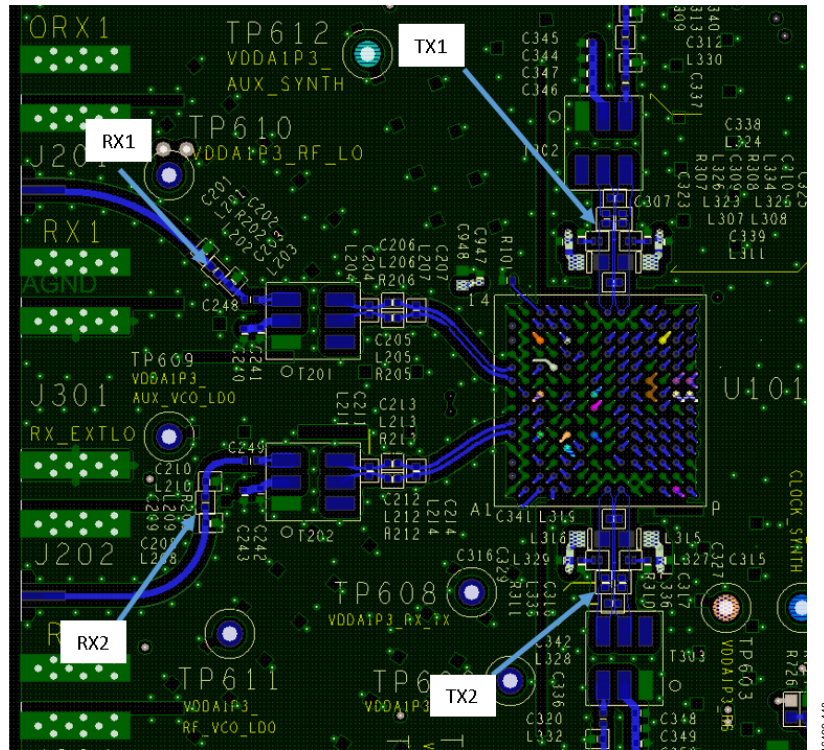
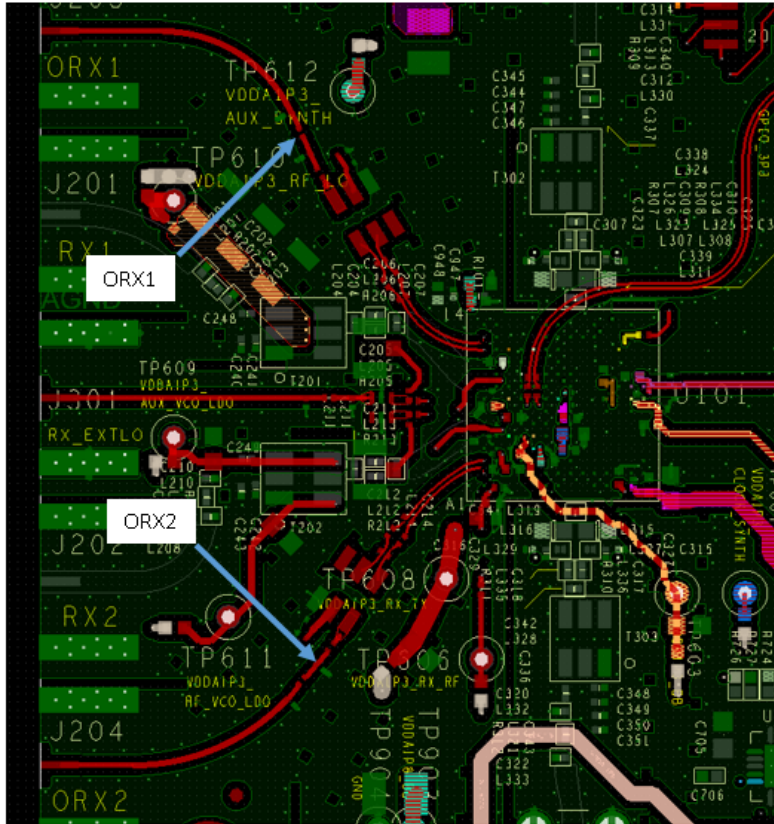


Figure 440. Pi Network Matching Components Available on Transmitter and Receiver



16498-449

Figure 441. Pi Network Matching Components Available on Observation Receiver Inputs

**Transmitter Balun DC Feed Supplies**

Each transmitter requires approximately 200 mA supplied through an external connection. On the [ADRV9008-2](#) and ADRV9009 evaluation boards, bias voltages are supplied at the dc feed of the baluns. Layout of both boards allows the use of external chokes to provide a 1.8 V power domain to the ADRV9009 outputs. This configuration is useful in scenarios where a balun used at the transmitter output is not capable of conducting the current necessary for the transmitter outputs to

operate. To reduce switching transients when attenuation settings change, power the balun dc feed or transmitter output chokes directly by the 1.8 V plane. Design the geometry of the 1.8 V plane so that each balun supply or each set of two chokes is isolated from the other. This geometry can affect transmitter to transmitter isolation. Figure 442 shows the layout configuration used on the [ADRV9009-W/PCBZ](#).

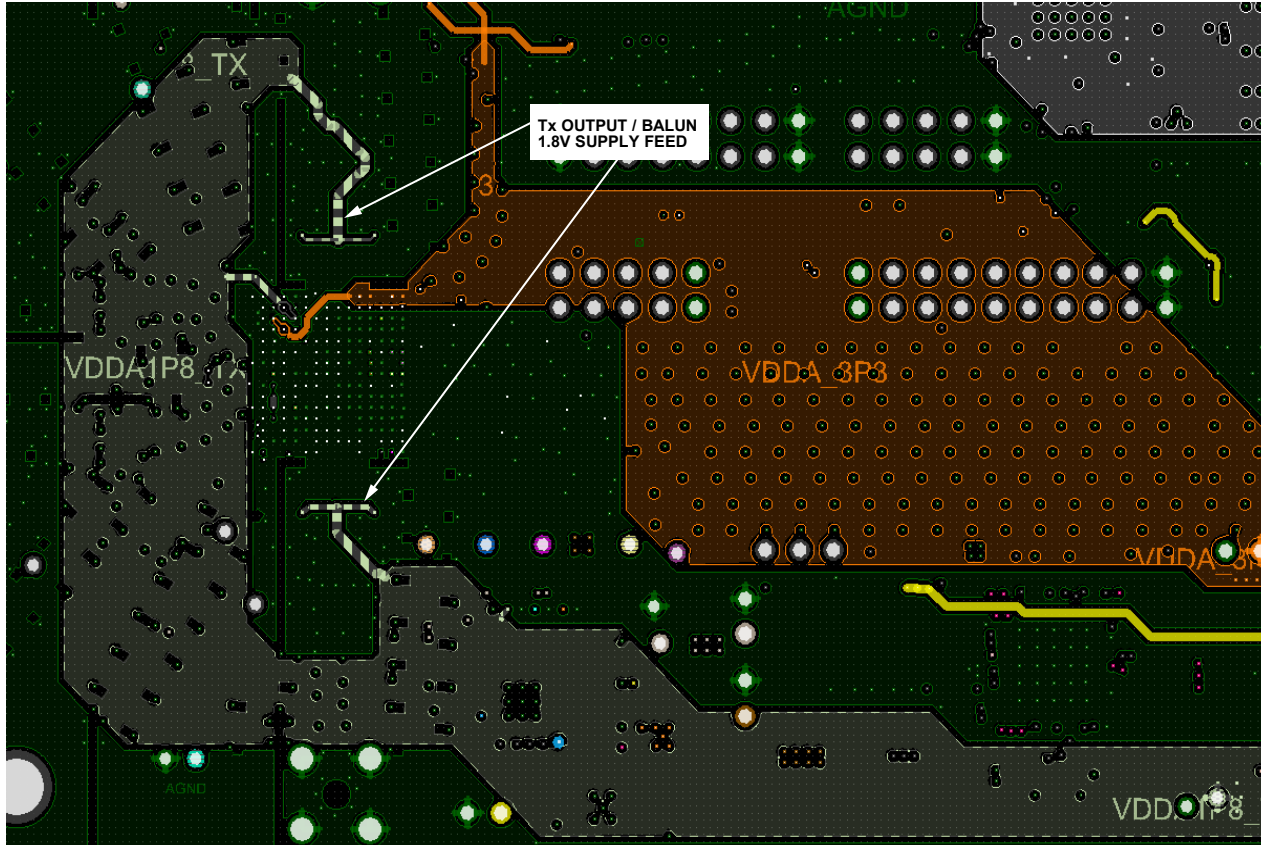


Figure 442. Transmitter Power Supply Planes (VDDA1P8\_TX) on the [ADRV9009-W/PCBZ](#)

16499-450



Both the positive and negative transmitter pins must be biased with 1.8 V. This biasing is accomplished on the evaluation board through chokes and decoupling capacitors, as shown in Figure 443. Match both chokes and their layout to avoid potential current spikes. A difference in parameters between both chokes can cause unwanted emission at transmitter outputs. Place the decoupling capacitors that are near the transmitter balun as close as possible to the dc feed of the balun or the ground pin. Make orientation of the capacitor perpendicular to the device so that the return current forms as small a loop as possible with the ground pins surrounding the transmitter input. A combination network of capacitors provides a wideband and low impedance ground path, eliminates transmitter spectrum spurs, and dampens the transients.



Figure 443. Transmitter DC Chokes and Balun Feed Supply

### JESD204B Trace Routing Recommendations

The ADRV9009 transceiver uses the JESD204B, high speed serial interface. To ensure optimal performance of this interface, keep the differential traces as short as possible by placing the ADRV9009 as close as possible to the FPGA or BBP, and route the traces directly between the devices. Use a PCB material with a low dielectric constant ( $<4$ ) to minimize loss. For distances greater than 6 inches, use a premium PCB material such as RO4350B or RO4003C.

### Routing Recommendations

Route the differential pairs on a single plane using a solid ground plane as a reference on the layers above and below these traces.

All JESD204B lane traces must be impedance controlled to achieve  $50\ \Omega$  to ground. It is recommended that the differential pair be coplanar and loosely coupled. An example of a typical configuration is a 5 mil trace width and 15 mil edge to edge spacing, with the trace width maximized, as shown in Figure 444.

Match trace widths with pin and ball widths while maintaining impedance control. If possible, use 1 oz. copper trace widths of at least 8 mil ( $200\ \mu\text{m}$ ). The coupling capacitor pad size must match JESD204B lane trace widths. If the trace width does not match the pad size, use a smooth transition between different widths.

The pad area for all connector and passive component choices must be minimized due to a capacitive plate effect that leads to problems with signal integrity.

Reference planes for impedance controlled signals must not be segmented or broken for the entire length of a trace.

The REF\_CLK\_IN $\pm$  signal trace and the SYSREF signal trace are impedance controlled for characteristic impedance ( $Z_0$ ) =  $50\ \Omega$ .

### Stripline Transmission Lines vs. Microstrip Transmission Lines

Stripline transmission lines have less signal loss and emit less electromagnetic interference than microstrip transmission lines. However, stripline transmission lines require the use of vias that add line inductance, increasing the difficulty of controlling the impedance.

Microstrip transmission lines are easier to implement if the component placement and density allow routing on the top layer. Microstrip transmission lines make controlling the impedance easier.

If the top layer of the PCB is used by other circuits or signals, or if the advantages of stripline transmission lines are more desirable than the advantages of microstrip transmission lines, implement the following recommendations:

- Minimize the number of vias.
- Use blind vias where possible to eliminate via stub effects, and use microvias to minimize via inductance.
- When using standard vias, use a maximum via length to minimize the stub size. For example, on an 8-layer board, use Layer 7 for the stripline pair.
- Place a pair of ground vias in proximity to each via pair to minimize the impedance discontinuity.

Route the JESD204B lines on the top side of the evaluation board as a differential 100 Ω pair (microstrip). For the [ADRV9009-W/PCBZ](#), the JESD204B differential signals are routed on the inner layers of the board (Layer 5 and Layer 10) as differential 100 Ω pairs (stripline). To minimize potential coupling, these signals are placed on an inner layer using a via embedded in the component footprint pad where the ball connects to the PCB. The ac coupling capacitors (100 nF) on these signals are placed near the connector and away from the chip to minimize coupling. The JESD204B interface can operate at frequencies of up to 12 GHz. Ensure that signal integrity from the chip to the connector is maintained.

**ISOLATION TECHNIQUES USED ON THE ADRV9009-W/PCBZ**

**Isolation Goals**

Significant isolation challenges were overcome in designing the [ADRV9009-W/PCBZ](#). The following isolation requirements accurately evaluate the ADRV9009 transceiver performance:

- Transmitter to transmitter: 75 dB out to 6 GHz
- Transmitter to receiver: 65 dB out to 6 GHz
- Receiver to receiver: 65 dB out to 6 GHz
- Transmitter to observation receiver: 65 dB out to 6 GHz

To meet these isolation goals with significant margin, isolation structures are introduced.

Figure 445 shows the isolation structures used on the [ADRV9009-W/PCBZ](#). These structures consist of a combination of slots and square apertures. These structures are present on every copper layer of the PCB stack. The advantage of using square apertures is that signals can be routed between the openings without affecting the isolation benefits of the array of apertures. When using these isolation structures, make sure to place ground vias around the slots and apertures.

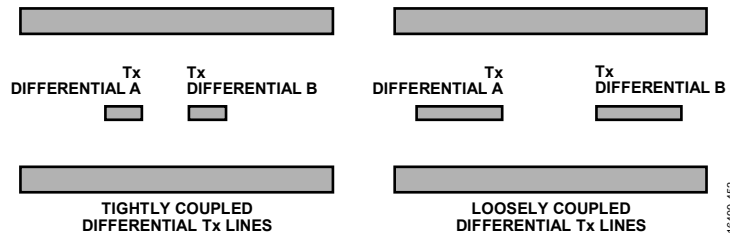


Figure 444. Routing JESD204B, Differential A and Differential B Correspond to Differential Positive Signals or Negative Signals (One Differential Pair)

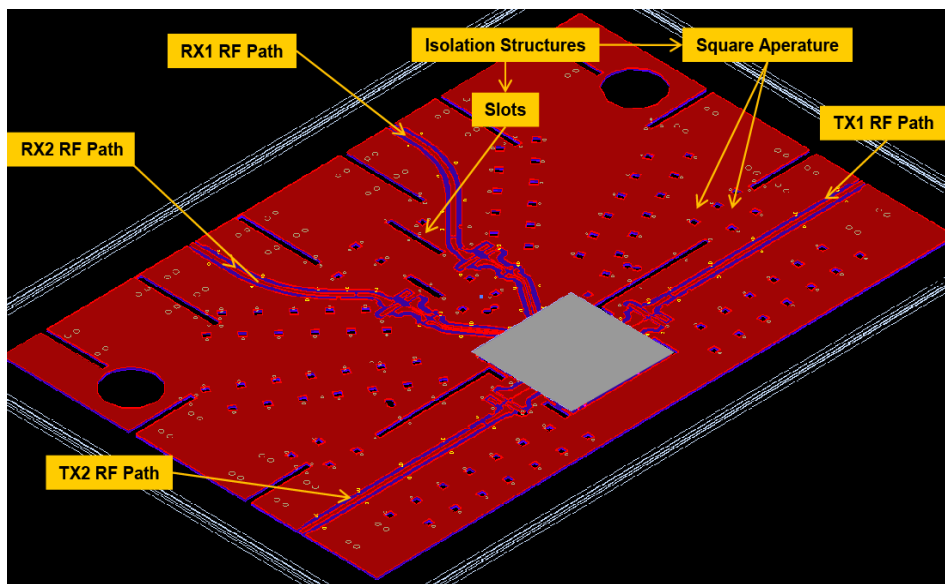


Figure 445. Isolation Structures on the [ADRV9009-W/PCBZ](#)

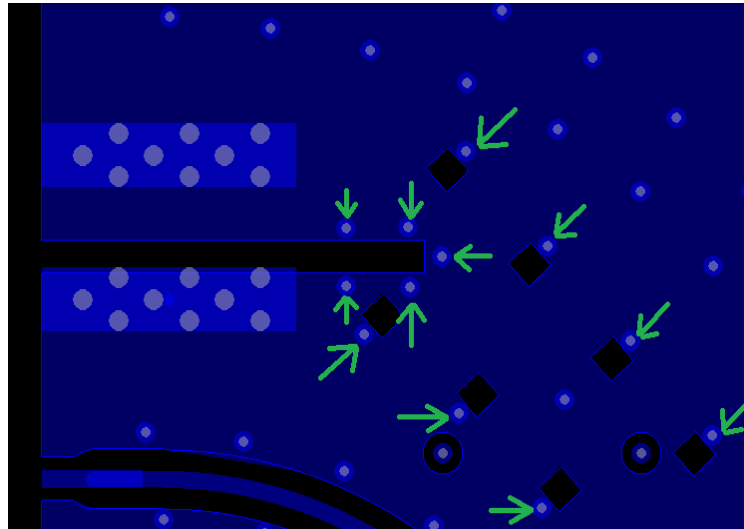


Figure 446. Current Steering Vias Placed Next to Isolation Structures

Figure 446 outlines the methodology used on the [ADRV9009-W/PCBZ](#). When using slots, ground vias must be placed at the ends of the slots and along the sides of the slots. When using square apertures, at least one single ground via must be placed adjacent to each square. These vias must be through-hole vias from the top layer to the bottom layer. The function of these vias is to steer return current to the ground planes near the apertures.

For accurate slot spacing and square apertures layout, use simulation software when designing a PCB for the ADRV9009 transceiver. Spacing between square apertures must be no more than 1/10 of a wavelength.

Calculate the wavelength using Equation 1:

$$\text{Wavelength}(m) = \frac{300}{\text{Frequency}(\text{MHz}) \times \sqrt{E_R}} \quad (1)$$

where  $E_R$  is the dielectric constant of the isolator material. For RO4003C material, microstrip structure (+ air),  $E_R = 2.8$ . For FR4-370HR material, stripline structure,  $E_R = 4.1$ .

For example, if the maximum RF signal frequency is 6 GHz, and  $E_R = 2.8$  for RO4003C material, microstrip structure (+ air), the minimum wavelength is approximately 29.8 mm.

To follow the 1/10 wavelength spacing rule, square aperture spacing must be 2.98 mm or less.

### Isolation Between JESD204B Lines

The JESD204B interface uses eight line pairs that can operate at speeds of up to 12 GHz. When configuring the PCB layout, ensure that these lines are routed according to the rules outlined in the JESD204B Trace Routing Recommendations section. In addition,

use isolation techniques to prevent crosstalk between different JESD204B lane pairs.

Figure 447 shows a technique used on the [ADRV9009-W/PCBZ](#) that involves via fencing. Placing ground vias around each JESD204B pair provides isolation and decreases crosstalk. The spacing between vias is 1.24 mm.

Figure 447 shows the rule provided in Equation 1. JESD204B lines are routed on Layer 5 and Layer 10 so that the lines use stripline structures. The dielectric material used in the inner layers of the [ADRV9009-W/PCBZ](#) PCB is FR4-370HR.

For accurate spacing of the JESD204B fencing via, use layout simulation software. Input the following data into Equation 1 to calculate the wavelength and square aperture spacing:

- The maximum JESD204B signal frequency is approximately 12 GHz.
- For FR4-370HR material, stripline structure,  $E_R = 4.1$ , the minimum wavelength is approximately 12.4 mm.

To follow the 1/10 wavelength spacing rule, spacing between vias must be 1.24 mm or less. The minimum spacing recommendation according to transmission line theory is 1/4 wavelength.

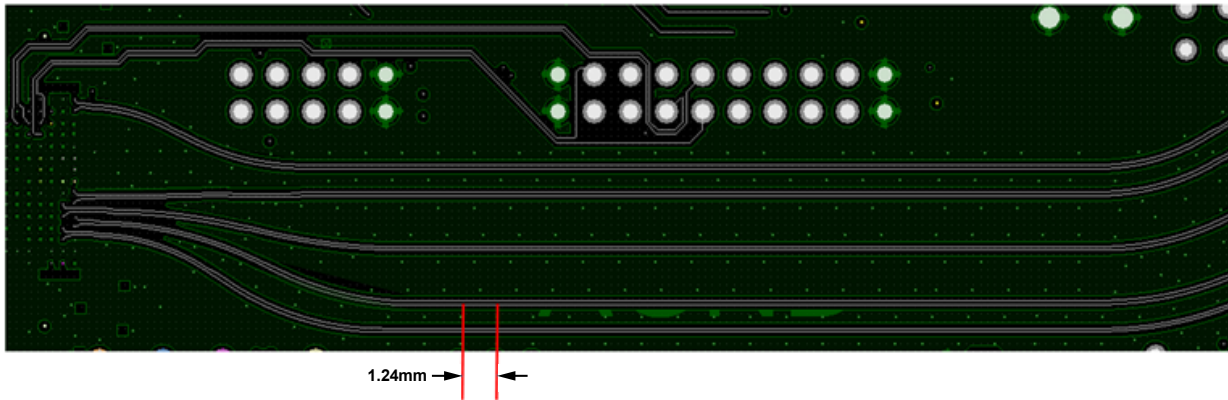


Figure 447. Via Fencing Around JESD204B Lines, PCB Layer 10

16499-455

## RF PORT INTERFACE INFORMATION

This section details the RF transmitter and receiver interfaces for optimal device performance. This section also includes data for the ADRV9009 RF port impedance values (see Figure 448 and Figure 449 for impedance values) and examples of impedance matching networks used in the evaluation platform. This section also provides information on board layout techniques and balun selection guidelines.

The ADRV9009 is a highly integrated transceiver with transmit, receive, and observation (DPD) receive signal chains. External impedance matching networks are required on the transmitter and receiver ports to achieve the performance levels indicated in this data sheet.

It is recommended to use simulation tools in the design and optimization of impedance matching networks. To achieve the closest match between computer simulated results and measured results, accurate models of the board environment, surface-mount device (SMD) components (including baluns and filters), and ADRV9009 port impedances are required.

## RF Port Impedance Data

This section provides the port impedance data for all transmitters and receivers in the ADRV9009 integrated transceiver. Note the following:

- $Z_o$  is defined as 50  $\Omega$ .
- The ADRV9009 ball pads are the reference plane for this data.
- Single-ended mode port impedance data is not available. However, a rough assessment is possible by taking the differential mode port impedance data and dividing both the real and imaginary components by 2.
- Contact Analog Devices applications engineering for the impedance data in Touchstone format.

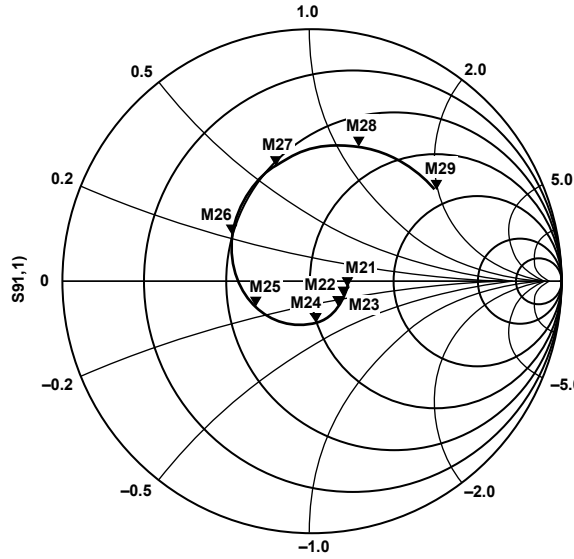
m21  
 FREQUENCY = 100MHz  
 $S(1,1) = 0.143/-7.865$   
 IMPEDANCE =  $66.439 - j2.654$

m22  
 FREQUENCY = 300MHz  
 $S(1,1) = 0.141/-25.589$   
 IMPEDANCE =  $64.063 - j7.987$

m23  
 FREQUENCY = 500MHz  
 $S(1,1) = 0.145/-42.661$   
 IMPEDANCE =  $60.623 - j12.201$

m24  
 FREQUENCY = 1GHz  
 $S(1,1) = 0.164/-84.046$   
 IMPEDANCE =  $49.000 + j16.447$

m25  
 FREQUENCY = 2GHz  
 $S(1,1) = 0.247/-155.186$   
 IMPEDANCE =  $31.131 - j6.860$



m26  
 FREQUENCY = 3GHz  
 $S(1,1) = 0.368/150.626$   
 IMPEDANCE =  $24.355 + j10.153$

m27  
 FREQUENCY = 4GHz  
 $S(1,1) = 0.484/107.379$   
 IMPEDANCE =  $25.118 + j30.329$

m28  
 FREQUENCY = 5GHz  
 $S(1,1) = 0.569/70.352$   
 IMPEDANCE =  $35.932 + j56.936$

m29  
 FREQUENCY = 6GHz  
 $S(1,1) = 0.614/36.074$   
 IMPEDANCE =  $81.032 + j94.014$

FREQUENCY (0.000Hz TO 6.000Hz)

Figure 448. Transmitter 1 and Transmitter 2 SEDZ and Parallel Equivalent Differential Impedance (PEDZ) Data

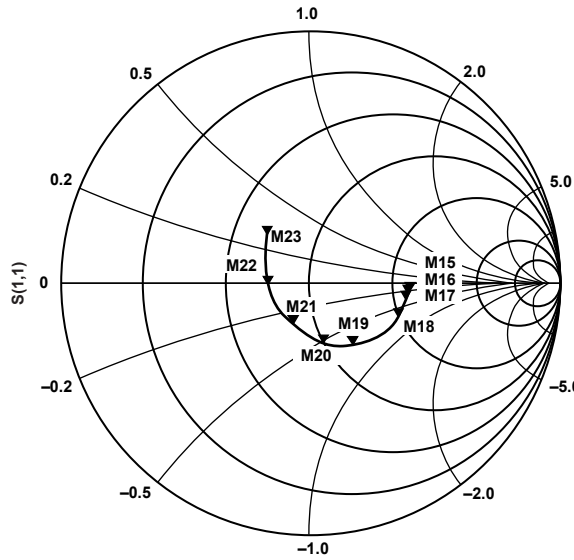
m15  
 FREQUENCY = 100MHz  
 $S(1,1) = 0.390/-1.819$   
 IMPEDANCE =  $113.933 - j3.331$

m16  
 FREQUENCY = 300MHz  
 $S(1,1) = 0.390/-5.495$   
 IMPEDANCE =  $112.803 - j9.931$

m17  
 FREQUENCY = 500MHz  
 $S(1,1) = 0.388/-9.198$   
 IMPEDANCE =  $110.398 - j16.107$

m18  
 FREQUENCY = 1GHz  
 $S(1,1) = 0.377/-18.643$   
 IMPEDANCE =  $100.377 - j28.250$

m19  
 FREQUENCY = 2GHz  
 $S(1,1) = 0.336/-39.123$   
 IMPEDANCE =  $74.966 - j35.800$



FREQUENCY (0Hz TO 6GHz)

Figure 449. Receiver 1 and Receiver 2 SEDZ and PEDZ Data

m20  
 FREQUENCY = 3GHz  
 $S(1,1) = 0.267/-64.650$   
 IMPEDANCE =  $55.102 - j28.685$

m21  
 FREQUENCY = 4GHz  
 $S(1,1) = 0.186/-104.336$   
 IMPEDANCE =  $42.821 - j16.026$

m22  
 FREQUENCY = 5GHz  
 $S(1,1) = 0.164/-173.106$   
 IMPEDANCE =  $35.977 - j1.455$

m23  
 FREQUENCY = 6GHz  
 $S(1,1) = 0.266/130.063$   
 IMPEDANCE =  $32.890 + j14.399$

16489-458

16489-459

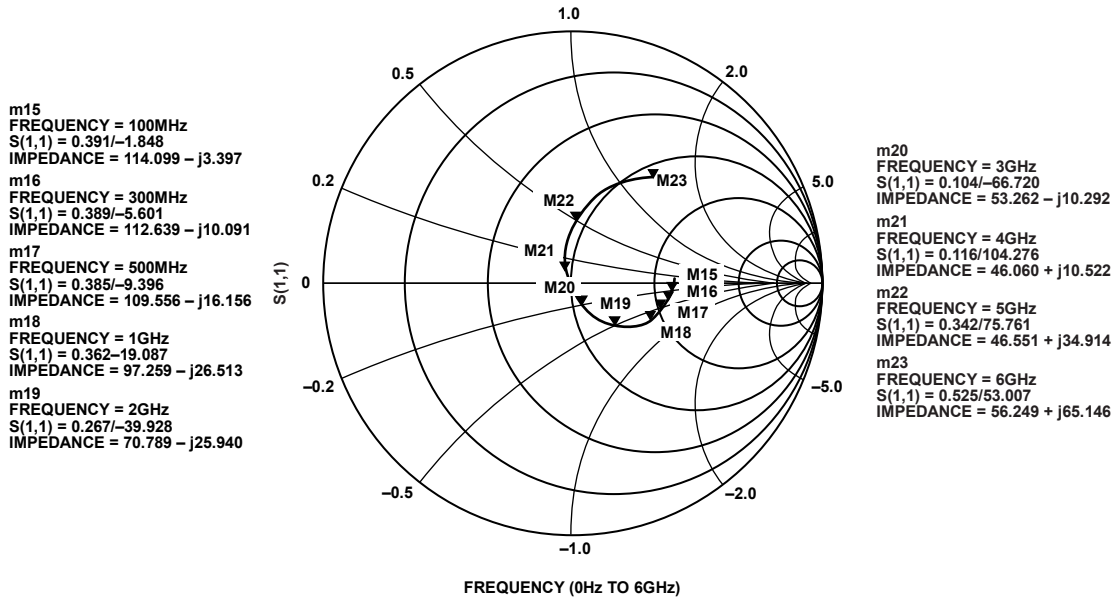


Figure 450. Observation Receiver 1 and Observation Receiver 2 SEDZ and PEDZ Data

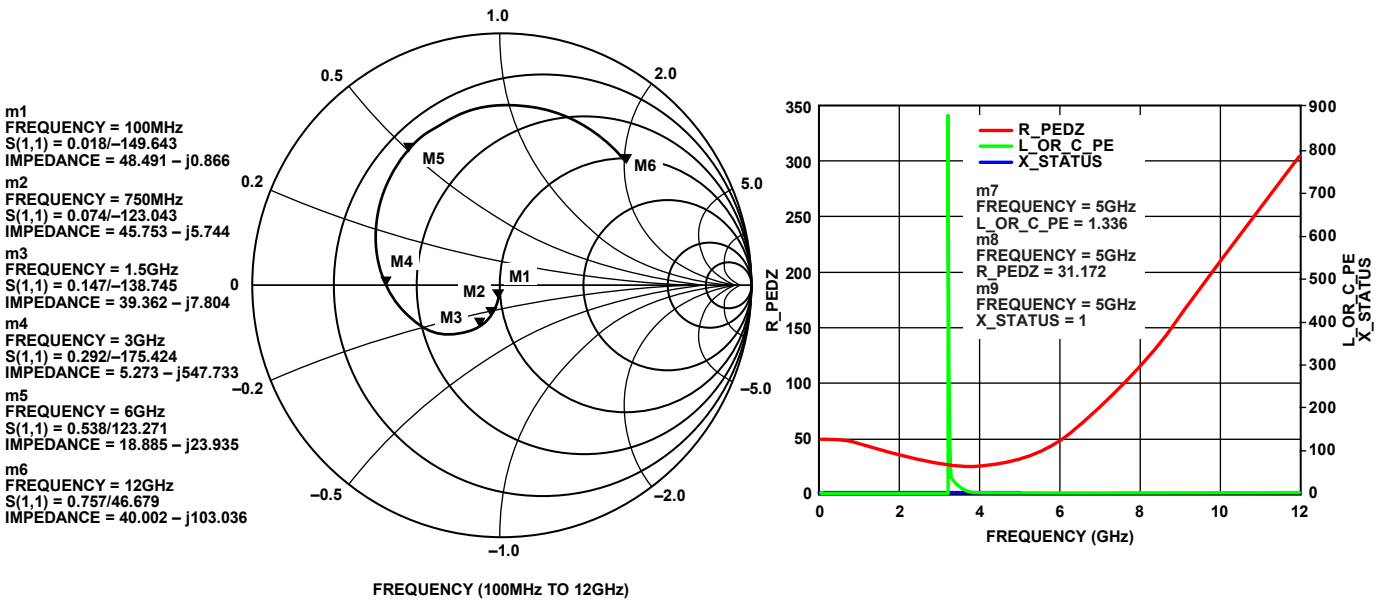


Figure 451. RF\_EXT\_LO\_I/O± SEDZ and PEDZ Data

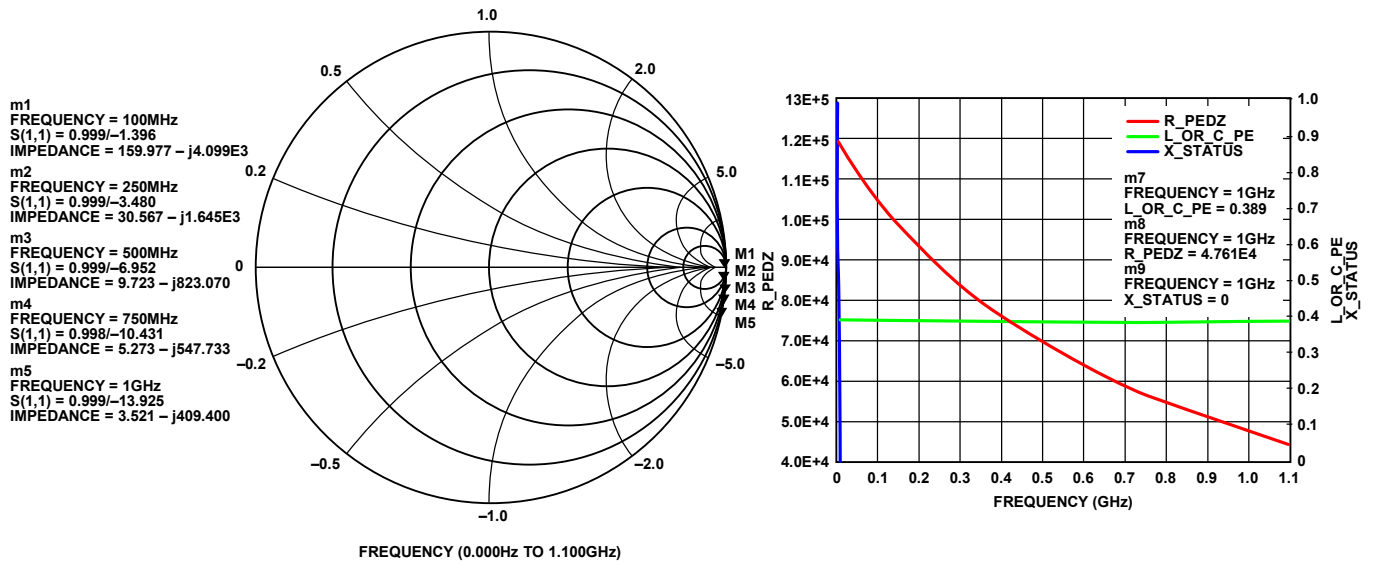


Figure 452. REF\_CLK\_IN± SEDZ and PEDZ Data, On Average, the Real Part of the Parallel Equivalent Differential Impedance ( $R_P$ ) = Approximately 70 kΩ

16489-462

**Advanced Design System (ADS) Setup Using the DataAccessComponent and SEDZ File**

Analog Devices supplies the port impedance as an **.s1p** file that can be downloaded from the ADRV9009 product page. This format allows simple interfacing to the ADS by using the DataAccessComponent. In Figure 453, Term 1 is the single-ended input or output, and Term 2 is the differential input or output RF port on the ADRV9009. The pi on the single-ended side and the differential pi configuration on the differential side allow maximum flexibility in designing matching circuits. The pi configuration is suggested for all design layouts because the pi configuration can step the impedance up or down as needed with appropriate component population.

Take the following steps to set up a simulation for impedance measurement and impedance matching:

1. The DataAccessComponent block reads the **rf port.s1p** file. This file is the device RF port reflection coefficient.
2. The two equations convert the RF port reflection coefficient to a complex impedance. The result is the RX\_SEDZ variable.
3. The RF port calculated complex impedance (RX\_SEDZ) defines the Term 2 impedance.
4. Term 2 is used in a differential mode, and Term 1 is used in a single-ended mode.

Setting up the simulation this way allows the user to measure the input reflection (S11), output reflection (S22), and through reflection (S21) of the three-port system without complex math operations within the display page.

For the highest accuracy, the electromagnetic momentum (EM) modeling result of the PCB artwork, S11, S22, and S21 of the matching components and balun must be used in the simulations.

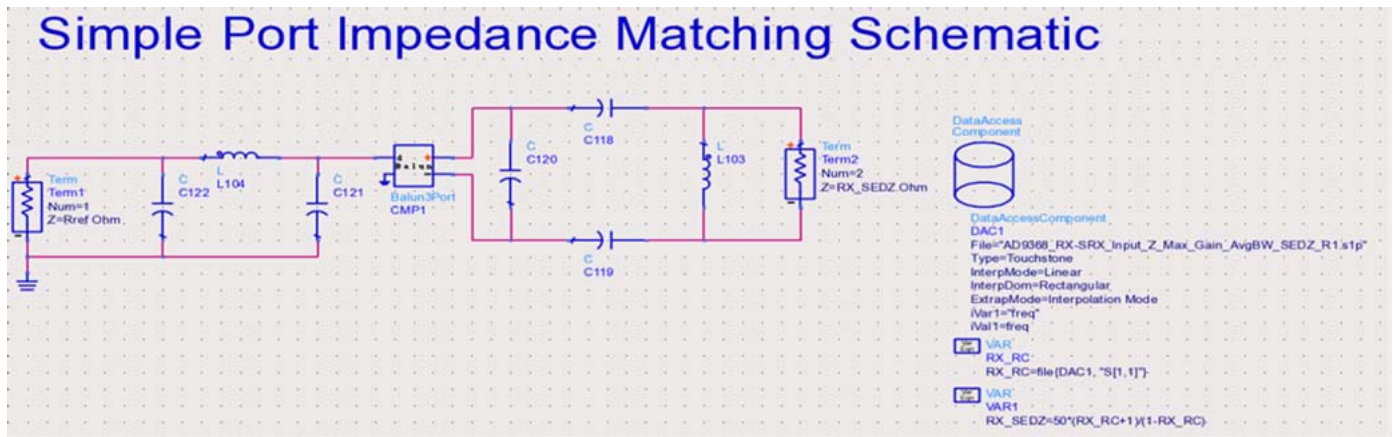


Figure 453. Simulation Setup in ADS with SEDZ .s1p Files and DataAccessComponent

Table 11. Sample Wire Wound DC Bias Choke Resistance vs. Size vs. Inductance

| Inductance (nH) | Resistance (Size: 0603) (Ω) | Resistance (Size: 1206) (Ω) |
|-----------------|-----------------------------|-----------------------------|
| 100             | 0.10                        | 0.08                        |
| 200             | 0.15                        | 0.10                        |
| 300             | 0.16                        | 0.12                        |
| 400             | 0.28                        | 0.14                        |
| 500             | 0.45                        | 0.15                        |
| 600             | 0.52                        | 0.20                        |



**Transmitter Bias and Port Interface**

This section considers the dc biasing of the ADRV9009 transmitter outputs and how to interface to each transmitter port. The ADRV9009 transmitters operate over a range of frequencies. At full output power, each differential output side draws approximately 100 mA of dc bias current. The transmitter outputs are dc biased to a 1.8 V supply voltage using either RF chokes (wire wound inductors) or a transformer center tap connection.

Careful design of the dc bias network is required to ensure optimal RF performance levels. When designing the dc bias network, select components with low dc resistance ( $R_{DCR}$ ) to minimize the voltage drop across the series parasitic resistance element with either of the suggested dc bias schemes suggested in Figure 454. The  $R_{DCR}$  resistors indicate the parasitic elements. As the impedance of the parasitics increases, the voltage drop ( $\Delta V$ ) across the parasitic element increases, which causes the transmitter RF performance ( $P_{O,1dB}$  and  $P_{O,MAX}$ , for example) to degrade. The choke inductance ( $L_C$ ) must be at least  $3\times$  higher than the load impedance at the lowest desired frequency so that the  $L_C$  does not degrade the output power (see Table 11).

The recommended dc bias network is shown in Figure 455. This network has fewer parasitics and fewer total components.

Figure 456 through Figure 459 show four basic differential transmitter output configurations. Except for cases in which impedance is already matched, impedance matching networks (balun single-ended port) are required to achieve optimum device performance from the device. In applications where the transmitter is not connected to another circuit that requires or can tolerate dc bias on the transmitter outputs, the transmitter outputs must be ac-coupled because of the dc bias voltage applied to the differential output lines of the transmitter.

The recommended RF transmitter interface, shown in Figure 454 to Figure 459, features a center tapped balun. This configuration offers the lowest component count of the options presented.

Descriptions of the transmitter port interface schemes are as follows:

- In Figure 456, the center tapped transformer passes the bias voltage directly to the transmitter outputs.
- In Figure 457, RF chokes bias the differential transmitter output lines. Additional coupling capacitors ( $C_C$ ) are added in the creation of a transmission line balun.
- In Figure 458, RF chokes bias the differential transmitter output lines and connect to a transformer.
- In Figure 459, RF chokes bias the differential output lines that are ac-coupled to the input of a driver amplifier.

If a transmitter balun that requires a set of external dc bias chokes is selected, careful planning is required. It is necessary to find the optimum compromise between the choke physical size, choke dc resistance, and the balun low frequency insertion loss. In commercially available dc bias chokes, resistance decreases as size increases. As choke inductance increases, resistance increases. It is undesirable to use physically small chokes with high inductance

because small chokes exhibit the greatest resistance. For example, the voltage drop of a 500 nH 0603 choke at 100 mA is roughly 50 mV.

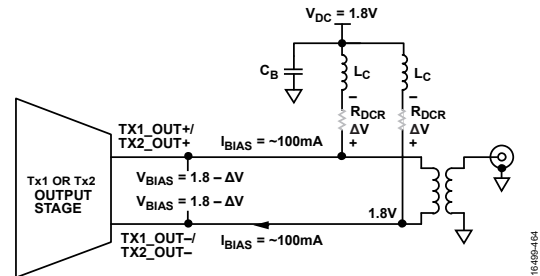


Figure 454. RF DC Bias Configurations Showing Parasitic Losses Due to Wire Wound Chokes

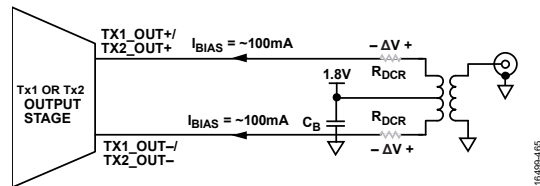


Figure 455. RF DC Bias Configurations Showing Parasitic Losses Due to Center Tapped Transformers

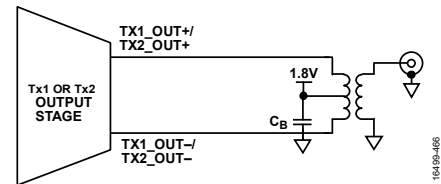


Figure 456. Using a Center Tapped Transformer

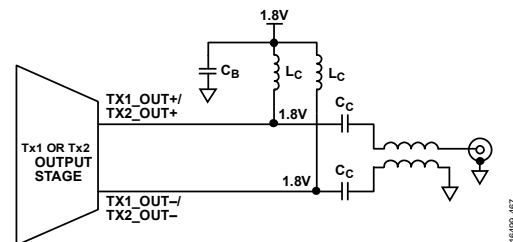


Figure 457. Using Bias Chokes and a Transmission Line Balun

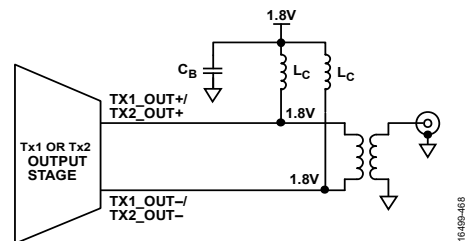


Figure 458. Using Bias Chokes and a Transformer

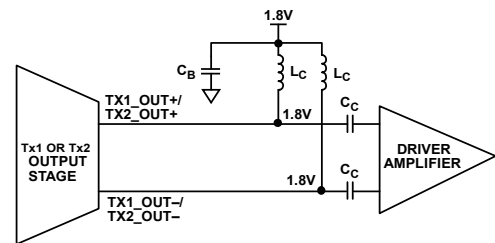


Figure 459. Using a Differential to Single-Ended Driver Amplifier

**General Receiver Path Interface**

The ADRV9009 has the following two types of receivers: receiver and observation receiver. These receivers include two main receive pathways (Receiver 1 and Receiver 2) and two observation or DPD receivers (Observation Receiver 1 and Observation Receiver 2). The receivers can support up to 200 MHz bandwidth, and the observation receivers can support up to 450 MHz bandwidth. The receiver channels and observation receiver channels are designed for differential use.

The ADRV9009 receivers support a wide range of operation frequencies. In the case of the receiver channels and observation receiver channels, the differential signals interface to an integrated mixer. The mixer input pins have a dc bias of approximately 0.7 V and may need to be ac-coupled, depending on the common-mode voltage level of the external circuit.

Important considerations for the receiver port interface are as follows:

- The device to be interfaced (filter, balun, transmit receive (T/R) switch, external low noise amplifier (LNA), and external PA, for example).
- The receiver and observation receiver maximum safe input power is 23 dBm (peak).
- The receiver and observation receiver optimum dc bias voltage is 0.7 V bias to ground.
- The board design (reference planes, transmission lines, and impedance matching, for example).

Figure 460 and Figure 461 show possible differential receiver port interface circuits. The options in Figure 460 and Figure 461 are valid for all receiver inputs operating in differential mode, though only the Receiver 1 signal names are indicated. Impedance matching may be necessary to obtain the performance levels described in this data sheet.

Given wide RF bandwidth applications, SMD balun devices function well. Decent loss and differential balance are available in a relatively small (0603, 0805) package.

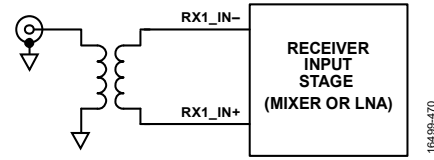


Figure 460. Differential Receiver Interface Using a Transformer

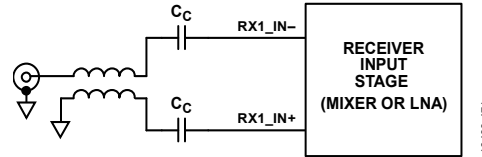


Figure 461. Differential Receiver Interface Using a Transmission Line Balun

**Impedance Matching Network Examples**

Impedance matching networks are required to achieve the ADRV9009 data sheet performance levels. This section provides example topologies and components used on the [ADRV9009-W/PCBZ](#).

Device models, board models, and balun and SMD component models are required to build an accurate system level simulation. The board layout model can be obtained from an EM simulator. The balun and SMD component models can be obtained from the device vendors or built locally. Contact Analog Devices applications engineering for ADRV9009 modeling details.

The impedance matching networks provided in this section are not evaluated in terms of mean time to failure (MTTF) in high volume production. Consult with component vendors for long-term reliability concerns. Consult with balun vendors to determine appropriate conditions for dc biasing.

Figure 464 shows three elements in parallel marked do not install (DNI). However, only one set of SMD component pads is placed on the board. For example, R202, L202, and C202 components only have one set of SMD pads for one SMD component. Figure 464 shows that in a generic port impedance matching network, the shunt or series elements can be resistors, inductors, or capacitors.

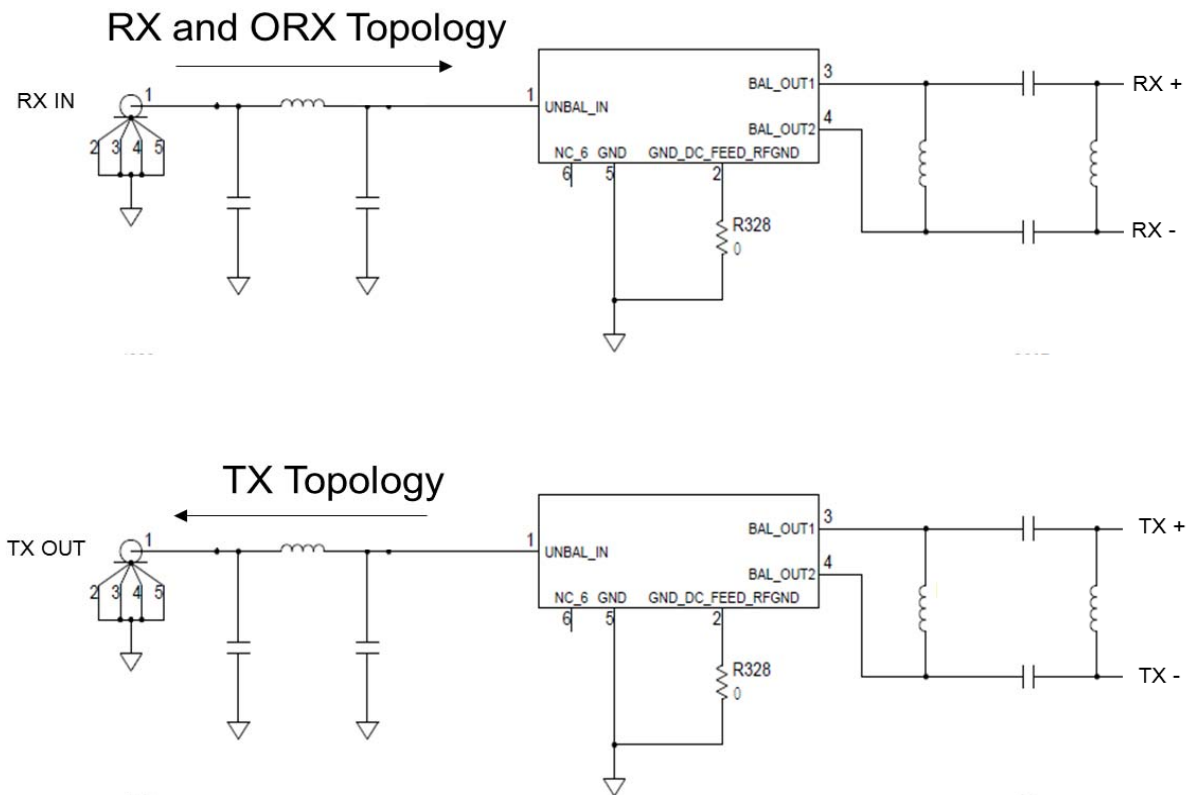
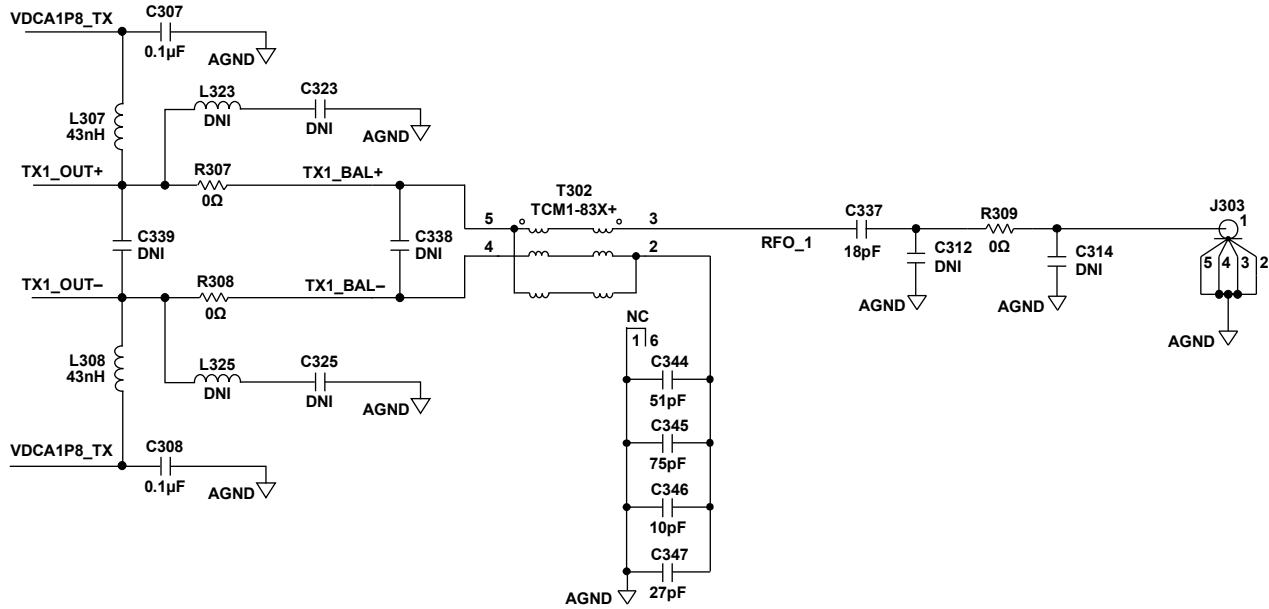


Figure 462. Impedance Matching Topology

16459-472

TX1



TX2

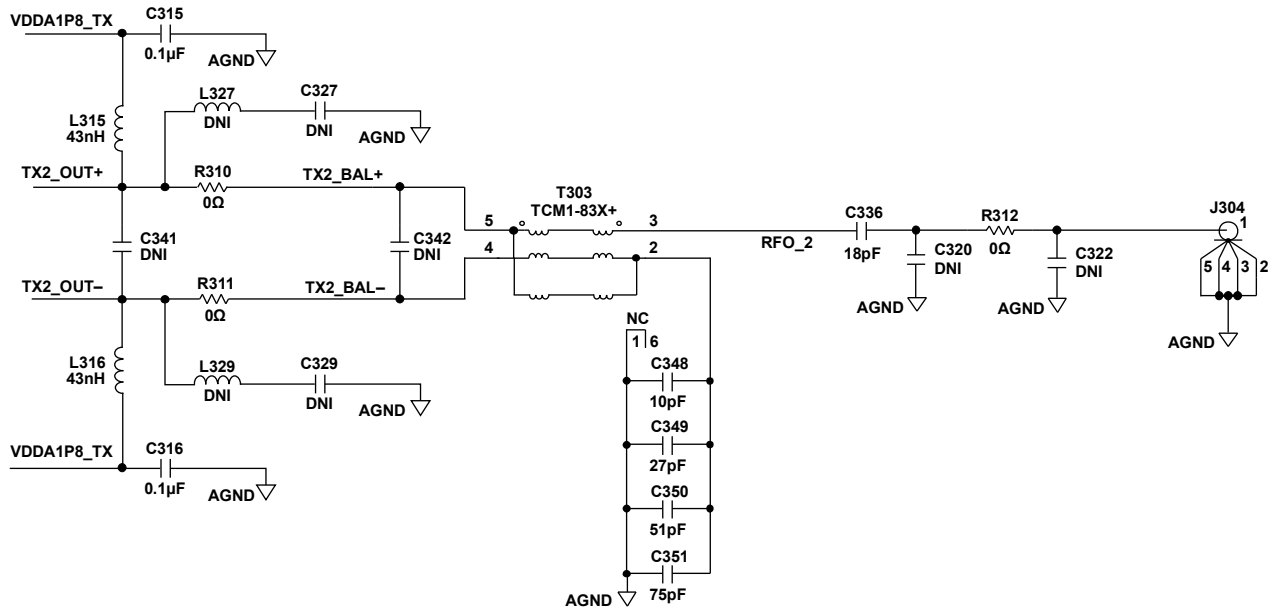


Figure 463. Transmitter 1 and Transmitter 2 Generic Matching Network Topology

16499-473

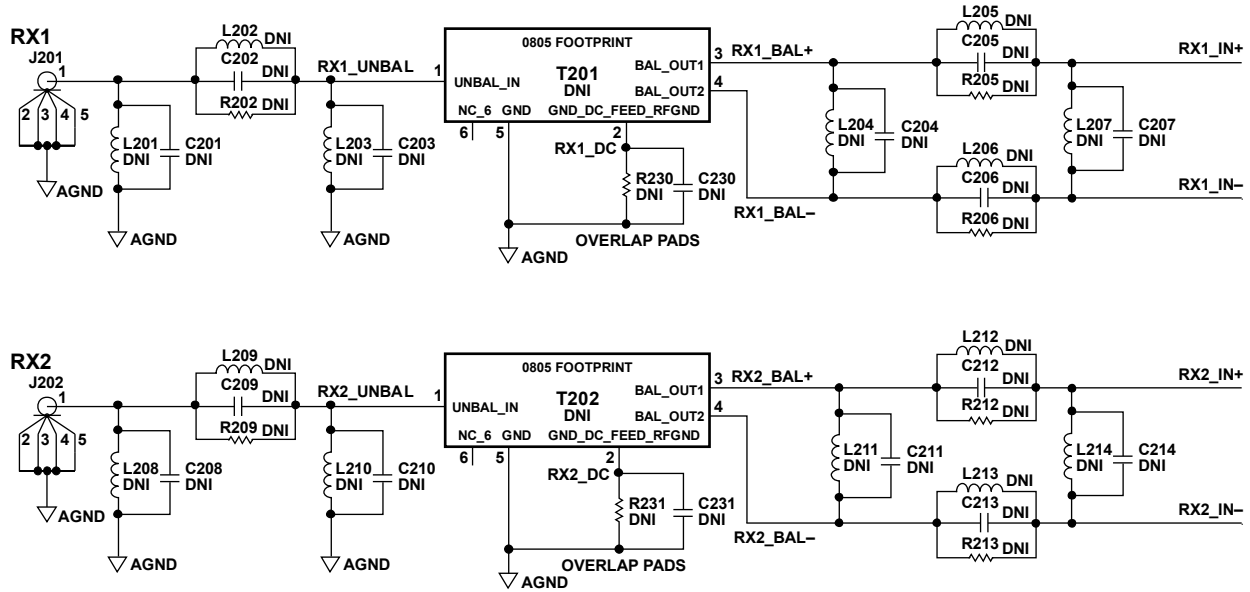


Figure 464. Receiver 1 and Receiver 2 Generic Matching Network Topology

16499-474

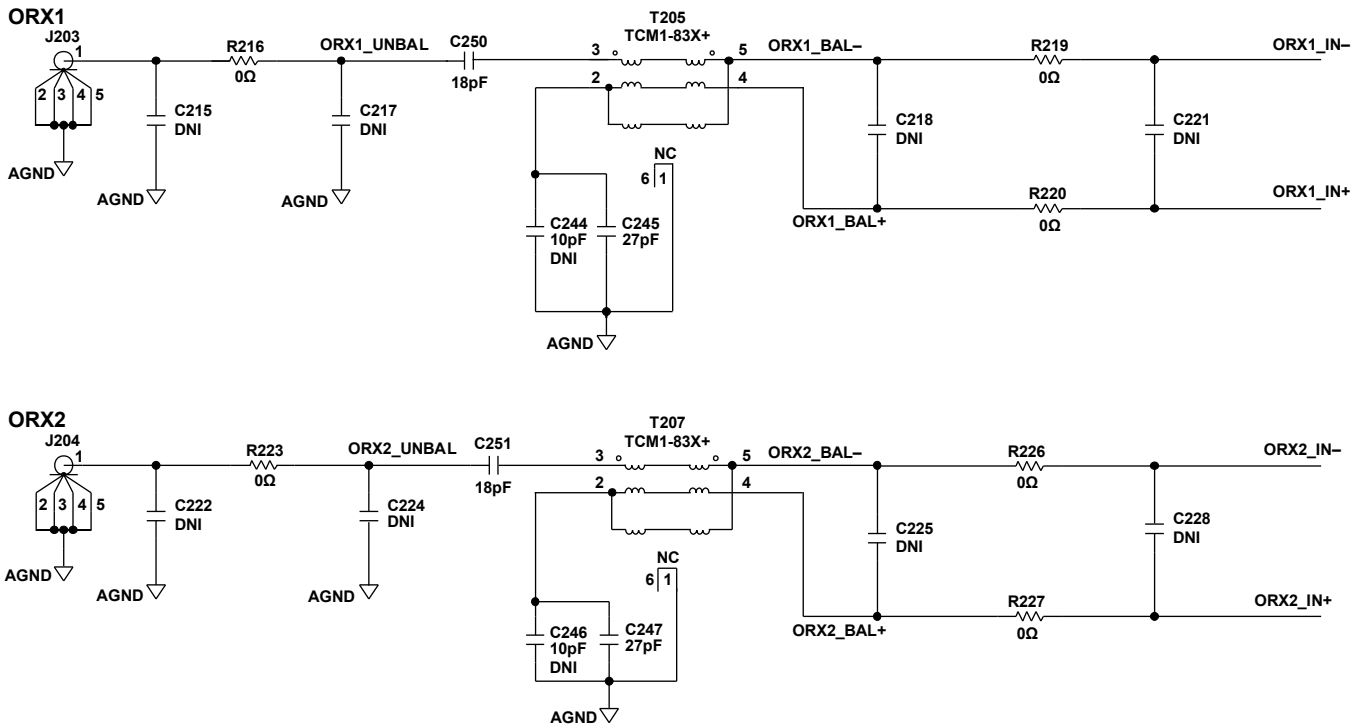


Figure 465. Observation Receiver 1 and Observation Receiver 2 Generic Matching Network Topology

16499-475

Table 12 through Table 17 show the selected balun and component values used for three matching network sets. Refer to Figure 463 or Figure 465 for a wideband matching example that operates across the entire device frequency range with reduced performance.

The RF matching used in the [ADRV9009-W/PCBZ](#) allows the ADRV9009 to operate across the entire chip frequency range with slightly reduced performance. Components C, R, and L can be used in all frequency bands.

**Table 12. Receiver 1 Evaluation Board Matching Components**

| Frequency Band       | 201   | 202    | 203   | 204    | 205, 206 | 207    | T201                   |
|----------------------|-------|--------|-------|--------|----------|--------|------------------------|
| 625 MHz to 2815 MHz  | 22 nH | 12 pF  | 62 nH | 180 nH | 39 pF    | 91 nH  | Johanson 1720BL15A0100 |
| 3400 MHz to 4800 MHz | DNI   | 0 Ω    | DNI   | 18 nH  | 1.3 nH   | 0.4 pF | Anaren BD3150L50100AHF |
| 5300 MHz to 5900 MHz | DNI   | 0.6 nH | DNI   | DNI    | 0.4 pF   | 4.3 nH | Johanson 5400BL15B200  |

**Table 13. Receiver 2 Evaluation Board Matching Components**

| Frequency Band       | 208   | 209    | 210   | 211    | 212, 213 | 214    | T202                   |
|----------------------|-------|--------|-------|--------|----------|--------|------------------------|
| 625 MHz to 2815 MHz  | 22 nH | 12 pF  | 62 nH | 180 nH | 39 pF    | 91 nH  | Johanson 1720BL15A0100 |
| 3400 MHz to 4800 MHz | DNI   | 0 Ω    | DNI   | 18 nH  | 1.3 nH   | 0.4 pF | Anaren BD3150L50100AHF |
| 5300 MHz to 5900 MHz | DNI   | 0.6 nH | DNI   | DNI    | 0.4 pF   | 4.3 nH | Johanson 5400BL15B200  |

**Table 14. Observation Receiver 1 Evaluation Board Matching Components**

| Frequency Band       | 215    | 216    | 217    | 218    | 219, 220 | 221    | T205                   |
|----------------------|--------|--------|--------|--------|----------|--------|------------------------|
| 625 MHz to 2815 MHz  | DNI    | 0 Ω    | DNI    | 56 nH  | 5.6 pF   | 180 nH | Johanson 1720BL15A0100 |
| 3400 MHz to 4800 MHz | 0.3 pF | 1.6 pF | 2 nH   | 6.8 nH | 1.7 nH   | 220 nH | Anaren BD3150L50100AHF |
| 5300 MHz to 5900 MHz | 100 nH | 6.8 pF | 5.6 nH | DNI    | 0.8 pF   | 1.5 nH | Johanson 5400BL15B200  |

**Table 15. Observation Receiver 2 Evaluation Board Matching Components**

| Frequency Band       | 222    | 223    | 224            | 225    | 226, 227 | 228    | T207                   |
|----------------------|--------|--------|----------------|--------|----------|--------|------------------------|
| 625 MHz to 2815 MHz  | DNI    | 0 Ω    | Do not install | 56 nH  | 5.6 pF   | 180 nH | Johanson 1720BL15A0100 |
| 3400 MHz to 4800 MHz | 0.3 pF | 1.6 pF | 2 nH           | 6.8 nH | 1.7 nH   | 220 nH | Anaren BD3150L50100AHF |
| 5300 MHz to 5900 MHz | 100 nH | 6.8 pF | 5.6 nH         | DNI    | 0.8 pF   | 1.5 nH | Johanson 5400BL15B200  |

**Table 16. Transmitter 1 Evaluation Board Matching Components<sup>1</sup>**

| Frequency Band       | 314   | 313    | 312   | 309, 310 | 311    | T302                   | T302 Pin 2, Bypass Capacitor C332 | C307, C308, L307, L308 |
|----------------------|-------|--------|-------|----------|--------|------------------------|-----------------------------------|------------------------|
| 625 MHz to 2815 MHz  | 22 nH | 4.7 pF | 43 nH | 0 Ω      | 0.2 pF | Johanson 1720BL15B0050 | 33 pF                             | DNI                    |
| 3400 MHz to 4800 MHz | DNI   | 0 Ω    | DNI   | 2.7 nH   | 0.2 pF | Anaren BD3150L50100AHF | 3.9 pF                            | DNI                    |
| 5300 MHz to 5900 MHz | DNI   | 0 Ω    | DNI   | 0.9 nH   | 8.2 nH | Johanson 5400BL14B100  | 1.8 pF                            | DNI                    |

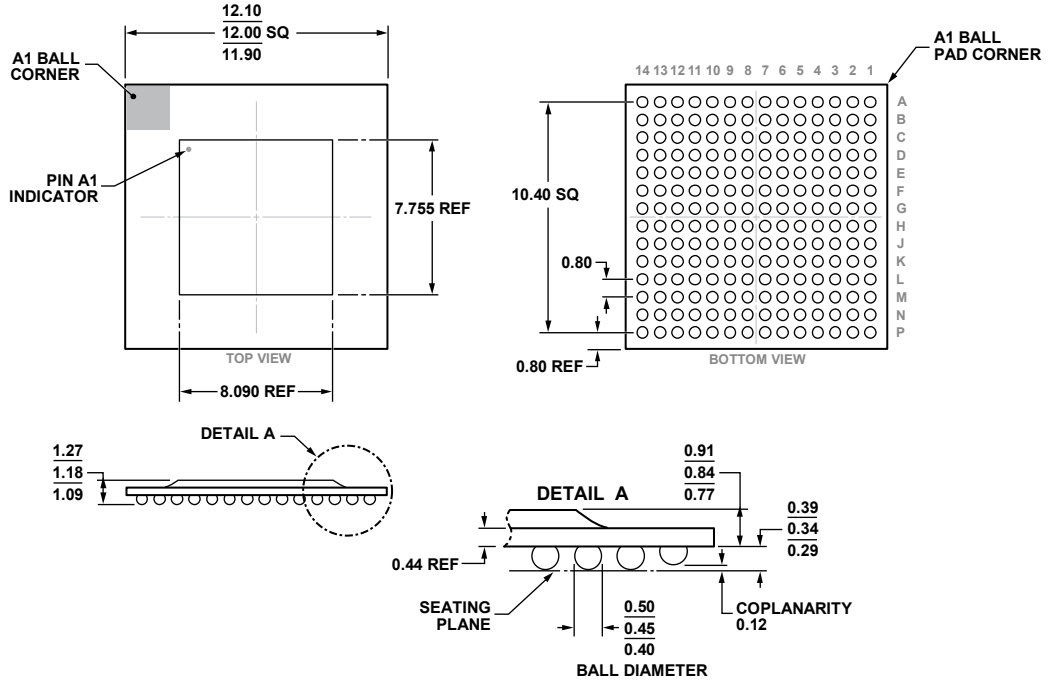
<sup>1</sup> These matches provide VDDA1P8\_TX to the TXx\_OUT± pins through the balun.

**Table 17. Transmitter 2 Evaluation Board Matching Components<sup>1</sup>**

| Frequency Band       | 322   | 321    | 320   | 317, 318 | 319    | T303                   | T303 Pin 2, Bypass Capacitor C335 | C315, C316, L315, L316 |
|----------------------|-------|--------|-------|----------|--------|------------------------|-----------------------------------|------------------------|
| 625 MHz to 2815 MHz  | 22 nH | 4.7 pF | 43 nH | 0 Ω      | 0.2 pF | Johanson 1720BL15B0050 | 33 pF                             | DNI                    |
| 3400 MHz to 4800 MHz | DNI   | 0 Ω    | DNI   | 2.7 nH   | 0.2 pF | Anaren BD3150L50100AHF | 3.9 pF                            | DNI                    |
| 5300 MHz to 5900 MHz | DNI   | 0 Ω    | DNI   | 0.9 nH   | 8.2 nH | Johanson 5400BL14B100  | 1.8 pF                            | DNI                    |

<sup>1</sup> These matches provide VDDA1P8\_TX to the TXx\_OUT± pins through the balun.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-275-GGAB-1.

Figure 466. 196-Ball Chip Scale Package Ball Grid Array [CSP\_BGA] (BC-196-13)

Dimensions shown in millimeters

ORDERING GUIDE

| Model <sup>1</sup> | Temperature Range <sup>2</sup> | Package Description                                   | Package Option |
|--------------------|--------------------------------|---|----------------|
| ADRV9009BBCZ       | -40°C to +85°C                 | 196-Ball Chip Scale Package Ball Grid Array [CSP_BGA] | BC-196-13      |
| ADRV9009BBCZ-REEL  | -40°C to +85°C                 | 196-Ball Chip Scale Package Ball Grid Array [CSP_BGA] | BC-196-13      |
| ADRV9009-W/PCBZ    |                                | Pb-Free Evaluation Board, 75 MHz to 6000 MHz          |                |

<sup>1</sup> Z = RoHS Compliant Part.

<sup>2</sup> See the Thermal Management section.



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