

LCD Segment Drivers

Standard Segment Drivers


BU9796FS, BU9795AKV, BU9795AFV, BU9795AGUW, BU9794KV, BU9799KV

No.10044EAT05

●Description

ROHM standard function segment driver series achieve "Ultra-Low power consumption". Also these drivers need not external components. And this driver series is very simple that only has segment driver function. So, this driver series are very suitable to add in LCD display function for various applications.

●Features

- 1) 2wire serial interface (BU9796FS, BU9799KV)
- 2) 3wire serial interface (BU9794KV, BU9795AKV/FV/GUW)
- 3) Integrated RAM for display data (DDRAM)
- 4) Power supply circuit for LCD driving
 - 1/2, 1/3Bias selectable
 - 1/4Duty
 - Integrated Buffer AMP
- 5) Integrated Oscillation circuit
- 6) Integrated Power-on Reset circuit
- 7) No external components
- 8) Support blink function
- 9) Support standby mode
- 10) Low voltage / Ultra low power consumption design
- 11) Support EVR function (BU9799KV)
- 12) Support unity voltage supply (BU9795AKV/FV/GUW, BU9796FS)
- 13) Support Independent power supply circuit for LCD driving (BU9794KV, BU9799KV)

●Applications

Telephone, FAX, Portable equipment (POS, ECR, PDA etc.),
DSC, DVC, Car Audio, Home electrical appliance, Meter equipment, Healthcare equipment etc.

●Line up matrix

Parameter	BU9796FS	BU9795A			BU9794KV	BU9799KV
		KV	FV	GUW		
Segment output	20	35	27	31	50	50
Common output	4	4	4	4	4	4
Total display dot number	80	140	108	124	200	200
Adjustable contrast function	-	-	-	-	-	Yes
Support split voltage supply	-	-	-	-	Yes	Yes
Interface	2wire	3wire	3wire	3wire	3wire	2wire
Package	SSOP-A32	VQFP48C	SSOP-B40	VBGA48W040	VQFP64	VQFP64

● Absolute maximum ratings (VSS=0V)

Parameter	BU9796FS	BU9795AKV /FV/GUW	BU9794KV	BU9799KV	Unit	Remarks
Power Supply Voltage 1 (VDD)	-0.5~+7.0				V	Power supply
Power Supply Voltage 2 (VLCD)	-0.5 ~ VDD	-0.5 ~ VDD	-0.5 ~ +7.0	-0.5 ~ +7.0	V	LCD drive Voltage
Allowable Loss (Pd)	0.64 ^{*1}	0.6 ^{*2} 0.7 ^{*3} 0.27 ^{*4}	0.75 ^{*5}	0.75 ^{*5}	W	Allowable loss at package only
Input Voltage Range (VIN)	-0.5 ~ VDD+0.5				V	
Operational Temperature Range (Topr)	-40 ~ -85				°C	
Storage Temperature Range (Tstg)	-55 ~ +125				°C	

*1 When use more than Ta=25°C, subtract 6.4mW per degree

*2 When use more than Ta=25°C, subtract 6.0mW per degree (BU9795AKV)

*3 When use more than Ta=25°C, subtract 7.0mW per degree (BU9795AFV)

*4 When use more than Ta=25°C, subtract 2.7mW per degree (BU9795AGUW)

*5 When use more than Ta=25°C, subtract 7.5mW per degree

● Recommend operating conditions (Ta=-40~85°C, VSS=0V)

Parameter	BU9796FS ^{*1}			BU9795AKV /FV/GUW ^{*1}			BU9794KV			BU9799KV			Unit	Remarks
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
Power Supply Voltage 1 (VDD)	2.5	-	5.5	2.5	-	5.5	2.5	-	5.5	2.5	-	5.5	V	Power supply
Power Supply Voltage 2 (VLCD)	0	-	VDD -2.4	0	-	VDD -2.4	2.5	-	5.5	2.5	-	5.5	V	LCD drive Voltage

*1 Please use VDD-VLCD ≥ 2.4V condition.

●Electrical characteristics

<BU9796FS>

DC Characteristics (VDD=2.5~5.5V, VLCD=0V, VSS=0V, Ta=-40~85°C, unless otherwise specified)

Parameter	Symbol	Limits			Unit	Condition	
		MIN	TYP	MAX			
“H” level input voltage	VIH	0.7VDD	-	VDD	V		
“L” level input voltage	VIL	VSS	-	0.3VDD	V		
“H” level input current	I _{IH}	-	-	1	μA		
“L” level input current	I _{IL}	-1	-	-	μA		
LCD Driver on resistance	SEG	RON	-	3	-	kΩ	I _{load} =±10μA
	COM	RON	-	3	-	kΩ	
VLCD supply voltage	VLCD	0	-	VDD - 2.4	V	VDD-VLCD ≥ 2.4V	
Standby current	IDD1	-	-	5	μA	Display off, Oscillation off	
Power consumption	IDD2	-	12.5	30	μA	VDD=3.3V, VLCD=0V, Ta=25°C Power save mode SR = Power save mode1, Power save mode FR = Power save mode1 1/3 bias, Frame inverse	

Oscillation Characteristics (VDD=2.5~5.5V, VSS=0V, Ta=-40~85°C, unless otherwise specified)

Parameter	Symbol	Limits			Unit	Condition
		MIN	TYP	MAX		
Frame frequency	fCLK	56	80	104	Hz	Power save mode FR = Normal mode

MPU interface Characteristics (VDD=2.5~5.5V, VLCD=0V, VSS=0V, Ta=-40~85°C, unless otherwise specified)

Parameter	Symbol	Limits			Unit	Condition
		MIN.	TYP.	MAX.		
Input rise time	t _r	-	-	0.3	μs	
Input fall time	t _f	-	-	0.3	μs	
SCL cycle time	t _{SCYC}	2.5	-	-	μs	
“H” SCL pulse width	t _{SHW}	0.6	-	-	μs	
“L” SCL pulse width	t _{SLW}	1.3	-	-	μs	
SDA setup time	t _{SDS}	100	-	-	ns	
SDA hold time	t _{SDH}	100	-	-	ns	
Buss free time	t _{BUF}	1.3	-	-	μs	
START condition hold time	t _{HD;STA}	0.6	-	-	μs	
START condition setup time	t _{SU;STA}	0.6	-	-	μs	
STOP condition setup time	t _{SU;STO}	0.6	-	-	μs	

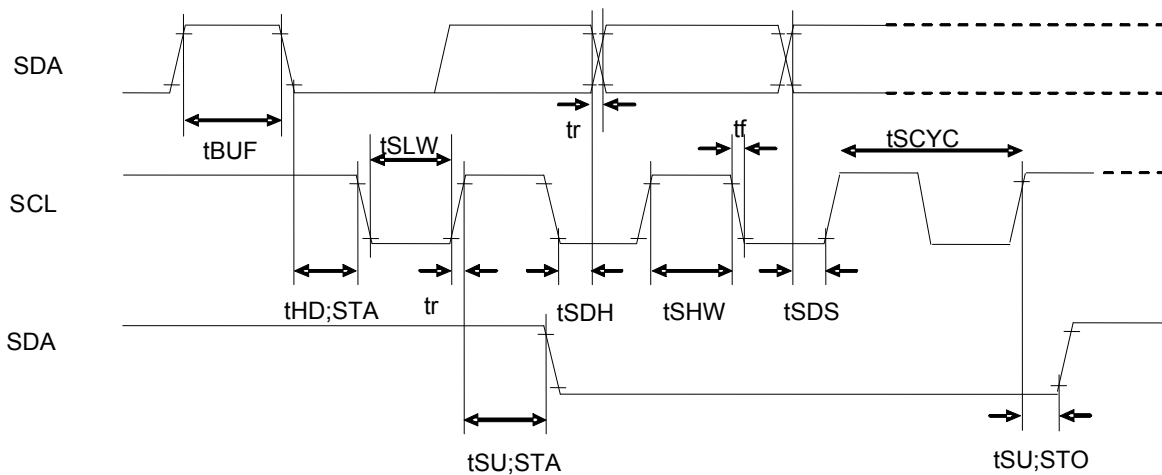


Fig.1 Interface timing (BU9796FS)

<BU9795AKV/FV/GUW>

DC Characteristics (VDD=2.5~5.5V, VSS=0V, Ta=-40~85°C, unless otherwise specified)

Parameter	Symbol	Limits			Unit	Condition	
		MIN	TYP	MAX			
"H" level input voltage	VIH	0.7VDD	-	VDD	V		
"L" level input voltage	VIL	VSS	-	0.3VDD	V		
"H" level input current	IiH	-	-	1	μA		
"L" level input current	IiL	-1	-	-	μA		
LCD Driver on resistance	SEG	RON	-	3.5	-	kΩ	Iload=±10μA
	COM	RON	-	3.5	-	kΩ	
VLCD supply voltage	VLCD	0	-	VDD-2.4	V	VDD-VLCD ≥ 2.5V	
Standby current	Ist	-	-	5	μA	Display off, Oscillator off	
Power consumption 1	IDD1	-	12.5	30	μA	VDD=3.3[V], Ta=25°C, Power save mode1, FR=70Hz 1/3 bias, Frame inverse	
Power consumption 2	IDD2	-	20	40	μA	VDD=3.3[V], Ta=25°C, Normal mode, FR=80Hz 1/3 bias, Line inverse	

Oscillation Characteristics (VDD=2.5~5.5V, VSS=0V, Ta=-40~85°C)

Parameter	Symbol	Limits			Unit	Condition
		MIN	TYP	MAX		
Frame frequency	fCLK	56	80	104	Hz	FR = 80Hz setting
Frame frequency1	fCLK1	70	80	90	Hz	VDD=3.5V, 25°C

MPU interface Characteristics (VDD=2.5V~5.5V, VSS=0V, Ta=-40~85°C)

Parameter	Symbol	Limits			Unit	Condition
		MIN	TYP	MAX		
Input rise time	tr	-	-	80	ns	
Input fall time	tf	-	-	80	ns	
SCL cycle time	tSCYC	400	-	-	ns	
"H" SCL pulse width	tSHW	100	-	-	ns	
"L" SCL pulse width	tSLW	100	-	-	ns	
SD setup time	tSDS	20	-	-	ns	
SD hold time	tSDH	50	-	-	ns	
CSB setup time	tCSS	50	-	-	ns	
CSB hold time	tCSH	50	-	-	ns	
"H" CSB pulse width	tCHW	50	-	-	ns	

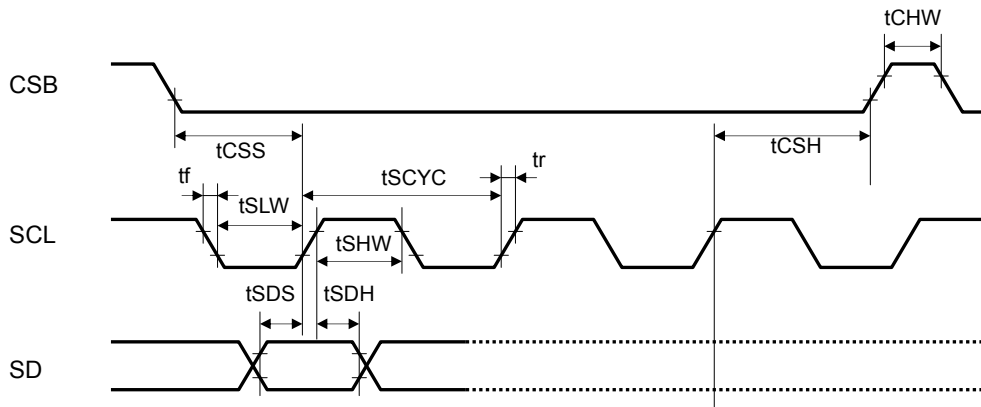


Fig.2 Interface Timing (BU9795AKV/FV/GUW)

<BU9794KV>

DC Characteristics (VDD=2.5~5.5V, VLCD=2.5~5.5V, VSS=0V, Ta=-40~85°C, unless otherwise specified)

Parameter	Symbol	Limits			Unit	Condition
		MIN	TYP	MAX		
"H" level input voltage	V _{IH}	0.8V _{DD}	-	V _{DD}	V	SD, SCL, CSB
"L" level input voltage	V _{IL}	V _{SS}	-	0.2V _{DD}	V	SD, SCL, CSB
"H" level input current	I _{IH}	-	-	1	μA	SD, SCL, CSB
"L" level input current	I _{IL}	-1	-	-	μA	SD, SCL, CSB
LCD Driver on resistance	SEG	RON	-	3.5	-	I _{load} =±10μA
	COM	RON	-	3.5	-	
Standby current	I _{st}	-	-	5	μA	Display off, Oscillation off
Power consumption 1	I _{DD}	-	5	15	μA	VDD=3.3V, VLCD=5V, Ta=25°C Power save mode1, FR=70Hz 1/3 bias, Frame inverse
Power consumption 2	I _{LCD}	-	10	20	μA	VDD=3.3V, VLCD=5V, Ta=25°C Power save mode1, FR=70Hz 1/3 bias, Frame inverse

Oscillation Characteristics (VDD=2.5~5.5V, VLCD=2.5~5.5V, VSS=0V, Ta=-40~85°C, unless otherwise specified)

Parameter	Symbol	Limits			Unit	Condition
		MIN	TYP	MAX		
Frame frequency	f _{CLK}	68	80	92	Hz	FR = 80Hz setting, VDD=3.3V

MPU interface Characteristics (VDD=2.5~5.5V, VLCD=2.5~5.5V, VSS=0V, Ta=-40~85°C, unless otherwise specified)

Parameter	Symbol	Limits			Unit	Condition
		MIN.	TYP.	MAX.		
Input rise time	t _r	-	-	80	ns	
Input fall time	t _f	-	-	80	ns	
SCL cycle time	t _{SCYC}	400	-	-	ns	
"H" SCL pulse width	t _{SHW}	100	-	-	ns	
"L" SCL pulse width	t _{SLW}	100	-	-	ns	
SD setup time	t _{SDS}	20	-	-	ns	
SD hold time	t _{SDH}	50	-	-	ns	
CSB setup time	t _{CSS}	50	-	-	ns	
CSB hold time	t _{CSH}	50	-	-	ns	
"H" CSB pulse time	t _{CHW}	50	-	-	ns	

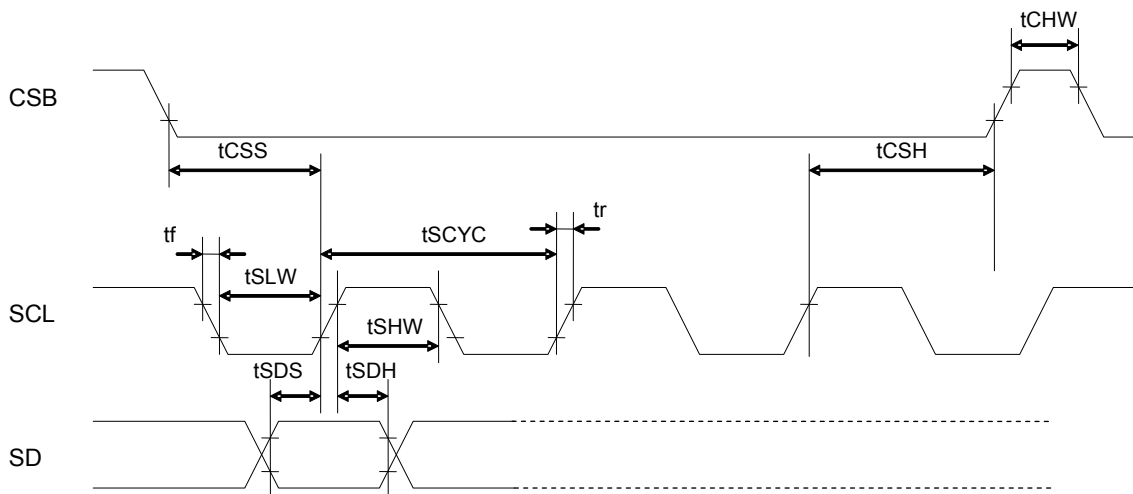


Fig.3 Interface Timing (BU9794KV)

<BU9799KV>

DC Characteristics (VDD=2.5~5.5V, VLCD=2.5~5.5V, VSS=0V, Ta=-40~85°C, unless otherwise specified)

Parameter	Symbol	Limits			Unit	Condition
		MIN	TYP	MAX		
“H” level input voltage	VIH	0.8VDD	-	VDD	V	SDA,SCL
“L” level input voltage	VIL	VSS	-	0.2VDD	V	SDA,SCL
“H” level input current	IIH	-	-	1	μA	SDA,SCL
“L” level input current	IIL	-1	-	-	μA	SDA,SCL
LCD Driver on resistance	SEG	RON	-	3.5	kΩ	Iload=±10μA
	COM	RON	-	3.5	kΩ	
Standby current	Ist	-	-	5	μA	Display off, Oscillation off
Power consumption 1	IDD	-	2.5	15	μA	VDD=3.3V, VLCD=5V, Ta=25°C Power save mode1, FR=70Hz 1/3 bias, Frame inverse
Power consumption 2	ILCD	-	10	20	μA	VDD=3.3V, VLCD=5V, Ta=25°C Power save mode1, FR=70Hz 1/3 bias, Frame inverse

Oscillation Characteristics (VDD=2.5~5.5V, VLCD=2.5~5.5V, VSS=0V, Ta=-40~85°C, unless otherwise specified)

Parameter	Symbol	Limits			Unit	Condition
		MIN	TYP	MAX		
Frame frequency	fCLK	56	80	104	Hz	FR = 80Hz setting, VDD=3.3V

MPU interface Characteristics (VDD=2.5~5.5V, VLCD=2.5~5.5V, VSS=0V, Ta=-40~85°C, unless otherwise specified)

Parameter	Symbol	Limits			Unit	Condition
		MIN	TYP	MAX		
Input rise time	tr	-	-	0.3	μs	
Input fall time	tf	-	-	0.3	μs	
SCL cycle time	tSCYC	2.5	-	-	μs	
“H” SCL pulse width	tSHW	0.6	-	-	μs	
“L” SCL pulse width	tSLW	1.3	-	-	μs	
SDA setup time	tSDS	100	-	-	μs	
SDA hold time	tSDH	100	-	-	μs	
Buss free time	tBUF	1.3	-	-	μs	
START condition hold time	tHD;STA	0.6	-	-	μs	
START condition setup time	tSU;STA	0.6	-	-	μs	
STOP condition setup time	tSU;STO	0.6	-	-	μs	

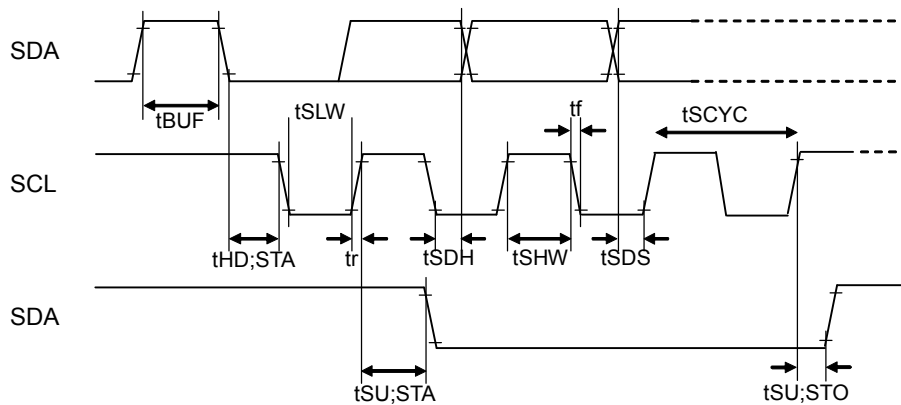


Fig.4 interface timing (BU9799KV)

●Block Diagram / Pin Arrangement / Terminal Description

<BU9796FS>

●Block Diagram

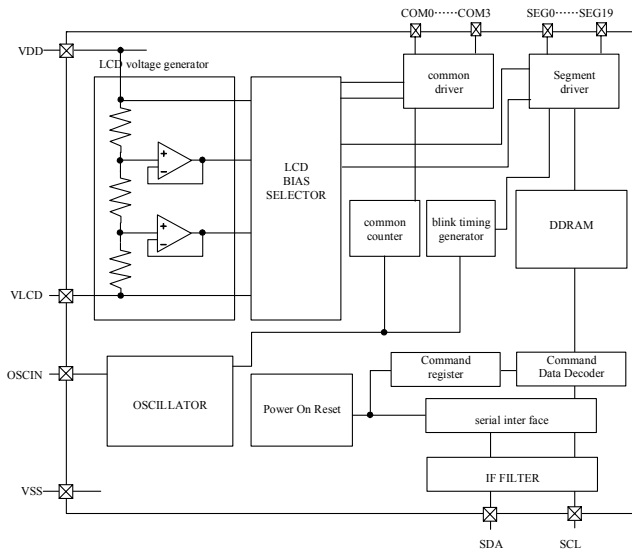


Fig.5 Block Diagram (BU9796FS)

●Pin Arrangement

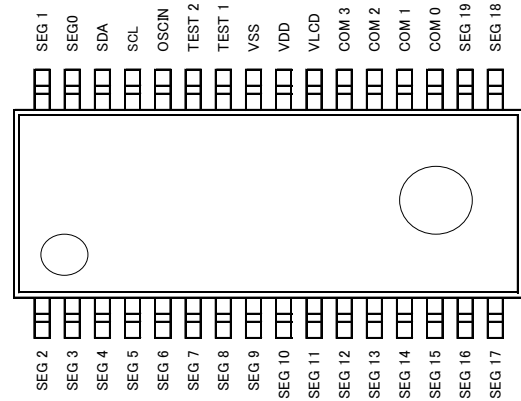


Fig.6 Pin Arrangement (BU9796FS)

●Terminal Description

Terminal	Terminal No.	I/O	Function
TEST1	26	I	Test input (ROHM use only) Must be connect to VSS
TEST2	27	I	Test input (ROHM use only) TEST2="L": POR circuit enable TEST2="H": POR circuit disenable, refer to "Cautions in Power ON/OFF"
OSCIN	28	I	External clock input Ext clock and Int clock can be selected by command. Must be connect to VSS when use internal oscillation circuit.
SDA	30	I/O	serial data in-out terminal
SCL	29	I	serial data transfer clock
VSS	25		GND
VDD	24		Power supply
VLCD	23		Power supply for LCD driving
SEG0-19	31,32 1-18	O	SEGMENT output for LCD driving
COM0-3	19-22	O	COMMON output for LCD driving

<BU9795AKV>

●Block Diagram

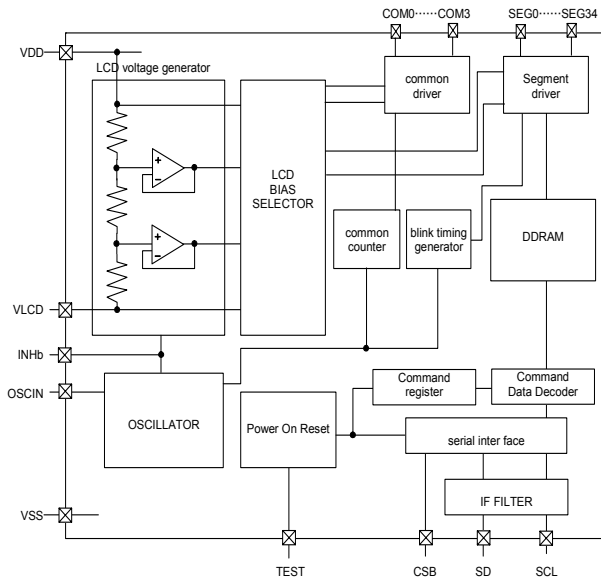


Fig.7 Block Diagram (BU9795AKV)

●Pin Arrangement

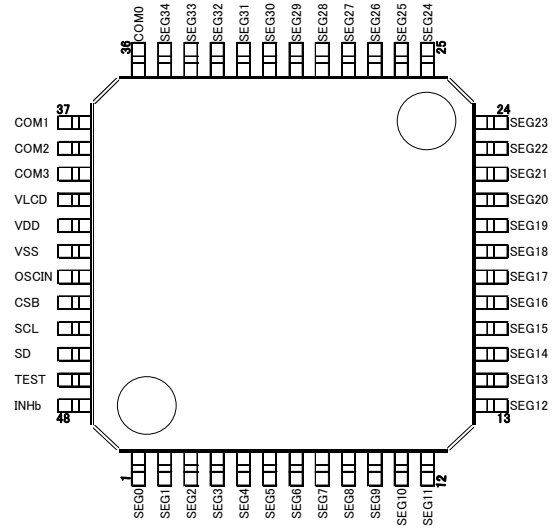


Fig.8 Pin Arrangement (BU9795AKV)

●Terminal Description

Terminal	Terminal No.	I/O	Function
INHb	48	I	Input terminal for turn off display H: turn on display L: turn off display
TEST	47	I	Test input (ROHM use only) Must be connect to VSS
OSCIN	43	I	External clock input Ext clock and Int clock can be changed by command. Must be connect to VSS when use internal oscillation circuit.
SD	46	I	serial data input
SCL	45	I	serial data transfer clock
CSB	44	I	Chip select : "L" active
VSS	42		GND
VDD	41		Power supply
VLCD	40		Power supply for LCD driving
SEG0-34	1-35	O	SEGMENT output for LCD driving
COM0-3	36-39	O	COMMON output for LCD driving

<BU9795AFV>

•Block Diagram

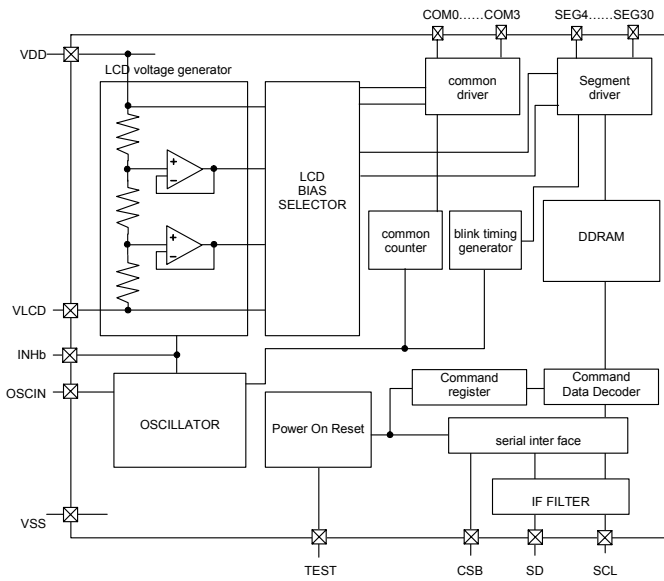


Fig.9 Block Diagram (BU9795AFV)

•Pin Arrangement

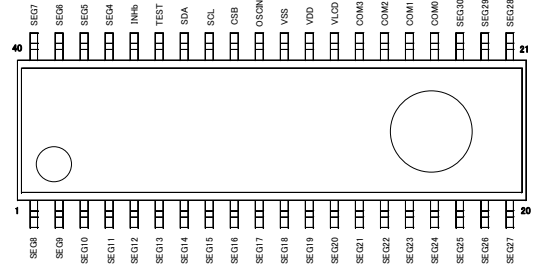


Fig.10 Pin Arrangement (BU9795AFV)

•Terminal Description

Terminal	Terminal No.	I/O	Function
INHb	36	I	Input terminal for turn off display H: turn on display L: turn off display
TEST	35	I	Test input (ROHM use only) Must be connect to VSS
OSCIN	31	I	External clock input Ex clock and Int clock can be changed by command. Must be connect to VSS when use internal oscillation circuit.
SD	34	I	serial data input
SCL	33	I	serial data transfer clock
CSB	32	I	Chip select : "L" active
VSS	30		GND
VDD	29		Power supply
VLCD	28	I	Power supply for LCD driving
SEG4-30	1-23, 37-40	O	SEGMENT output for LCD driving
COM0-3	24-27	O	COMMON output for LCD driving

<BU9795AGUW>

•Block Diagram

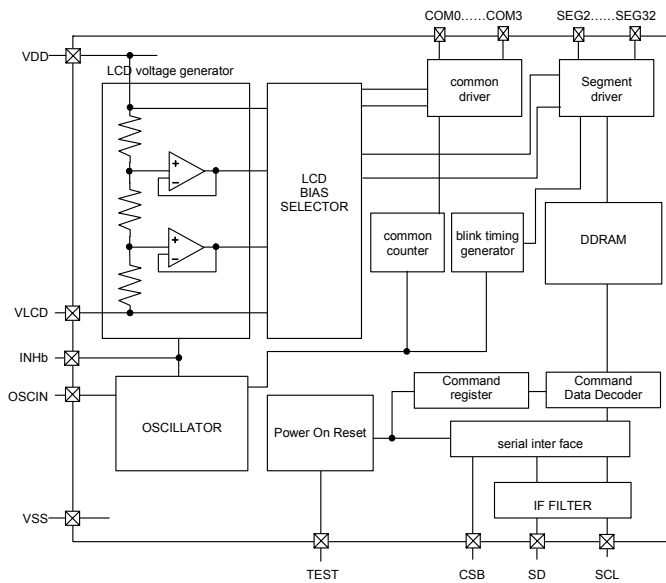


Fig.11 Block Diagram (BU9795AGUW)

•Pin Arrangement

	1	2	3	4	5	6	7
G	(NC)	SEG13	SEG15	SEG18	SEG20	SEG22	(NC)
F	SEG11	SEG12	SEG16	SEG17	SEG21	SEG23	SEG24
E	SEG9	SEG10	SEG14	SEG19	SEG25	SEG27	SEG26
D	SEG7	SEG6	SEG8	SEG5	SEG30	SEG28	SEG29
C	SEG4	SEG3	SEG2	CSB	COM3	SEG32	SEG31
B	(X)	INHb	SD	VSS	VDD	COM1	COM0
A	(NC)	TEST2	SCL	OSCIN	VLCD	COM2	(NC)

Fig.12 Pin Arrangement (BU9795AGUW)

•Terminal Description

Terminal	I/O	Function
INHb	I	Input terminal for turn off display H: turn on display L: turn off display
TEST	I	Test input (ROHM use only) Must be connect to VSS
OSCIN	I	External clock input Ex clock and Int clock can be changed by command. Must be connect to VSS when use internal oscillation circuit.
SD	I	serial data input
SCL	I	serial data transfer clock
CSB	I	Chip select : "L" active
VSS		GND
VDD		Power supply
VLCD	I	Power supply for LCD driving
SEG2-32	O	SEGMENT output for LCD driving
COM0-3	O	COMMON output for LCD driving

(Caution) About terminal number, please refer to above pin arrangement

<BU9794KV>
 ●Block Diagram

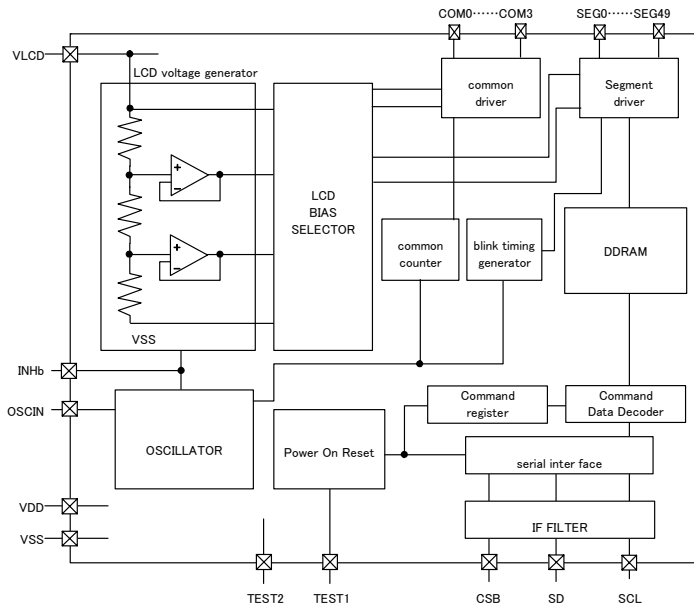


Fig.13 Block Diagram (BU9794KV)

●Pin Arrangement

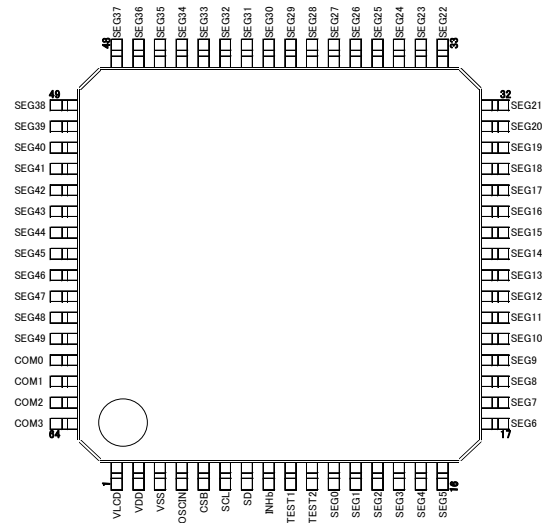


Fig.14 Pin Arrangement (BU9794KV)

●Terminal Description

Terminal	Terminal No.	I/O	Function
INHb	8	I	Input terminal for turn off display H: turn on display, L: turn off display
TEST1	9	I	Test input (ROHM use only) Must be connect to VSS
TEST2	10	I	Test input (ROHM use only) Must be connect to VSS
OSCIN	4	I	External clock input Ex clock and Int clock can be changed by command. Must be connect to VSS when use internal oscillation circuit.
SD	7	I	serial data input
SCL	6	I	serial data transfer clock
CSB	5	I	Chip select : "L" active
VSS	3		GND
VDD	2		Power supply
VLCD	1		Power supply for LCD driving
SEG0-49	11-60	O	SEGMENT output for LCD driving
COM0-3	61-64	O	COMMON output for LCD driving

<BU9799KV>
 ●Block Diagram

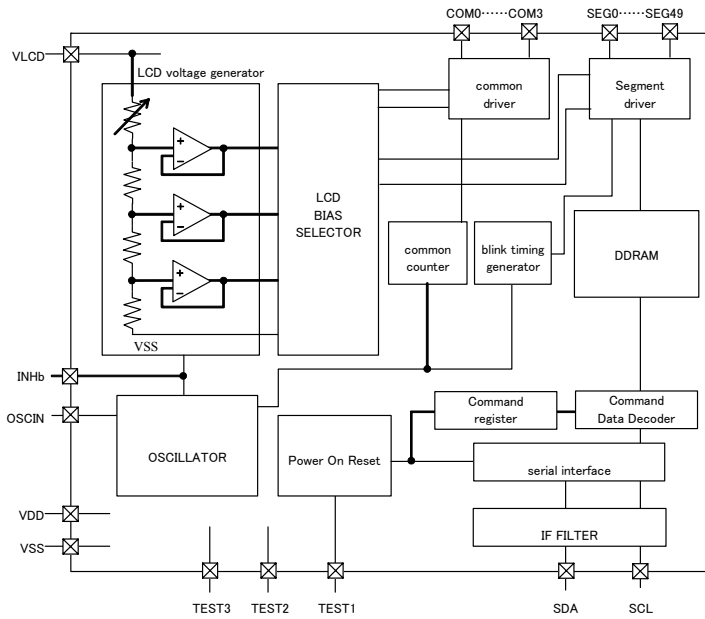


Fig.15 Block Diagram (BU9799KV)

●Pin Arrangement

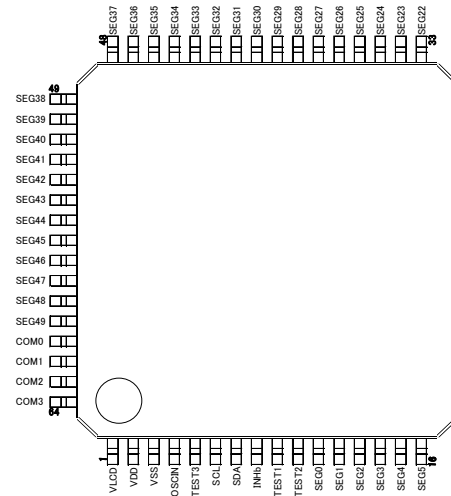


Fig.16 Pin Arrangement (BU9799KV)

●Terminal Description

Terminal	Terminal No.	I/O	Function
INHb	8	I	Input terminal for turn off display H: turn on display L: turn off display
TEST1	9	I	Test input (ROHM use only) TEST1="L": POR circuit enable TEST1="H": POR circuit disable, refer to "Cautions in Power ON/OFF"
TEST2	10	I	Test input (ROHM use only) Must be connect to VSS
TEST3	5	I	Test input (ROHM use only) Must be connect to VSS
OSCIN	4	I	External clock input Ex clock and Int clock can be changed by command. Must be connect to VSS when use internal oscillation circuit.
SDA	7	I	serial data input
SCL	6	I	serial data transfer clock
VSS	3		GND
VDD	2		Power supply
VLCD	1		Power supply for LCD driving
SEG0-49	11-60	O	SEGMENT output for LCD driving
COM0-3	61-64	O	COMMON output for LCD driving

●IO Equivalent Circuit
<BU9796FS>

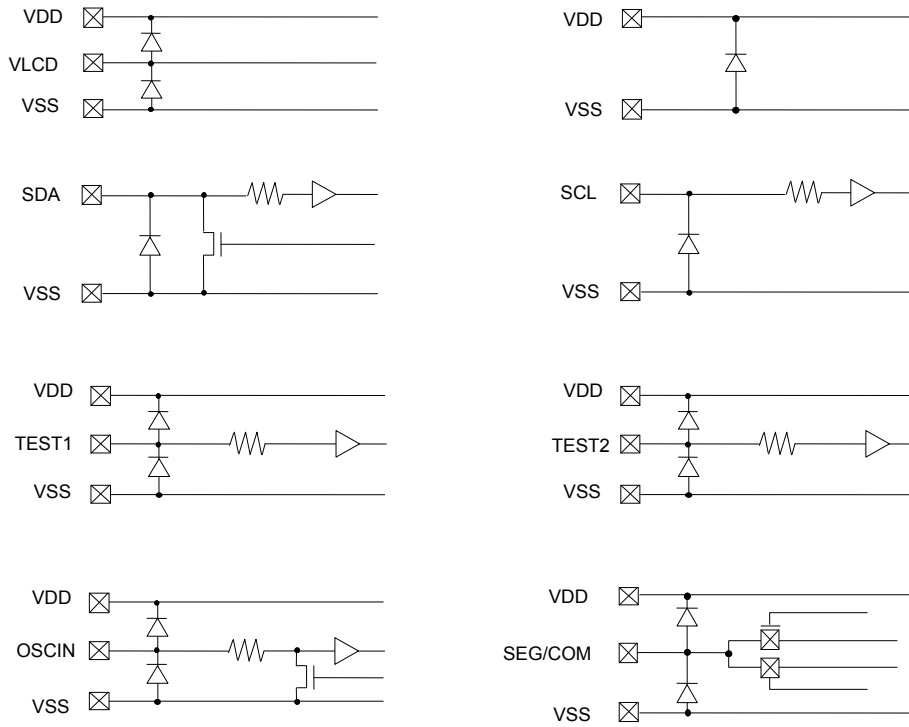


Fig.17 I/O equivalent circuit (BU9796FS)

<BU9795AKV/FV/GUW>

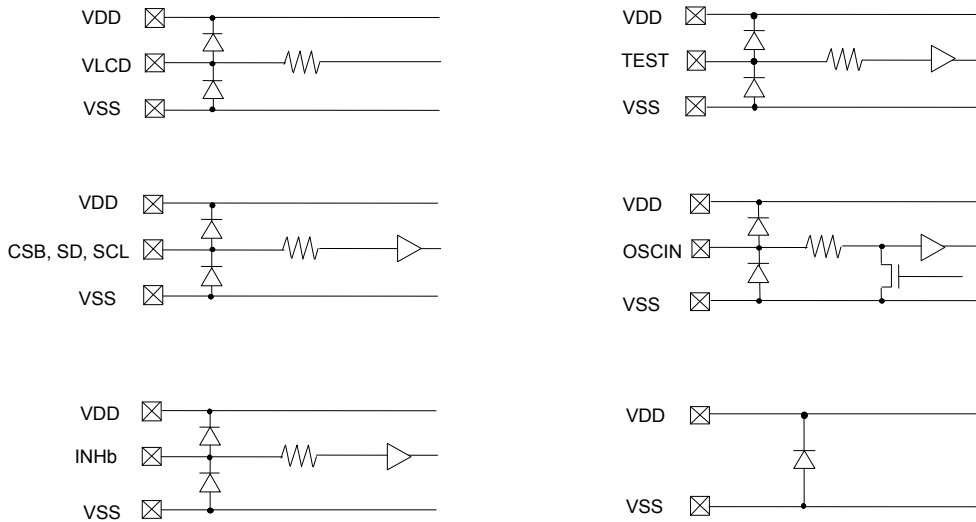


Fig.18 I/O equivalent circuit (BU9795AKV/FV/GUW)

<BU9794KV>

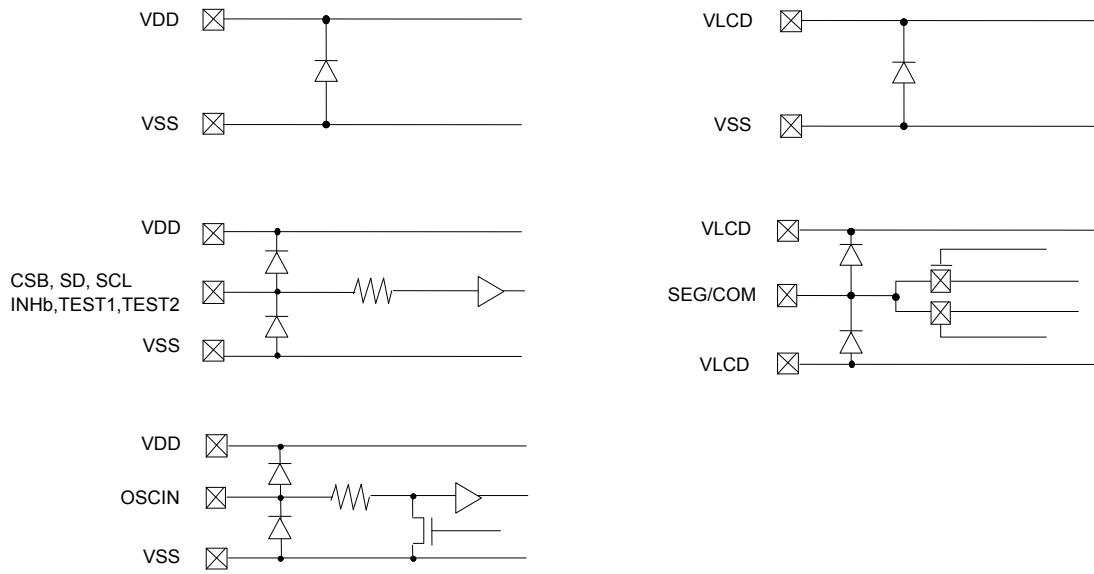


Fig.19 I/O equivalent circuit (BU9794KV)

<BU9799KV>

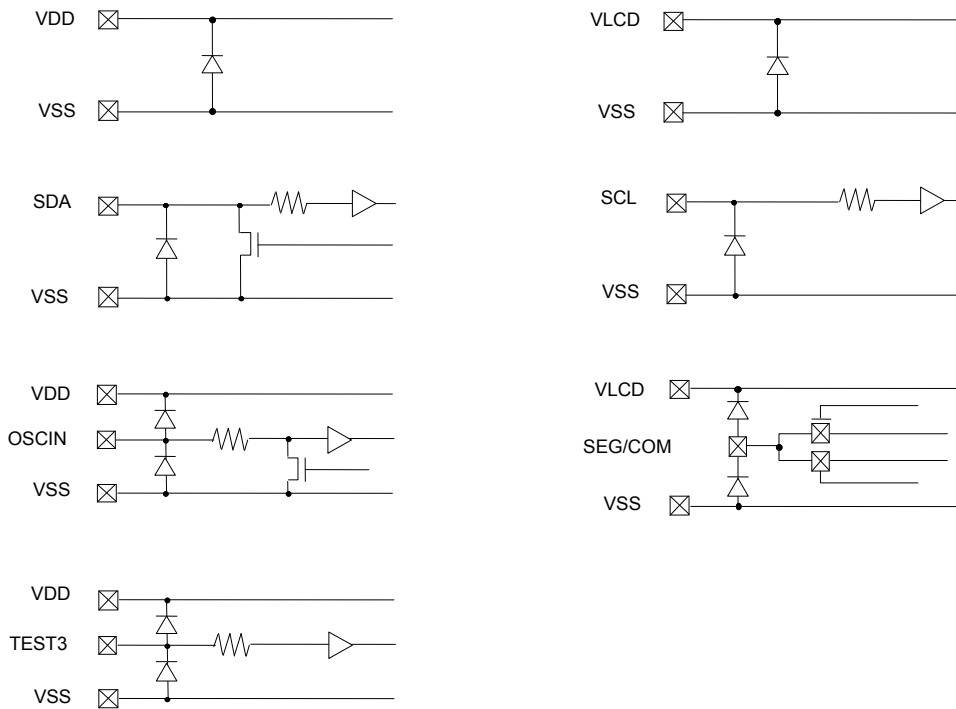


Fig.20 I/O equivalent circuit (BU9799KV)

● Ordering part number

B U

Part No.

9 7 9 6

Part No.
 BU9794
 BU9795A
 BU9796
 BU9799

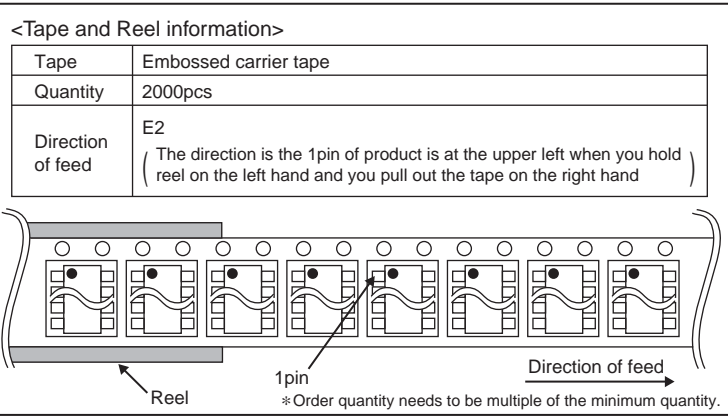
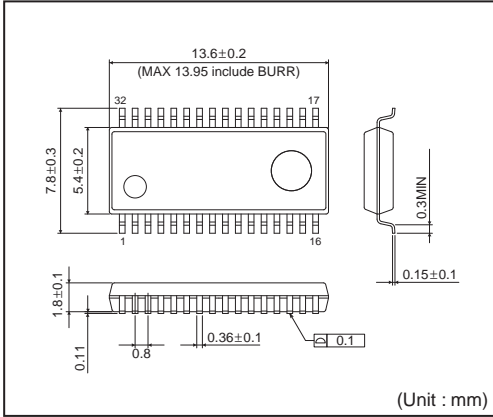
F S

Package
 FS: SSOP-A32
 FV: SSOP-B40
 GUW: VBGA048W040
 KV: VQFP48C
 KV: VQFP64

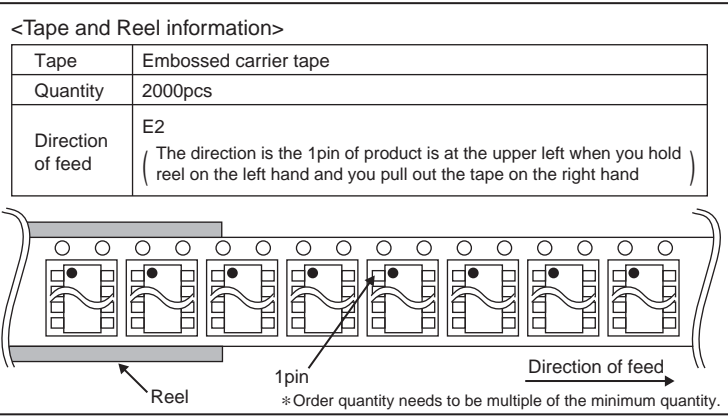
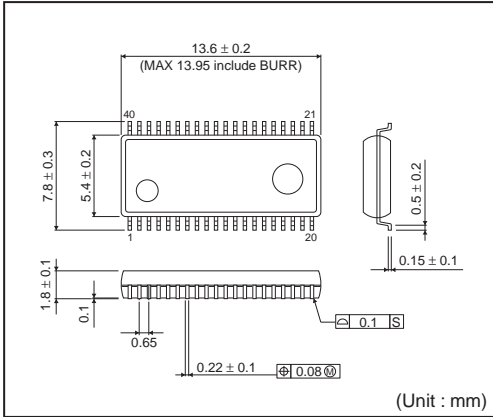
E 2

Packaging and forming specification
 E2: Embossed tape and reel

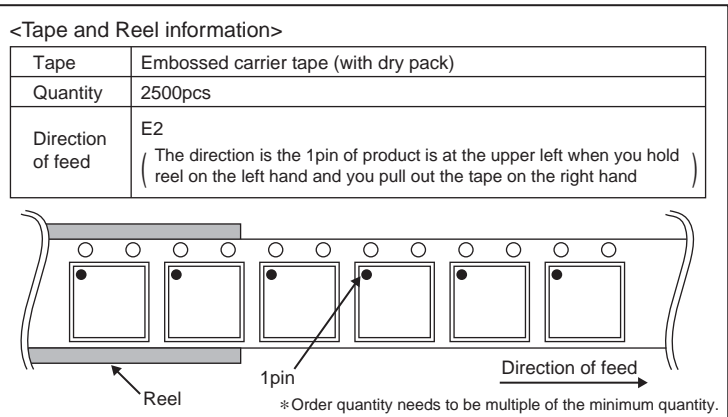
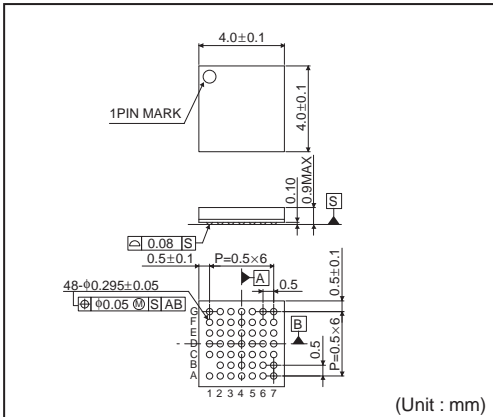
SSOP-A32



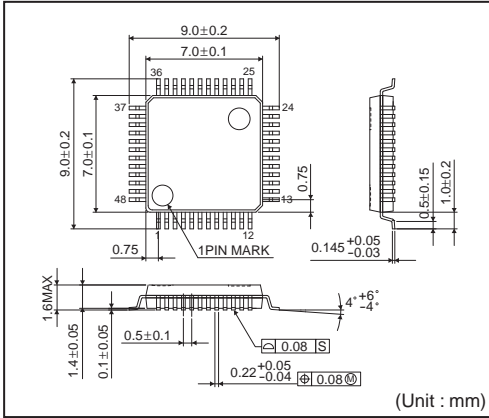
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VBGA048W040

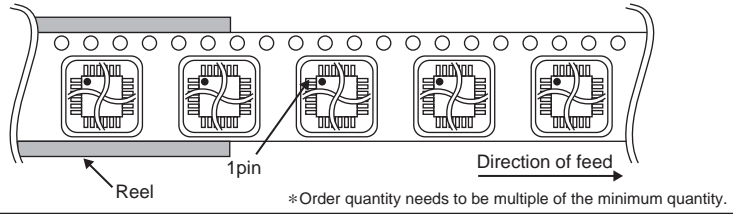


VQFP48C

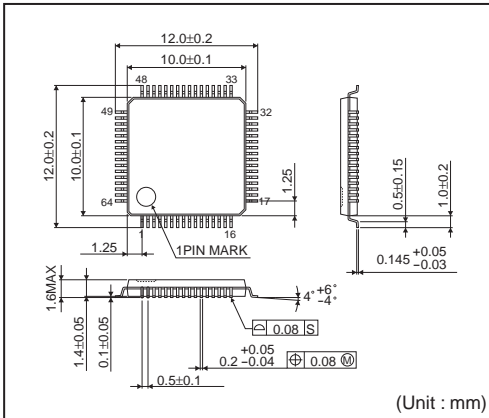


<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	1500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)

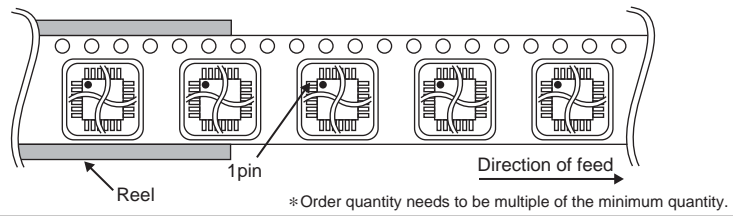


VQFP64



<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	1000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



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