STM32F415xx
STM32F417xx

ARM Cortex-M4 32b MCU+FPU, 210DMIPS, up to 1MB Flash/192+4KB RAM, crypto, USB OTG HS/FS, Ethernet, 17 TIMs, 3 ADCs, 15 comm. interfaces & camera

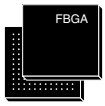
Datasheet - production data

Features

- Core: ARM® 32-bit Cortex®-M4 CPU with FPU, Adaptive real-time accelerator (ART Accelerator™) allowing 0-wait state execution from Flash memory, frequency up to 168 MHz, memory protection unit, 210 DMIPS/ 1.25 DMIPS/MHz (Dhrystone 2.1), and DSP instructions
- Memories
  - Up to 1 Mbyte of Flash memory
  - Up to 192+4 Kbytes of SRAM including 64-Kbyte of CCM (core coupled memory) data RAM
  - Flexible static memory controller supporting Compact Flash, SRAM, PSRAM, NOR and NAND memories
- LCD parallel interface, 8080/6800 modes
- Clock, reset and supply management
  - 1.8 V to 3.6 V application supply and I/Os
  - POR, PDR, PVD and BOR
  - 4-to-26 MHz crystal oscillator
  - Internal 16 MHz factory-trimmed RC (1% accuracy)
  - 32 kHz oscillator for RTC with calibration
  - Internal 32 kHz RC with calibration
- Low-power operation
  - Sleep, Stop and Standby modes
  - V_{BAT} supply for RTC, 20×32 bit backup registers + optional 4 KB backup SRAM
- 3×12-bit, 2.4 MSPS A/D converters: up to 24 channels and 7.2 MSPS in triple interleaved mode
- 2×12-bit D/A converters
- General-purpose DMA: 16-stream DMA controller with FIFOs and burst support
- Up to 17 timers: up to twelve 16-bit and two 32-bit timers up to 168 MHz, each with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input
- Debug mode
  - Serial wire debug (SWD) & JTAG interfaces
  - Cortex-M4 Embedded Trace Macrocell™

LQFP64 (10 × 10 mm)
LQFP100 (14 × 14 mm)
LQFP144 (20 × 20 mm)
LQFP176 (24 × 24 mm)

WLCSP90



UFBGA176
(10 × 10 mm)

- Up to 140 I/O ports with interrupt capability
  - Up to 136 fast I/Os up to 84 MHz
  - Up to 138 5 V-tolerant I/Os
- Up to 15 communication interfaces
  - Up to 3 × I^2C interfaces (SMBus/PMBus)
  - Up to 4 USARTs/2 UARTs (10.5 Mbit/s, ISO 7816 interface, LIN, IrDA, modem control)
  - Up to 3 SPIs (42 Mbits/s), 2 with muxed full-duplex I^2S to achieve audio class accuracy via internal audio PLL or external clock
  - 2 × CAN interfaces (2.0B Active)
  - SDIO interface
- Advanced connectivity
  - USB 2.0 full-speed device/host/OTG controller with on-chip PHY
  - USB 2.0 high-speed/full-speed device/host/OTG controller with dedicated DMA, on-chip full-speed PHY and ULPI
  - 10/100 Ethernet MAC with dedicated DMA: supports IEEE 1588v2 hardware, MII/RMII
- 8- to 14-bit parallel camera interface up to 54 Mbytes/s
- Cryptographic acceleration: hardware acceleration for AES 128, 192, 256, Triple DES, HASH (MD5, SHA-1), and HMAC
- True random number generator
- CRC calculation unit
- 96-bit unique ID
- RTC: subsecond accuracy, hardware calendar

Table 1. Device summary

Reference	Part number
STM32F415xx	STM32F415RG, STM32F415VG, STM32F415ZG, STM32F415OG
STM32F417xx	STM32F417VG, STM32F417IG, STM32F417ZG, STM32F417VE, STM32F417ZE, STM32F417IE

Contents

List of tables

List of figures

1 Introduction

This datasheet provides the description of the STM32F415xx and STM32F417xx lines of microcontrollers. For more details on the whole STMicroelectronics STM32™ family, please refer to *Section 2.1: Full compatibility throughout the family*.

The STM32F415xx and STM32F417xx datasheet should be read in conjunction with the STM32F4xx reference manual which is available from the STMicroelectronics website *www.st.com*.

For information on the Cortex®-M4 core, please refer to the Cortex®-M4 programming manual (PM0214) available from *www.st.com*.

2 Description

The STM32F415xx and STM32F417xx family is based on the high-performance ARM® Cortex®-M4 32-bit RISC core operating at a frequency of up to 168 MHz. The Cortex-M4 core features a Floating point unit (FPU) single precision which supports all ARM single-precision data-processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) which enhances application security.

The STM32F415xx and STM32F417xx family incorporates high-speed embedded memories (Flash memory up to 1 Mbyte, up to 192 Kbytes of SRAM), up to 4 Kbytes of backup SRAM, and an extensive range of enhanced I/Os and peripherals connected to two APB buses, three AHB buses and a 32-bit multi-AHB bus matrix.

All devices offer three 12-bit ADCs, two DACs, a low-power RTC, twelve general-purpose 16-bit timers including two PWM timers for motor control, two general-purpose 32-bit timers. a true random number generator (RNG), and a cryptographic acceleration cell. They also feature standard and advanced communication interfaces.

- Up to three I^2Cs
- Three SPIs, two I^2Ss full duplex. To achieve audio class accuracy, the I2S peripherals can be clocked via a dedicated internal audio PLL or via an external clock to allow synchronization.
- Four USARTs plus two UARTs
- An USB OTG full-speed and a USB OTG high-speed with full-speed capability (with the ULPI),
- Two CANs
- An SDIO/MMC interface
- Ethernet and the camera interface available on STM32F417xx devices only.

New advanced peripherals include an SDIO, an enhanced flexible static memory control (FSMC) interface (for devices offered in packages of 100 pins and more), a camera interface for CMOS sensors and a cryptographic acceleration cell. Refer to *Table 2: STM32F415xx and STM32F417xx: features and peripheral counts* for the list of peripherals available on each part number.

The STM32F415xx and STM32F417xx family operates in the –40 to +105 °C temperature range from a 1.8 to 3.6 V power supply. The supply voltage can drop to 1.7 V when the device operates in the 0 to 70 °C temperature range using an external power supply supervisor: refer to *Section : Internal reset OFF*. A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F415xx and STM32F417xx family offers devices in various packages ranging from 64 pins to 176 pins. The set of included peripherals changes with the device chosen.

These features make the STM32F415xx and STM32F417xx microcontroller family suitable for a wide range of applications:

- Motor drive and application control
- Medical equipment
- Industrial applications: PLC, inverters, circuit breakers
- Printers, and scanners
- Alarm systems, video intercom, and HVAC
- Home audio appliances

Figure 5 shows the general block diagram of the device family.

Table 2. STM32F415xx and STM32F417xx: features and peripheral counts

Peripherals		STM32F415RG	STM32F415OG	STM32F415VG	STM32F415ZG	STM32F417Vx		STM32F417Zx		STM32F417Ix	
Flash memory in Kbytes		1024				512	1024	512	1024	512	1024
SRAM in Kbytes	System	192(112+16+64)									
	Backup	4									
FSMC memory controller		No	Yes(1)								
Ethernet		No				Yes					
Timers	General-purpose	10									
	Advanced-control	2									
	Basic	2									
	IWDG	Yes									
	WWDG	Yes									
	RTC	Yes									
Random number generator		Yes									
Communication interfaces	SPI / I^2S	3/2 (full duplex)(2)									
	I^2C	3									
	USART/UART	4/2									
	USB OTG FS	Yes									
	USB OTG HS	Yes									
	CAN	2									
	SDIO	Yes									
Camera interface		No				Yes					
Cryptography		Yes									

Table 2. STM32F415xx and STM32F417xx: features and peripheral counts

Peripherals	STM32F415RG	STM32F415OG	STM32F415VG	STM32F415ZG	STM32F417Vx	STM32F417Zx	STM32F417Ix
GPIOs	51	72	82	114	82	114	140
12-bit ADC Number of channels	3						
	16	13	16	24	16	24	24
12-bit DAC Number of channels	Yes 2						
Maximum CPU frequency	168 MHz						
Operating voltage	1.8 to 3.6 V(3)						
Operating temperatures	Ambient temperatures: –40 to +85 °C /–40 to +105 °C						
	Junction temperature: –40 to + 125 °C						
Package	LQFP64	WLCSP90	LQFP100	LQFP144	LQFP100	LQFP144	UFBGA176 LQFP176

1. For the LQFP100 and WLCSP90 packages, only FSMC Bank1 or Bank2 are available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 Chip Select. Bank2 can only support a 16- or 8-bit NAND Flash memory using the NCE2 Chip Select. The interrupt line cannot be used since Port G is not available in this package.
2. The SPI2 and SPI3 interfaces give the flexibility to work in an exclusive way in either the SPI mode or the I2S audio mode.
3. V_{DD}/V_{DDA} minimum value of 1.7 V is obtained when the device operates in reduced temperature range, and with the use of an external power supply supervisor (refer to *Section : Internal reset OFF*).

2.1 Full compatibility throughout the family

The STM32F415xx and STM32F417xx are part of the STM32F4 family. They are fully pin-to-pin, software and feature compatible with the STM32F2xx devices, allowing the user to try different memory densities, peripherals, and performances (FPU, higher frequency) for a greater degree of freedom during the development cycle.

The STM32F415xx and STM32F417xx devices maintain a close compatibility with the whole STM32F10xxx family. All functional pins are pin-to-pin compatible. The STM32F415xx and STM32F417xx, however, are not drop-in replacements for the STM32F10xxx devices: the two families do not have the same power scheme, and so their power pins are different. Nonetheless, transition from the STM32F10xxx to the STM32F41xxx family remains simple as only a few pins are impacted.

Figure 4, *Figure 3*, *Figure 2*, and *Figure 1* give compatible board designs between the STM32F41xxx, STM32F2, and STM32F10xxx families.

Figure 1. Compatible board design between STM32F10xx/STM32F41xxx for LQFP64

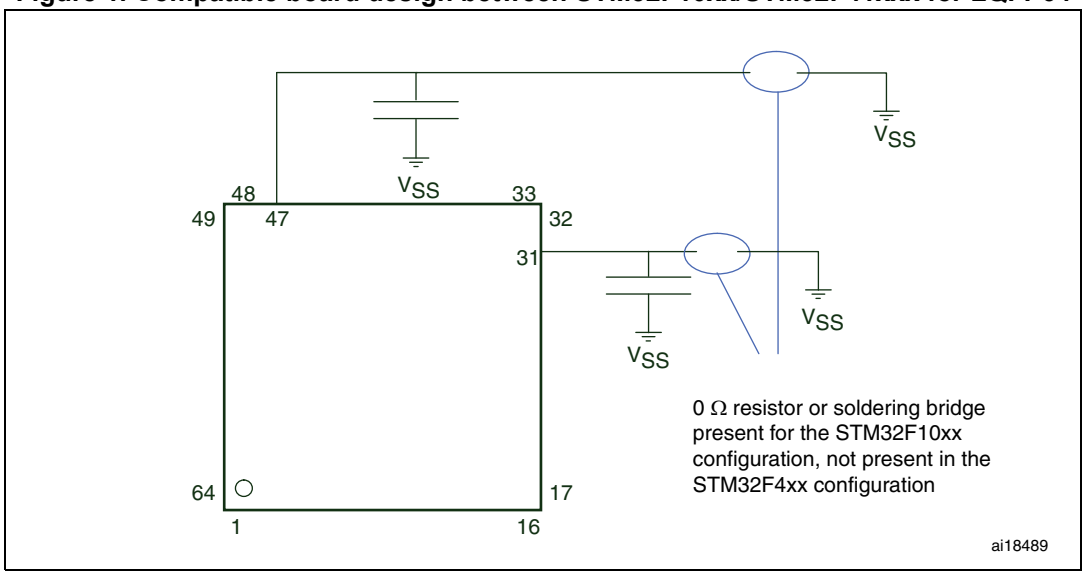


Figure 2. Compatible board design STM32F10xx/STM32F2/STM32F41xxx for LQFP100 package

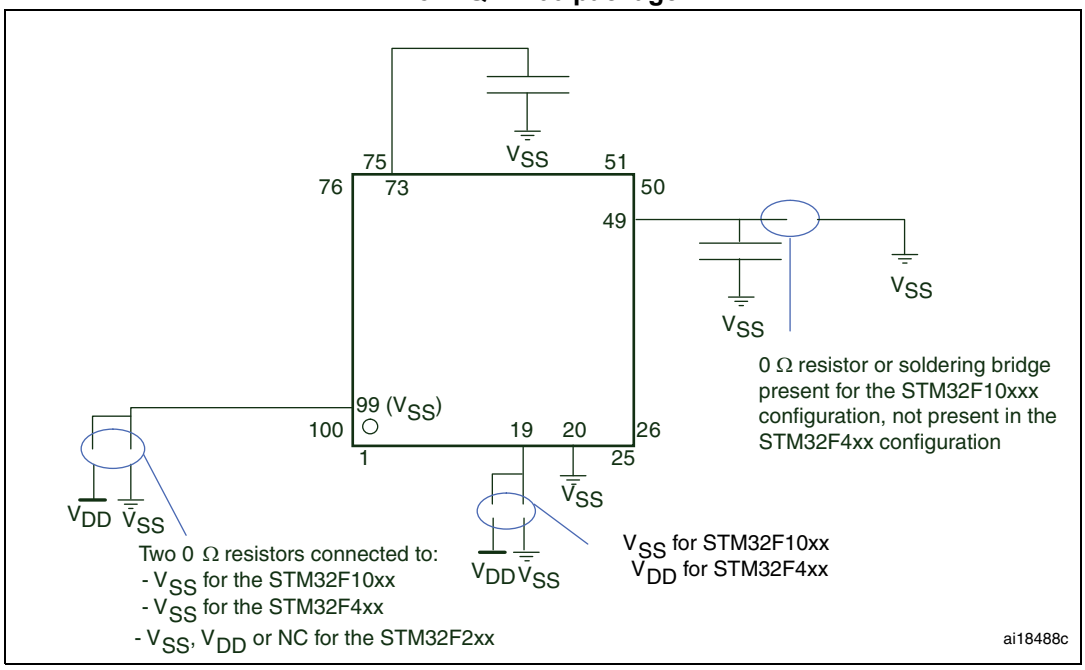


Figure 3. Compatible board design between STM32F10xx/STM32F2/STM32F41xxx for LQFP144 package

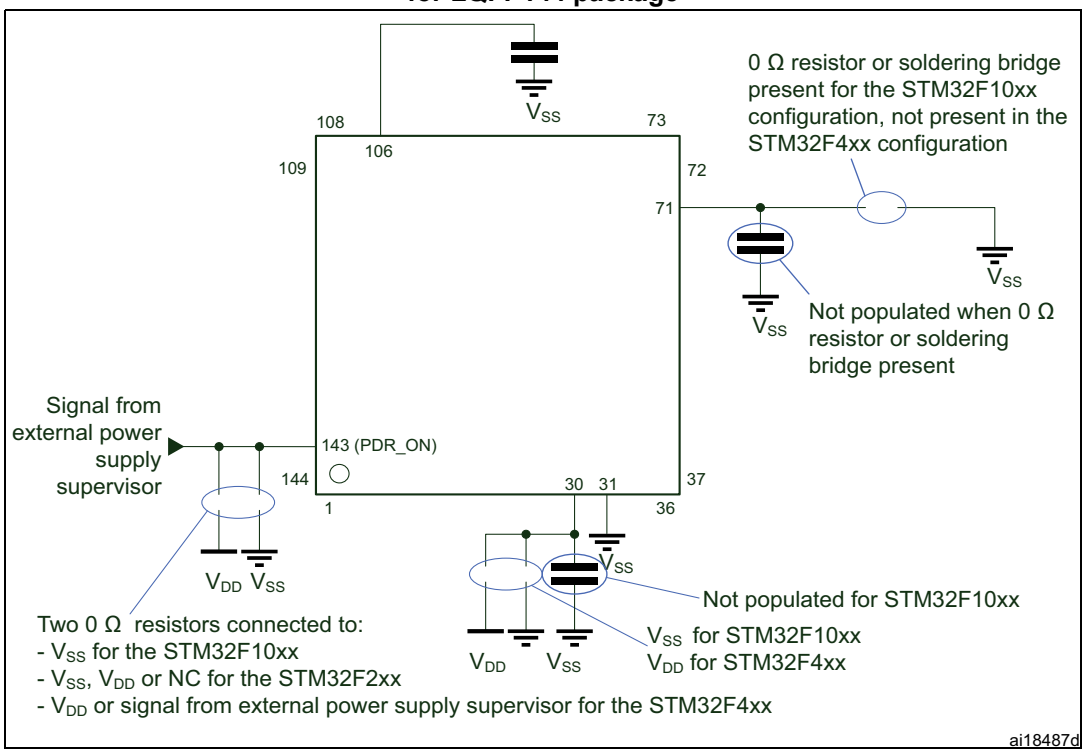
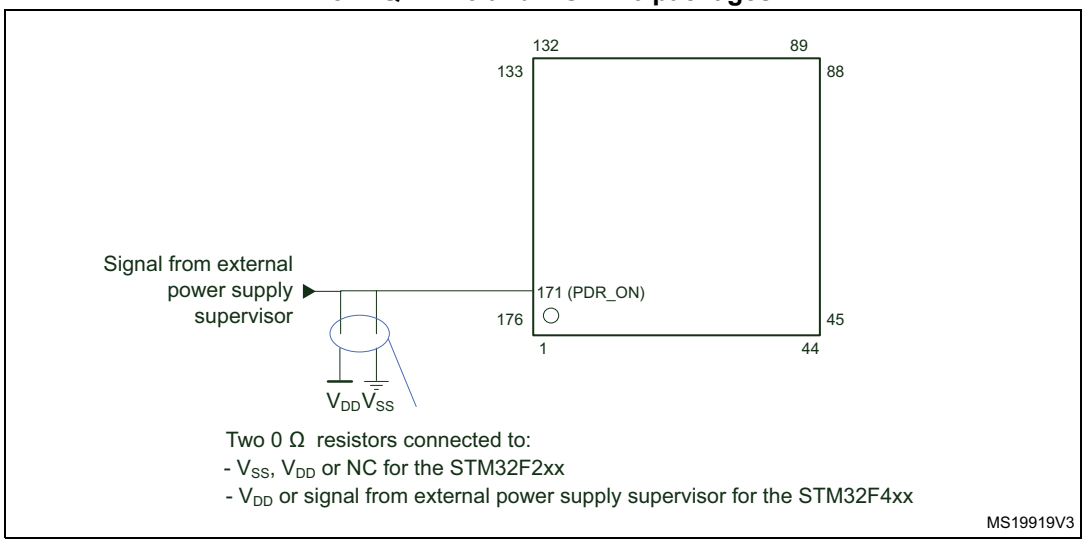
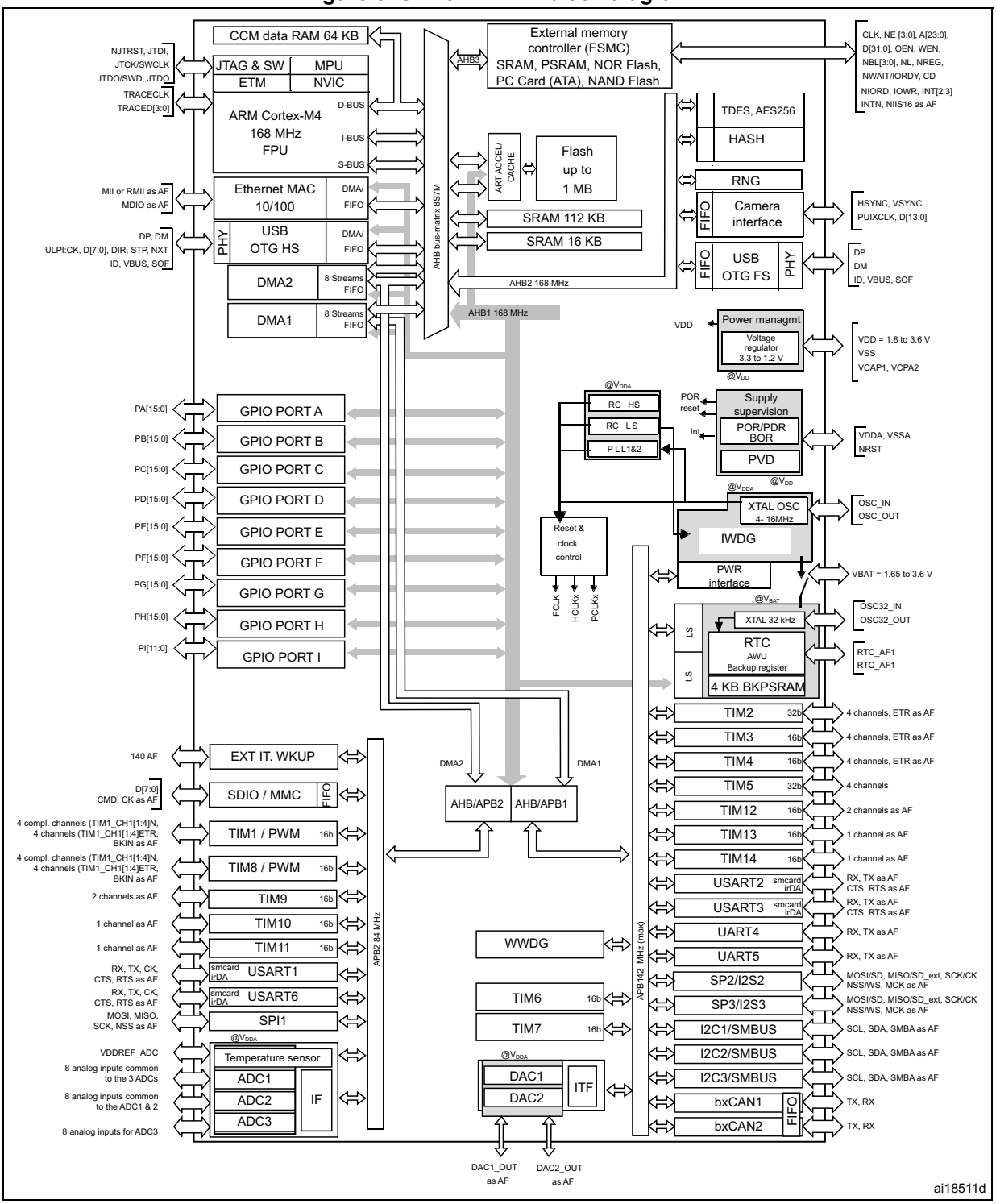


Figure 4. Compatible board design between STM32F2 and STM32F41xxx for LQFP176 and BGA176 packages



2.2 Device overview

Figure 5. STM32F41xxx block diagram



1. The timers connected to APB2 are clocked from TIMxCLK up to 168 MHz, while the timers connected to APB1 are clocked from TIMxCLK either up to 84 MHz or 168 MHz, depending on TIMPRE bit configuration in the RCC_DCKCFGR register.
2. The camera interface and ethernet are available only on STM32F417xx devices.

2.2.1 ARM® Cortex®-M4 core with FPU and embedded Flash and SRAM

The ARM Cortex-M4 processor with FPU is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM Cortex-M4 32-bit RISC processor with FPU features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Its single precision FPU (floating point unit) speeds up software development by using metalanguage development tools, while avoiding saturation.

The STM32F415xx and STM32F417xx family is compatible with all ARM tools and software.

Figure 5 shows the general block diagram of the STM32F41xxx family.

Note: Cortex-M4 with FPU is binary compatible with Cortex-M3.

2.2.2 Adaptive real-time memory accelerator (ART Accelerator™)

The ART Accelerator™ is a memory accelerator which is optimized for STM32 industry-standard ARM® Cortex®-M4 with FPU processors. It balances the inherent performance advantage of the ARM Cortex-M4 with FPU over Flash memory technologies, which normally requires the processor to wait for the Flash memory at higher frequencies.

To release the processor full 210 DMIPS performance at this frequency, the accelerator implements an instruction prefetch queue and branch cache, which increases program execution speed from the 128-bit Flash memory. Based on CoreMark benchmark, the performance achieved thanks to the ART accelerator is equivalent to 0 wait state program execution from Flash memory at a CPU frequency up to 168 MHz.

2.2.3 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

2.2.4 Embedded Flash memory

The STM32F41xxx devices embed a Flash memory of 512 Kbytes or 1 Mbytes available for storing programs and data.

2.2.5 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a software signature during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

2.2.6 Embedded SRAM

All STM32F41xxx products embed:

- Up to 192 Kbytes of system SRAM including 64 Kbytes of CCM (core coupled memory) data RAM

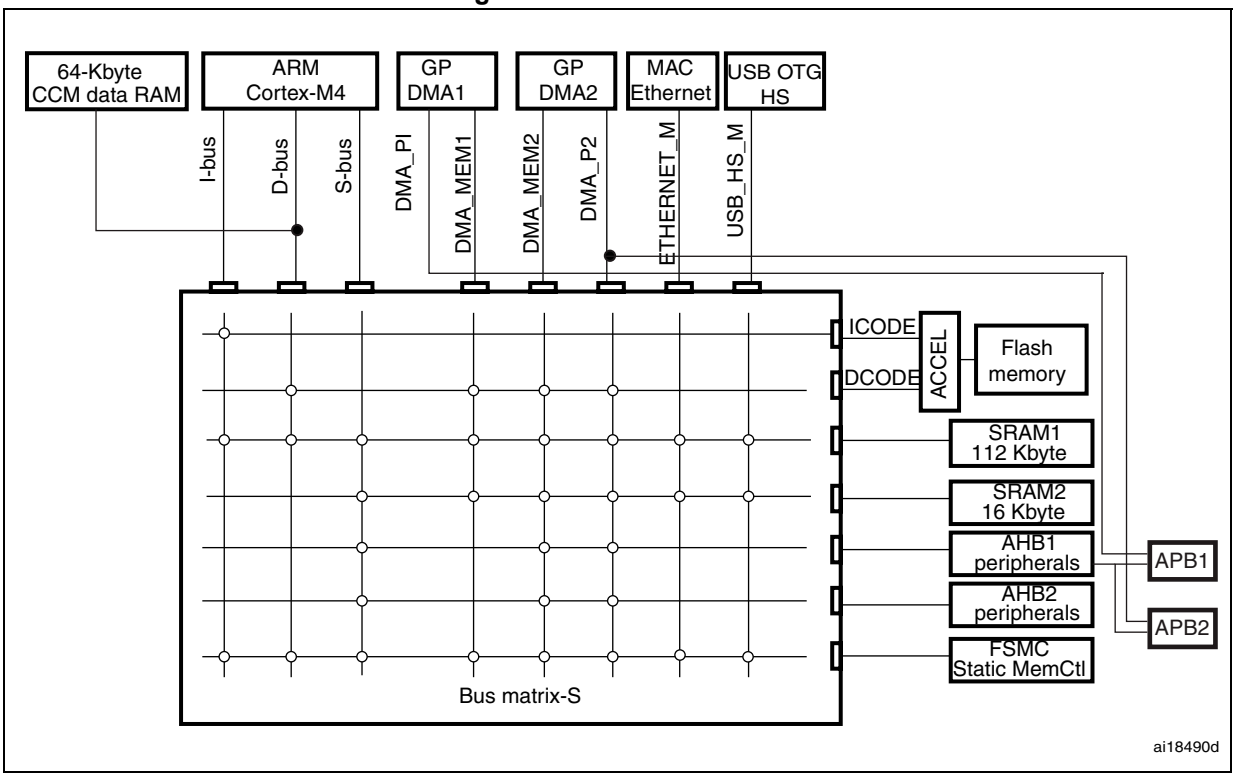
  RAM memory is accessed (read/write) at CPU clock speed with 0 wait states.
- 4 Kbytes of backup SRAM

  This area is accessible only from the CPU. Its content is protected against possible unwanted write accesses, and is retained in Standby or V_{BAT} mode.

2.2.7 Multi-AHB bus matrix

The 32-bit multi-AHB bus matrix interconnects all the masters (CPU, DMAs, Ethernet, USB HS) and the slaves (Flash memory, RAM, FSMC, AHB and APB peripherals) and ensures a seamless and efficient operation even when several high-speed peripherals work simultaneously.

Figure 6. Multi-AHB matrix



2.2.8 DMA controller (DMA)

The devices feature two general-purpose dual-port DMAs (DMA1 and DMA2) with 8 streams each. They are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. They feature dedicated FIFOs for APB/AHB peripherals, support burst transfer and are designed to provide the maximum peripheral bandwidth (AHB/APB).

The two DMA controllers support circular buffer management, so that no specific code is needed when the controller reaches the end of the buffer. The two DMA controllers also have a double buffering feature, which automates the use and switching of two memory buffers without requiring any special code.

Each stream is connected to dedicated hardware DMA requests, with support for software trigger on each stream. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals:

- SPI and I^2S
- I^2C
- USART
- General-purpose, basic and advanced-control timers TIMx
- DAC
- SDIO
- Cryptographic acceleration
- Camera interface (DCMI)
- ADC.

2.2.9 Flexible static memory controller (FSMC)

The FSMC is embedded in the STM32F415xx and STM32F417xx family. It has four Chip Select outputs supporting the following modes: PCCard/Compact Flash, SRAM, PSRAM, NOR Flash and NAND Flash.

Functionality overview:

- Write FIFO
- Maximum FSMC_CLK frequency for synchronous accesses is 60 MHz.

LCD parallel interface

The FSMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost-effective graphic applications using LCD modules with embedded controllers or high performance solutions using external controllers with dedicated acceleration.

2.2.10 Nested vectored interrupt controller (NVIC)

The STM32F415xx and STM32F417xx embed a nested vectored interrupt controller able to manage 16 priority levels, and handle up to 82 maskable interrupt channels plus the 16 interrupt lines of the Cortex®-M4 with FPU core.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving, higher-priority interrupts
- Support tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimum interrupt latency.

2.2.11 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 23 edge-detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger

event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 140 GPIOs can be connected to the 16 external interrupt lines.

2.2.12 Clocks and startup

On reset the 16 MHz internal RC oscillator is selected as the default CPU clock. The 16 MHz internal RC oscillator is factory-trimmed to offer 1% accuracy over the full temperature range. The application can then select as system clock either the RC oscillator or an external 4-26 MHz clock source. This clock can be monitored for failure. If a failure is detected, the system automatically switches back to the internal RC oscillator and a software interrupt is generated (if enabled). This clock source is input to a PLL thus allowing to increase the frequency up to 168 MHz. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example if an indirectly used external oscillator fails).

Several prescalers allow the configuration of the three AHB buses, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the three AHB buses is 168 MHz while the maximum frequency of the high-speed APB domains is 84 MHz. The maximum allowed frequency of the low-speed APB domain is 42 MHz.

The devices embed a dedicated PLL (PLLI2S) which allows to achieve audio class performance. In this case, the I^2S master clock can generate all standard sampling frequencies from 8 kHz to 192 kHz.

2.2.13 Boot modes

At startup, boot pins are used to select one out of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in system memory. It is used to reprogram the Flash memory by using USART1 (PA9/PA10), USART3 (PC10/PC11 or PB10/PB11), CAN2 (PB5/PB13), USB OTG FS in Device mode (PA11/PA12) through DFU (device firmware upgrade).

2.2.14 Power supply schemes

- V_{DD} = 1.8 to 3.6 V: external power supply for I/Os and the internal regulator (when enabled), provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 1.8 to 3.6 V: external analog power supplies for ADC, DAC, Reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.
- V_{BAT} = 1.65 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

Refer to *Figure 21: Power supply scheme* for more details.

Note: V_{DD}/V_{DDA} minimum value of 1.7 V is obtained when the device operates in reduced temperature range, and with the use of an external power supply supervisor (refer to Section : Internal reset OFF).

Refer to Table 2 in order to identify the packages supporting this option.

2.2.15 Power supply supervisor

Internal reset ON

On packages embedding the PDR_ON pin, the power supply supervisor is enabled by holding PDR_ON high. On all other packages, the power supply supervisor is always enabled.

The device has an integrated power-on reset (POR) / power-down reset (PDR) circuitry coupled with a Brownout reset (BOR) circuitry. At power-on, POR/PDR is always active and ensures proper operation starting from 1.8 V. After the 1.8 V POR threshold level is reached, the option byte loading process starts, either to confirm or modify default BOR threshold levels, or to disable BOR permanently. Three BOR thresholds are available through option bytes. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR}, without the need for an external reset circuit.

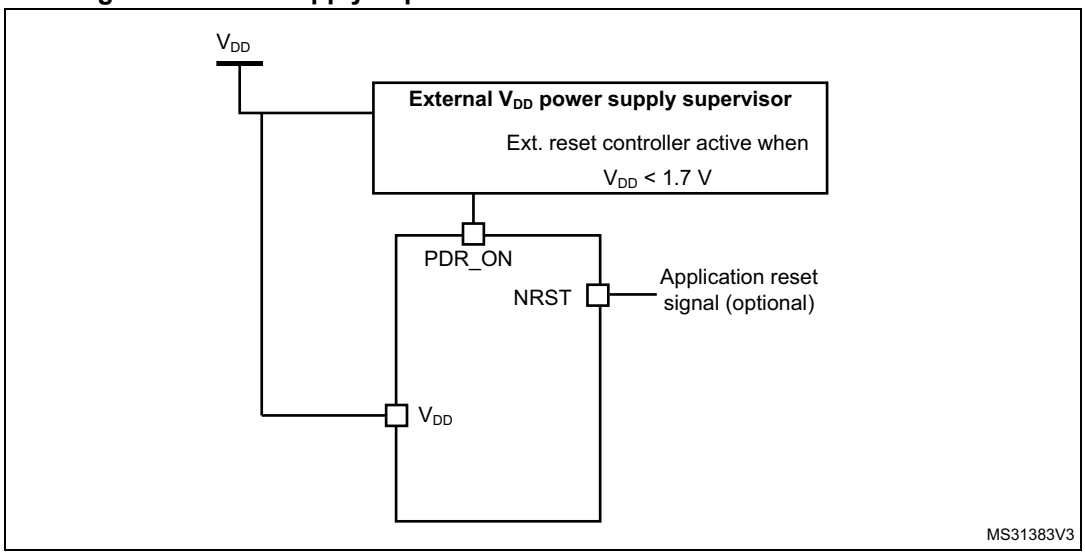
The device also features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

Internal reset OFF

This feature is available only on packages featuring the PDR_ON pin. The internal power-on reset (POR) / power-down reset (PDR) circuitry is disabled with the PDR_ON pin.

An external power supply supervisor should monitor V_{DD} and should maintain the device in reset mode as long as V_{DD} is below a specified threshold. PDR_ON should be connected to this external power supply supervisor. Refer to *Figure 7: Power supply supervisor interconnection with internal reset OFF*.

Figure 7. Power supply supervisor interconnection with internal reset OFF



1. PDR = 1.7 V for reduce temperature range; PDR = 1.8 V for all temperature range.

The V_{DD} specified threshold, below which the device must be maintained under reset, is 1.8 V (see *Figure 7*). This supply voltage can drop to 1.7 V when the device operates in the 0 to 70 °C temperature range.

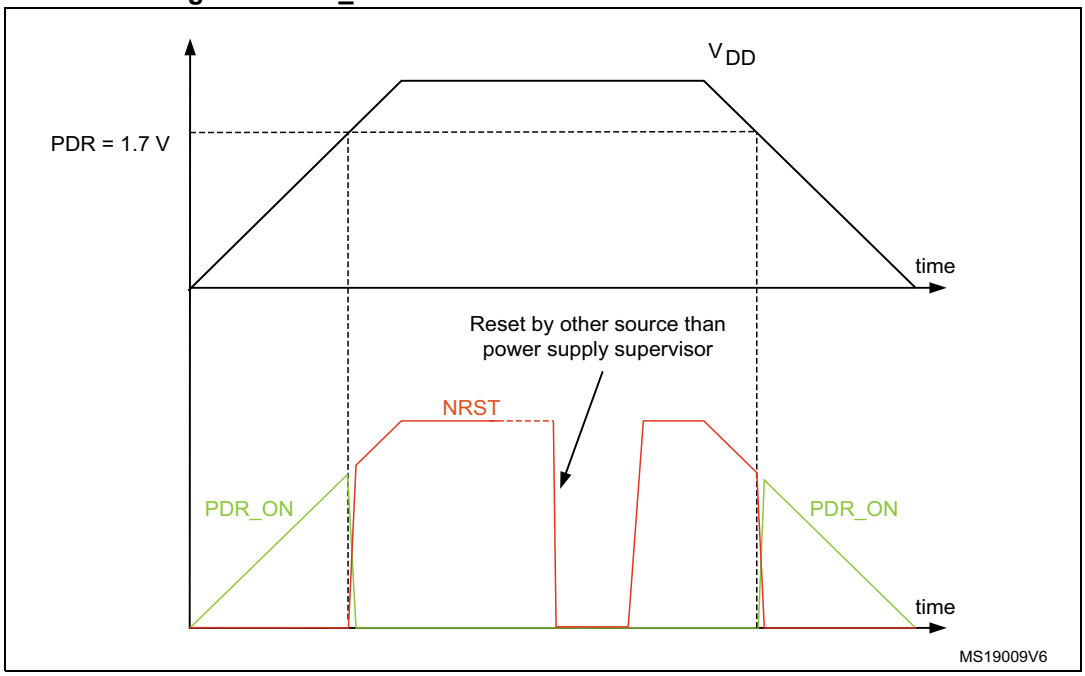
A comprehensive set of power-saving mode allows to design low-power applications.

When the internal reset is OFF, the following integrated features are no more supported:

- The integrated power-on reset (POR) / power-down reset (PDR) circuitry is disabled
- The brownout reset (BOR) circuitry is disabled
- The embedded programmable voltage detector (PVD) is disabled
- V_{BAT} functionality is no more available and V_{BAT} pin should be connected to V_{DD}

All packages, except for the LQFP64 and LQFP100, allow to disable the internal reset through the PDR_ON signal.

Figure 8. PDR_ON and NRST control with internal reset OFF



1. PDR = 1.7 V for reduce temperature range; PDR = 1.8 V for all temperature range.

2.2.16 Voltage regulator

The regulator has four operating modes:

- Regulator ON
  - Main regulator mode (MR)
  - Low-power regulator (LPR)
  - Power-down
- Regulator OFF

Regulator ON

On packages embedding the BYPASS_REG pin, the regulator is enabled by holding BYPASS_REG low. On all other packages, the regulator is always enabled.

There are three power modes configured by software when regulator is ON:

- MR is used in the nominal regulation mode (With different voltage scaling in Run)

  In Main regulator mode (MR mode), different voltage scaling are provided to reach the best compromise between maximum frequency and dynamic power consumption. Refer to *Table 14: General operating conditions*.
- LPR is used in the Stop modes

  The LP regulator mode is configured by software when entering Stop mode.
- Power-down is used in Standby mode.

  The Power-down mode is activated only when entering in Standby mode. The regulator output is in high impedance and the kernel circuitry is powered down, inducing zero consumption. The contents of the registers and SRAM are lost)

Two external ceramic capacitors should be connected on V_{CAP_1} & V_{CAP_2} pin. Refer to *Figure 21: Power supply scheme* and *Figure 16: VCAP_1/VCAP_2 operating conditions*.

All packages have regulator ON feature.

Regulator OFF

This feature is available only on packages featuring the BYPASS_REG pin. The regulator is disabled by holding BYPASS_REG high. The regulator OFF mode allows to supply externally a V_{12} voltage source through V_{CAP_1} and V_{CAP_2} pins.

Since the internal voltage scaling is not manage internally, the external voltage value must be aligned with the targeted maximum frequency. Refer to *Table 14: General operating conditions*.

The two 2.2 µF ceramic capacitors should be replaced by two 100 nF decoupling capacitors.

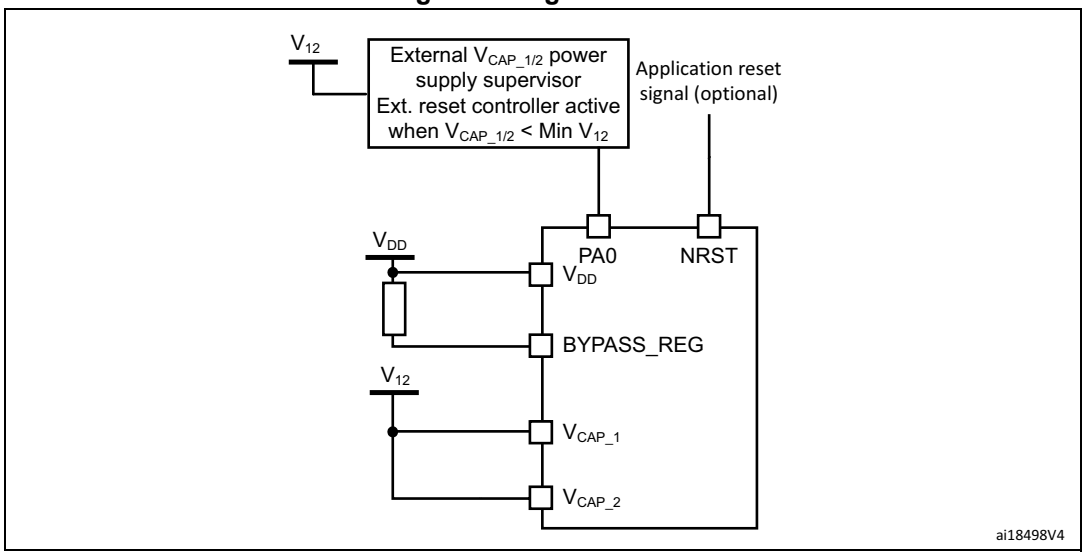
Refer to *Figure 21: Power supply scheme*

When the regulator is OFF, there is no more internal monitoring on V_{12}. An external power supply supervisor should be used to monitor the V_{12} of the logic power domain. PA0 pin should be used for this purpose, and act as power-on reset on V_{12} power domain.

In regulator OFF mode the following features are no more supported:

- PA0 cannot be used as a GPIO pin since it allows to reset a part of the V_{12} logic power domain which is not reset by the NRST pin.
- As long as PA0 is kept low, the debug mode cannot be used under power-on reset. As a consequence, PA0 and NRST pins must be managed separately if the debug connection under reset or pre-reset is required.
- The standby mode is not available

Figure 9. Regulator OFF

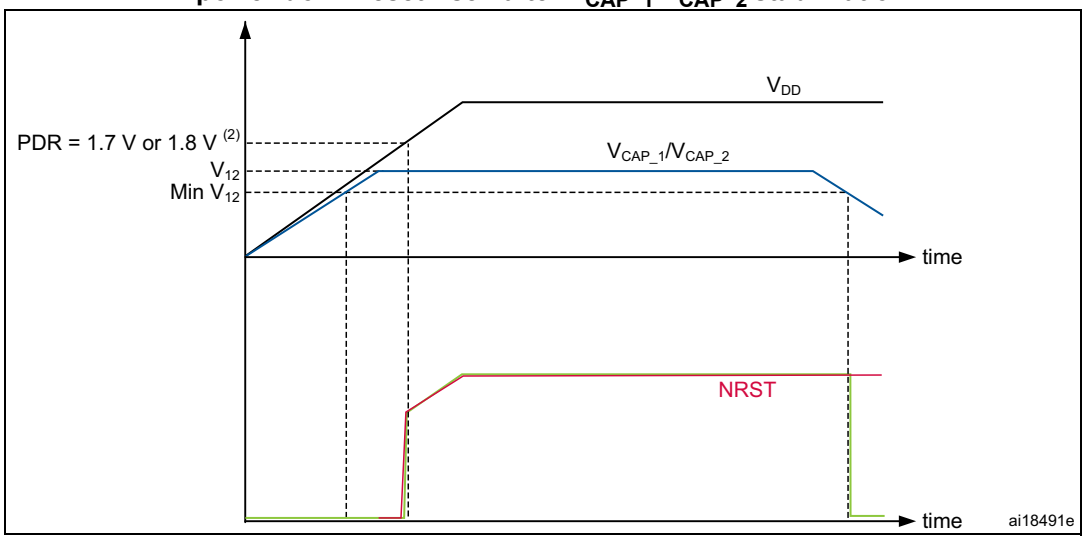


The following conditions must be respected:

- V_{DD} should always be higher than V_{CAP_1} and V_{CAP_2} to avoid current injection between power domains.
- If the time for V_{CAP_1} and V_{CAP_2} to reach V_{12} minimum value is faster than the time for V_{DD} to reach 1.8 V, then PA0 should be kept low to cover both conditions: until V_{CAP_1} and V_{CAP_2} reach V_{12} minimum value and until V_{DD} reaches 1.8 V (see *Figure 10*).
- Otherwise, if the time for V_{CAP_1} and V_{CAP_2} to reach V_{12} minimum value is slower than the time for V_{DD} to reach 1.8 V, then PA0 could be asserted low externally (see *Figure 11*).
- If V_{CAP_1} and V_{CAP_2} go below V_{12} minimum value and V_{DD} is higher than 1.8 V, then a reset must be asserted on PA0 pin.

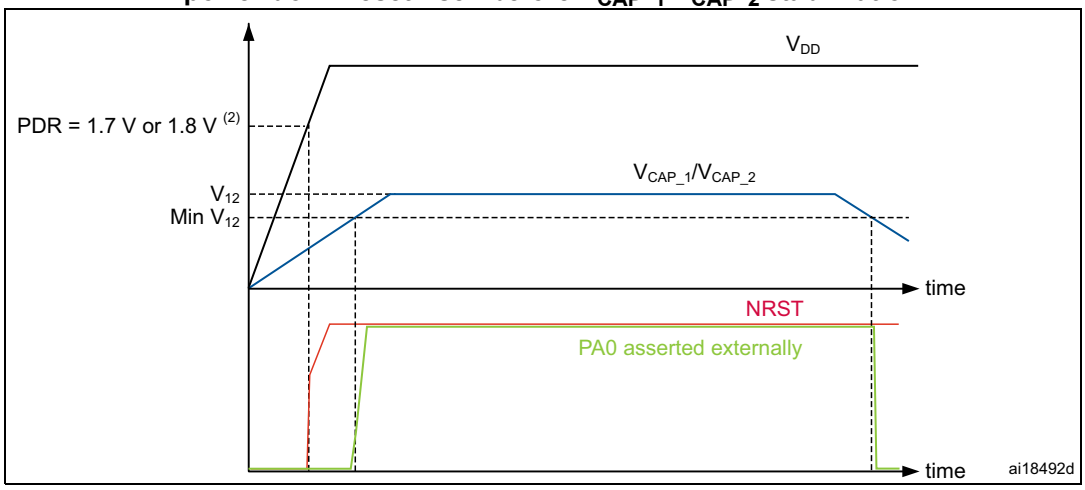
Note: The minimum value of V_{12} depends on the maximum frequency targeted in the application (see Table 14: General operating conditions).

Figure 10. Startup in regulator OFF mode: slow V_{DD} slope - power-down reset risen after V_{CAP_1}/V_{CAP_2} stabilization



1. This figure is valid both whatever the internal reset mode (ON or OFF).
2. PDR = 1.7 V for reduced temperature range; PDR = 1.8 V for all temperature ranges.

Figure 11. Startup in regulator OFF mode: fast V_{DD} slope - power-down reset risen before V_{CAP_1}/V_{CAP_2} stabilization



1. This figure is valid both whatever the internal reset mode (ON or OFF).
2. PDR = 1.7 V for a reduced temperature range; PDR = 1.8 V for all temperature ranges.

2.2.17 Regulator ON/OFF and internal reset ON/OFF availability

Table 3. Regulator ON/OFF and internal reset ON/OFF availability

	Regulator ON	Regulator OFF	Internal reset ON	Internal reset OFF
LQFP64 LQFP100	Yes	No	Yes	No
LQFP144			Yes PDR_ON set to V_{DD}	Yes PDR_ON connected to an external power supply supervisor
WLCSP90 UFBGA176 LQFP176	Yes BYPASS_REG set to V_{SS}	Yes BYPASS_REG set to V_{DD}		

2.2.18 Real-time clock (RTC), backup SRAM and backup registers

The backup domain of the STM32F415xx and STM32F417xx includes:

- The real-time clock (RTC)
- 4 Kbytes of backup SRAM
- 20 backup registers

The real-time clock (RTC) is an independent BCD timer/counter. Dedicated registers contain the second, minute, hour (in 12/24 hour), week day, date, month, year, in BCD (binary-coded decimal) format. Correction for 28, 29 (leap year), 30, and 31 day of the month are performed automatically. The RTC provides a programmable alarm and programmable periodic interrupts with wakeup from Stop and Standby modes. The sub-seconds value is also available in binary format.

It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low-power RC oscillator or the high-speed external clock divided by 128. The internal low-speed RC has a typical frequency of 32 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural quartz deviation.

Two alarm registers are used to generate an alarm at a specific time and calendar fields can be independently masked for alarm comparison. To generate a periodic interrupt, a 16-bit programmable binary auto-reload downcounter with programmable resolution is available and allows automatic wakeup and periodic alarms from every 120 µs to every 36 hours.

A 20-bit prescaler is used for the time base clock. It is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

The 4-Kbyte backup SRAM is an EEPROM-like memory area. It can be used to store data which need to be retained in V_{BAT} and standby mode. This memory area is disabled by default to minimize power consumption (see *Section 2.2.19: Low-power modes*). It can be enabled by software.

The backup registers are 32-bit registers used to store 80 bytes of user application data when V_{DD} power is not present. Backup registers are not reset by a system, a power reset, or when the device wakes up from the Standby mode (see *Section 2.2.19: Low-power modes*).

Additional 32-bit registers contain the programmable alarm subseconds, seconds, minutes, hours, day, and date.

Like backup SRAM, the RTC and backup registers are supplied through a switch that is powered either from the V_{DD} supply when present or from the V_{BAT} pin.

2.2.19 Low-power modes

The STM32F415xx and STM32F417xx support three low-power modes to achieve the best compromise between low-power consumption, short startup time and available wakeup sources:

- **Sleep mode**

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop mode**

  The Stop mode achieves the lowest power consumption while retaining the contents of SRAM and registers. All clocks in the V_{12} domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low-power mode.

  The device can be woken up from the Stop mode by any of the EXTI line (the EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm / wakeup / tamper / time stamp events, the USB OTG FS/HS wakeup or the Ethernet wakeup).

- **Standby mode**

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire V_{12} domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, the SRAM and register contents are lost except for registers in the backup domain and the backup SRAM when selected.

  The device exits the Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm / wakeup / tamper /time stamp event occurs.

  The standby mode is not supported when the embedded voltage regulator is bypassed and the V_{12} domain is controlled by an external power.

2.2.20 V_{BAT} operation

The V_{BAT} pin allows to power the device V_{BAT} domain from an external battery, an external supercapacitor, or from V_{DD} when no external battery and an external supercapacitor are present.

V_{BAT} operation is activated when V_{DD} is not present.

The V_{BAT} pin supplies the RTC, the backup registers and the backup SRAM.

Note: When the microcontroller is supplied from V_{BAT}, external interrupts and RTC alarm/events do not exit it from V_{BAT} operation.

When PDR_ON pin is not connected to V_{DD} (internal reset OFF), the V_{BAT} functionality is no more available and V_{BAT} pin should be connected to V_{DD}.

2.2.21 Timers and watchdogs

The STM32F415xx and STM32F417xx devices include two advanced-control timers, eight general-purpose timers, two basic timers and two watchdog timers.

All timer counters can be frozen in debug mode.

Table 4 compares the features of the advanced-control, general-purpose and basic timers.

Table 4. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary output	Max interface clock (MHz)	Max timer clock (MHz)
Advanced -control	TIM1, TIM8	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	Yes	84	168
General purpose	TIM2, TIM5	32-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	42	84
	TIM3, TIM4	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	42	84
	TIM9	16-bit	Up	Any integer between 1 and 65536	No	2	No	84	168
	TIM10 , TIM11	16-bit	Up	Any integer between 1 and 65536	No	1	No	84	168
	TIM12	16-bit	Up	Any integer between 1 and 65536	No	2	No	42	84
	TIM13 , TIM14	16-bit	Up	Any integer between 1 and 65536	No	1	No	42	84
Basic	TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No	42	84

Advanced-control timers (TIM1, TIM8)

The advanced-control timers (TIM1, TIM8) can be seen as three-phase PWM generators multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead times. They can also be considered as complete general-purpose timers. Their 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge- or center-aligned modes)
- One-pulse mode output

If configured as standard 16-bit timers, they have the same features as the general-purpose TIMx timers. If configured as 16-bit PWM generators, they have full modulation capability (0-100%).

The advanced-control timer can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

TIM1 and TIM8 support independent DMA request generation.

General-purpose timers (TIMx)

There are ten synchronizable general-purpose timers embedded in the STM32F41xxx devices (see *Table 4* for differences).

- **TIM2, TIM3, TIM4, TIM5**

  The STM32F41xxx include 4 full-featured general-purpose timers: TIM2, TIM5, TIM3, and TIM4.The TIM2 and TIM5 timers are based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. The TIM3 and TIM4 timers are based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. They all feature 4 independent channels for input capture/output compare, PWM or one-pulse mode output. This gives up to 16 input capture/output compare/PWMs on the largest packages.

  The TIM2, TIM3, TIM4, TIM5 general-purpose timers can work together, or with the other general-purpose timers and the advanced-control timers TIM1 and TIM8 via the Timer Link feature for synchronization or event chaining.

  Any of these general-purpose timers can be used to generate PWM outputs.

  TIM2, TIM3, TIM4, TIM5 all have independent DMA request generation. They are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 4 hall-effect sensors.

- **TIM9, TIM10, TIM11, TIM12, TIM13, and TIM14**

  These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM10, TIM11, TIM13, and TIM14 feature one independent channel, whereas TIM9 and TIM12 have two independent channels for input capture/output compare, PWM or one-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4, TIM5 full-featured general-purpose timers. They can also be used as simple time bases.

Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger and waveform generation. They can also be used as a generic 16-bit time base.

TIM6 and TIM7 support independent DMA request generation.

Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 32 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes.

Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard downcounter. It features:

- A 24-bit downcounter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source.

2.2.22 Inter-integrated circuit interface (I²C)

Up to three I²C bus interfaces can operate in multimaster and slave modes. They can support the Standard-mode (up to 100 kHz) and Fast-mode (up to 400 kHz). They support the 7/10-bit addressing mode and the 7-bit dual addressing mode (as slave). A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SMBus 2.0/PMBus.

2.2.23 Universal synchronous/asynchronous receiver transmitters (USART)

The STM32F415xx and STM32F417xx embed four universal synchronous/asynchronous receiver transmitters (USART1, USART2, USART3 and USART6) and two universal asynchronous receiver transmitters (UART4 and UART5).

These six interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN Master/Slave capability. The USART1 and USART6 interfaces are able to communicate at speeds of up to 10.5 Mbit/s. The other available interfaces communicate at up to 5.25 Mbit/s.

USART1, USART2, USART3 and USART6 also provide hardware management of the CTS and RTS signals, Smart Card mode (ISO 7816 compliant) and SPI-like communication capability. All interfaces can be served by the DMA controller.

Table 5. USART feature comparison

USART name	Standard features	Modem (RTS/ CTS)	LIN	SPI master	irDA	Smartcard (ISO 7816)	Max. baud rate in Mbit/s (oversampling by 16)	Max. baud rate in Mbit/s (oversampling by 8)	APB mapping
USART1	X	X	X	X	X	X	5.25	10.5	APB2 (max. 84 MHz)
USART2	X	X	X	X	X	X	2.62	5.25	APB1 (max. 42 MHz)
USART3	X	X	X	X	X	X	2.62	5.25	APB1 (max. 42 MHz)
UART4	X	-	X	-	X	-	2.62	5.25	APB1 (max. 42 MHz)
UART5	X	-	X	-	X	-	2.62	5.25	APB1 (max. 42 MHz)
USART6	X	X	X	X	X	X	5.25	10.5	APB2 (max. 84 MHz)

2.2.24 Serial peripheral interface (SPI)

The STM32F41xxx feature up to three SPIs in slave and master modes in full-duplex and simplex communication modes. SPI1 can communicate at up to 42 Mbits/s, SPI2 and SPI3 can communicate at up to 21 Mbit/s. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes. All SPIs can be served by the DMA controller.

The SPI interface can be configured to operate in TI mode for communications in master mode and slave mode.

2.2.25 Inter-integrated sound (I^2S)

Two standard I^2S interfaces (multiplexed with SPI2 and SPI3) are available. They can be operated in master or slave mode, in full duplex and half-duplex communication modes, and can be configured to operate with a 16-/32-bit resolution as an input or output channel. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When either or both of the I^2S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

All I^2Sx can be served by the DMA controller.

2.2.26 Audio PLL (PLLI2S)

The devices feature an additional dedicated PLL for audio I^2S application. It allows to achieve error-free I^2S sampling clock accuracy without compromising on the CPU performance, while using USB peripherals.

The PLLI2S configuration can be modified to manage an I^2S sample rate change without disabling the main PLL (PLL) used for CPU, USB and Ethernet interfaces.

The audio PLL can be programmed with very low error to obtain sampling rates ranging from 8 KHz to 192 KHz.

In addition to the audio PLL, a master clock input pin can be used to synchronize the I^2S flow with an external PLL (or Codec output).

2.2.27 Secure digital input/output interface (SDIO)

An SD/SDIO/MMC host interface is available, that supports MultiMediaCard System Specification Version 4.2 in three different databus modes: 1-bit (default), 4-bit and 8-bit.

The interface allows data transfer at up to 48 MHz, and is compliant with the SD Memory Card Specification Version 2.0.

The SDIO Card Specification Version 2.0 is also supported with two different databus modes: 1-bit (default) and 4-bit.

The current version supports only one SD/SDIO/MMC4.2 card at any one time and a stack of MMC4.1 or previous.

In addition to SD/SDIO/MMC, this interface is fully compliant with the CE-ATA digital protocol Rev1.1.

2.2.28 Ethernet MAC interface with dedicated DMA and IEEE 1588 support

Peripheral available only on the STM32F417xx devices.

The STM32F417xx devices provide an IEEE-802.3-2002-compliant media access controller (MAC) for ethernet LAN communications through an industry-standard medium-independent interface (MII) or a reduced medium-independent interface (RMII). The STM32F417xx requires an external physical interface device (PHY) to connect to the physical LAN bus (twisted-pair, fiber, etc.). the PHY is connected to the STM32F417xx MII port using 17 signals for MII or 9 signals for RMII, and can be clocked using the 25 MHz (MII) from the STM32F417xx.

The STM32F417xx includes the following features:

- Supports 10 and 100 Mbit/s rates
- Dedicated DMA controller allowing high-speed transfers between the dedicated SRAM and the descriptors (see the STM32F40xxx/41xxx reference manual for details)
- Tagged MAC frame support (VLAN support)
- Half-duplex (CSMA/CD) and full-duplex operation
- MAC control sublayer (control frames) support
- 32-bit CRC generation and removal
- Several address filtering modes for physical and multicast address (multicast and group addresses)
- 32-bit status code for each transmitted or received frame
- Internal FIFOs to buffer transmit and receive frames. The transmit FIFO and the receive FIFO are both 2 Kbytes.
- Supports hardware PTP (precision time protocol) in accordance with IEEE 1588 2008 (PTP V2) with the time stamp comparator connected to the TIM2 input
- Triggers interrupt when system time becomes greater than target time

2.2.29 Controller area network (bxCAN)

The two CANs are compliant with the 2.0A and B (active) specifications with a bitrate up to 1 Mbit/s. They can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. Each CAN has three transmit mailboxes, two receive FIFOS with 3 stages and 28 shared scalable filter banks (all of them can be used even if one CAN is used). 256 bytes of SRAM are allocated for each CAN.

2.2.30 Universal serial bus on-the-go full-speed (OTG_FS)

The STM32F415xx and STM32F417xx embed an USB OTG full-speed device/host/OTG peripheral with integrated transceivers. The USB OTG FS peripheral is compliant with the USB 2.0 specification and with the OTG 1.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG full-speed controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator. The major features are:

- Combined Rx and Tx FIFO size of 320 × 35 bits with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 4 bidirectional endpoints
- 8 host channels with periodic OUT support
- HNP/SNP/IP inside (no need for any external resistor)
- For OTG/Host modes, a power switch is needed in case bus-powered devices are connected

2.2.31 Universal serial bus on-the-go high-speed (OTG_HS)

The STM32F415xx and STM32F417xx devices embed a USB OTG high-speed (up to 480 Mb/s) device/host/OTG peripheral. The USB OTG HS supports both full-speed and high-speed operations. It integrates the transceivers for full-speed operation (12 MB/s) and features a UTMI low-pin interface (ULPI) for high-speed operation (480 MB/s). When using the USB OTG HS in HS mode, an external PHY device connected to the ULPI is required.

The USB OTG HS peripheral is compliant with the USB 2.0 specification and with the OTG 1.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG full-speed controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator.

The major features are:

- Combined Rx and Tx FIFO size of 1 Kbit × 35 with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 6 bidirectional endpoints
- 12 host channels with periodic OUT support
- Internal FS OTG PHY support
- External HS or HS OTG operation supporting ULPI in SDR mode. The OTG PHY is connected to the microcontroller ULPI port through 12 signals. It can be clocked using the 60 MHz output.
- Internal USB DMA
- HNP/SNP/IP inside (no need for any external resistor)
- for OTG/Host modes, a power switch is needed in case bus-powered devices are connected

2.2.32 Digital camera interface (DCMI)

The camera interface is *not* available in STM32F415xx devices.

STM32F417xx products embed a camera interface that can connect with camera modules and CMOS sensors through an 8-bit to 14-bit parallel interface, to receive video data. The camera interface can sustain a data transfer rate up to 54 Mbyte/s at 54 MHz. It features:

- Programmable polarity for the input pixel clock and synchronization signals
- Parallel data communication can be 8-, 10-, 12- or 14-bit
- Supports 8-bit progressive video monochrome or raw bayer format, YCbCr 4:2:2 progressive video, RGB 565 progressive video or compressed data (like JPEG)
- Supports continuous mode or snapshot (a single frame) mode
- Capability to automatically crop the image

2.2.33 Cryptographic acceleration

The STM32F415xx and STM32F417xx devices embed a cryptographic accelerator. This cryptographic accelerator provides a set of hardware acceleration for the advanced cryptographic algorithms usually needed to provide confidentiality, authentication, data integrity and non repudiation when exchanging messages with a peer.

These algorithms consists of:

Encryption/Decryption

– DES/TDES (data encryption standard/triple data encryption standard): ECB (electronic codebook) and CBC (cipher block chaining) chaining algorithms, 64-, 128- or 192-bit key

– AES (advanced encryption standard): ECB, CBC and CTR (counter mode) chaining algorithms, 128, 192 or 256-bit key

Universal hash

– SHA-1 (secure hash algorithm)

– MD5

– HMAC

The cryptographic accelerator supports DMA request generation.

2.2.34 Random number generator (RNG)

All STM32F415xx and STM32F417xx products embed an RNG that delivers 32-bit random numbers generated by an integrated analog circuit.

2.2.35 General-purpose input/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain, with or without pull-up or pull-down), as input (floating, with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current-capable and have speed selection to better manage internal noise, power consumption and electromagnetic emission.

The I/O configuration can be locked if needed by following a specific sequence in order to avoid spurious writing to the I/Os registers.

Fast I/O handling allowing maximum I/O toggling up to 84 MHz.

2.2.36 Analog-to-digital converters (ADCs)

Three 12-bit analog-to-digital converters are embedded and each ADC shares up to 16 external channels, performing conversions in the single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hold

The ADC can be served by the DMA controller. An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

To synchronize A/D conversion and timers, the ADCs could be triggered by any of TIM1, TIM2, TIM3, TIM4, TIM5, or TIM8 timer.

2.2.37 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 1.8 V and 3.6 V. The temperature sensor is internally

connected to the ADC1_IN16 input channel which is used to convert the sensor output voltage into a digital value.

As the offset of the temperature sensor varies from chip to chip due to process variation, the internal temperature sensor is mainly suitable for applications that detect temperature changes instead of absolute temperatures. If an accurate temperature reading is needed, then an external temperature sensor part should be used.

2.2.38 Digital-to-analog converter (DAC)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs.

This dual digital Interface supports the following features:

- two DAC converters: one for each output channel
- 8-bit or 12-bit monotonic output
- left or right data alignment in 12-bit mode
- synchronized update capability
- noise-wave generation
- triangular-wave generation
- dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- external triggers for conversion
- input voltage reference V_{REF+}

Eight DAC trigger inputs are used in the device. The DAC channels are triggered through the timer update outputs that are also connected to different DMA streams.

2.2.39 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

Debug is performed using 2 pins only instead of 5 required by the JTAG (JTAG pins could be re-use as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

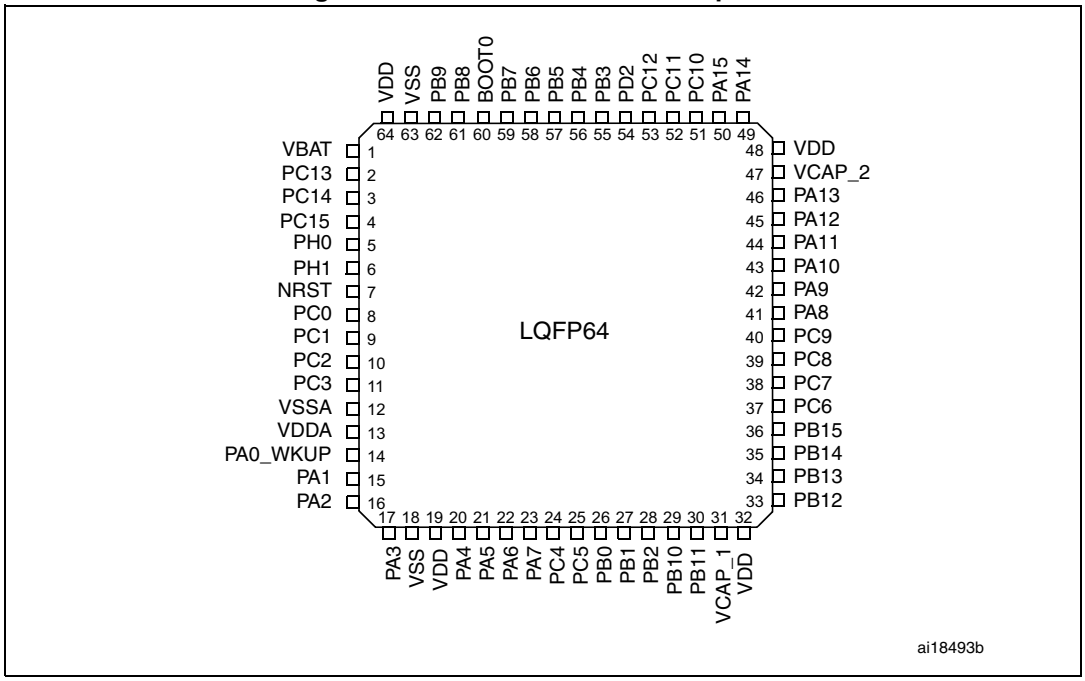
2.2.40 Embedded Trace Macrocell™

The ARM Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F41xxx through a small number of ETM pins to an external hardware trace port analyser (TPA) device. The TPA is connected to a host computer using USB, Ethernet, or any other high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer that runs the debugger software. TPA hardware is commercially available from common development tool vendors.

The Embedded Trace Macrocell operates with third party debugger software tools.

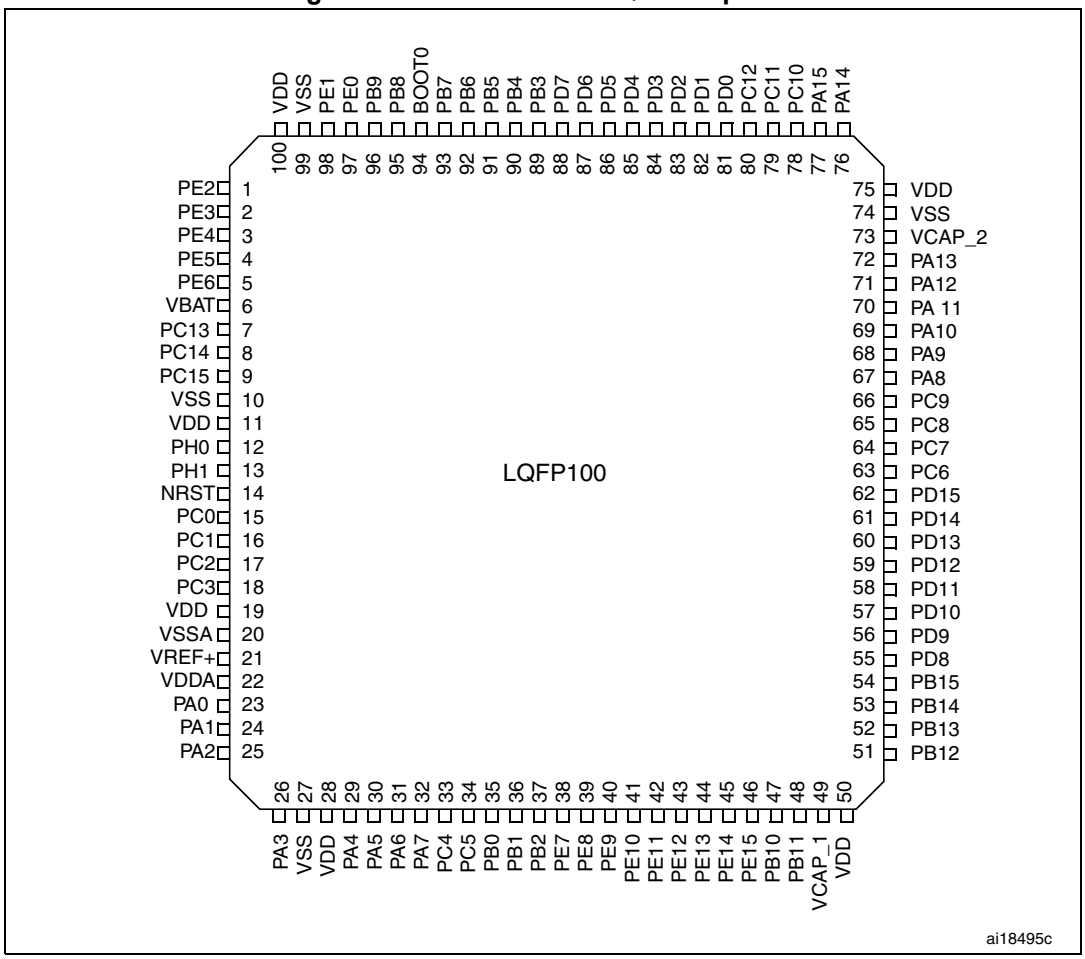
3 Pinouts and pin description

Figure 12. STM32F41xxx LQFP64 pinout



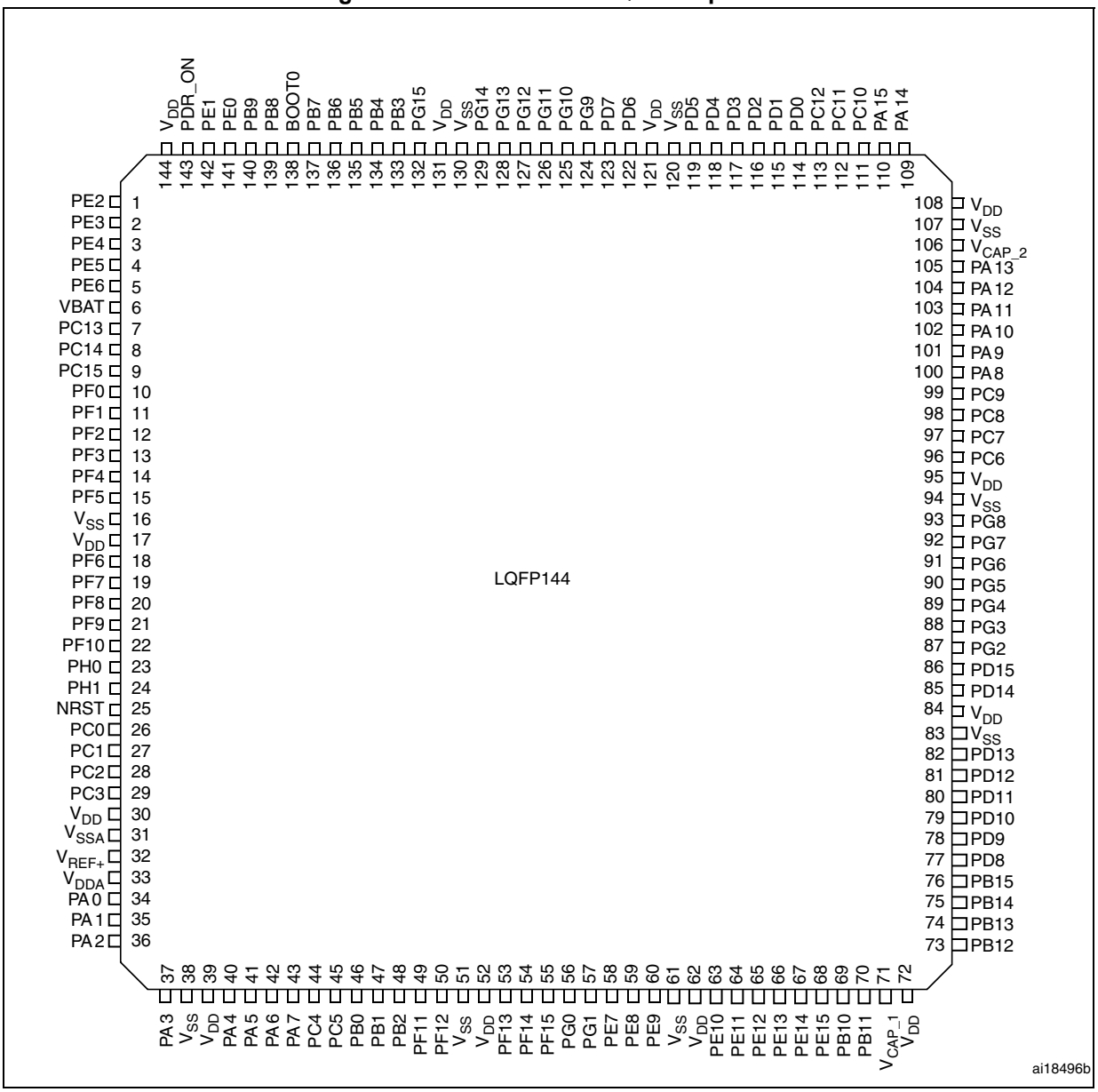
1. The above figure shows the package top view.

Figure 13. STM32F41xxx LQFP100 pinout



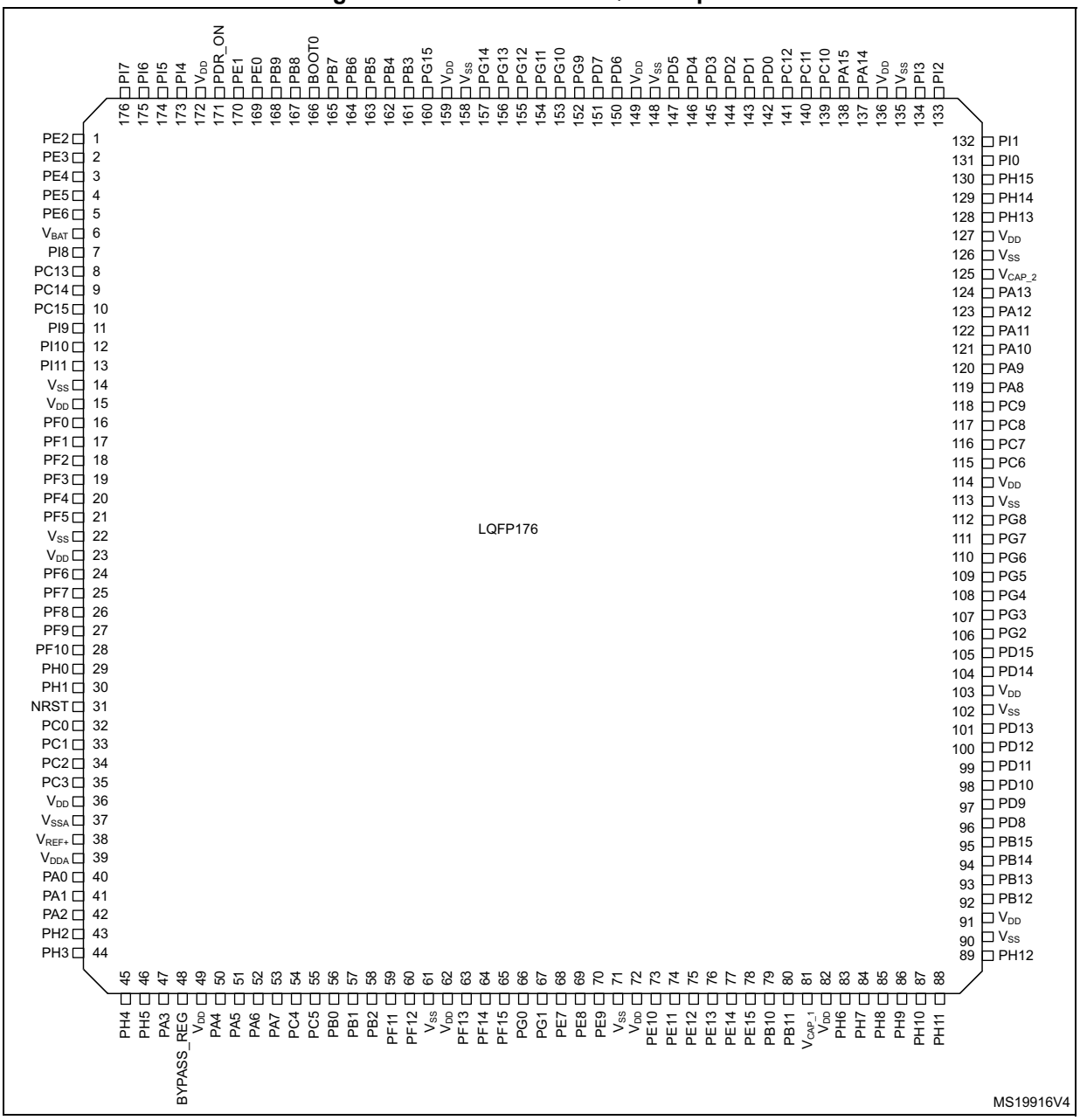
1. The above figure shows the package top view.

Figure 14. STM32F41xxx LQFP144 pinout



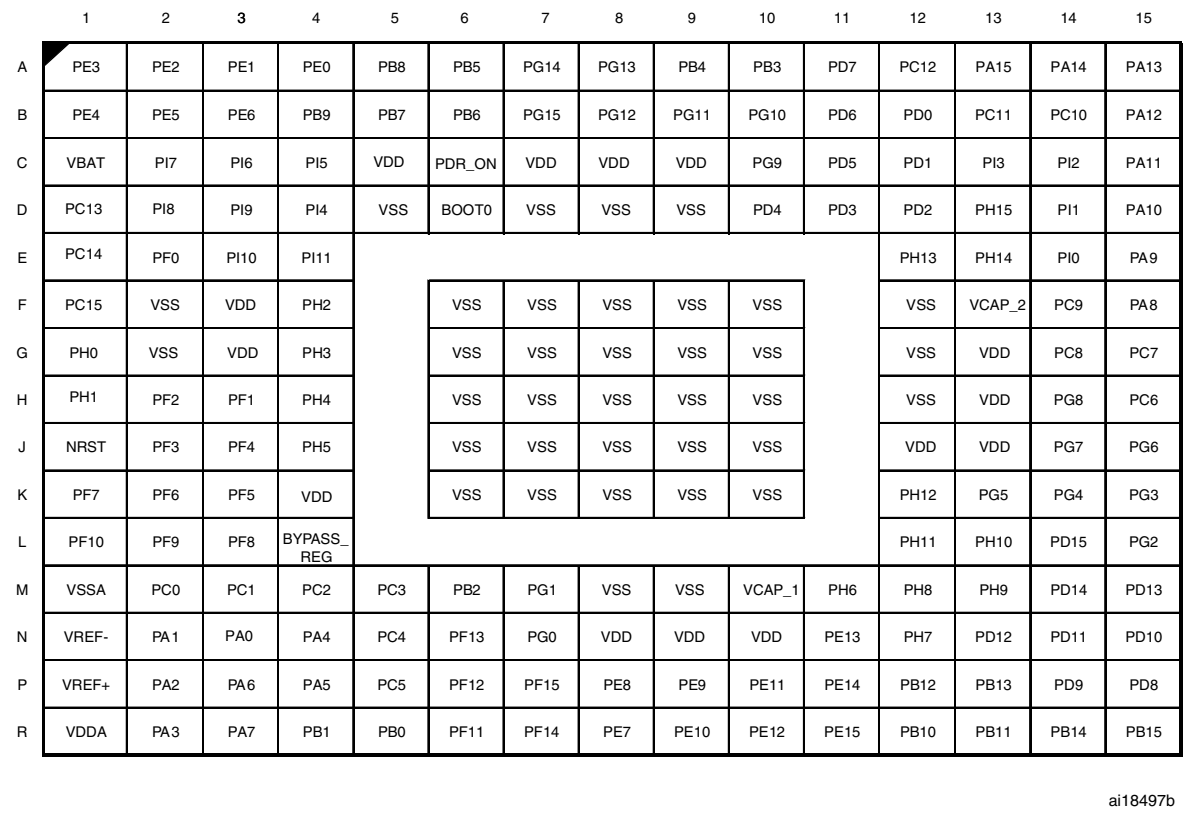
1. The above figure shows the package top view.

Figure 15. STM32F41xxx LQFP176 pinout



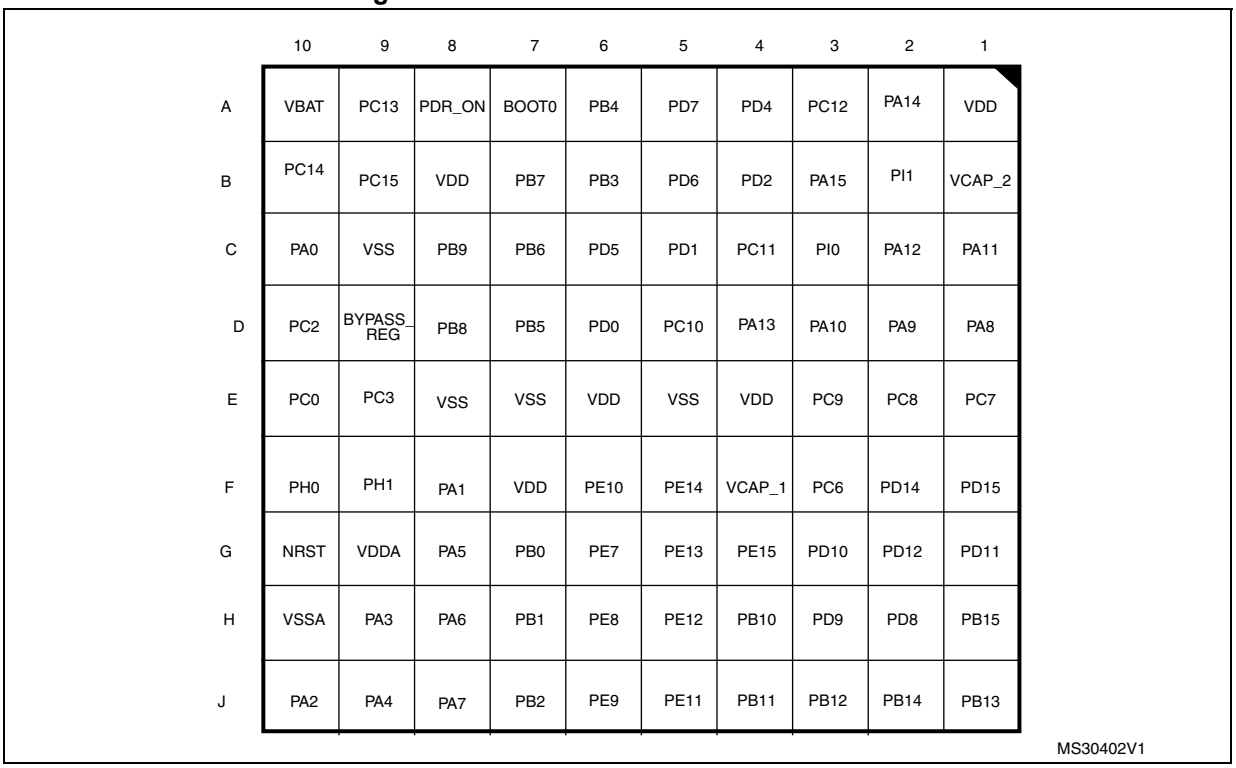
1. The above figure shows the package top view.

Figure 16. STM32F41xxx UFBGA176 ballout



1. This figure shows the package top view.

Figure 17. STM32F41xxx WLCSP90 ballout



1. This figure shows the package bump view.

Table 6. Legend/abbreviations used in the pinout table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type	S	Supply pin
	I	Input only pin
	I/O	Input / output pin
I/O structure	FT	5 V tolerant I/O
	TTa	3.3 V tolerant I/O directly connected to ADC
	B	Dedicated BOOT0 pin
	RST	Bidirectional reset pin with embedded weak pull-up resistor
Notes	Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Alternate functions	Functions selected through GPIOx_AFR registers	
Additional functions	Functions directly selected/enabled through peripheral registers	

Table 7. STM32F41xxx pin and ball definitions

Pin number						Pin name (function after reset)[1]	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP64	WLCSP90	LQFP100	LQFP144	UFBGA176	LQFP176						
-	-	1	1	A2	1	PE2	I/O	FT		TRACECLK/ FSMC_A23 / ETH_MII_TXD3 / EVENTOUT	
-	-	2	2	A1	2	PE3	I/O	FT		TRACED0/FSMC_A19 / EVENTOUT	
-	-	3	3	B1	3	PE4	I/O	FT		TRACED1/FSMC_A20 / DCMI_D4/ EVENTOUT	
-	-	4	4	B2	4	PE5	I/O	FT		TRACED2 / FSMC_A21 / TIM9_CH1 / DCMI_D6 / EVENTOUT	
-	-	5	5	B3	5	PE6	I/O	FT		TRACED3 / FSMC_A22 / TIM9_CH2 / DCMI_D7 / EVENTOUT	
1	A10	6	6	C1	6	V_{BAT}	S				
-	-	-	-	D2	7	PI8	I/O	FT	(2)(3)	EVENTOUT	RTC_TAMP1, RTC_TAMP2, RTC_TS
2	A9	7	7	D1	8	PC13	I/O	FT	(2)(3)	EVENTOUT	RTC_OUT, RTC_TAMP1, RTC_TS
3	B10	8	8	E1	9	PC14/OSC32_IN (PC14)	I/O	FT	(2)(3)	EVENTOUT	OSC32_IN[4]
4	B9	9	9	F1	10	PC15/ OSC32_OUT (PC15)	I/O	FT	(2)(3)	EVENTOUT	OSC32_OUT[4]
-	-	-	-	D3	11	PI9	I/O	FT		CAN1_RX / EVENTOUT	
-	-	-	-	E3	12	PI10	I/O	FT		ETH_MII_RX_ER / EVENTOUT	
-	-	-	-	E4	13	PI11	I/O	FT		OTG_HS_ULPI_DIR / EVENTOUT	
-	-	-	-	F2	14	V_{SS}	S				
-	-	-	-	F3	15	V_{DD}	S				
-	-	-	10	E2	16	PF0	I/O	FT		FSMC_A0 / I2C2_SDA / EVENTOUT	

Table 7. STM32F41xxx pin and ball definitions (continued)

Pin number						Pin name (function after reset)(1)	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP64	WLCSP90	LQFP100	LQFP144	UFBGA176	LQFP176						
-	-	-	11	H3	17	PF1	I/O	FT		FSMC_A1 / I2C2_SCL / EVENTOUT	
-	-	-	12	H2	18	PF2	I/O	FT		FSMC_A2 / I2C2_SMBA / EVENTOUT	
-	-	-	13	J2	19	PF3	I/O	FT	(4)	FSMC_A3/EVENTOUT	ADC3_IN9
-	-	-	14	J3	20	PF4	I/O	FT	(4)	FSMC_A4/EVENTOUT	ADC3_IN14
-	-	-	15	K3	21	PF5	I/O	FT	(4)	FSMC_A5/EVENTOUT	ADC3_IN15
-	C9	10	16	G2	22	V_{SS}	S				
-	B8	11	17	G3	23	V_{DD}	S				
-	-	-	18	K2	24	PF6	I/O	FT	(4)	TIM10_CH1 / FSMC_NIORD/ EVENTOUT	ADC3_IN4
-	-	-	19	K1	25	PF7	I/O	FT	(4)	TIM11_CH1/FSMC_NREG / EVENTOUT	ADC3_IN5
-	-	-	20	L3	26	PF8	I/O	FT	(4)	TIM13_CH1 / FSMC_NIOWR/ EVENTOUT	ADC3_IN6
-	-	-	21	L2	27	PF9	I/O	FT	(4)	TIM14_CH1 / FSMC_CD/ EVENTOUT	ADC3_IN7
-	-	-	22	L1	28	PF10	I/O	FT	(4)	FSMC_INTR/ EVENTOUT	ADC3_IN8
5	F10	12	23	G1	29	PH0/OSC_IN (PH0)	I/O	FT		EVENTOUT	OSC_IN(4)
6	F9	13	24	H1	30	PH1/OSC_OUT (PH1)	I/O	FT		EVENTOUT	OSC_OUT(4)
7	G10	14	25	J1	31	NRST	I/O	RST			
8	E10	15	26	M2	32	PC0	I/O	FT	(4)	OTG_HS_ULPI_STP/ EVENTOUT	ADC123_IN10
9	-	16	27	M3	33	PC1	I/O	FT	(4)	ETH_MDC/ EVENTOUT	ADC123_IN11
10	D10	17	28	M4	34	PC2	I/O	FT	(4)	SPI2_MISO / OTG_HS_ULPI_DIR / ETH_MII_TXD2 /I2S2ext_SD/ EVENTOUT	ADC123_IN12

Table 7. STM32F41xxx pin and ball definitions (continued)

Pin number						Pin name (function after reset)(1)	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP64	WLCSP90	LQFP100	LQFP144	UFBGA176	LQFP176						
11	E9	18	29	M5	35	PC3	I/O	FT	(4)	SPI2_MOSI / I2S2_SD / OTG_HS_ULPI_NXT / ETH_MII_TX_CLK/ EVENTOUT	ADC123_IN13
-	-	19	30	-	36	V_{DD}	S				
12	H10	20	31	M1	37	V_{SSA}	S				
-	-	-	-	N1	-	V_{REF-}	S				
-	-	21	32	P1	38	V_{REF+}	S				
13	G9	22	33	R1	39	V_{DDA}	S				
14	C10	23	34	N3	40	PA0/WKUP (PA0)	I/O	FT	(5)	USART2_CTS/ UART4_TX/ ETH_MII_CRS / TIM2_CH1_ETR/ TIM5_CH1 / TIM8_ETR/ EVENTOUT	ADC123_IN0/WKUP(4)
15	F8	24	35	N2	41	PA1	I/O	FT	(4)	USART2_RTS / UART4_RX/ ETH_RMII_REF_CLK / ETH_MII_RX_CLK / TIM5_CH2 / TIM2_CH2/ EVENTOUT	ADC123_IN1
16	J10	25	36	P2	42	PA2	I/O	FT	(4)	USART2_TX/TIM5_CH3 / TIM9_CH1 / TIM2_CH3 / ETH_MDIO/ EVENTOUT	ADC123_IN2
-	-	-	-	F4	43	PH2	I/O	FT		ETH_MII_CRS/EVENTOUT	
-	-	-	-	G4	44	PH3	I/O	FT		ETH_MII_COL/EVENTOUT	
-	-	-	-	H4	45	PH4	I/O	FT		I2C2_SCL / OTG_HS_ULPI_NXT/ EVENTOUT	
-	-	-	-	J4	46	PH5	I/O	FT		I2C2_SDA/ EVENTOUT	

Table 7. STM32F41xxx pin and ball definitions (continued)

Pin number						Pin name (function after reset)(1)	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP64	WLCSP90	LQFP100	LQFP144	UFBGA176	LQFP176						
17	H9	26	37	R2	47	PA3	I/O	FT	(4)	USART2_RX/TIM5_CH4 / TIM9_CH2 / TIM2_CH4 / OTG_HS_ULPI_D0 / ETH_MII_COL/ EVENTOUT	ADC123_IN3
18	E5	27	38	-	-	V_{SS}	S				
	D9			L4	48	BYPASS_REG	I	FT			
19	E4	28	39	K4	49	V_{DD}	S				
20	J9	29	40	N4	50	PA4	I/O	TTa	(4)	SPI1_NSS / SPI3_NSS / USART2_CK / DCMI_HSYNC / OTG_HS_SOF/ I2S3_WS/ EVENTOUT	ADC12_IN4 /DAC_OUT1
21	G8	30	41	P4	51	PA5	I/O	TTa	(4)	SPI1_SCK/ OTG_HS_ULPI_CK / TIM2_CH1_ETR/ TIM8_CH1N/ EVENTOUT	ADC12_IN5/DAC_OUT2
22	H8	31	42	P3	52	PA6	I/O	FT	(4)	SPI1_MISO / TIM8_BKIN/TIM13_CH1 / DCMI_PIXCLK / TIM3_CH1 / TIM1_BKIN/ EVENTOUT	ADC12_IN6
23	J8	32	43	R3	53	PA7	I/O	FT	(4)	SPI1_MOSI/ TIM8_CH1N / TIM14_CH1/TIM3_CH2/ ETH_MII_RX_DV / TIM1_CH1N / ETH_RMII_CRS_DV/ EVENTOUT	ADC12_IN7
24	-	33	44	N5	54	PC4	I/O	FT	(4)	ETH_RMII_RX_D0 / ETH_MII_RX_D0/ EVENTOUT	ADC12_IN14
25	-	34	45	P5	55	PC5	I/O	FT	(4)	ETH_RMII_RX_D1 / ETH_MII_RX_D1/ EVENTOUT	ADC12_IN15
26	G7	35	46	R5	56	PB0	I/O	FT	(4)	TIM3_CH3 / TIM8_CH2N/ OTG_HS_ULPI_D1/ ETH_MII_RXD2 / TIM1_CH2N/ EVENTOUT	ADC12_IN8

Table 7. STM32F41xxx pin and ball definitions (continued)

Pin number						Pin name (function after reset)(1)	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP64	WLCSP90	LQFP100	LQFP144	UFBGA176	LQFP176						
27	H7	36	47	R4	57	PB1	I/O	FT	(4)	TIM3_CH4 / TIM8_CH3N/ OTG_HS_ULPI_D2/ ETH_MII_RXD3 / TIM1_CH3N/ EVENTOUT	ADC12_IN9
28	J7	37	48	M6	58	PB2/BOOT1 (PB2)	I/O	FT		EVENTOUT	
-	-	-	49	R6	59	PF11	I/O	FT		DCMI_D12/ EVENTOUT	
-	-	-	50	P6	60	PF12	I/O	FT		FSMC_A6/ EVENTOUT	
-	-	-	51	M8	61	V_{SS}	S				
-	-	-	52	N8	62	V_{DD}	S				
-	-	-	53	N6	63	PF13	I/O	FT		FSMC_A7/ EVENTOUT	
-	-	-	54	R7	64	PF14	I/O	FT		FSMC_A8/ EVENTOUT	
-	-	-	55	P7	65	PF15	I/O	FT		FSMC_A9/ EVENTOUT	
-	-	-	56	N7	66	PG0	I/O	FT		FSMC_A10/ EVENTOUT	
-	-	-	57	M7	67	PG1	I/O	FT		FSMC_A11/ EVENTOUT	
-	G6	38	58	R8	68	PE7	I/O	FT		FSMC_D4/TIM1_ETR/ EVENTOUT	
-	H6	39	59	P8	69	PE8	I/O	FT		FSMC_D5/ TIM1_CH1N/ EVENTOUT	
-	J6	40	60	P9	70	PE9	I/O	FT		FSMC_D6/TIM1_CH1/ EVENTOUT	
-	-	-	61	M9	71	V_{SS}	S				
-	-	-	62	N9	72	V_{DD}	S				
-	F6	41	63	R9	73	PE10	I/O	FT		FSMC_D7/TIM1_CH2N/ EVENTOUT	
-	J5	42	64	P10	74	PE11	I/O	FT		FSMC_D8/TIM1_CH2/ EVENTOUT	
-	H5	43	65	R10	75	PE12	I/O	FT		FSMC_D9/TIM1_CH3N/ EVENTOUT	
-	G5	44	66	N11	76	PE13	I/O	FT		FSMC_D10/TIM1_CH3/ EVENTOUT	

Table 7. STM32F41xxx pin and ball definitions (continued)

Pin number						Pin name (function after reset)(1)	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP64	WLCSP90	LQFP100	LQFP144	UFBGA176	LQFP176						
-	F5	45	67	P11	77	PE14	I/O	FT		FSMC_D11/TIM1_CH4/ EVENTOUT	
-	G4	46	68	R11	78	PE15	I/O	FT		FSMC_D12/TIM1_BKIN/ EVENTOUT	
29	H4	47	69	R12	79	PB10	I/O	FT		SPI2_SCK / I2S2_CK / I2C2_SCL/ USART3_TX / OTG_HS_ULPI_D3 / ETH_MII_RX_ER / TIM2_CH3/ EVENTOUT	
30	J4	48	70	R13	80	PB11	I/O	FT		I2C2_SDA/USART3_RX/ OTG_HS_ULPI_D4 / ETH_RMII_TX_EN/ ETH_MII_TX_EN / TIM2_CH4/ EVENTOUT	
31	F4	49	71	M10	81	V_{CAP_1}	S				
32	-	50	72	N10	82	V_{DD}	S				
-	-	-	-	M11	83	PH6	I/O	FT		I2C2_SMBA / TIM12_CH1 / ETH_MII_RXD2/ EVENTOUT	
-	-	-	-	N12	84	PH7	I/O	FT		I2C3_SCL / ETH_MII_RXD3/ EVENTOUT	
-	-	-	-	M12	85	PH8	I/O	FT		I2C3_SDA / DCMI_HSYNC/ EVENTOUT	
-	-	-	-	M13	86	PH9	I/O	FT		I2C3_SMBA / TIM12_CH2/ DCMI_D0/ EVENTOUT	
-	-	-	-	L13	87	PH10	I/O	FT		TIM5_CH1 / DCMI_D1/ EVENTOUT	
-	-	-	-	L12	88	PH11	I/O	FT		TIM5_CH2 / DCMI_D2/ EVENTOUT	
-	-	-	-	K12	89	PH12	I/O	FT		TIM5_CH3 / DCMI_D3/ EVENTOUT	
-	-	-	-	H12	90	V_{SS}	S				
-	-	-	-	J12	91	V_{DD}	S				

Table 7. STM32F41xxx pin and ball definitions (continued)

Pin number						Pin name (function after reset)[1]	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP64	WLCSP90	LQFP100	LQFP144	UFBGA176	LQFP176						
33	J3	51	73	P12	92	PB12	I/O	FT		SPI2_NSS / I2S2_WS / I2C2_SMBA/ USART3_CK/ TIM1_BKIN / CAN2_RX / OTG_HS_ULPI_D5/ ETH_RMII_TXD0 / ETH_MII_TXD0/ OTG_HS_ID/ EVENTOUT	
34	J1	52	74	P13	93	PB13	I/O	FT		SPI2_SCK / I2S2_CK / USART3_CTS/ TIM1_CH1N /CAN2_TX / OTG_HS_ULPI_D6 / ETH_RMII_TXD1 / ETH_MII_TXD1/ EVENTOUT	OTG_HS_VBUS
35	J2	53	75	R14	94	PB14	I/O	FT		SPI2_MISO/ TIM1_CH2N / TIM12_CH1 / OTG_HS_DM/ USART3_RTS / TIM8_CH2N/I2S2ext_SD/ EVENTOUT	
36	H1	54	76	R15	95	PB15	I/O	FT		SPI2_MOSI / I2S2_SD/ TIM1_CH3N / TIM8_CH3N / TIM12_CH2 / OTG_HS_DP/ EVENTOUT	RTC_REFIN
-	H2	55	77	P15	96	PD8	I/O	FT		FSMC_D13 / USART3_TX/ EVENTOUT	
-	H3	56	78	P14	97	PD9	I/O	FT		FSMC_D14 / USART3_RX/ EVENTOUT	
-	G3	57	79	N15	98	PD10	I/O	FT		FSMC_D15 / USART3_CK/ EVENTOUT	
-	G1	58	80	N14	99	PD11	I/O	FT		FSMC_CLE / FSMC_A16/USART3_CTS/ EVENTOUT	
-	G2	59	81	N13	100	PD12	I/O	FT		FSMC_ALE/ FSMC_A17/TIM4_CH1 / USART3_RTS/ EVENTOUT	

Table 7. STM32F41xxx pin and ball definitions (continued)

Pin number						Pin name (function after reset)(1)	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP64	WLCSP90	LQFP100	LQFP144	UFBGA176	LQFP176						
-	-	60	82	M15	101	PD13	I/O	FT		FSMC_A18/TIM4_CH2/ EVENTOUT	
-	-	-	83	-	102	V_{SS}	S				
-	-	-	84	J13	103	V_{DD}	S				
-	F2	61	85	M14	104	PD14	I/O	FT		FSMC_D0/TIM4_CH3/ EVENTOUT/ EVENTOUT	
-	F1	62	86	L14	105	PD15	I/O	FT		FSMC_D1/TIM4_CH4/ EVENTOUT	
-	-	-	87	L15	106	PG2	I/O	FT		FSMC_A12/ EVENTOUT	
-	-	-	88	K15	107	PG3	I/O	FT		FSMC_A13/ EVENTOUT	
-	-	-	89	K14	108	PG4	I/O	FT		FSMC_A14/ EVENTOUT	
-	-	-	90	K13	109	PG5	I/O	FT		FSMC_A15/ EVENTOUT	
-	-	-	91	J15	110	PG6	I/O	FT		FSMC_INT2/ EVENTOUT	
-	-	-	92	J14	111	PG7	I/O	FT		FSMC_INT3 /USART6_CK/ EVENTOUT	
-	-	-	93	H14	112	PG8	I/O	FT		USART6_RTS / ETH_PPS_OUT/ EVENTOUT	
-	-	-	94	G12	113	V_{SS}	S				
-	-	-	95	H13	114	V_{DD}	S				
37	F3	63	96	H15	115	PC6	I/O	FT		I2S2_MCK / TIM8_CH1/SDIO_D6 / USART6_TX / DCMI_D0/TIM3_CH1/ EVENTOUT	
38	E1	64	97	G15	116	PC7	I/O	FT		I2S3_MCK / TIM8_CH2/SDIO_D7 / USART6_RX / DCMI_D1/TIM3_CH2/ EVENTOUT	
39	E2	65	98	G14	117	PC8	I/O	FT		TIM8_CH3/SDIO_D0 /TIM3_CH3/ USART6_CK / DCMI_D2/ EVENTOUT	

Table 7. STM32F41xxx pin and ball definitions (continued)

Pin number						Pin name (function after reset)[1]	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP64	WLCSP90	LQFP100	LQFP144	UFBGA176	LQFP176						
40	E3	66	99	F14	118	PC9	I/O	FT		I2S_CKIN/ MCO2 / TIM8_CH4/SDIO_D1 / /I2C3_SDA / DCMI_D3 / TIM3_CH4/ EVENTOUT	
41	D1	67	100	F15	119	PA8	I/O	FT		MCO1 / USART1_CK/ TIM1_CH1/ I2C3_SCL/ OTG_FS_SOF/ EVENTOUT	
42	D2	68	101	E15	120	PA9	I/O	FT		USART1_TX/ TIM1_CH2 / I2C3_SMBA / DCMI_D0/ EVENTOUT	OTG_FS_VBUS
43	D3	69	102	D15	121	PA10	I/O	FT		USART1_RX/ TIM1_CH3/ OTG_FS_ID/DCMI_D1/ EVENTOUT	
44	C1	70	103	C15	122	PA11	I/O	FT		USART1_CTS / CAN1_RX / TIM1_CH4 / OTG_FS_DM/ EVENTOUT	
45	C2	71	104	B15	123	PA12	I/O	FT		USART1_RTS / CAN1_TX/ TIM1_ETR/ OTG_FS_DP/ EVENTOUT	
46	D4	72	105	A15	124	PA13 (JTMS-SWDIO)	I/O	FT		JTMS-SWDIO/ EVENTOUT	
47	B1	73	106	F13	125	V_{CAP_2}	S				
-	E7	74	107	F12	126	V_{SS}	S				
48	E6	75	108	G13	127	V_{DD}	S				
-	-	-	-	E12	128	PH13	I/O	FT		TIM8_CH1N / CAN1_TX/ EVENTOUT	
-	-	-	-	E13	129	PH14	I/O	FT		TIM8_CH2N / DCMI_D4/ EVENTOUT	
-	-	-	-	D13	130	PH15	I/O	FT		TIM8_CH3N / DCMI_D11/ EVENTOUT	
-	C3	-	-	E14	131	PI0	I/O	FT		TIM5_CH4 / SPI2_NSS / I2S2_WS / DCMI_D13/ EVENTOUT	

Table 7. STM32F41xxx pin and ball definitions (continued)

Pin number						Pin name (function after reset)(1)	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP64	WLCSP90	LQFP100	LQFP144	UFBGA176	LQFP176						
-	B2	-	-	D14	132	PI1	I/O	FT		SPI2_SCK / I2S2_CK / DCMI_D8/ EVENTOUT	
-	-	-	-	C14	133	PI2	I/O	FT		TIM8_CH4 /SPI2_MISO / DCMI_D9 / I2S2ext_SD/ EVENTOUT	
-	-	-	-	C13	134	PI3	I/O	FT		TIM8_ETR / SPI2_MOSI / I2S2_SD / DCMI_D10/ EVENTOUT	
-	-	-	-	D9	135	V_{SS}	S				
-	-	-	-	C9	136	V_{DD}	S				
49	A2	76	109	A14	137	PA14 (JTCK/SWCLK)	I/O	FT		JTCK-SWCLK/ EVENTOUT	
50	B3	77	110	A13	138	PA15 (JTDI)	I/O	FT		JTDI/ SPI3_NSS/ I2S3_WS/TIM2_CH1_ETR / SPI1_NSS / EVENTOUT	
51	D5	78	111	B14	139	PC10	I/O	FT		SPI3_SCK / I2S3_CK/ UART4_TX/SDIO_D2 / DCMI_D8 / USART3_TX/ EVENTOUT	
52	C4	79	112	B13	140	PC11	I/O	FT		UART4_RX/ SPI3_MISO / SDIO_D3 / DCMI_D4/USART3_RX / I2S3ext_SD/ EVENTOUT	
53	A3	80	113	A12	141	PC12	I/O	FT		UART5_TX/SDIO_CK / DCMI_D9 / SPI3_MOSI /I2S3_SD / USART3_CK/ EVENTOUT	
-	D6	81	114	B12	142	PD0	I/O	FT		FSMC_D2/CAN1_RX/ EVENTOUT	
-	C5	82	115	C12	143	PD1	I/O	FT		FSMC_D3 / CAN1_TX/ EVENTOUT	
54	B4	83	116	D12	144	PD2	I/O	FT		TIM3_ETR/UART5_RX/ SDIO_CMD / DCMI_D11/ EVENTOUT	

Table 7. STM32F41xxx pin and ball definitions (continued)

Pin number						Pin name (function after reset)(1)	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP64	WLCSP90	LQFP100	LQFP144	UFBGA176	LQFP176						
-	-	84	117	D11	145	PD3	I/O	FT		FSMC_CLK/ USART2_CTS/ EVENTOUT	
-	A4	85	118	D10	146	PD4	I/O	FT		FSMC_NOE/ USART2_RTS/ EVENTOUT	
-	C6	86	119	C11	147	PD5	I/O	FT		FSMC_NWE/USART2_TX / EVENTOUT	
-	-	-	120	D8	148	V_{SS}	S				
-	-	-	121	C8	149	V_{DD}	S				
-	B5	87	122	B11	150	PD6	I/O	FT		FSMC_NWAIT/ USART2_RX/ EVENTOUT	
-	A5	88	123	A11	151	PD7	I/O	FT		USART2_CK/FSMC_NE1/ FSMC_NCE2/ EVENTOUT	
-	-	-	124	C10	152	PG9	I/O	FT		USART6_RX / FSMC_NE2/FSMC_NCE3 / EVENTOUT	
-	-	-	125	B10	153	PG10	I/O	FT		FSMC_NCE4_1/ FSMC_NE3/ EVENTOUT	
-	-	-	126	B9	154	PG11	I/O	FT		FSMC_NCE4_2 / ETH_MII_TX_EN/ ETH _RMII_TX_EN/ EVENTOUT	
-	-	-	127	B8	155	PG12	I/O	FT		FSMC_NE4 / USART6_RTS/ EVENTOUT	
-	-	-	128	A8	156	PG13	I/O	FT		FSMC_A24 / USART6_CTS /ETH_MII_TXD0/ ETH_RMII_TXD0/ EVENTOUT	
-	-	-	129	A7	157	PG14	I/O	FT		FSMC_A25 / USART6_TX /ETH_MII_TXD1/ ETH_RMII_TXD1/ EVENTOUT	

Table 7. STM32F41xxx pin and ball definitions (continued)

Pin number						Pin name (function after reset)(1)	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP64	WLCSP90	LQFP100	LQFP144	UFBGA176	LQFP176						
-	E8	-	130	D7	158	V_{SS}	S				
-	F7	-	131	C7	159	V_{DD}	S				
-	-	-	132	B7	160	PG15	I/O	FT		USART6_CTS / DCMI_D13/ EVENTOUT	
55	B6	89	133	A10	161	PB3 (JTDO/ TRACESWO)	I/O	FT		JTDO/ TRACESWO/ SPI3_SCK / I2S3_CK / TIM2_CH2 / SPI1_SCK/ EVENTOUT	
56	A6	90	134	A9	162	PB4 (NJTRST)	I/O	FT		NJTRST/ SPI3_MISO / TIM3_CH1 / SPI1_MISO / I2S3ext_SD/ EVENTOUT	
57	D7	91	135	A6	163	PB5	I/O	FT		I2C1_SMBA/ CAN2_RX / OTG_HS_ULPI_D7 / ETH_PPS_OUT/TIM3_CH 2 / SPI1_MOSI/ SPI3_MOSI / DCMI_D10 / I2S3_SD/ EVENTOUT	
58	C7	92	136	B6	164	PB6	I/O	FT		I2C1_SCL/ TIM4_CH1 / CAN2_TX / DCMI_D5/USART1_TX/ EVENTOUT	
59	B7	93	137	B5	165	PB7	I/O	FT		I2C1_SDA / FSMC_NL / DCMI_VSYNC / USART1_RX/ TIM4_CH2/ EVENTOUT	
60	A7	94	138	D6	166	BOOT0	I	B			V_{PP}
61	D8	95	139	A5	167	PB8	I/O	FT		TIM4_CH3/SDIO_D4/ TIM10_CH1 / DCMI_D6 / ETH_MII_TXD3 / I2C1_SCL/ CAN1_RX/ EVENTOUT	
62	C8	96	140	B4	168	PB9	I/O	FT		SPI2_NSS/ I2S2_WS / TIM4_CH4/ TIM11_CH1/ SDIO_D5 / DCMI_D7 / I2C1_SDA / CAN1_TX/ EVENTOUT	

Table 7. STM32F41xxx pin and ball definitions (continued)

Pin number						Pin name (function after reset)[1]	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP64	WLCSP90	LQFP100	LQFP144	UFBGA176	LQFP176						
-	-	97	141	A4	169	PE0	I/O	FT		TIM4_ETR / FSMC_NBL0 / DCMI_D2/ EVENTOUT	
-	-	98	142	A3	170	PE1	I/O	FT		FSMC_NBL1 / DCMI_D3/ EVENTOUT	
63	-	99	-	D5	-	V_{SS}	S				
-	A8	-	143	C6	171	PDR_ON	I	FT			
64	A1	100	144	C5	172	V_{DD}	S				
-	-	-	-	D4	173	PI4	I/O	FT		TIM8_BKIN / DCMI_D5/ EVENTOUT	
-	-	-	-	C4	174	PI5	I/O	FT		TIM8_CH1 / DCMI_VSYNC/ EVENTOUT	
-	-	-	-	C3	175	PI6	I/O	FT		TIM8_CH2 / DCMI_D6/ EVENTOUT	
-	-	-	-	C2	176	PI7	I/O	FT		TIM8_CH3 / DCMI_D7/ EVENTOUT	

1. Function availability depends on the chosen device.
2. PC13, PC14, PC15 and PI8 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 and PI8 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF.
   - These I/Os must not be used as a current source (e.g. to drive an LED).
3. Main function after the first backup domain power-up. Later on, it depends on the contents of the RTC registers even after reset (because these registers are not reset by the main reset). For details on how to manage these I/Os, refer to the RTC register description sections in the STM32F4xx reference manual, available from the STMicroelectronics website: *www.st.com*.
4. FT = 5 V tolerant except when in analog mode or oscillator mode (for PC14, PC15, PH0 and PH1).
5. If the device is delivered in an UFBGA176 or WLCSP90 and the BYPASS_REG pin is set to VDD (Regulator off/internal reset ON mode), then PA0 is used as an internal Reset (active low).

Table 8. FSMC pin definition

Pins(1)	FSMC				LQFP100(2)	WLCSP90 (2)
	CF	NOR/PSRAM/ SRAM	NOR/PSRAM Mux	NAND 16 bit		
PE2		A23	A23		Yes	
PE3		A19	A19		Yes	
PE4		A20	A20		Yes	
PE5		A21	A21		Yes	
PE6		A22	A22		Yes	
PF0	A0	A0			-	-
PF1	A1	A1			-	-
PF2	A2	A2			-	-
PF3	A3	A3			-	-
PF4	A4	A4			-	-
PF5	A5	A5			-	-
PF6	NIORD				-	-
PF7	NREG				-	-
PF8	NIOWR				-	-
PF9	CD				-	-
PF10	INTR				-	-
PF12	A6	A6			-	-
PF13	A7	A7			-	-
PF14	A8	A8			-	-
PF15	A9	A9			-	-
PG0	A10	A10			-	-
PG1		A11			-	-
PE7	D4	D4	DA4	D4	Yes	Yes
PE8	D5	D5	DA5	D5	Yes	Yes
PE9	D6	D6	DA6	D6	Yes	Yes
PE10	D7	D7	DA7	D7	Yes	Yes
PE11	D8	D8	DA8	D8	Yes	Yes
PE12	D9	D9	DA9	D9	Yes	Yes
PE13	D10	D10	DA10	D10	Yes	Yes
PE14	D11	D11	DA11	D11	Yes	Yes
PE15	D12	D12	DA12	D12	Yes	Yes
PD8	D13	D13	DA13	D13	Yes	Yes
PD9	D14	D14	DA14	D14	Yes	Yes

Table 8. FSMC pin definition (continued)

Pins[1]	FSMC				LQFP100[2]	WLCSP90 (2)
	CF	NOR/PSRAM/ SRAM	NOR/PSRAM Mux	NAND 16 bit		
PD10	D15	D15	DA15	D15	Yes	Yes
PD11		A16	A16	CLE	Yes	Yes
PD12		A17	A17	ALE	Yes	Yes
PD13		A18	A18		Yes	
PD14	D0	D0	DA0	D0	Yes	Yes
PD15	D1	D1	DA1	D1	Yes	Yes
PG2		A12			-	-
PG3		A13			-	-
PG4		A14			-	-
PG5		A15			-	-
PG6				INT2	-	-
PG7				INT3	-	-
PD0	D2	D2	DA2	D2	Yes	Yes
PD1	D3	D3	DA3	D3	Yes	Yes
PD3		CLK	CLK		Yes	
PD4	NOE	NOE	NOE	NOE	Yes	Yes
PD5	NWE	NWE	NWE	NWE	Yes	Yes
PD6	NWAIT	NWAIT	NWAIT	NWAIT	Yes	Yes
PD7		NE1	NE1	NCE2	Yes	Yes
PG9		NE2	NE2	NCE3	-	-
PG10	NCE4_1	NE3	NE3		-	-
PG11	NCE4_2				-	-
PG12		NE4	NE4		-	-
PG13		A24	A24		-	-
PG14		A25	A25		-	-
PB7		NADV	NADV		Yes	Yes
PE0		NBL0	NBL0		Yes	
PE1		NBL1	NBL1		Yes	

1. Full FSMC features are available on LQFP144, LQFP176, and UFBGA176. The features available on smaller packages are given in the dedicated package column.
2. Ports F and G are not available in devices delivered in 100-pin packages.

Table 9. Alternate function mapping

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10 /11	I2C1/2/3	SPI1/SPI2/ I2S2/I2S2e xt	SPI3/I2Sext /I2S3	USART1/2/3/ I2S3ext	UART4/5/ USART6	CAN1/2 TIM12/13/ 14	OTG_FS/ OTG_HS	ETH	FSMC/SDIO /OTG_FS	DCMI		
Port A	PA0		TIM2_CH1_ ETR	TIM 5_CH1	TIM8_ETR				USART2_CTS	UART4_TX			ETH_MII_CRS				EVENTOUT
	PA1		TIM2_CH2	TIM5_CH2					USART2_RTS	UART4_RX			ETH_MII _RX_CLK ETH_RMII__REF _CLK				EVENTOUT
	PA2		TIM2_CH3	TIM5_CH3	TIM9_CH1				USART2_TX				ETH_MDIO				EVENTOUT
	PA3		TIM2_CH4	TIM5_CH4	TIM9_CH2				USART2_RX			OTG_HS_ULPI_ D0	ETH _MII_COL				EVENTOUT
	PA4						SPI1_NSS	SPI3_NSS I2S3_WS	USART2_CK					OTG_HS_SOF	DCMI_HSYN C		EVENTOUT
	PA5		TIM2_CH1_ ETR		TIM8_CH1N		SPI1_SCK					OTG_HS_ULPI_ CK					EVENTOUT
	PA6		TIM1_BKIN	TIM3_CH1	TIM8_BKIN		SPI1_MISO				TIM13_CH1				DCMI_PIXCK		EVENTOUT
	PA7		TIM1_CH1N	TIM3_CH2	TIM8_CH1N		SPI1_MOSI				TIM14_CH1		ETH_MII _RX_DV ETH_RMII _CRS_DV				EVENTOUT
	PA8	MCO1	TIM1_CH1			I2C3_SCL			USART1_CK			OTG_FS_SOF					EVENTOUT
	PA9		TIM1_CH2			I2C3_SMB A			USART1_TX						DCMI_D0		EVENTOUT
	PA10		TIM1_CH3						USART1_RX			OTG_FS_ID			DCMI_D1		EVENTOUT
	PA11		TIM1_CH4						USART1_CTS		CAN1_RX	OTG_FS_DM					EVENTOUT
	PA12		TIM1_ETR						USART1_RTS		CAN1_TX	OTG_FS_DP					EVENTOUT
	PA13	JTMS-SWDIO															EVENTOUT
	PA14	JTCK-SWCLK															EVENTOUT
	PA15	JTDI	TIM 2_CH1 TIM 2_ETR				SPI1_NSS	SPI3_NSS/ I2S3_WS									EVENTOUT

Table 9. Alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/2/3	SPI1/SPI2/I2S2/I2S2ext	SPI3/I2Sext/I2S3	USART1/2/3/I2S3ext	UART4/5/USART6	CAN1/2 TIM12/13/14	OTG_FS/OTG_HS	ETH	FSMC/SDIO/OTG_FS	DCMI		
Port B	PB0		TIM1_CH2N	TIM3_CH3	TIM8_CH2N							OTG_HS_ULPI_D1	ETH _MII_RXD2				EVENTOUT
	PB1		TIM1_CH3N	TIM3_CH4	TIM8_CH3N							OTG_HS_ULPI_D2	ETH _MII_RXD3				EVENTOUT
	PB2																EVENTOUT
	PB3	JTDO/TRACESWO	TIM2_CH2				SPI1_SCK	SPI3_SCK I2S3_CK									EVENTOUT
	PB4	NJTRST		TIM3_CH1			SPI1_MISO	SPI3_MISO	I2S3ext_SD								EVENTOUT
	PB5			TIM3_CH2		I2C1_SMBA	SPI1_MOSI	SPI3_MOSI I2S3_SD			CAN2_RX	OTG_HS_ULPI_D7	ETH _PPS_OUT		DCMI_D10		EVENTOUT
	PB6			TIM4_CH1		I2C1_SCL			USART1_TX		CAN2_TX				DCMI_D5		EVENTOUT
	PB7			TIM4_CH2		I2C1_SDA			USART1_RX					FSMC_NL	DCMI_VSYNC		EVENTOUT
	PB8			TIM4_CH3	TIM10_CH1	I2C1_SCL					CAN1_RX		ETH _MII_TXD3	SDIO_D4	DCMI_D6		EVENTOUT
	PB9			TIM4_CH4	TIM11_CH1	I2C1_SDA	SPI2_NSS I2S2_WS				CAN1_TX			SDIO_D5	DCMI_D7		EVENTOUT
	PB10		TIM2_CH3			I2C2_SCL	SPI2_SCK I2S2_CK		USART3_TX			OTG_HS_ULPI_D3	ETH_ MII_RX_ER				EVENTOUT
	PB11		TIM2_CH4			I2C2_SDA			USART3_RX			OTG_HS_ULPI_D4	ETH _MII_TX_EN ETH _RMII_TX_EN				EVENTOUT
	PB12		TIM1_BKIN			I2C2_SMBA	SPI2_NSS I2S2_WS		USART3_CK		CAN2_RX	OTG_HS_ULPI_D5	ETH _MII_TXD0 ETH _RMII_TXD0	OTG_HS_ID			EVENTOUT
	PB13		TIM1_CH1N				SPI2_SCK I2S2_CK		USART3_CTS		CAN2_TX	OTG_HS_ULPI_D6	ETH _MII_TXD1 ETH _RMII_TXD1				EVENTOUT
	PB14		TIM1_CH2N		TIM8_CH2N		SPI2_MISO	I2S2ext_SD	USART3_RTS		TIM12_CH1			OTG_HS_DM			EVENTOUT
	PB15	RTC_REFIN	TIM1_CH3N		TIM8_CH3N		SPI2_MOSI I2S2_SD				TIM12_CH2			OTG_HS_DP			EVENTOUT

Table 9. Alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10 /11	I2C1/2/3	SPI1/SPI2/ I2S2/I2S2ext	SPI3/I2Sext /I2S3	USART1/2/3/ I2S3ext	UART4/5/ USART6	CAN1/2 TIM12/13/ 14	OTG_FS/ OTG_HS	ETH	FSMC/SDIO /OTG_FS	DCMI		
Port C	PC0											OTG_HS_ULPI_ STP					EVENTOUT
	PC1												ETH_MDC				EVENTOUT
	PC2						SPI2_MISO	I2S2ext_SD				OTG_HS_ULPI_ DIR	ETH _MII_TXD2				EVENTOUT
	PC3						SPI2_MOSI I2S2_SD					OTG_HS_ULPI_ NXT	ETH _MII_TX_CLK				EVENTOUT
	PC4												ETH_MII_RXD0 ETH_RMII_RXD0				EVENTOUT
	PC5												ETH _MII_RXD1 ETH _RMII_RXD1				EVENTOUT
	PC6			TIM3_CH1	TIM8_CH1		I2S2_MCK			USART6_TX				SDIO_D6	DCMI_D0		EVENTOUT
	PC7			TIM3_CH2	TIM8_CH2			I2S3_MCK		USART6_RX				SDIO_D7	DCMI_D1		EVENTOUT
	PC8			TIM3_CH3	TIM8_CH3					USART6_CK				SDIO_D0	DCMI_D2		EVENTOUT
	PC9	MCO2		TIM3_CH4	TIM8_CH4	I2C3_SDA	I2S_CKIN							SDIO_D1	DCMI_D3		EVENTOUT
	PC10							SPI3_SCK/ I2S3_CK	USART3_TX/	UART4_TX				SDIO_D2	DCMI_D8		EVENTOUT
	PC11						I2S3ext_SD	SPI3_MISO/	USART3_RX	UART4_RX				SDIO_D3	DCMI_D4		EVENTOUT
	PC12							SPI3_MOSI I2S3_SD	USART3_CK	UART5_TX				SDIO_CK	DCMI_D9		EVENTOUT
	PC13																EVENTOUT
	PC14																EVENTOUT
	PC15																EVENTOUT

Table 9. Alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10 /11	I2C1/2/3	SPI1/SPI2/ I2S2/I2S2ext	SPI3/I2Sext /I2S3	USART1/2/3/ I2S3ext	UART4/5/ USART6	CAN1/2 TIM12/13/ 14	OTG_FS/ OTG_HS	ETH	FSMC/SDIO /OTG_FS	DCMI		
Port D	PD0										CAN1_RX			FSMC_D2			EVENTOUT
	PD1										CAN1_TX			FSMC_D3			EVENTOUT
	PD2			TIM3_ETR						UART5_RX				SDIO_CMD	DCMI_D11		EVENTOUT
	PD3								USART2_CTS					FSMC_CLK			EVENTOUT
	PD4								USART2_RTS					FSMC_NOE			EVENTOUT
	PD5								USART2_TX					FSMC_NWE			EVENTOUT
	PD6								USART2_RX					FSMC_NWAIT			EVENTOUT
	PD7								USART2_CK					FSMC_NE1/ FSMC_NCE2			EVENTOUT
	PD8								USART3_TX					FSMC_D13			EVENTOUT
	PD9								USART3_RX					FSMC_D14			EVENTOUT
	PD10								USART3_CK					FSMC_D15			EVENTOUT
	PD11								USART3_CTS					FSMC_A16			EVENTOUT
	PD12			TIM4_CH1					USART3_RTS					FSMC_A17			EVENTOUT
	PD13			TIM4_CH2										FSMC_A18			EVENTOUT
	PD14			TIM4_CH3										FSMC_D0			EVENTOUT
	PD15			TIM4_CH4										FSMC_D1			EVENTOUT

Table 9. Alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/2/3	SPI1/SPI2/I2S2/I2S2ext	SPI3/I2Sext/I2S3	USART1/2/3/I2S3ext	UART4/5/USART6	CAN1/2 TIM12/13/14	OTG_FS/OTG_HS	ETH	FSMC/SDIO/OTG_FS	DCMI		
Port E	PE0			TIM4_ETR										FSMC_NBL0	DCMI_D2		EVENTOUT
	PE1													FSMC_NBL1	DCMI_D3		EVENTOUT
	PE2	TRACECLK											ETH _MII_TXD3	FSMC_A23			EVENTOUT
	PE3	TRACED0												FSMC_A19			EVENTOUT
	PE4	TRACED1												FSMC_A20	DCMI_D4		EVENTOUT
	PE5	TRACED2			TIM9_CH1									FSMC_A21	DCMI_D6		EVENTOUT
	PE6	TRACED3			TIM9_CH2									FSMC_A22	DCMI_D7		EVENTOUT
	PE7		TIM1_ETR											FSMC_D4			EVENTOUT
	PE8		TIM1_CH1N											FSMC_D5			EVENTOUT
	PE9		TIM1_CH1											FSMC_D6			EVENTOUT
	PE10		TIM1_CH2N											FSMC_D7			EVENTOUT
	PE11		TIM1_CH2											FSMC_D8			EVENTOUT
	PE12		TIM1_CH3N											FSMC_D9			EVENTOUT
	PE13		TIM1_CH3											FSMC_D10			EVENTOUT
	PE14		TIM1_CH4											FSMC_D11			EVENTOUT
	PE15		TIM1_BKIN											FSMC_D12			EVENTOUT

Table 9. Alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10 /11	I2C1/2/3	SPI1/SPI2/ I2S2/I2S2e xt	SPI3/I2Sext /I2S3	USART1/2/3/ I2S3ext	UART4/5/ USART6	CAN1/2 TIM12/13/ 14	OTG_FS/ OTG_HS	ETH	FSMC/SDIO /OTG_FS	DCMI		
Port F	PF0					I2C2_SDA								FSMC_A0			EVENTOUT
	PF1					I2C2_SCL								FSMC_A1			EVENTOUT
	PF2					I2C2_ SMBA								FSMC_A2			EVENTOUT
	PF3													FSMC_A3			EVENTOUT
	PF4													FSMC_A4			EVENTOUT
	PF5													FSMC_A5			EVENTOUT
	PF6				TIM10_CH1									FSMC_NIORD			EVENTOUT
	PF7				TIM11_CH1									FSMC_NREG			EVENTOUT
	PF8										TIM13_CH1			FSMC_ NIOWR			EVENTOUT
	PF9										TIM14_CH1			FSMC_CD			EVENTOUT
	PF10													FSMC_INTR			EVENTOUT
	PF11														DCMI_D12		EVENTOUT
	PF12													FSMC_A6			EVENTOUT
	PF13													FSMC_A7			EVENTOUT
	PF14													FSMC_A8			EVENTOUT
	PF15													FSMC_A9			EVENTOUT

Table 9. Alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10 /11	I2C1/2/3	SPI1/SPI2/ I2S2/I2S2ext	SPI3/I2Sext /I2S3	USART1/2/3/ I2S3ext	UART4/5/ USART6	CAN1/2 TIM12/13/ 14	OTG_FS/ OTG_HS	ETH	FSMC/SDIO /OTG_FS	DCMI		
Port G	PG0													FSMC_A10			EVENTOUT
	PG1													FSMC_A11			EVENTOUT
	PG2													FSMC_A12			EVENTOUT
	PG3													FSMC_A13			EVENTOUT
	PG4													FSMC_A14			EVENTOUT
	PG5													FSMC_A15			EVENTOUT
	PG6													FSMC_INT2			EVENTOUT
	PG7									USART6_CK				FSMC_INT3			EVENTOUT
	PG8									USART6_ RTS			ETH _PPS_OUT				EVENTOUT
	PG9									USART6_RX				FSMC_NE2/ FSMC_NCE3			EVENTOUT
	PG10													FSMC_ NCE4_1/ FSMC_NE3			EVENTOUT
	PG11												ETH _MII_TX_EN ETH _RMII_ TX_EN	FSMC_NCE4_ 2			EVENTOUT
	PG12									USART6_ RTS				FSMC_NE4			EVENTOUT
	PG13									UART6_CTS			ETH _MII_TXD0 ETH _RMII_TXD0	FSMC_A24			EVENTOUT
	PG14									USART6_TX			ETH _MII_TXD1 ETH _RMII_TXD1	FSMC_A25			EVENTOUT
	PG15									USART6_ CTS					DCMI_D13		EVENTOUT

Table 9. Alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/2/3	SPI1/SPI2/I2S2/I2S2ext	SPI3/I2Sext/I2S3	USART1/2/3/I2S3ext	UART4/5/USART6	CAN1/2 TIM12/13/14	OTG_FS/OTG_HS	ETH	FSMC/SDIO/OTG_FS	DCMI		
Port H	PH0																EVENTOUT
	PH1																EVENTOUT
	PH2												ETH _MII_CRS				EVENTOUT
	PH3												ETH _MII_COL				EVENTOUT
	PH4					I2C2_SCL						OTG_HS_ULPI_NXT					EVENTOUT
	PH5					I2C2_SDA											EVENTOUT
	PH6					I2C2_SMBA					TIM12_CH1		ETH _MII_RXD2				EVENTOUT
	PH7					I2C3_SCL							ETH _MII_RXD3				EVENTOUT
	PH8					I2C3_SDA									DCMI_HSYNC		EVENTOUT
	PH9					I2C3_SMBA					TIM12_CH2				DCMI_D0		EVENTOUT
	PH10			TIM5_CH1											DCMI_D1		EVENTOUT
	PH11			TIM5_CH2											DCMI_D2		EVENTOUT
	PH12			TIM5_CH3											DCMI_D3		EVENTOUT
	PH13				TIM8_CH1N						CAN1_TX						EVENTOUT
	PH14				TIM8_CH2N										DCMI_D4		EVENTOUT
	PH15				TIM8_CH3N										DCMI_D11		EVENTOUT

Table 9. Alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/2/3	SPI1/SPI2/I2S2/I2S2ext	SPI3/I2Sext/I2S3	USART1/2/3/I2S3ext	UART4/5/USART6	CAN1/2 TIM12/13/14	OTG_FS/OTG_HS	ETH	FSMC/SDIO/OTG_FS	DCMI		
Port I	PI0			TIM5_CH4			SPI2_NSS I2S2_WS								DCMI_D13		EVENTOUT
	PI1						SPI2_SCK I2S2_CK								DCMI_D8		EVENTOUT
	PI2				TIM8_CH4		SPI2_MISO	I2S2ext_SD							DCMI_D9		EVENTOUT
	PI3				TIM8_ETR		SPI2_MOSI I2S2_SD								DCMI_D10		EVENTOUT
	PI4				TIM8_BKIN										DCMI_D5		EVENTOUT
	PI5				TIM8_CH1										DCMI_VSYNC		EVENTOUT
	PI6				TIM8_CH2										DCMI_D6		EVENTOUT
	PI7				TIM8_CH3										DCMI_D7		EVENTOUT
	PI8																EVENTOUT
	PI9										CAN1_RX						EVENTOUT
	PI10												ETH _MII_RX_ER				EVENTOUT
	PI11											OTG_HS_ULPI_DIR					EVENTOUT

4 Memory mapping

The memory map is shown in *Figure 18*.

Figure 18. STM32F41xxx memory map

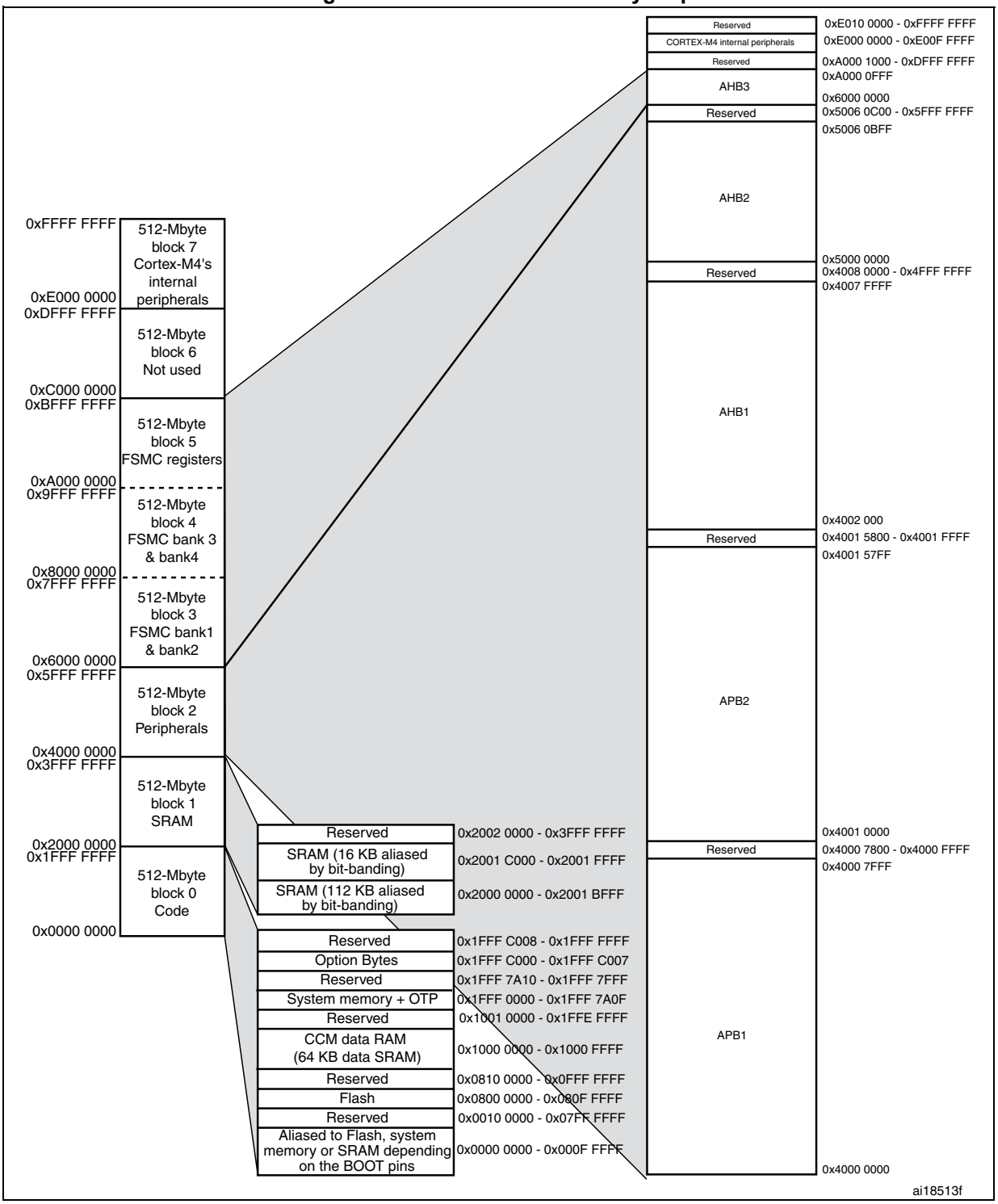


Table 10. STM32F41x register boundary addresses

Bus	Boundary address	Peripheral
	0xE00F FFFF - 0xFFFF FFFF	Reserved
Cortex-M4	0xE000 0000 - 0xE00F FFFF	Cortex-M4 internal peripherals
	0xA000 1000 - 0xDFFF FFFF	Reserved
AHB3	0xA000 0000 - 0xA000 0FFF	FSMC control register
	0x9000 0000 - 0x9FFF FFFF	FSMC bank 4
	0x8000 0000 - 0x8FFF FFFF	FSMC bank 3
	0x7000 0000 - 0x7FFF FFFF	FSMC bank 2
	0x6000 0000 - 0x6FFF FFFF	FSMC bank 1
	0x5006 0C00- 0x5FFF FFFF	Reserved
AHB2	0x5006 0800 - 0x5006 0BFF	RNG
	0x5006 0400 - 0x5006 07FF	HASH
	0x5006 0000 - 0x5006 03FF	CRYP
	0x5005 0400 - 0x5005 FFFF	Reserved
	0x5005 0000 - 0x5005 03FF	DCMI
	0x5004 0000- 0x5004 FFFF	Reserved
	0x5000 0000 - 0x5003 FFFF	USB OTG FS
	0x4008 0000- 0x4FFF FFFF	Reserved

Table 10. STM32F41x register boundary addresses (continued)

Bus	Boundary address	Peripheral
AHB1	0x4004 0000 - 0x4007 FFFF	USB OTG HS
	0x4002 9400 - 0x4003 FFFF	Reserved
	0x4002 9000 - 0x4002 93FF	ETHERNET MAC
	0x4002 8C00 - 0x4002 8FFF	
	0x4002 8800 - 0x4002 8BFF	
	0x4002 8400 - 0x4002 87FF	
	0x4002 8000 - 0x4002 83FF	
	0x4002 6800 - 0x4002 7FFF	Reserved
	0x4002 6400 - 0x4002 67FF	DMA2
	0x4002 6000 - 0x4002 63FF	DMA1
	0x4002 5000 - 0x4002 5FFF	Reserved
	0x4002 4000 - 0x4002 4FFF	BKPSRAM
	0x4002 3C00 - 0x4002 3FFF	Flash interface register
	0x4002 3800 - 0x4002 3BFF	RCC
	0x4002 3400 - 0x4002 37FF	Reserved
	0x4002 3000 - 0x4002 33FF	CRC
	0x4002 2400 - 0x4002 2FFF	Reserved
	0x4002 2000 - 0x4002 23FF	GPIOI
	0x4002 1C00 - 0x4002 1FFF	GPIOH
	0x4002 1800 - 0x4002 1BFF	GPIOG
	0x4002 1400 - 0x4002 17FF	GPIOF
	0x4002 1000 - 0x4002 13FF	GPIOE
	0x4002 0C00 - 0x4002 0FFF	GPIOD
	0x4002 0800 - 0x4002 0BFF	GPIOC
	0x4002 0400 - 0x4002 07FF	GPIOB
	0x4002 0000 - 0x4002 03FF	GPIOA
	0x4001 5800- 0x4001 FFFF	Reserved

Table 10. STM32F41x register boundary addresses (continued)

Bus	Boundary address	Peripheral
APB2	0x4001 4C00 - 0x4001 57FF	Reserved
	0x4001 4800 - 0x4001 4BFF	TIM11
	0x4001 4400 - 0x4001 47FF	TIM10
	0x4001 4000 - 0x4001 43FF	TIM9
	0x4001 3C00 - 0x4001 3FFF	EXTI
	0x4001 3800 - 0x4001 3BFF	SYSCFG
	0x4001 3400 - 0x4001 37FF	Reserved
	0x4001 3000 - 0x4001 33FF	SPI1
	0x4001 2C00 - 0x4001 2FFF	SDIO
	0x4001 2400 - 0x4001 2BFF	Reserved
	0x4001 2000 - 0x4001 23FF	ADC1 - ADC2 - ADC3
	0x4001 1800 - 0x4001 1FFF	Reserved
	0x4001 1400 - 0x4001 17FF	USART6
	0x4001 1000 - 0x4001 13FF	USART1
	0x4001 0800 - 0x4001 0FFF	Reserved
	0x4001 0400 - 0x4001 07FF	TIM8
	0x4001 0000 - 0x4001 03FF	TIM1
	0x4000 7800- 0x4000 FFFF	Reserved

Table 10. STM32F41x register boundary addresses (continued)

Bus	Boundary address	Peripheral
APB1	0x4000 7800 - 0x4000 7FFF	Reserved
	0x4000 7400 - 0x4000 77FF	DAC
	0x4000 7000 - 0x4000 73FF	PWR
	0x4000 6C00 - 0x4000 6FFF	Reserved
	0x4000 6800 - 0x4000 6BFF	CAN2
	0x4000 6400 - 0x4000 67FF	CAN1
	0x4000 6000 - 0x4000 63FF	Reserved
	0x4000 5C00 - 0x4000 5FFF	I2C3
	0x4000 5800 - 0x4000 5BFF	I2C2
	0x4000 5400 - 0x4000 57FF	I2C1
	0x4000 5000 - 0x4000 53FF	UART5
	0x4000 4C00 - 0x4000 4FFF	UART4
	0x4000 4800 - 0x4000 4BFF	USART3
	0x4000 4400 - 0x4000 47FF	USART2
	0x4000 4000 - 0x4000 43FF	I2S3ext
	0x4000 3C00 - 0x4000 3FFF	SPI3 / I2S3
	0x4000 3800 - 0x4000 3BFF	SPI2 / I2S2
	0x4000 3400 - 0x4000 37FF	I2S2ext
	0x4000 3000 - 0x4000 33FF	IWDG
	0x4000 2C00 - 0x4000 2FFF	WWDG
	0x4000 2800 - 0x4000 2BFF	RTC & BKP Registers
	0x4000 2400 - 0x4000 27FF	Reserved
	0x4000 2000 - 0x4000 23FF	TIM14
	0x4000 1C00 - 0x4000 1FFF	TIM13
	0x4000 1800 - 0x4000 1BFF	TIM12
	0x4000 1400 - 0x4000 17FF	TIM7
	0x4000 1000 - 0x4000 13FF	TIM6
	0x4000 0C00 - 0x4000 0FFF	TIM5
	0x4000 0800 - 0x4000 0BFF	TIM4
	0x4000 0400 - 0x4000 07FF	TIM3
	0x4000 0000 - 0x4000 03FF	TIM2

5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

5.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

5.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.3 V (for the 1.8 V ≤ V_{DD} ≤ 3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2Σ).

5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 19*.

5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 20*.

Figure 19. Pin loading conditions

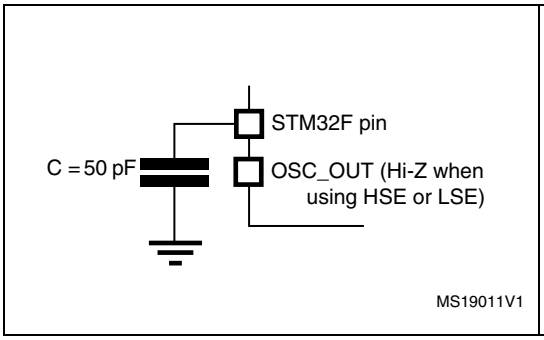
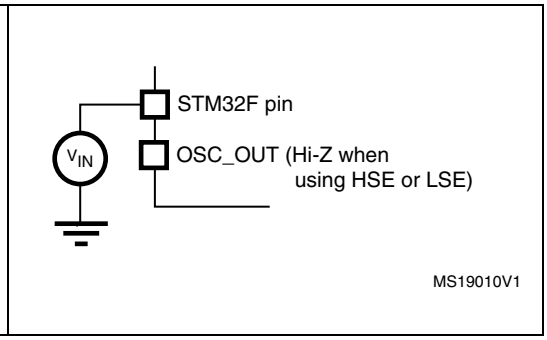
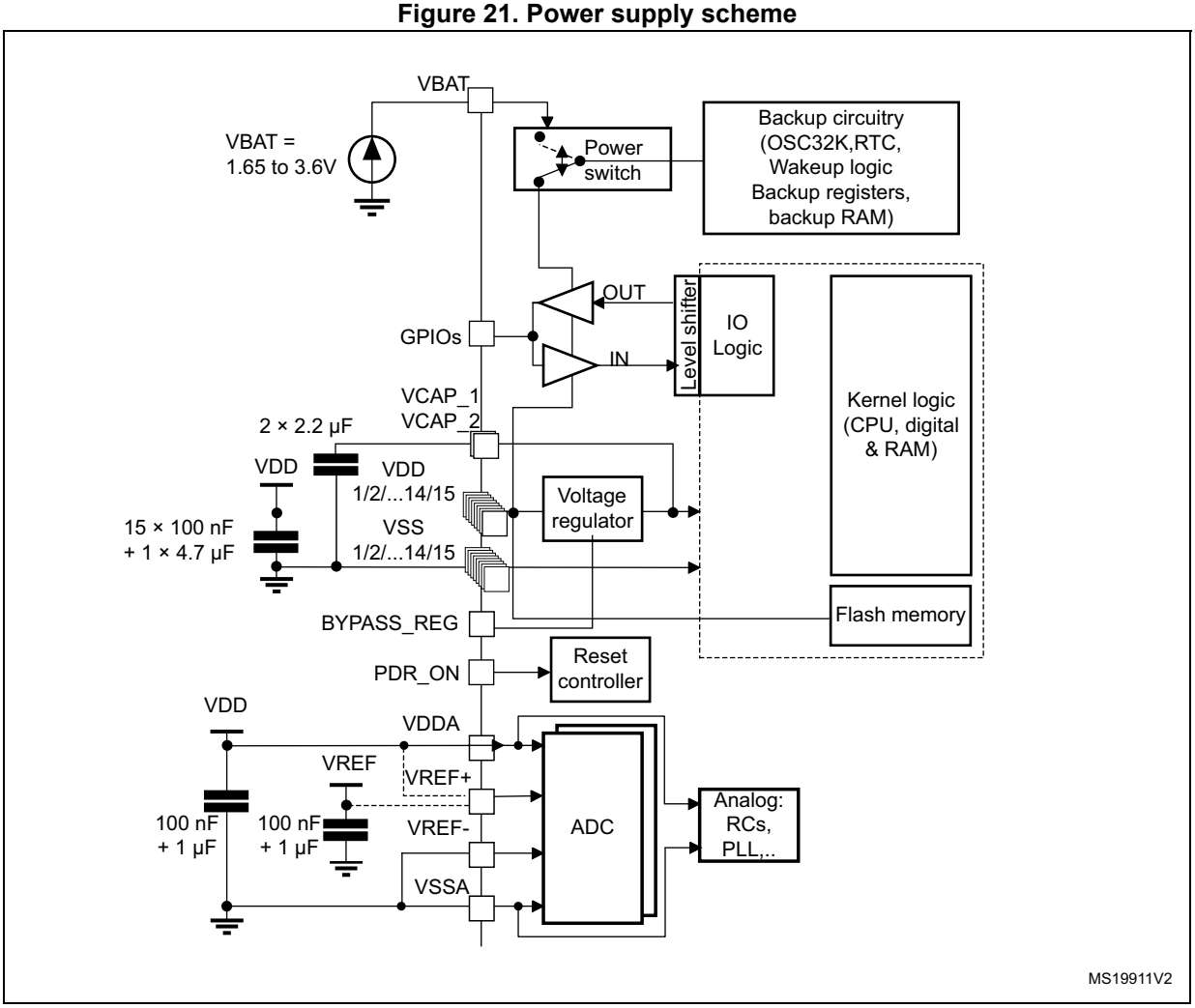


Figure 20. Pin input voltage



5.1.6 Power supply scheme

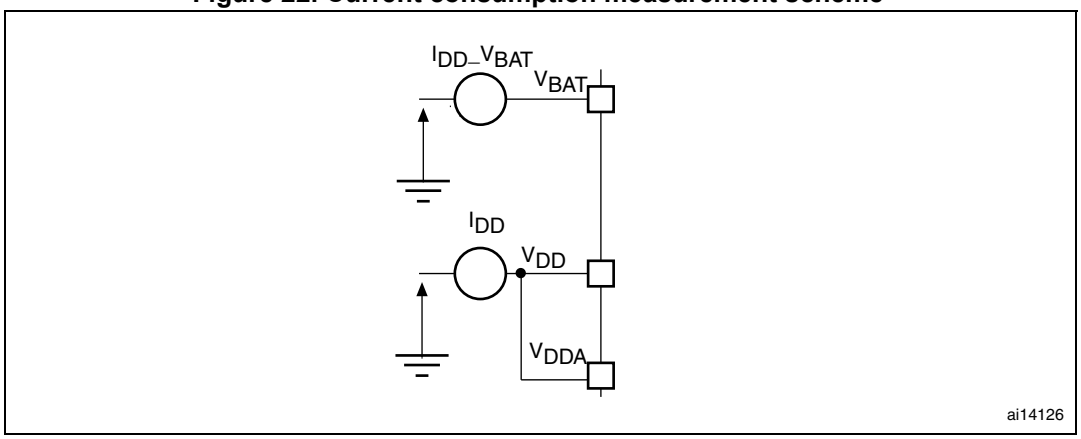
Figure 21. Power supply scheme



1. Each power supply pair must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.
2. To connect BYPASS_REG and PDR_ON pins, refer to *Section 2.2.16: Voltage regulator* and *Table 2.2.15: Power supply supervisor*.
3. The two 2.2 µF ceramic capacitors should be replaced by two 100 nF decoupling capacitors when the voltage regulator is OFF.
4. The 4.7 µF ceramic capacitor must be connected to one of the V_{DD} pin.
5. V_{DDA}=V_{DD} and V_{SSA}=V_{SS}.

5.1.7 Current consumption measurement

Figure 22. Current consumption measurement scheme



5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 11: Voltage characteristics*, *Table 12: Current characteristics*, and *Table 13: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 11. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD}–V_{SS}	External main supply voltage (including V_{DDA}, V_{DD})(1)	–0.3	4.0	V
V_{IN}	Input voltage on five-volt tolerant pin(2)	V_{SS}–0.3	V_{DD}+4	
	Input voltage on any other pin	V_{SS}–0.3	4.0	
$\lvert\Delta V_{DDx}\rvert$	Variations between different V_{DD} power pins	-	50	mV
$\lvert V_{SSX} - V_{SS}\rvert$	Variations between all the different ground pins	-	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 5.3.14: Absolute maximum ratings (electrical sensitivity)*		

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum value must always be respected. Refer to *Table 12* for the values of the maximum allowed injected current.

Table 12. Current characteristics

Symbol	Ratings	Max.	Unit
I_{VDD}	Total current into V_{DD} power lines (source)(1)	240	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)(1)	240	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current source by any I/Os and control pin	25	
$I_{INJ(PIN)}$ (2)	Injected current on five-volt tolerant I/O(3)	–5/+0	
	Injected current on any other pin(4)	±5	
$\Sigma I_{INJ(PIN)}$(4)	Total injected current (sum of all I/O and control pins)(5)	±25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. Negative injection disturbs the analog performance of the device. See note in *Section 5.3.21: 12-bit ADC characteristics*.
3. Positive injection is not possible on these I/Os. A negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 11* for the values of the maximum allowed input voltage.
4. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 11* for the values of the maximum allowed input voltage.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 13. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	125	°C

5.3 Operating conditions

5.3.1 General operating conditions

Table 14. General operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HCLK}	Internal AHB clock frequency	VOS bit in PWR_CR register = 0(1)	0		144	MHz
		VOS bit in PWR_CR register= 1	0		168	
f_{PCLK1}	Internal APB1 clock frequency		0		42	
f_{PCLK2}	Internal APB2 clock frequency		0		84	
V_{DD}	Standard operating voltage		1.8(2)		3.6	V
V_{DDA}(3)(4)	Analog operating voltage (ADC limited to 1.2 M samples)	Must be the same potential as V_{DD}(5)	1.8(2)		2.4	V
	Analog operating voltage (ADC limited to 1.4 M samples)		2.4		3.6	
V_{BAT}	Backup operating voltage		1.65		3.6	V

Table 14. General operating conditions (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{12}	Regulator ON: 1.2 V internal voltage on V_{CAP_1}/V_{CAP_2} pins	VOS bit in PWR_CR register = 0(1) Max frequency 144MHz	1.08	1.14	1.20	V
		VOS bit in PWR_CR register= 1 Max frequency 168MHz	1.20	1.26	1.32	V
	Regulator OFF: 1.2 V external voltage must be supplied from external regulator on V_{CAP_1}/V_{CAP_2} pins	Max frequency 144MHz	1.10	1.14	1.20	V
		Max frequency 168MHz	1.20	1.26	1.30	V
V_{IN}	Input voltage on RST and FT pins(6)	2 V ≤ V_{DD} ≤ 3.6 V	–0.3	-	5.5	V
		V_{DD} ≤ 2 V	–0.3	-	5.2	
	Input voltage on TTa pins		–0.3	-	V_{DDA}+ 0.3	
	Input voltage on B pin			-	5.5	
P_D	Power dissipation at T_A = 85 °C for suffix 6 or T_A = 105 °C for suffix 7(7)	LQFP64	-		435	mW
		LQFP100	-		465	
		LQFP144	-		500	
		LQFP176	-		526	
		UFBGA176	-		513	
		WLCSP90	-		543	
T_A	Ambient temperature for 6 suffix version	Maximum power dissipation	–40		85	°C
		Low-power dissipation(8)	–40		105	
	Ambient temperature for 7 suffix version	Maximum power dissipation	–40		105	°C
		Low-power dissipation(8)	–40		125	
T_J	Junction temperature range	6 suffix version	–40		105	°C
		7 suffix version	–40		125	

1. The average expected gain in power consumption when VOS = 0 compared to VOS = 1 is around 10% for the whole temperature range, when the system clock frequency is between 30 and 144 MHz.
2. V_{DD}/V_{DDA} minimum value of 1.7 V is obtained when the device operates in reduced temperature range, and with the use of an external power supply supervisor (refer to *Section : Internal reset OFF*).
3. When the ADC is used, refer to *Table 67: ADC characteristics*.
4. If V_{REF+} pin is present, it must respect the following condition: V_{DDA}-V_{REF+} < 1.2 V.
5. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and power-down operation.
6. To sustain a voltage higher than V_{DD}+0.3, the internal pull-up and pull-down resistors must be disabled.
7. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax}.
8. In low-power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax}.

Table 15. Limitations depending on the operating power supply range

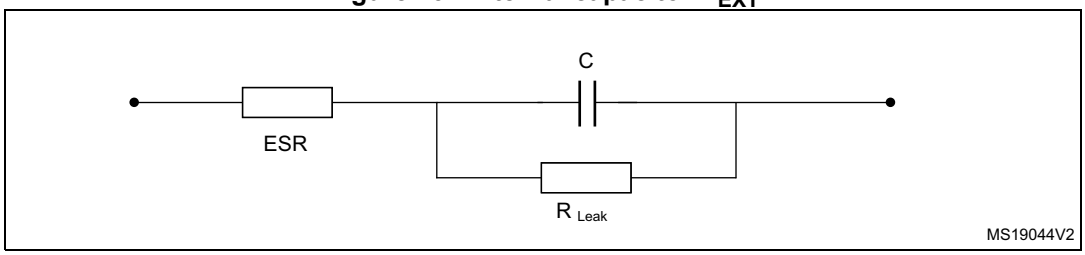
Operating power supply range	ADC operation	Maximum Flash memory access frequency with no wait state ($f_{Flashmax}$)	Maximum Flash memory access frequency with wait states(1) (2)	I/O operation	Clock output Frequency on I/O pins	Possible Flash memory operations
V_{DD} =1.8 to 2.1 V(3)	Conversion time up to 1.2 Msps	20 MHz(4)	160 MHz with 7 wait states	– Degraded speed performance – No I/O compensation	up to 30 MHz	8-bit erase and program operations only
V_{DD} = 2.1 to 2.4 V	Conversion time up to 1.2 Msps	22 MHz	168 MHz with 7 wait states	– Degraded speed performance – No I/O compensation	up to 30 MHz	16-bit erase and program operations
V_{DD} = 2.4 to 2.7 V	Conversion time up to 2.4 Msps	24 MHz	168 MHz with 6 wait states	– Degraded speed performance – I/O compensation works	up to 48 MHz	16-bit erase and program operations
V_{DD} = 2.7 to 3.6 V(5)	Conversion time up to 2.4 Msps	30 MHz	168 MHz with 5 wait states	– Full-speed operation – I/O compensation works	– up to 60 MHz when V_{DD} = 3.0 to 3.6 V – up to 48 MHz when V_{DD} = 2.7 to 3.0 V	32-bit erase and program operations

1. It applies only when code executed from Flash memory access, when code executed from RAM, no wait state is required.
2. Thanks to the ART accelerator and the 128-bit Flash memory, the number of wait states given here does not impact the execution speed from Flash memory since the ART accelerator allows to achieve a performance equivalent to 0 wait state program execution.
3. V_{DD}/VDDA minimum value of 1.7 V is obtained when the device operates in reduced temperature range, and with the use of an external power supply supervisor (refer to *Section : Internal reset OFF*).
4. Prefetch is not available. Refer to AN3430 application note for details on how to adjust performance and power.
5. The voltage range for OTG USB FS can drop down to 2.7 V. However it is degraded between 2.7 and 3 V.

5.3.2 V_{CAP_1}/V_{CAP_2} external capacitor

Stabilization for the main regulator is achieved by connecting an external capacitor C_{EXT} to the V_{CAP_1}/V_{CAP_2} pins. C_{EXT} is specified in *Table 16*.

Figure 23. External capacitor C_{EXT}



1. Legend: ESR is the equivalent series resistance.

Table 16. V_{CAP_1}/V_{CAP_2} operating conditions(1)

Symbol	Parameter	Conditions
CEXT	Capacitance of external capacitor	2.2 µF
ESR	ESR of external capacitor	< 2 Ω

1. When bypassing the voltage regulator, the two 2.2 µF V_{CAP} capacitors are not required and should be replaced by two 100 nF decoupling capacitors.

5.3.3 Operating conditions at power-up / power-down (regulator ON)

Subject to general operating conditions for T_A.

Table 17. Operating conditions at power-up / power-down (regulator ON)

Symbol	Parameter	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	20	∞	µs/V
	V_{DD} fall time rate	20	∞	

5.3.4 Operating conditions at power-up / power-down (regulator OFF)

Subject to general operating conditions for T_A.

Table 18. Operating conditions at power-up / power-down (regulator OFF)(1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	Power-up	20	∞	µs/V
	V_{DD} fall time rate	Power-down	20	∞	
t_{VCAP}	V_{CAP_1} and V_{CAP_2} rise time rate	Power-up	20	∞	
	V_{CAP_1} and V_{CAP_2} fall time rate	Power-down	20	∞	

1. To reset the internal logic at power-down, a reset must be applied on pin PA0 when V_{DD} reach below minimum value of V_{12}.

5.3.5 Embedded reset and power control block characteristics

The parameters given in *Table 19* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 14*.

Table 19. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection	PLS[2:0]=000 (rising edge)	2.09	2.14	2.19	V
		PLS[2:0]=000 (falling edge)	1.98	2.04	2.08	V
		PLS[2:0]=001 (rising edge)	2.23	2.30	2.37	V
		PLS[2:0]=001 (falling edge)	2.13	2.19	2.25	V
		PLS[2:0]=010 (rising edge)	2.39	2.45	2.51	V
		PLS[2:0]=010 (falling edge)	2.29	2.35	2.39	V
		PLS[2:0]=011 (rising edge)	2.54	2.60	2.65	V
		PLS[2:0]=011 (falling edge)	2.44	2.51	2.56	V
		PLS[2:0]=100 (rising edge)	2.70	2.76	2.82	V
		PLS[2:0]=100 (falling edge)	2.59	2.66	2.71	V
		PLS[2:0]=101 (rising edge)	2.86	2.93	2.99	V
		PLS[2:0]=101 (falling edge)	2.65	2.84	2.92	V
		PLS[2:0]=110 (rising edge)	2.96	3.03	3.10	V
		PLS[2:0]=110 (falling edge)	2.85	2.93	2.99	V
		PLS[2:0]=111 (rising edge)	3.07	3.14	3.21	V
		PLS[2:0]=111 (falling edge)	2.95	3.03	3.09	V
$V_{PVDhyst}$(1)	PVD hysteresis		-	100	-	mV
$V_{POR/PDR}$	Power-on/power-down reset threshold	Falling edge	1.60	1.68	1.76	V
		Rising edge	1.64	1.72	1.80	V
$V_{PDRhyst}$(1)	PDR hysteresis		-	40	-	mV
V_{BOR1}	Brownout level 1 threshold	Falling edge	2.13	2.19	2.24	V
		Rising edge	2.23	2.29	2.33	V

Table 19. Embedded reset and power control block characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BOR2}	Brownout level 2 threshold	Falling edge	2.44	2.50	2.56	V
		Rising edge	2.53	2.59	2.63	V
V_{BOR3}	Brownout level 3 threshold	Falling edge	2.75	2.83	2.88	V
		Rising edge	2.85	2.92	2.97	V
$V_{BORhyst}$(1)	BOR hysteresis		-	100	-	mV
$T_{RSTTEMPO}$(1)(2)	Reset temporization		0.5	1.5	3.0	ms
I_{RUSH}(1)	InRush current on voltage regulator power-on (POR or wakeup from Standby)		-	160	200	mA
E_{RUSH}(1)	InRush energy on voltage regulator power-on (POR or wakeup from Standby)	V_{DD} = 1.8 V, T_A = 105 °C, I_{RUSH} = 171 mA for 31 µs	-	-	5.4	µC

1. Guaranteed by design, not tested in production.
2. The reset temporization is measured from the power-on (POR reset or wakeup from V_{BAT}) to the instant when first instruction is read by the user application code.

5.3.6 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.
The current consumption is measured as described in *Figure 22: Current consumption measurement scheme*.

All Run mode current consumption measurements given in this section are performed using a CoreMark-compliant code.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- At startup, all I/O pins are configured as analog inputs by firmware.
- All peripherals are disabled except if it is explicitly mentioned.
- The Flash memory access time is adjusted to f_{HCLK} frequency (0 wait state from 0 to 30 MHz, 1 wait state from 30 to 60 MHz, 2 wait states from 60 to 90 MHz, 3 wait states from 90 to 120 MHz, 4 wait states from 120 to 150 MHz, and 5 wait states from 150 to 168 MHz).
- When the peripherals are enabled HCLK is the system clock, $f_{PCLK1} = f_{HCLK}/4$, and $f_{PCLK2} = f_{HCLK}/2$, except is explicitly mentioned.
- The maximum values are obtained for V_{DD} = 3.6 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 3.3 V unless otherwise specified.

Table 20. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator enabled) or RAM (1)

Symbol	Parameter	Conditions	f_{HCLK}	Typ	Max(2)		Unit
				T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Run mode	External clock(3), all peripherals enabled(4)(5)	168 MHz	87	102	109	mA
			144 MHz	67	80	86	
			120 MHz	56	69	75	
			90 MHz	44	56	62	
			60 MHz	30	42	49	
			30 MHz	16	28	35	
			25 MHz	12	24	31	
			16 MHz(6)	9	20	28	
			8 MHz	5	17	24	
			4 MHz	3	15	22	
			2 MHz	2	14	21	
		External clock(3), all peripherals disabled(4)(5)	168 MHz	40	54	61	
			144 MHz	31	43	50	
			120 MHz	26	38	45	
			90 MHz	20	32	39	
			60 MHz	14	26	33	
			30 MHz	8	20	27	
			25 MHz	6	18	25	
			16 MHz(6)	5	16	24	
			8 MHz	3	15	22	
			4 MHz	2	14	21	
			2 MHz	2	14	21	

1. Code and data processing running from SRAM1 using boot pins.
2. Guaranteed by characterization results, tested in production at V_{DD} max and f_{HCLK} max with peripherals enabled.
3. External clock is 4 MHz and PLL is on when f_{HCLK} > 25 MHz.
4. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.6 mA per ADC for the analog part.
5. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.
6. In this case HCLK = system clock/2.

Table 21. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator disabled)

Symbol	Parameter	Conditions	f_{HCLK}	Typ	Max(1)		Unit
				T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Run mode	External clock(2), all peripherals enabled(3)(4)	168 MHz	93	109	117	mA
			144 MHz	76	89	96	
			120 MHz	67	79	86	
			90 MHz	53	65	73	
			60 MHz	37	49	56	
			30 MHz	20	32	39	
			25 MHz	16	27	35	
			16 MHz	11	23	30	
			8 MHz	6	18	25	
			4 MHz	4	16	23	
			2 MHz	3	15	22	
		External clock(2), all peripherals disabled(3)(4)	168 MHz	46	61	69	
			144 MHz	40	52	60	
			120 MHz	37	48	56	
			90 MHz	30	42	50	
			60 MHz	22	33	41	
			30 MHz	12	24	31	
			25 MHz	10	21	29	
			16 MHz	7	19	26	
			8 MHz	4	16	23	
			4 MHz	3	15	22	
			2 MHz	2	14	21	

1. Guaranteed by characterization results, tested in production at V_{DD} max and f_{HCLK} max with peripherals enabled.
2. External clock is 4 MHz and PLL is on when f_{HCLK} > 25 MHz.
3. When analog peripheral blocks such as (ADCs, DACs, HSE, LSE, HSI,LSI) are on, an additional power consumption should be considered.
4. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.6 mA per ADC for the analog part.

Figure 24. Typical current consumption versus temperature, Run mode, code with data processing running from Flash (ART accelerator ON) or RAM, and peripherals OFF

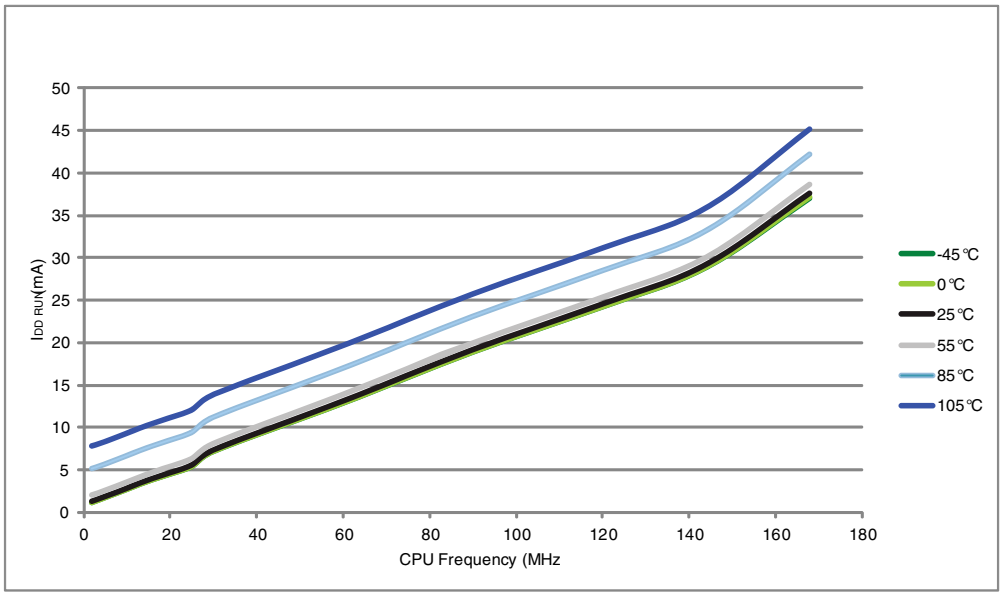


Figure 25. Typical current consumption versus temperature, Run mode, code with data processing running from Flash (ART accelerator ON) or RAM, and peripherals ON

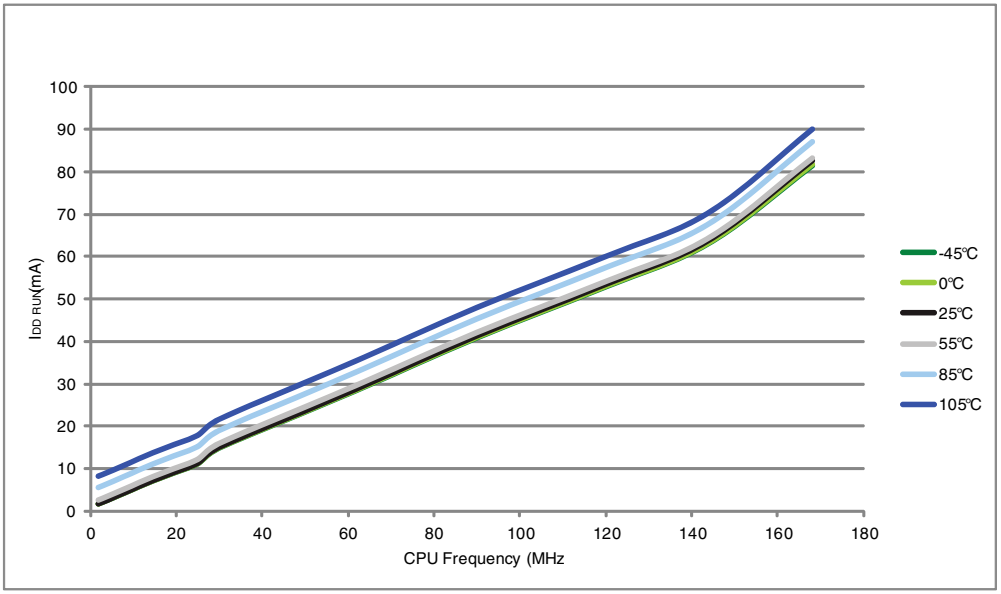


Figure 26. Typical current consumption versus temperature, Run mode, code with data processing running from Flash (ART accelerator OFF) or RAM, and peripherals OFF

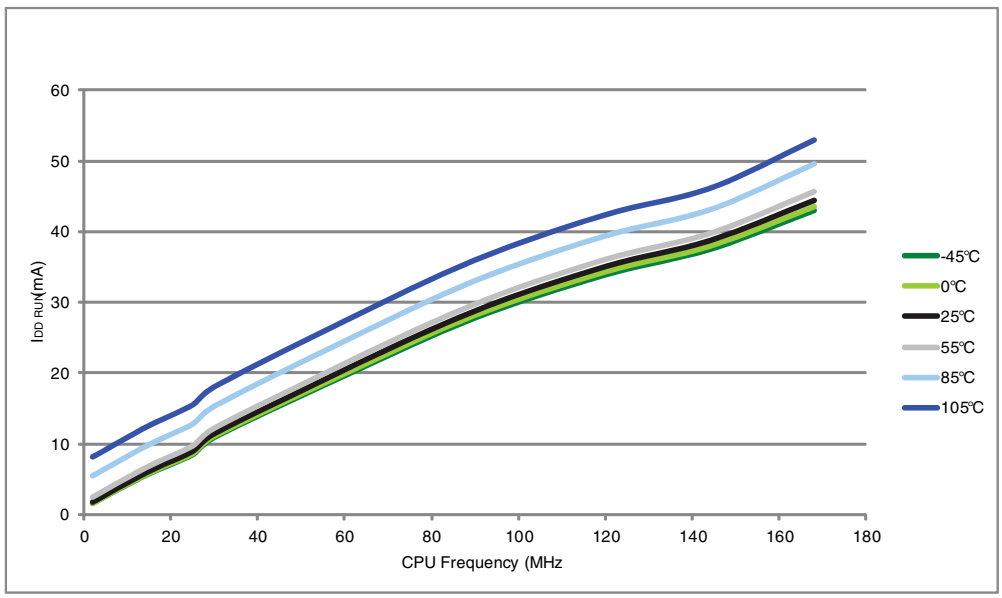


Figure 27. Typical current consumption versus temperature, Run mode, code with data processing running from Flash (ART accelerator OFF) or RAM, and peripherals ON

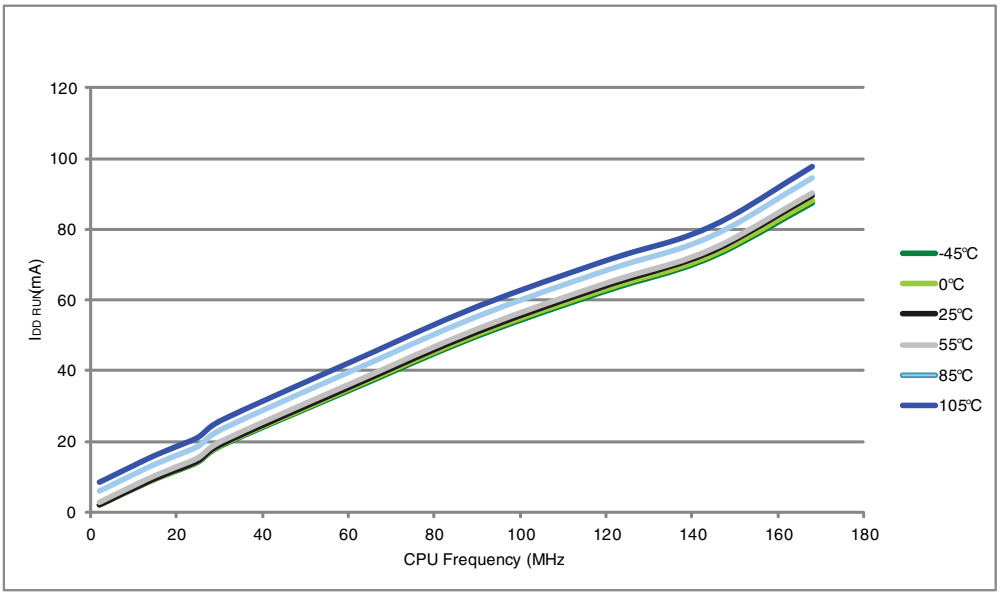


Table 22. Typical and maximum current consumption in Sleep mode

Symbol	Parameter	Conditions	f_{HCLK}	Typ	Max(1)		Unit
				T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Sleep mode	External clock(2), all peripherals enabled(3)	168 MHz	59	77	84	mA
			144 MHz	46	61	67	
			120 MHz	38	53	60	
			90 MHz	30	44	51	
			60 MHz	20	34	41	
			30 MHz	11	24	31	
			25 MHz	8	21	28	
			16 MHz	6	18	25	
			8 MHz	3	16	23	
			4 MHz	2	15	22	
			2 MHz	2	14	21	
		External clock(2), all peripherals disabled	168 MHz	12	27	35	
			144 MHz	9	22	29	
			120 MHz	8	20	28	
			90 MHz	7	19	26	
			60 MHz	5	17	24	
			30 MHz	3	16	23	
			25 MHz	2	15	22	
			16 MHz	2	14	21	
			8 MHz	1	14	21	
			4 MHz	1	13	21	
			2 MHz	1	13	21	

1. Guaranteed by characterization results, tested in production at V_{DD} max and f_{HCLK} max with peripherals enabled.
2. External clock is 4 MHz and PLL is on when f_{HCLK} > 25 MHz.
3. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).

Table 23. Typical and maximum current consumptions in Stop mode

Symbol	Parameter	Conditions	Typ	Max			Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_STOP}	Supply current in Stop mode with main regulator in Run mode	Flash in Stop mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	0.45	1.5	11.00	20.00	mA
		Flash in Deep power-down mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	0.40	1.5	11.00	20.00	
	Supply current in Stop mode with main regulator in Low-power mode	Flash in Stop mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	0.31	1.1	8.00	15.00	
		Flash in Deep power-down mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	0.28	1.1	8.00	15.00	

Table 24. Typical and maximum current consumptions in Standby mode

Symbol	Parameter	Conditions	Typ			Max(1)		Unit
			T_A = 25 °C			T_A = 85 °C	T_A = 105 °C	
			V_{DD} = 1.8 V	V_{DD}= 2.4 V	V_{DD} = 3.3 V	V_{DD} = 3.6 V		
I_{DD_STBY}	Supply current in Standby mode	Backup SRAM ON, low-speed oscillator and RTC ON	3.0	3.4	4.0	20	36	µA
		Backup SRAM OFF, low-speed oscillator and RTC ON	2.4	2.7	3.3	16	32	
		Backup SRAM ON, RTC OFF	2.4	2.6	3.0	12.5	24.8	
		Backup SRAM OFF, RTC OFF	1.7	1.9	2.2	9.8	19.2	

1. Guaranteed by characterization results, not tested in production.

Table 25. Typical and maximum current consumptions in V_{BAT} mode

Symbol	Parameter	Conditions	Typ			Max(1)		Unit
			T_A = 25 °C			T_A = 85 °C	T_A = 105 °C	
			V_{BAT} = 1.8 V	V_{BAT}= 2.4 V	V_{BAT} = 3.3 V	V_{BAT} = 3.6 V		
I_{DD_VBAT}	Backup domain supply current	Backup SRAM ON, low-speed oscillator and RTC ON	1.29	1.42	1.68	6	11	µA
		Backup SRAM OFF, low-speed oscillator and RTC ON	0.62	0.73	0.96	3	5	
		Backup SRAM ON, RTC OFF	0.79	0.81	0.86	5	10	
		Backup SRAM OFF, RTC OFF	0.10	0.10	0.10	2	4	

1. Guaranteed by characterization results, not tested in production.

Figure 28. Typical V_{BAT} current consumption (LSE and RTC ON/backup RAM OFF)

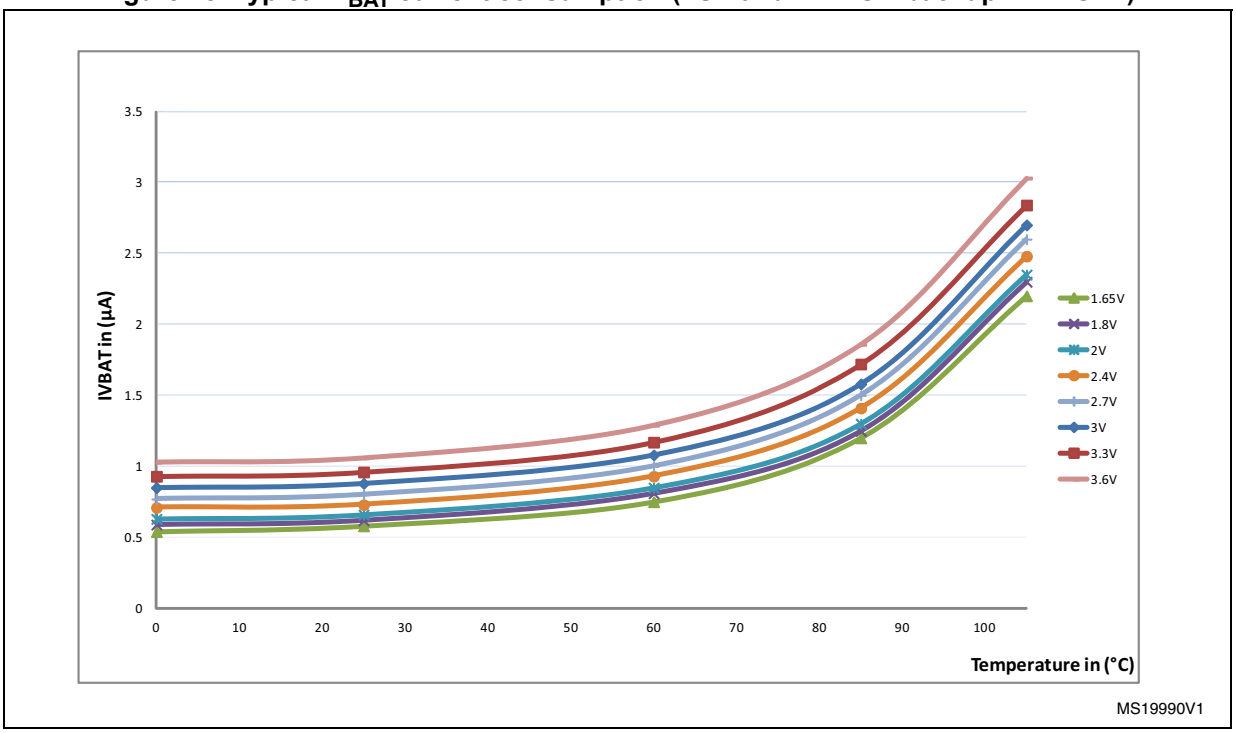
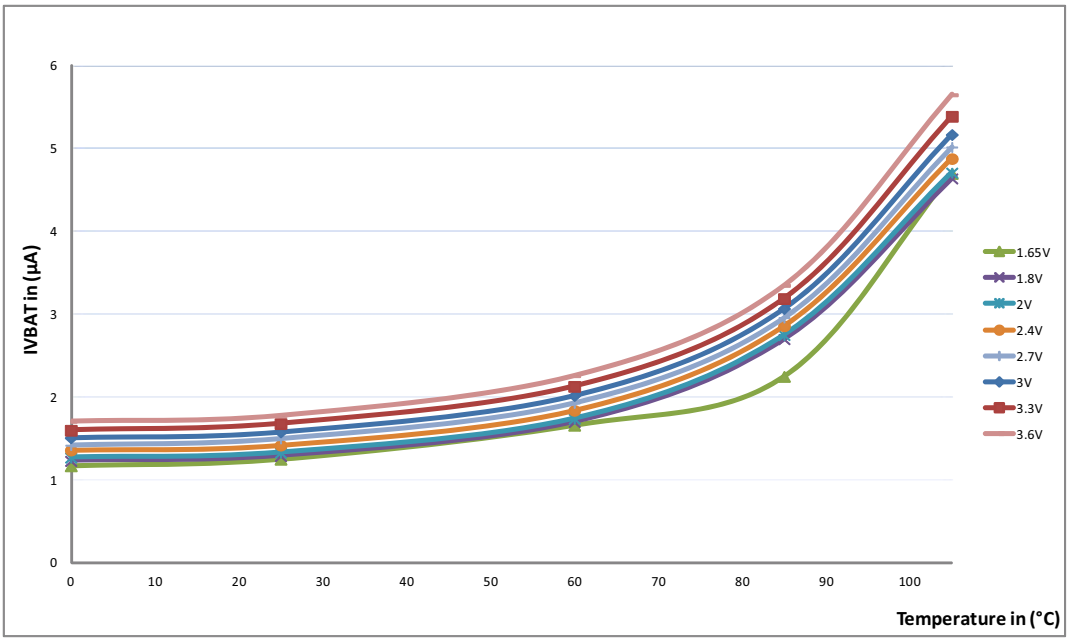


Figure 29. Typical V_{BAT} current consumption (LSE and RTC ON/backup RAM ON)



Additional current consumption

The MCU is placed under the following conditions:

- All I/O pins are configured in analog mode.
- The Flash memory access time is adjusted to f_{HCLK} frequency.
- The voltage scaling is adjusted to f_{HCLK} frequency as follows:
  - Scale 2 for $f_{HCLK} \leq 144$ MHz
  - Scale 1 for 144 MHz < $f_{HCLK} \leq 168$ MHz.
- The system clock is HCLK, $f_{PCLK1} = f_{HCLK}/4$, and $f_{PCLK2} = f_{HCLK}/2$.
- The HSE crystal clock frequency is 25 MHz.
- T_A= 25 °C.

Table 26. Typical current consumption in Run mode, code with data processing running from Flash memory, regulator ON (ART accelerator enabled except prefetch), V_{DD} = 1.8 V(1)

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ. at T_A = 25 °C	Unit
IDD	Supply current in Run mode	All peripheral disabled	160	36.2	mA
			144	29.3	
			120	24.7	
			90	19.3	
			60	13.4	
			30	7.7	
			25	6.0	

1. When peripherals are enabled, the power consumption corresponding to the analog part of the peripherals (such as ADC or DAC) is not included.

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 48: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to

floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption measured previously (see *Table 28: Peripheral current consumption*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DD} is the MCU supply voltage

f_{SW} is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT}$

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

Table 27. Switching output I/O current consumption

Symbol	Parameter	Conditions(1)	I/O toggling frequency (f_{SW})	Typ	Unit
I_{DDIO}	I/O switching current	V_{DD} = 3.3 V(2) C = C_{INT}	2 MHz	0.02	mA
			8 MHz	0.14	
			25 MHz	0.51	
			50 MHz	0.86	
			60 MHz	1.30	
		V_{DD} = 3.3 V C_{EXT} = 0 pF C = C_{INT} + C_{EXT}+ C_S	2 MHz	0.10	
			8 MHz	0.38	
			25 MHz	1.18	
			50 MHz	2.47	
			60 MHz	2.86	
		V_{DD} = 3.3 V C_{EXT} = 10 pF C = C_{INT} + C_{EXT}+ C_S	2 MHz	0.17	
			8 MHz	0.66	
			25 MHz	1.70	
			50 MHz	2.65	
			60 MHz	3.48	
		V_{DD} = 3.3 V C_{EXT} = 22 pF C = C_{INT} + C_{EXT}+ C_S	2 MHz	0.23	
			8 MHz	0.95	
			25 MHz	3.20	
			50 MHz	4.69	
			60 MHz	8.06	
		V_{DD} = 3.3 V C_{EXT} = 33 pF C = C_{INT} + C_{EXT}+ C_S	2 MHz	0.30	
			8 MHz	1.22	
			25 MHz	3.90	
			50 MHz	8.82	
			60 MHz	-(3)	

1. C_S is the PCB board capacitance including the pad pin. C_S = 7 pF (estimated value).
2. This test is performed by cutting the LQFP package pin (pad removal).
3. At 60 MHz, C maximum load is specified 30 pF.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 28*. The MCU is placed under the following conditions:

- At startup, all I/O pins are configured as analog pins by firmware.
- All peripherals are disabled unless otherwise mentioned
- The code is running from Flash memory and the Flash memory access time is equal to 5 wait states at 168 MHz.
- The code is running from Flash memory and the Flash memory access time is equal to 4 wait states at 144 MHz, and the power scale mode is set to 2.
- The ART accelerator is ON.
- The given value is calculated by measuring the difference of current consumption
  - with all peripherals clocked off
  - with one peripheral clocked on (with only the clock applied)
- When the peripherals are enabled: HCLK is the system clock, $f_{PCLK1} = f_{HCLK}/4$, and $f_{PCLK2} = f_{HCLK}/2$.
- The typical values are obtained for V_{DD} = 3.3 V and T_A= 25 °C, unless otherwise specified.

Table 28. Peripheral current consumption

Peripheral		I_{DD}(Typ)(1)		Unit
		Scale1 (up t 168 MHz)	Scale2 (up to 144 MHz)	
AHB1 (up to 168 MHz)	GPIOA	2.70	2.40	µA/MHz
	GPIOB	2.50	2.22	
	GPIOC	2.54	2.28	
	GPIOD	2.55	2.28	
	GPIOE	2.68	2.40	
	GPIOF	2.53	2.28	
	GPIOG	2.51	2.22	
	GPIOH	2.51	2.22	
	GPIOI	2.50	2.22	
	OTG_HS+ULPI	28.33	25.38	
	CRC	0.41	0.40	
	BKPSRAM	0.63	0.58	
	DMA1	37.44	33.58	
	DMA2	37.69	33.93	
	ETH_MAC ETH_MAC_TX ETH_MAC_RX ETH_MAC_PTP	20.43	18.39	

Table 28. Peripheral current consumption (continued)

Peripheral		I_{DD}(Typ)(1)		Unit
		Scale1 (up t 168 MHz)	Scale2 (up to 144 MHz)	
AHB2 (up to 168 MHz)	OTG_FS	26.45	26.67	µA/MHz
	DCMI	5.87	5.35	
	RNG	1.50	1.67	
	Hash	9.73	8.86	
	Crypto	2.23	2.08	
AHB3 (up to 168 MHz)	FSMC	12.46	11.31	µA/MHz
Bus matrix(2)		13.10	11.81	µA/MHz

Table 28. Peripheral current consumption (continued)

Peripheral		I_{DD}(Typ)(1)		Unit
		Scale1 (up t 168 MHz)	Scale2 (up to 144 MHz)	
APB1 (up to 42 MHz)	TIM2	16.71	16.50	µA/MHz
	TIM3	12.33	11.94	
	TIM4	13.45	12.92	
	TIM5	17.14	16.58	
	TIM6	2.43	3.06	
	TIM7	2.43	2.22	
	TIM12	6.62	6.83	
	TIM13	5.05	5.47	
	TIM14	5.26	5.61	
	PWR	1.00	0.56	
	USART2	2.69	2.78	
	USART3	2.74	2.78	
	UART4	3.24	3.33	
	UART5	2.69	2.78	
	I2C1	2.67	2.50	
	I2C2	2.83	2.78	
	I2C3	2.81	2.78	
	SPI2	2.43	2.22	
	SPI3	2.43	2.22	
	I2S2(3)	2.43	2.22	
	I2S3(3)	2.26	2.22	
	CAN1	5.12	5.56	
	CAN2	4.81	5.28	
	DAC(4)	1.67	1.67	
	WWDG	1.00	0.83	

Table 28. Peripheral current consumption (continued)

Peripheral		I_{DD}(Typ)(1)		Unit
		Scale1 (up t 168 MHz)	Scale2 (up to 144 MHz)	
APB2 (up to 84 MHz)	SDIO	7.08	7.92	µA/MHz
	TIM1	16.79	15.51	
	TIM8	17.88	16.53	
	TIM9	7.64	7.28	
	TIM10	4.89	4.82	
	TIM11	5.19	4.82	
	ADC1(5)	4.67	4.58	
	ADC2(5)	4.67	4.58	
	ADC3(5)	4.43	4.44	
	SPI1	1.32	1.39	
	USART1	3.51	3.72	
	USART6	3.55	3.75	
	SYSCFG	0.74	0.56	

1. When the I/O compensation cell is ON, I_{DD} typical value increases by 0.22 mA.
2. The BusMatrix is automatically active when at least one master is ON.
3. To enable an I2S peripheral, first set the I2SMOD bit and then the I2SE bit in the SPI_I2SCFGR register.
4. When the DAC is ON and EN1/2 bits are set in DAC_CR register, add an additional power consumption of 0.8 mA per DAC channel for the analog part.
5. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.6 mA per ADC for the analog part.

5.3.7 Wakeup time from low-power mode

The wakeup times given in *Table 29* is measured on a wakeup phase with a 16 MHz HSI RC oscillator. The clock source used to wake up the device depends from the current operating mode:

- Stop or Standby mode: the clock source is the RC oscillator
- Sleep mode: the clock source is the clock that was set before entering Sleep mode.

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 14*.

Table 29. Low-power mode wakeup timings

Symbol	Parameter	Min(1)	Typ(1)	Max(1)	Unit
$t_{WUSLEEP}$(2)	Wakeup from Sleep mode	-	5	-	CPU clock cycle
t_{WUSTOP}(2)	Wakeup from Stop mode (regulator in Run mode and Flash memory in Stop mode)	-	13	-	µs
	Wakeup from Stop mode (regulator in low-power mode and Flash memory in Stop mode)	-	17	40	
	Wakeup from Stop mode (regulator in Run mode and Flash memory in Deep power-down mode)	-	105	-	
	Wakeup from Stop mode (regulator in low-power mode and Flash memory in Deep power-down mode)	-	110	-	
$t_{WUSTDBY}$(2)(3)	Wakeup from Standby mode	260	375	480	µs

1. Guaranteed by characterization results, not tested in production.
2. The wakeup times are measured from the wakeup event to the point in which the application code reads the first instruction.
3. $t_{WUSTDBY}$ minimum and maximum values are given at 105 °C and –45 °C, respectively.

5.3.8 External clock source characteristics

High-speed external user clock generated from an external source

The characteristics given in *Table 30* result from tests performed using an high-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 14*.

Table 30. High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	External user clock source frequency(1)		1	-	50	MHz
V_{HSEH}	OSC_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HSE)}$ $t_{w(HSE)}$	OSC_IN high or low time(1)		5	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time(1)		-	-	10	
$C_{in(HSE)}$	OSC_IN input capacitance(1)		-	5	-	pF
$DuCy_{(HSE)}$	Duty cycle		45	-	55	%
I_L	OSC_IN Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	±1	µA

1. Guaranteed by design, not tested in production.

Low-speed external user clock generated from an external source

The characteristics given in *Table 31* result from tests performed using an low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 14*.

Table 31. Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User External clock source frequency(1)		-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSE)}$ $t_{f(LSE)}$	OSC32_IN high or low time(1)		450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time(1)		-	-	50	
$C_{in(LSE)}$	OSC32_IN input capacitance(1)		-	5	-	pF
$DuCy_{(LSE)}$	Duty cycle		30	-	70	%
I_L	OSC32_IN Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	±1	µA

1. Guaranteed by design, not tested in production.

Figure 30. High-speed external clock source AC timing diagram

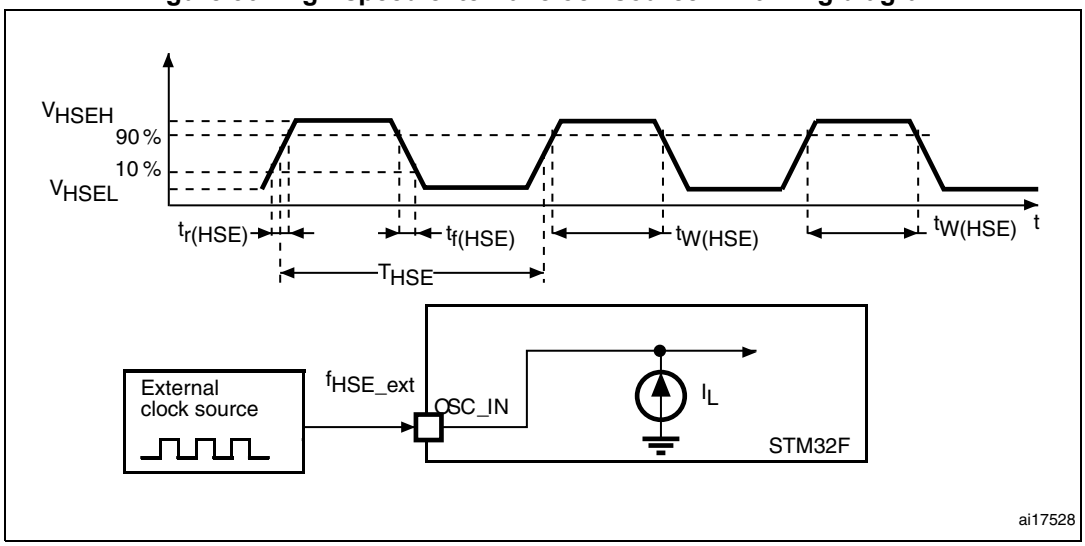
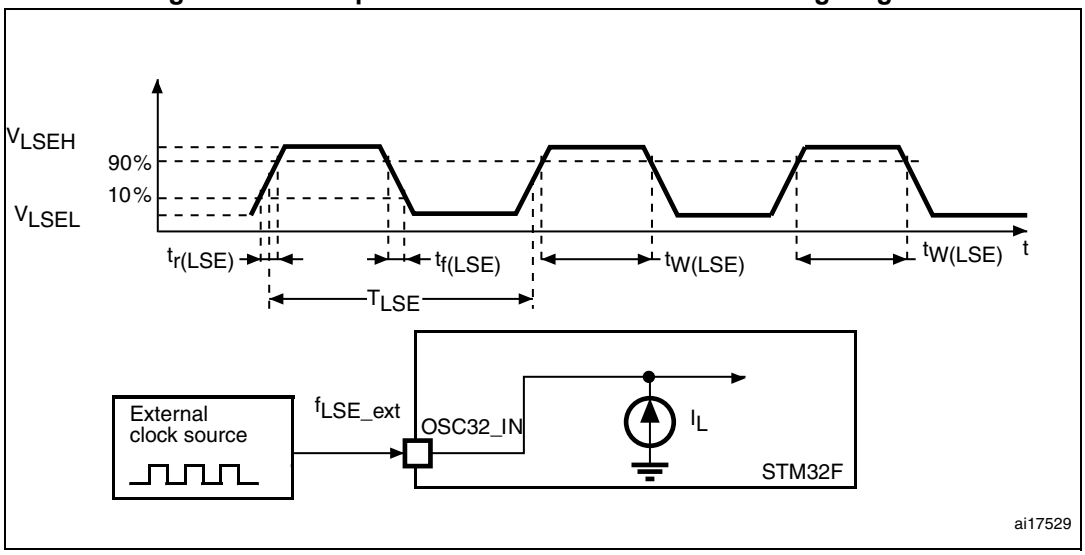


Figure 31. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 26 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 32*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 32. HSE 4-26 MHz oscillator characteristics (1)

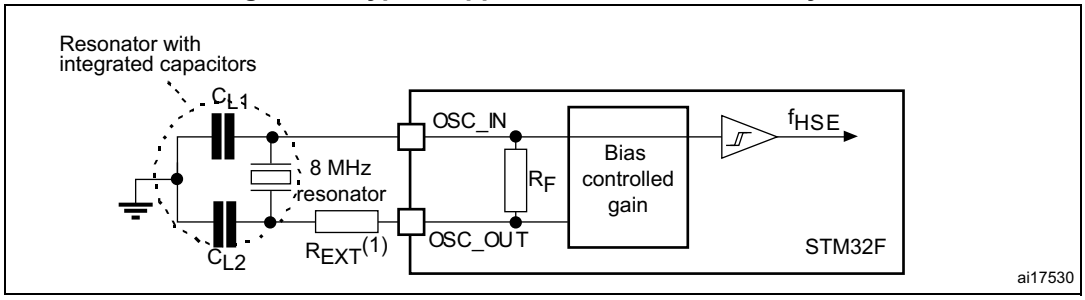
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency		4	-	26	MHz
R_F	Feedback resistor		-	200	-	kΩ
G_m	Oscillator transconductance	Startup	5	-	-	mA/V
$G_{mcritmax}$	Maximum critical crystal G_m		-	-	1	
$t_{SU(HSE)}$ (2)	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Guaranteed by design, not tested in production.
2. Guaranteed by characterization, not tested in production. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 32*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Note: For information on electing the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 32. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 33*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

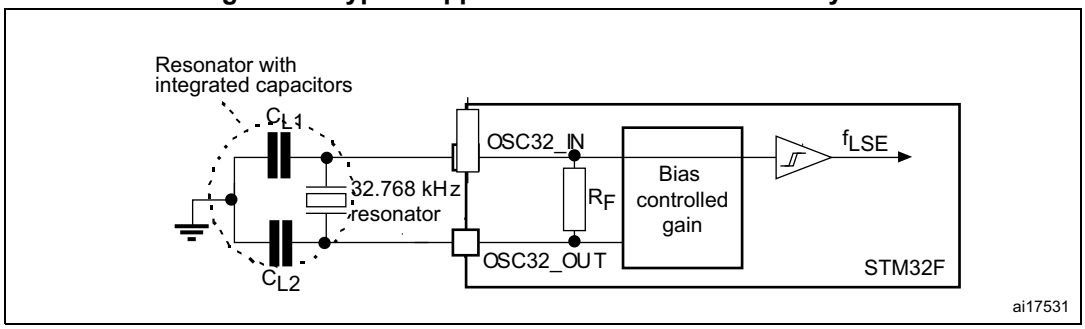
Table 33. LSE oscillator characteristics (f_{LSE} = 32.768 kHz) (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency		-	32.768	-	MHz
R_F	Feedback resistor		-	18.4	-	MΩ
I_{DD}	LSE current consumption		-	-	1	µA
G_m	Oscillator transconductance	Startup	2.8	-	-	µA/V
$G_{mcritmax}$	Maximum critical crystal G_m		-	-	0.56	
$t_{SU(LSE)}$ (2)	startup time	V_{DD} is stabilized	-	2	-	s

1. Guaranteed by design, not tested in production.
2. Guaranteed by characterization, not tested in production. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

Note: For information on electing the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 33. Typical application with a 32.768 kHz crystal



5.3.9 Internal clock source characteristics

The parameters given in *Table 34* and *Table 35* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 14*.

High-speed internal (HSI) RC oscillator

Table 34. HSI oscillator characteristics (1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{HSI}	Frequency			-	16	-	MHz
ACC_{HSI}	Accuracy of the HSI oscillator	User-trimmed with the RCC_CR register		-	-	1	%
		Factory-calibrated	T_A = –40 to 105 °C(2)	–8	-	4.5	%
			T_A = –10 to 85 °C(2)	–4	-	4	%
			T_A = 25 °C	–1	-	1	%
$t_{su(HSI)}$(3)	HSI oscillator startup time			-	2.2	4	µs
$I_{DD(HSI)}$	HSI oscillator power consumption			-	60	80	µA

1. V_{DD} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by characterization results not tested in production.
3. Guaranteed by design, not tested in production.

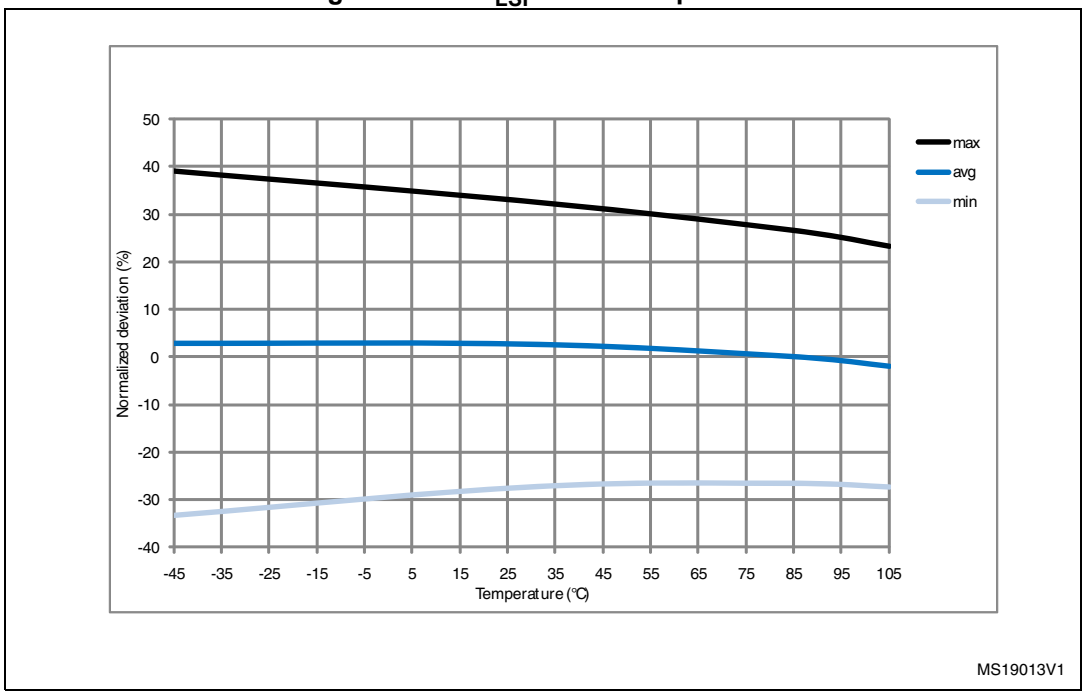
Low-speed internal (LSI) RC oscillator

Table 35. LSI oscillator characteristics (1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}(2)	Frequency	17	32	47	kHz
$t_{su(LSI)}$(3)	LSI oscillator startup time	-	15	40	µs
$I_{DD(LSI)}$(3)	LSI oscillator power consumption	-	0.4	0.6	µA

1. V_{DD} = 3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by characterization results, not tested in production.
3. Guaranteed by design, not tested in production.

Figure 34. ACC_{LSI} versus temperature



5.3.10 PLL characteristics

The parameters given in *Table 36* and *Table 37* are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in *Table 14*.

Table 36. Main PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock(1)		0.95(2)	1	2.10	MHz
f_{PLL_OUT}	PLL multiplier output clock		24	-	168	MHz
f_{PLL48_OUT}	48 MHz PLL multiplier output clock		-	48	75	MHz
f_{VCO_OUT}	PLL VCO output		192	-	432	MHz
t_{LOCK}	PLL lock time	VCO freq = 192 MHz	75	-	200	µs
		VCO freq = 432 MHz	100	-	300	

Table 36. Main PLL characteristics (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Jitter(3)	Cycle-to-cycle jitter	System clock 120 MHz	RMS	-	25	-	ps
			peak to peak	-	±150	-	
	Period Jitter		RMS	-	15	-	
			peak to peak	-	±200	-	
	Main clock output (MCO) for RMII Ethernet	Cycle to cycle at 50 MHz on 1000 samples		-	32	-	
	Main clock output (MCO) for MII Ethernet	Cycle to cycle at 25 MHz on 1000 samples		-	40	-	
	Bit Time CAN jitter	Cycle to cycle at 1 MHz on 1000 samples		-	330	-	
$I_{DD(PLL)}$(4)	PLL power consumption on VDD	VCO freq = 192 MHz VCO freq = 432 MHz		0.15 0.45	-	0.40 0.75	mA
$I_{DDA(PLL)}$(4)	PLL power consumption on VDDA	VCO freq = 192 MHz VCO freq = 432 MHz		0.30 0.55	-	0.40 0.85	mA

1. Take care of using the appropriate division factor M to obtain the specified PLL input clock values. The M factor is shared between PLL and PLLI2S.
2. Guaranteed by design, not tested in production.
3. The use of 2 PLLs in parallel could degraded the Jitter up to +30%.
4. Guaranteed by characterization results, not tested in production.

Table 37. PLLI2S (audio PLL) characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{PLLI2S_IN}	PLLI2S input clock(1)			0.95(2)	1	2.10	MHz
f_{PLLI2S_OUT}	PLLI2S multiplier output clock			-	-	216	MHz
f_{VCO_OUT}	PLLI2S VCO output			192	-	432	MHz
t_{LOCK}	PLLI2S lock time	VCO freq = 192 MHz		75	-	200	µs
		VCO freq = 432 MHz		100	-	300	
Jitter(3)	Master I^2S clock jitter	Cycle to cycle at 12.288 MHz on 48KHz period, N=432, R=5	RMS	-	90	-	
			peak to peak	-	±280	-	ps
		Average frequency of 12.288 MHz N = 432, R = 5 on 1000 samples		-	90	-	ps
	WS I^2S clock jitter	Cycle to cycle at 48 KHz on 1000 samples		-	400	-	ps

Table 37. PLLI2S (audio PLL) characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DD(PLLI2S)}$(4)	PLLI2S power consumption on V_{DD}	VCO freq = 192 MHz VCO freq = 432 MHz	0.15 0.45	-	0.40 0.75	mA
$I_{DDA(PLLI2S)}$(4)	PLLI2S power consumption on V_{DDA}	VCO freq = 192 MHz VCO freq = 432 MHz	0.30 0.55	-	0.40 0.85	mA

1. Take care of using the appropriate division factor M to have the specified PLL input clock values.
2. Guaranteed by design, not tested in production.
3. Value given with main PLL running.
4. Guaranteed by characterization results, not tested in production.

5.3.11 PLL spread spectrum clock generation (SSCG) characteristics

The spread spectrum clock generation (SSCG) feature allows to reduce electromagnetic interferences (see *Table 44: EMI characteristics*). It is available only on the main PLL.

Table 38. SSCG parameters constraint

Symbol	Parameter	Min	Typ	Max(1)	Unit
f_{Mod}	Modulation frequency	-	-	10	KHz
md	Peak modulation depth	0.25	-	2	%
MODEPER * INCSTEP		-	-	$2^{15}-1$	-

1. Guaranteed by design, not tested in production.

Equation 1

The frequency modulation period (MODEPER) is given by the equation below:

$$MODEPER = round[f_{PLL\_IN}/(4 \times f_{Mod})]$$

f_{PLL_IN} and f_{Mod} must be expressed in Hz.

As an example:

If f_{PLL_IN} = 1 MHz, and f_{MOD} = 1 kHz, the modulation depth (MODEPER) is given by equation 1:

$$MODEPER = round[10^6/(4 \times 10^3)] = 250$$

Equation 2

Equation 2 allows to calculate the increment step (INCSTEP):

$$INCSTEP = round[((2^{15} - 1) \times md \times PLLN)/(100 \times 5 \times MODEPER)]$$

f_{VCO_OUT} must be expressed in MHz.

With a modulation depth (md) = ±2 % (4 % peak to peak), and PLLN = 240 (in MHz):

$$INCSTEP = round[((2^{15} - 1) \times 2 \times 240)/(100 \times 5 \times 250)] = 126md(quantitazed)\%$$

An amplitude quantization error may be generated because the linear modulation profile is obtained by taking the quantized values (rounded to the nearest integer) of MODPER and INCSTEP. As a result, the achieved modulation depth is quantized. The percentage quantized modulation depth is given by the following formula:

$$md_{quantized}\% = (MODEPER \times INCSTEP \times 100 \times 5)/((2^{15} - 1) \times PLLN)$$

As a result:

$$md_{quantized}\% = (250 \times 126 \times 100 \times 5)/((2^{15} - 1) \times 240) = 2{,}002\%(peak)$$

Figure 35 and *Figure 36* show the main PLL output clock waveforms in center spread and down spread modes, where:

F0 is f_{PLL_OUT} nominal.

T_{mode} is the modulation period.

md is the modulation depth.

Figure 35. PLL output clock waveforms in center spread mode

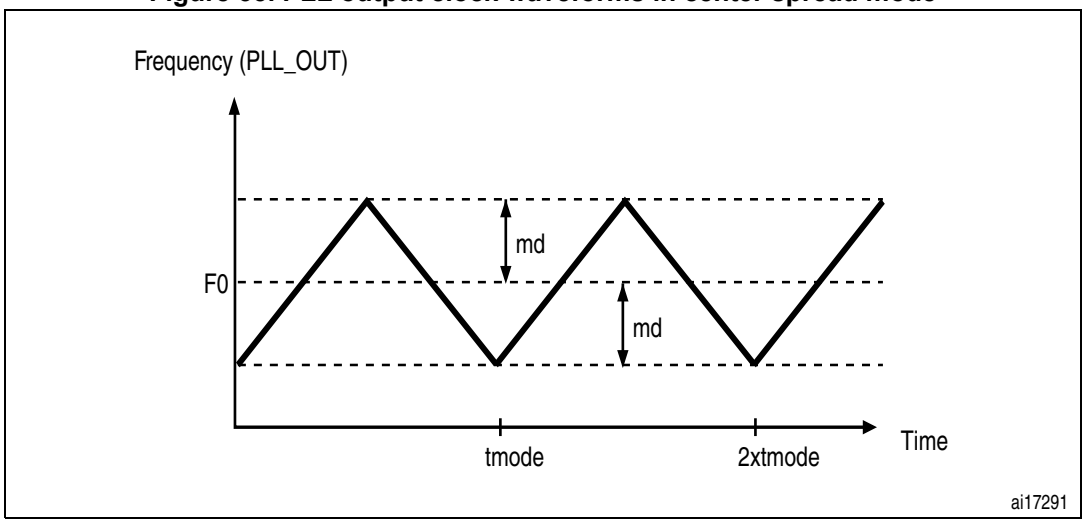
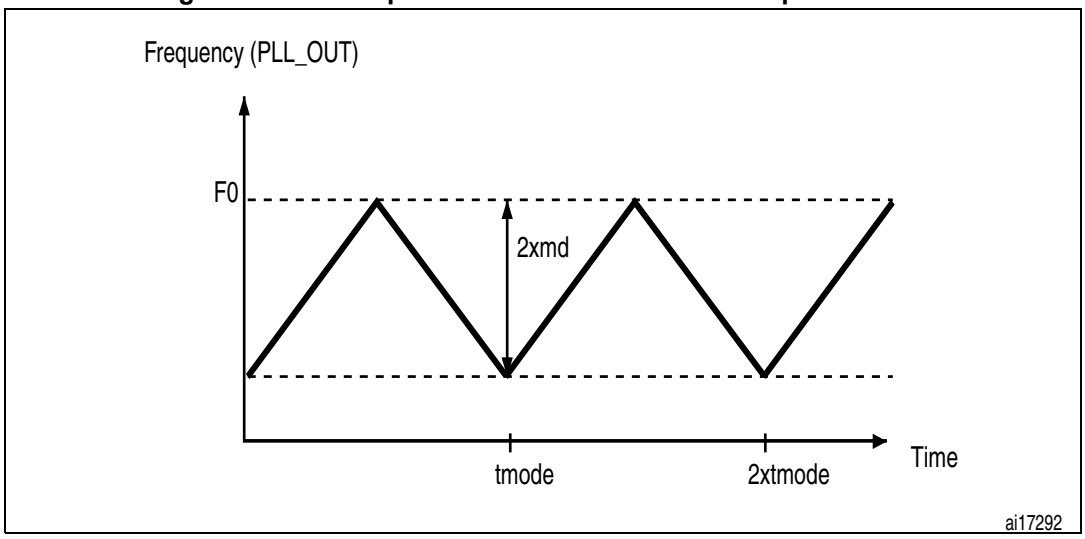


Figure 36. PLL output clock waveforms in down spread mode



5.3.12 Memory characteristics

Flash memory

The characteristics are given at T_A = –40 to 105 °C unless otherwise specified.

The devices are shipped to customers with the Flash memory erased.

Table 39. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	Supply current	Write / Erase 8-bit mode, V_{DD} = 1.8 V	-	5	-	mA
		Write / Erase 16-bit mode, V_{DD} = 2.1 V	-	8	-	
		Write / Erase 32-bit mode, V_{DD} = 3.3 V	-	12	-	

Table 40. Flash memory programming

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
t_{prog}	Word programming time	Program/erase parallelism (PSIZE) = x 8/16/32	-	16	100(2)	µs
$t_{ERASE16KB}$	Sector (16 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	400	800	ms
		Program/erase parallelism (PSIZE) = x 16	-	300	600	
		Program/erase parallelism (PSIZE) = x 32	-	250	500	

Table 40. Flash memory programming (continued)

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
$t_{ERASE64KB}$	Sector (64 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	1200	2400	ms
		Program/erase parallelism (PSIZE) = x 16	-	700	1400	
		Program/erase parallelism (PSIZE) = x 32	-	550	1100	
$t_{ERASE128KB}$	Sector (128 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	2	4	s
		Program/erase parallelism (PSIZE) = x 16	-	1.3	2.6	
		Program/erase parallelism (PSIZE) = x 32	-	1	2	
t_{ME}	Mass erase time	Program/erase parallelism (PSIZE) = x 8	-	16	32	s
		Program/erase parallelism (PSIZE) = x 16	-	11	22	
		Program/erase parallelism (PSIZE) = x 32	-	8	16	
V_{prog}	Programming voltage	32-bit program operation	2.7	-	3.6	V
		16-bit program operation	2.1	-	3.6	V
		8-bit program operation	1.8	-	3.6	V

1. Guaranteed by characterization results, not tested in production.
2. The maximum programming time is measured after 100K erase operations.

Table 41. Flash memory programming with V_{PP}

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
t_{prog}	Double word programming	T_A = 0 to +40 °C V_{DD} = 3.3 V V_{PP} = 8.5 V	-	16	100(2)	µs
$t_{ERASE16KB}$	Sector (16 KB) erase time		-	230	-	ms
$t_{ERASE64KB}$	Sector (64 KB) erase time		-	490	-	
$t_{ERASE128KB}$	Sector (128 KB) erase time		-	875	-	
t_{ME}	Mass erase time		-	6.9	-	s
V_{prog}	Programming voltage		2.7	-	3.6	V
V_{PP}	V_{PP} voltage range		7	-	9	V
I_{PP}	Minimum current sunk on the V_{PP} pin		10	-	-	mA
t_{VPP}(3)	Cumulative time during which V_{PP} is applied		-	-	1	hour

1. Guaranteed by design, not tested in production.
2. The maximum programming time is measured after 100K erase operations.
3. V_{PP} should only be connected during programming/erasing.

Table 42. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value	Unit
			Min(1)	
N_{END}	Endurance	T_A = –40 to +85 °C (6 suffix versions) T_A = –40 to +105 °C (7 suffix versions)	10	kcycles
t_{RET}	Data retention	1 kcycle(2) at T_A = 85 °C	30	Years
		1 kcycle(2) at T_A = 105 °C	10	
		10 kcycles(2) at T_A = 55 °C	20	

1. Guaranteed by characterization results, not tested in production.
2. Cycling performed over the whole temperature range.

5.3.13 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 43*. They are based on the EMS levels and classes defined in application note AN1709.

Table 43. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, LQFP176, T_A = +25 °C, f_{HCLK} = 168 MHz, conforms to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP176, T_A = +25 °C, f_{HCLK} = 168 MHz, conforms to IEC 61000-4-2	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application, executing EEMBC? code, is running. This emission test is compliant with SAE IEC61967-2 standard which specifies the test board and the pin loading.

Table 44. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{CPU}]	Unit
				25/168 MHz	
S_{EMI}	Peak level	V_{DD} = 3.3 V, T_A = 25 °C, LQFP176 package, conforming to SAE J1752/3 EEMBC, code running from Flash with ART accelerator enabled	0.1 to 30 MHz	32	dBµV
			30 to 130 MHz	25	
			130 MHz to 1GHz	29	
			SAE EMI Level	4	-
		V_{DD} = 3.3 V, T_A = 25 °C, LQFP176 package, conforming to SAE J1752/3 EEMBC, code running from Flash with ART accelerator and PLL spread spectrum enabled	0.1 to 30 MHz	19	dBµV
			30 to 130 MHz	16	
			130 MHz to 1GHz	18	
			SAE EMI level	3.5	-

5.3.14 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 45. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C conforming to JESD22-A114	2	2000(2)	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C conforming to ANSI/ESD STM5.3.1	II	500	

1. Guaranteed by characterization results, not tested in production.
2. On V_{BAT} pin, $V_{ESD(HBM)}$ is limited to 1000 V.

Static latchup

Two complementary static tests are required on six parts to assess the latchup performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latchup standard.

Table 46. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II level A

5.3.15 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibilty to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (>5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of 5 µA/+0 µA range), or other functional failure (for example reset, oscillator frequency deviation).

Negative induced leakage current is caused by negative injection and positive induced leakage current by positive injection.

The test results are given in *Table 47*.

Table 47. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}(1)	Injected current on BOOT0 pin	− 0	NA	mA
	Injected current on NRST pin	− 0	NA	
	Injected current on PE2, PE3, PE4, PE5, PE6, PI8, PC13, PC14, PC15, PI9, PI10, PI11, PF0, PF1, PF2, PF3, PF4, PF5, PF10, PH0/OSC_IN, PH1/OSC_OUT, PC0, PC1, PC2, PC3, PB6, PB7, PB8, PB9, PE0, PE1, PI4, PI5, PI6, PI7, PDR_ON, BYPASS_REG	− 0	NA	
	Injected current on all FT pins	− 5	NA	
	Injected current on any other pin	− 5	+5	

1. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

5.3.16 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 48* are derived from tests performed under the conditions summarized in *Table 14*. All I/Os are CMOS and TTL compliant.

Table 48. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	FT, TTa and NRST I/O input low level voltage	1.7 V ≤ V_{DD} ≤ 3.6 V	-	-	$0.3V_{DD}$-0.04(1)	V
			-	-	$0.3V_{DD}$(2)	
	BOOT0 I/O input low level voltage	1.75 V ≤ V_{DD} ≤ 3.6 V -40 °C≤ T_A ≤ 105 °C	-	-	$0.1V_{DD}$-+0.1(1)	
		1.7 V ≤ V_{DD} ≤ 3.6 V 0 °C≤ T_A ≤ 105 °C	-	-		
V_{IH}	FT, TTa and NRST I/O input low level voltage	1.7 V ≤ V_{DD} ≤ 3.6 V	$0.45V_{DD}$+0.3(1)	-	-	
			$0.7V_{DD}$(2)	-	-	
	BOOT0 I/O input low level voltage	1.75 V ≤ V_{DD} ≤ 3.6 V -40 °C≤ T_A ≤ 105 °C	$0.17V_{DD}$+0.7(1)	-	-	
		1.7 V ≤ V_{DD} ≤ 3.6 V 0 °C≤ T_A ≤ 105 °C		-	-	

Table 48. I/O static characteristics (continued)

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V_{HYS}	FT, TTa and NRST I/O input hysteresis		1.7 V ≤ V_{DD} ≤ 3.6 V	10%V_{DD}(3)	-	-	V
	BOOT0 I/O input hysteresis		1.75 V ≤ V_{DD} ≤ 3.6 V -40 °C≤ T_A ≤ 105 °C	0.1	-	-	
			1.7 V ≤ V_{DD} ≤ 3.6 V 0 °C≤ T_A ≤ 105 °C				
I_{lkg}	I/O input leakage current (4)		V_{SS} ≤ V_{IN} ≤ V_{DD}	-	-	±1	µA
	I/O FT input leakage current (5)		V_{IN} = 5 V	-	-	3	
R_{PU}	Weak pull-up equivalent resistor(6)	All pins except for PA10 and PB12 (OTG_FS_ID, OTG_HS_ID)	V_{IN} = V_{SS}	30	40	50	kΩ
		PA10 and PB12 (OTG_FS_ID, OTG_HS_ID)	-	7	10	14	
R_{PD}	Weak pull-down equivalent resistor(7)	All pins except for PA10 and PB12	V_{IN} = V_{DD}	30	40	50	
		PA10 and PB12	-	7	10	14	
C_{IO}(8)	I/O pin capacitance			-	5	-	pF

1. Guaranteed by design, not tested in production.
2. Tested in production.
3. With a minimum of 200 mV.
4. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins.Refer to *Table 47: I/O current injection susceptibility*
5. To sustain a voltage higher than V_{DD} + 0.3 V, the internal pull-up/pull-down resistors must be disabled. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins. Refer to *Table 47: I/O current injection susceptibility*.
6. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimum (~10% order).
7. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable NMOS. This NMOS contribution to the series resistance is minimum (~10% order).
8. Hysteresis voltage between Schmitt trigger switching levels. Guaranteed by characterization results, not tested in production.

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters.

Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ±20 mA (with a relaxed V_{OL}/V_{OH}) except PC13, PC14 and PC15 which can sink or source up to ±3mA. When using the PC13 to PC15 GPIOs in output mode, the speed should not exceed 2 MHz with a maximum load of 30 pF.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 5.2*. In particular:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating I_{VDD} (see *Table 12*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating I_{VSS} (see *Table 12*).

Output voltage levels

Unless otherwise specified, the parameters given in *Table 49* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 14*. All I/Os are CMOS and TTL compliant.

Table 49. Output voltage characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(2)	Output low level voltage	CMOS port I_{IO} = +8 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH}(3)	Output high level voltage		V_{DD}–0.4	-	
V_{OL} (2)	Output low level voltage	TTL port I_{IO} =+ 8mA 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH} (3)	Output high level voltage		2.4	-	
V_{OL}(2)(4)	Output low level voltage	I_{IO} = +20 mA 2.7 V < V_{DD} < 3.6 V	-	1.3	V
V_{OH}(3)(4)	Output high level voltage		V_{DD}–1.3	-	
V_{OL}(2)(4)	Output low level voltage	I_{IO} = +6 mA 2 V < V_{DD} < 2.7 V	-	0.4	V
V_{OH}(3)(4)	Output high level voltage		V_{DD}–0.4	-	

1. PC13, PC14, PC15 and PI8 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 and PI8 in output mode is limited: the speed should not exceed 2 MHz with a maximum load of 30 pF and these I/Os must not be used as a current source (e.g. to drive an LED).
2. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 12* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 12* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.
4. Guaranteed by characterization results, not tested in production.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 37* and *Table 50*, respectively.

Unless otherwise specified, the parameters given in *Table 50* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 14*.

Table 50. I/O AC characteristics(1)(2)

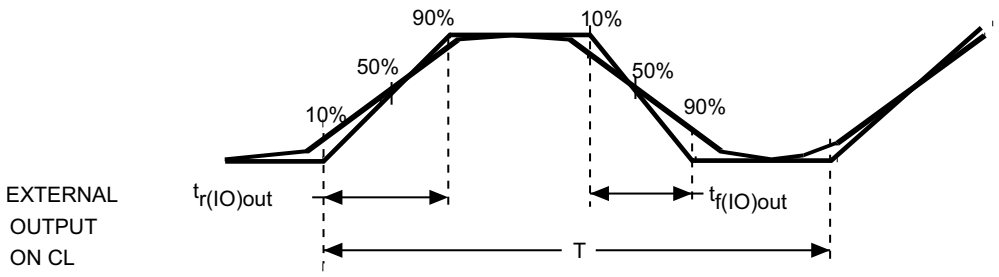
OSPEEDRy [1:0] bit value(1)	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
00	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, V_{DD} > 2.70 V	-	-	4	MHz
			C_L = 50 pF, V_{DD} > 1.8 V	-	-	2	
			C_L = 10 pF, V_{DD} > 2.70 V	-	-	8	
			C_L = 10 pF, V_{DD} > 1.8 V	-	-	4	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 50 pF, V_{DD} = 1.8 V to 3.6 V	-	-	100	ns
01	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, V_{DD} > 2.70 V	-	-	25	MHz
			C_L = 50 pF, V_{DD} > 1.8 V	-	-	12.5	
			C_L = 10 pF, V_{DD} > 2.70 V	-	-	50(4)	
			C_L = 10 pF, V_{DD} > 1.8 V	-	-	20	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 50 pF, V_{DD} >2.7 V	-	-	10	ns
			C_L = 50 pF, V_{DD} > 1.8 V	-	-	20	
			C_L = 10 pF, V_{DD} > 2.70 V	-	-	6	
			C_L = 10 pF, V_{DD} > 1.8 V	-	-	10	
10	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 40 pF, V_{DD} > 2.70 V	-	-	50(4)	MHz
			C_L = 40 pF, V_{DD} > 1.8 V	-	-	25	
			C_L = 10 pF, V_{DD} > 2.70 V	-	-	100(4)	
			C_L = 10 pF, V_{DD} > 1.8 V	-	-	50(4)	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 40 pF, V_{DD} > 2.70 V	-	-	6	ns
			C_L = 40 pF, V_{DD} > 1.8 V	-	-	10	
			C_L = 10 pF, V_{DD} > 2.70 V	-	-	4	
			C_L = 10 pF, V_{DD} > 1.8 V	-	-	6	

Table 50. I/O AC characteristics[1][2] (continued)

OSPEEDRy [1:0] bit value[1]	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
11	$F_{max(IO)out}$	Maximum frequency[3]	C_L = 30 pF, V_{DD} > 2.70 V	-	-	100[4]	MHz
			C_L = 30 pF, V_{DD} > 1.8 V	-	-	50[4]	
			C_L = 10 pF, V_{DD} > 2.70 V	-	-	180[4]	
			C_L = 10 pF, V_{DD} > 1.8 V	-	-	100[4]	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 30 pF, V_{DD} > 2.70 V	-	-	4	ns
			C_L = 30 pF, V_{DD} > 1.8 V	-	-	6	
			C_L = 10 pF, V_{DD} > 2.70 V	-	-	2.5	
			C_L = 10 pF, V_{DD} > 1.8 V	-	-	4	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller		10	-	-	ns

1. Guaranteed by characterization results, not tested in production.
2. The I/O speed is configured using the OSPEEDRy[1:0] bits. Refer to the STM32F4xx reference manual for a description of the GPIOx_SPEEDR GPIO port output speed register.
3. The maximum frequency is defined in *Figure 37*.
4. For maximum frequencies above 50 MHz, the compensation cell should be used.

Figure 37. I/O AC characteristics definition



Maximum frequency is achieved if (t_r + t_f) ≤ (2/3)T and if the duty cycle is (45-55%) when loaded by CL specified in the table " *I/O AC characteristics*".

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5.3.17 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 48*).

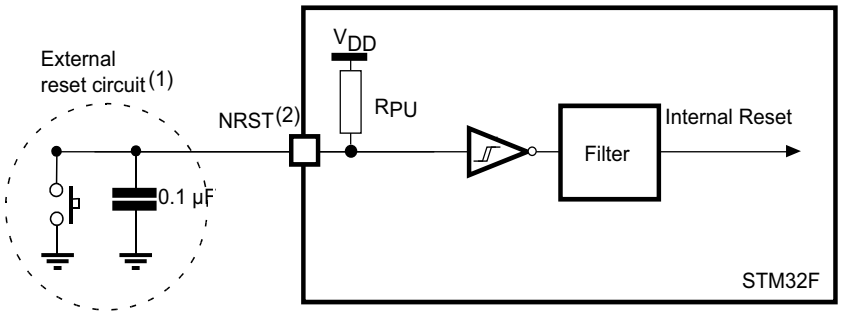
Unless otherwise specified, the parameters given in *Table 51* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 14*.

Table 51. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST Input low level voltage	TTL ports 2.7 V ≤ V_{DD} ≤ 3.6 V	-	-	0.8	V
$V_{IH(NRST)}$(1)	NRST Input high level voltage		2	-	-	
$V_{IL(NRST)}$(1)	NRST Input low level voltage	CMOS ports 1.8 V ≤ V_{DD} ≤ 3.6 V	-		$0.3V_{DD}$	
$V_{IH(NRST)}$(1)	NRST Input high level voltage		$0.7V_{DD}$		-	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis		-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	30	40	50	kΩ
$V_{F(NRST)}$(1)	NRST Input filtered pulse		-	-	100	ns
$V_{NF(NRST)}$(1)	NRST Input not filtered pulse	V_{DD} > 2.7 V	300	-	-	ns
T_{NRST_OUT}	Generated reset pulse duration	Internal Reset source	20	-	-	µs

1. Guaranteed by design, not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

Figure 38. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 51*. Otherwise the reset is not taken into account by the device.

5.3.18 TIM timer characteristics

The parameters given in *Table 52* and *Table 53* are guaranteed by design.

Refer to *Section 5.3.16: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 52. Characteristics of TIMx connected to the APB1 domain(1)

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	AHB/APB1 prescaler distinct from 1, $f_{TIMxCLK}$ = 84 MHz	1	-	$t_{TIMxCLK}$
			11.9	-	ns
		AHB/APB1 prescaler = 1, $f_{TIMxCLK}$ = 42 MHz	1	-	$t_{TIMxCLK}$
			23.8	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	$f_{TIMxCLK}$ = 84 MHz APB1= 42 MHz	0	$f_{TIMxCLK}/2$	MHz
			0	42	MHz
Res_{TIM}	Timer resolution		-	16/32	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected		1	65536	$t_{TIMxCLK}$
			0.0119	780	µs
	32-bit counter clock period when internal clock is selected		1	-	$t_{TIMxCLK}$
			0.0119	51130563	µs
t_{MAX_COUNT}	Maximum possible count		-	65536 × 65536	$t_{TIMxCLK}$
			-	51.1	s

1. TIMx is used as a general term to refer to the TIM2, TIM3, TIM4, TIM5, TIM6, TIM7, and TIM12 timers.

Table 53. Characteristics of TIMx connected to the APB2 domain(1)

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	AHB/APB2 prescaler distinct from 1, $f_{TIMxCLK}$ = 168 MHz	1	-	$t_{TIMxCLK}$
			5.95	-	ns
		AHB/APB2 prescaler = 1, $f_{TIMxCLK}$ = 84 MHz	1	-	$t_{TIMxCLK}$
			11.9	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	$f_{TIMxCLK}$ = 168 MHz APB2 = 84 MHz	0	$f_{TIMxCLK}/2$	MHz
			0	84	MHz
Res_{TIM}	Timer resolution		-	16	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected		1	65536	$t_{TIMxCLK}$
t_{MAX_COUNT}	Maximum possible count		-	32768	$t_{TIMxCLK}$

1. TIMx is used as a general term to refer to the TIM1, TIM8, TIM9, TIM10, and TIM11 timers.

5.3.19 Communications interfaces

I²C interface characteristics

The I²C interface meets the timings requirements of the I²C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s.

The I²C timings requirements are guaranteed by design when the I2C peripheral is properly configured (refer to RM0090 reference manual).

The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present. Refer to *Section 5.3.16: I/O port characteristics* for more details on the I²C I/O characteristics.

All I²C SDA and SCL I/Os embed an analog filter. Refer to the table below for the analog filter characteristics:

Table 54. I2C analog filter characteristics(1)

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes that are suppressed by the analog filter	50(2)	260(3)	ns

1. Guaranteed by design, not tested in production.
2. Spikes with widths below $t_{AF(min)}$ are filtered.
3. Spikes with widths above $t_{AF(max)}$ are not filtered

SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 55* for SPI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 14* with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 V_{DD}

Refer to *Section 5.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 55. SPI dynamic characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SPI clock frequency	Master mode, SPI1, 2.7V < V_{DD} < 3.6V	-	-	42	MHz
		Slave mode, SPI1, 2.7V < V_{DD} < 3.6V			42	
$1/t_{c(SCK)}$		Master mode, SPI1/2/3, 1.7V < V_{DD} < 3.6V	-	-	21	
		Slave mode, SPI1/2/3, 1.7V < V_{DD} < 3.6V			21	
Duty(SCK)	Duty cycle of SPI clock frequency	Slave mode	30	50	70	%

Table 55. SPI dynamic characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{w(SCKH)}$	SCK high and low time	Master mode, SPI presc = 2, 2.7V < V_{DD} < 3.6V	T_{PCLK}-0.5	T_{PCLK}	T_{PCLK}+0.5	ns
$t_{w(SCKL)}$		Master mode, SPI presc = 2, 1.7V < V_{DD} < 3.6V	T_{PCLK}-2	T_{PCLK}	T_{PCLK}+2	
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI presc = 2	4 x T_{PCLK}	-	-	
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI presc = 2	2 x T_{PCLK}			
$t_{su(MI)}$	Data input setup time	Master mode	6.5	-	-	
$t_{su(SI)}$		Slave mode	2.5	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	2.5	-	-	
$t_{h(SI)}$		Slave mode	4	-	-	
$t_{a(SO)}$(2)	Data output access time	Slave mode, SPI presc = 2	0	-	4 x T_{PCLK}	
$t_{dis(SO)}$(3)	Data output disable time	Slave mode, SPI1, 2.7V < V_{DD} < 3.6V	0	-	7.5	
		Slave mode, SPI1/2/3 1.7V < V_{DD} < 3.6V	0	-	16.5	
$t_{v(SO)}$ $t_{h(SO)}$	Data output valid/hold time	Slave mode (after enable edge), SPI1, 2.7V < V_{DD} < 3.6V	-	11	13	
		Slave mode (after enable edge), SPI2/3, 2.7V < V_{DD} < 3.6V	-	12	16.5	
		Slave mode (after enable edge), SPI1, 1.7V < V_{DD} < 3.6V	-	15.5	19	
		Slave mode (after enable edge), SPI2/3, 1.7V < V_{DD} < 3.6V	-	18	20.5	
$t_{v(MO)}$	Data output valid time	Master mode (after enable edge), SPI1, 2.7V < V_{DD} < 3.6V	-	-	2.5	
		Master mode (after enable edge), SPI1/2/3, 1.7V < V_{DD} < 3.6V	-	-	4.5	
$t_{h(MO)}$	Data output hold time	Master mode (after enable edge)	0	-	-	

1. Guaranteed by characterization results, not tested in production.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

Figure 39. SPI timing diagram - slave mode and CPHA = 0

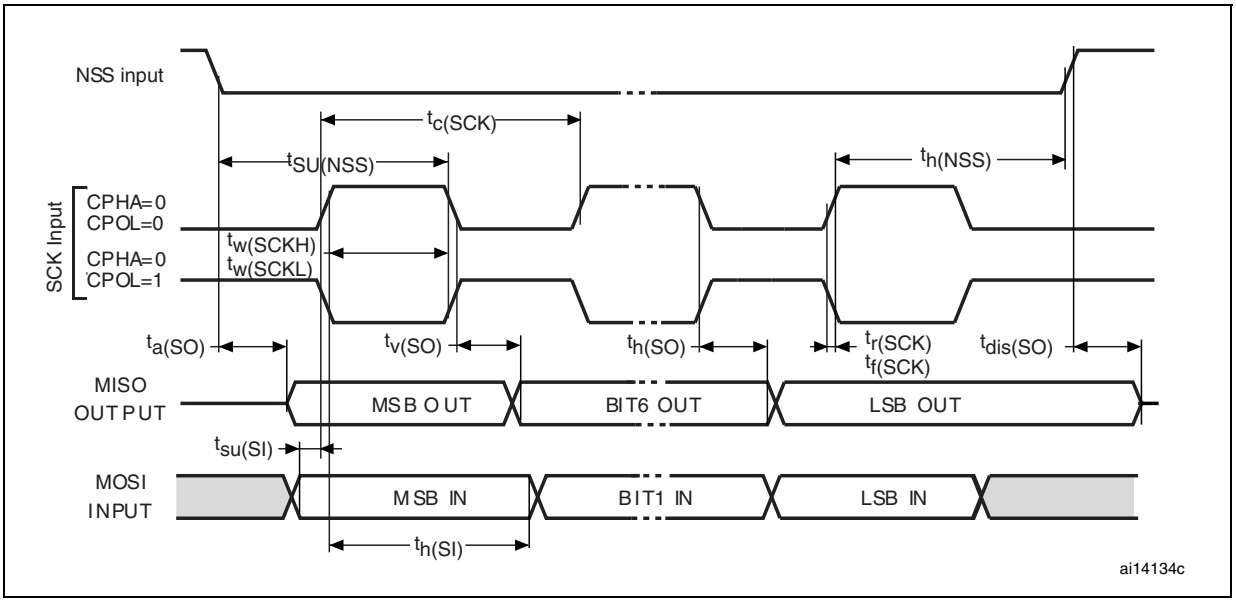


Figure 40. SPI timing diagram - slave mode and CPHA = 1

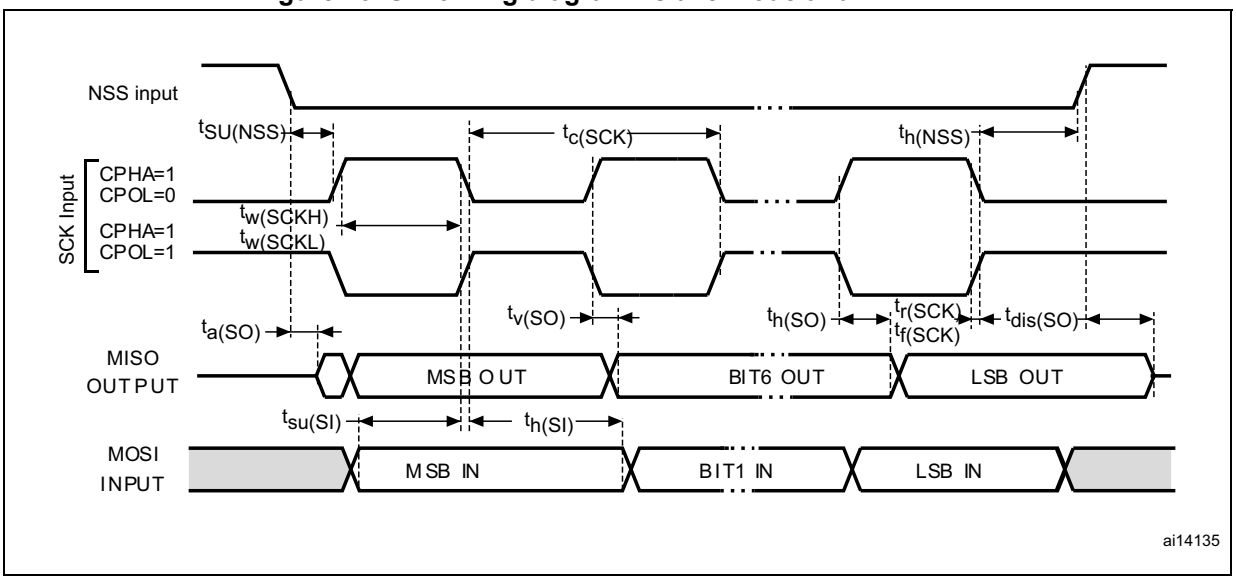
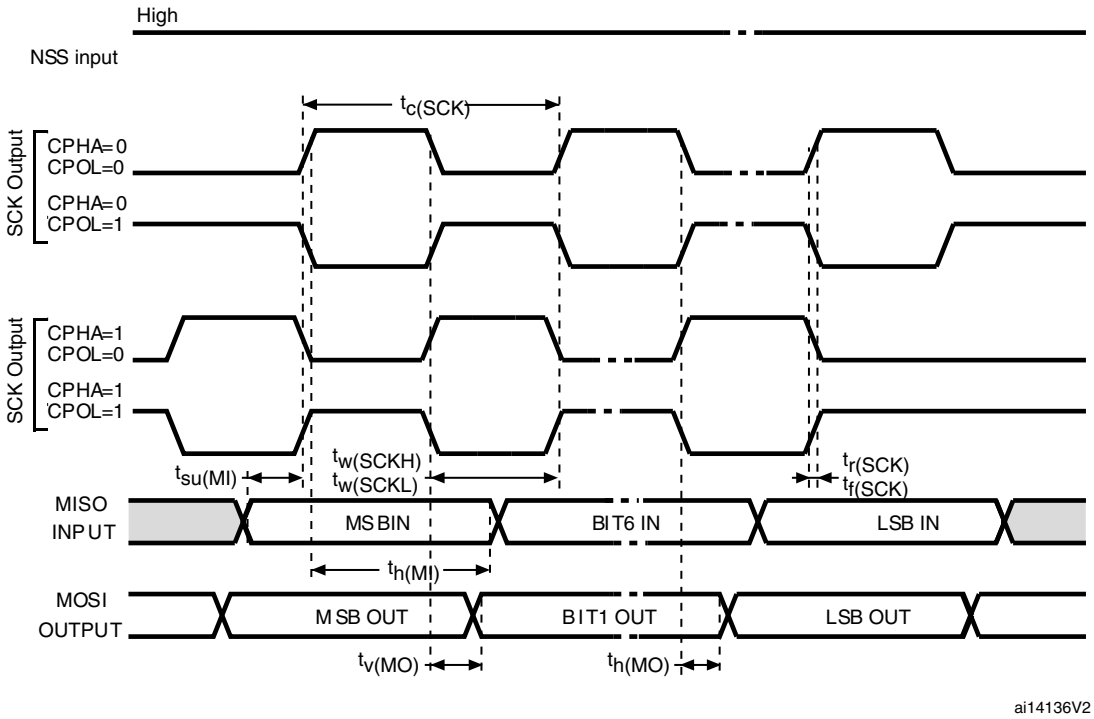


Figure 41. SPI timing diagram - master mode



I²S interface characteristics

Unless otherwise specified, the parameters given in *Table 56* for the i²S interface are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 14*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 V_{DD}

Refer to *Section 5.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (CK, SD, WS).

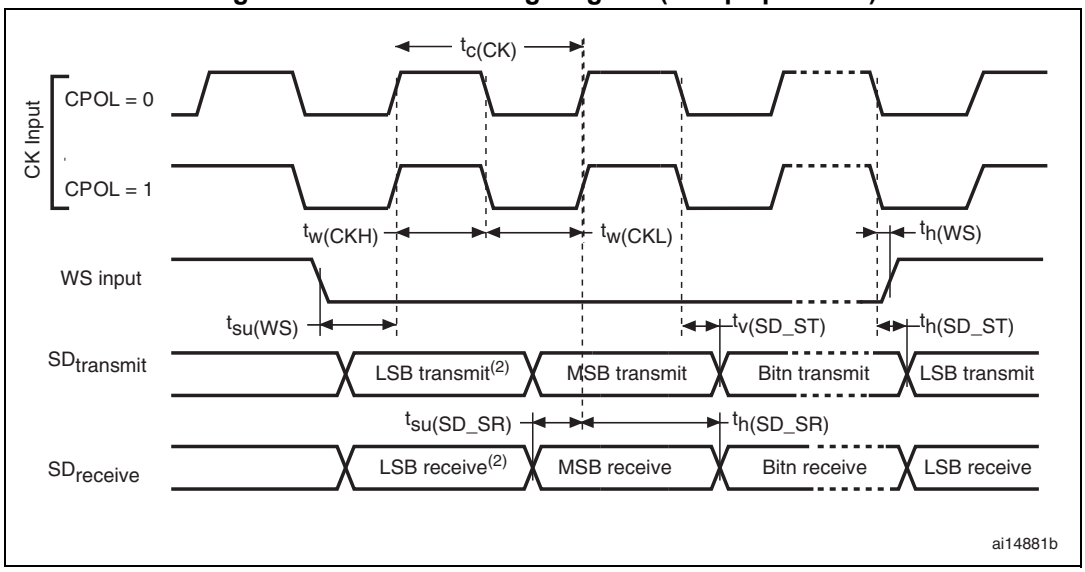
Table 56. I²S dynamic characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	I²S main clock output	-	256 x 8K	256 x F_S(2)	MHz
f_{CK}	I²S clock frequency	Master data: 32 bits	-	64 x F_S	MHz
		Slave data: 32 bits	-	64 x F_S	
D_{CK}	I²S clock frequency duty cycle	Slave receiver	30	70	%
$t_{v(WS)}$	WS valid time	Master mode	0	6	ns
$t_{h(WS)}$	WS hold time	Master mode	0	-	
$t_{su(WS)}$	WS setup time	Slave mode	1	-	
$t_{h(WS)}$	WS hold time	Slave mode	0	-	
$t_{su(SD\_MR)}$	Data input setup time	Master receiver	7.5	-	
$t_{su(SD\_SR)}$		Slave receiver	2	-	
$t_{h(SD\_MR)}$	Data input hold time	Master receiver	0	-	
$t_{h(SD\_SR)}$		Slave receiver	0	-	
$t_{v(SD\_ST)}$ $t_{h(SD\_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	27	
$t_{v(SD\_MT)}$		Master transmitter (after enable edge)	-	20	
$t_{h(SD\_MT)}$	Data output hold time	Master transmitter (after enable edge)	2.5	-	

1. Guaranteed by characterization results, not tested in production.
2. The maximum value of 256 x F_S is 42 MHz (APB1 maximum frequency).

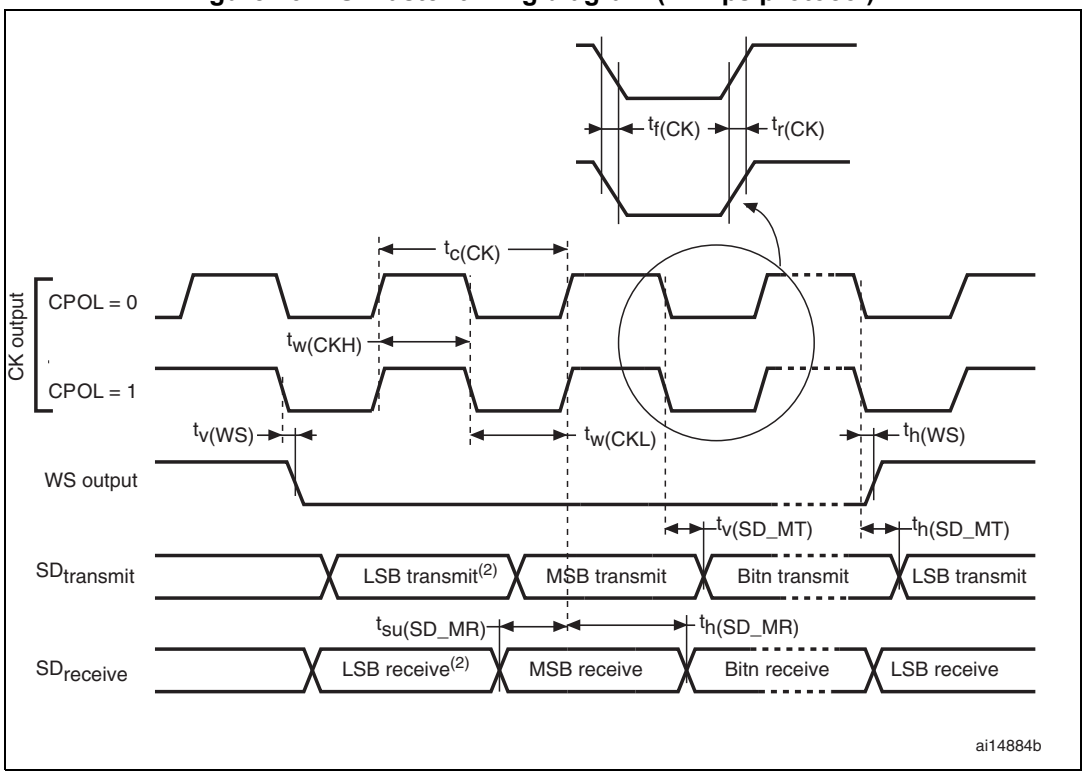
Note: Refer to the I²S section of RM0090 reference manual for more details on the sampling frequency (F_S). f_{MCK}, f_{CK}, and D_{CK} values reflect only the digital peripheral behavior. The value of these parameters might be slightly impacted by the source clock accuracy. D_{CK} depends mainly on the value of ODD bit. The digital contribution leads to a minimum value of I2SDIV / (2 x I2SDIV + ODD) and a maximum value of (I2SDIV + ODD) / (2 x I2SDIV + ODD). F_S maximum value is supported for each mode/condition.

Figure 42. I²S slave timing diagram (Philips protocol)



1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 43. I²S master timing diagram (Philips protocol)(1)



1. Guaranteed by characterization results, not tested in production.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

USB OTG FS characteristics

This interface is present in both the USB OTG HS and USB OTG FS controllers.

Table 57. USB OTG FS startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB OTG FS transceiver startup time	1	µs

1. Guaranteed by design, not tested in production.

Table 58. USB OTG FS DC electrical characteristics

Symbol		Parameter	Conditions	Min.(1)	Typ.	Max.(1)	Unit
Input levels	V_{DD}	USB OTG FS operating voltage		3.0(2)	-	3.6	V
	V_{DI}(3)	Differential input sensitivity	I(USB_FS_DP/DM, USB_HS_DP/DM)	0.2	-	-	V
	V_{CM}(3)	Differential common mode range	Includes V_{DI} range	0.8	-	2.5	
	V_{SE}(3)	Single ended receiver threshold		1.3	-	2.0	
Output levels	V_{OL}	Static output level low	R_L of 1.5 kΩ to 3.6 V(4)	-	-	0.3	V
	V_{OH}	Static output level high	R_L of 15 kΩ to V_{SS}(4)	2.8	-	3.6	
R_{PD}		PA11, PA12, PB14, PB15 (USB_FS_DP/DM, USB_HS_DP/DM)	$V_{IN} = V_{DD}$	17	21	24	kΩ
		PA9, PB13 (OTG_FS_VBUS, OTG_HS_VBUS)		0.65	1.1	2.0	
R_{PU}		PA12, PB15 (USB_FS_DP, USB_HS_DP)	$V_{IN} = V_{SS}$	1.5	1.8	2.1	
		PA9, PB13 (OTG_FS_VBUS, OTG_HS_VBUS)	$V_{IN} = V_{SS}$	0.25	0.37	0.55	

1. All the voltages are measured from the local ground potential.
2. The STM32F415xx and STM32F417xx USB OTG FS functionality is ensured down to 2.7 V but not the full USB OTG FS electrical characteristics which are degraded in the 2.7-to-3.0 V V_{DD} voltage range.
3. Guaranteed by design, not tested in production.
4. R_L is the load connected on the USB OTG FS drivers

Figure 44. USB OTG FS timings: definition of data signal rise and fall time

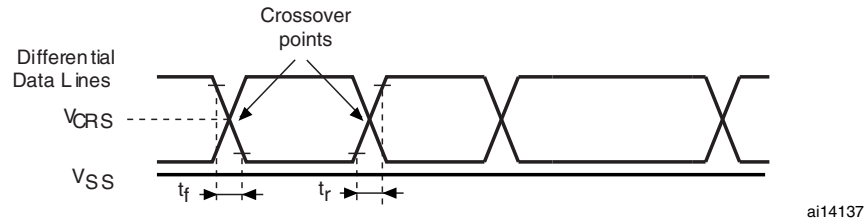


Table 59. USB OTG FS electrical characteristics(1)

Driver characteristics					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
t_r	Rise time(2)	C_L = 50 pF	4	20	ns
t_f	Fall time(2)	C_L = 50 pF	4	20	ns
t_{rfm}	Rise/ fall time matching	t_r/t_f	90	110	%
V_{CRS}	Output signal crossover voltage		1.3	2.0	V

1. Guaranteed by design, not tested in production.
2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).

USB HS characteristics

Unless otherwise specified, the parameters given in *Table 62* for ULPI are derived from tests performed under the ambient temperature, f_{HCLK} frequency summarized in *Table 61* and V_{DD} supply voltage conditions summarized in *Table 60*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$.

Refer to Section *Section 5.3.16: I/O port characteristics* for more details on the input/output characteristics.

Table 60. USB HS DC electrical characteristics

Symbol		Parameter	Min.(1)	Max.(1)	Unit
Input level	V_{DD}	USB OTG HS operating voltage	2.7	3.6	V

1. All the voltages are measured from the local ground potential.

Table 61. USB HS clock timing parameters(1)

Parameter		Symbol	Min	Nominal	Max	Unit
f_{HCLK} value to guarantee proper operation of USB HS interface			30			MHz
Frequency (first transition)	8-bit ±10%	F_{START_8BIT}	54	60	66	MHz
Frequency (steady state) ±500 ppm		F_{STEADY}	59.97	60	60.03	MHz

Table 61. USB HS clock timing parameters(1)

Parameter		Symbol	Min	Nominal	Max	Unit
Duty cycle (first transition)	8-bit ±10%	D_{START_8BIT}	40	50	60	%
Duty cycle (steady state) ±500 ppm		D_{STEADY}	49.975	50	50.025	%
Time to reach the steady state frequency and duty cycle after the first transition		T_{STEADY}	-	-	1.4	ms
Clock startup time after the de-assertion of SuspendM	Peripheral	T_{START_DEV}	-	-	5.6	ms
	Host	T_{START_HOST}	-	-	-	
PHY preparation time after the first transition of the input clock		T_{PREP}	-	-	-	µs

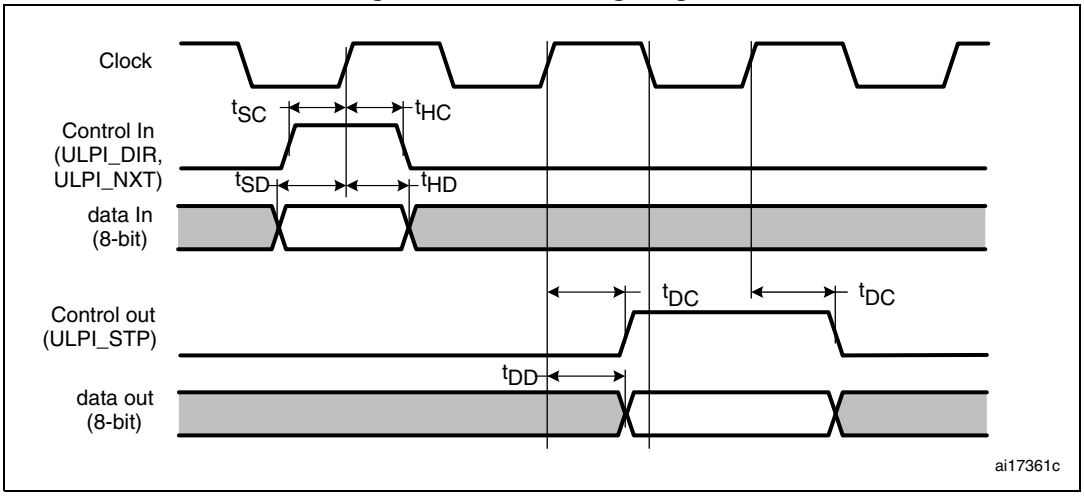
1. Guaranteed by design, not tested in production.

Table 62. ULPI timing

Parameter	Symbol	Value(1)		Unit
		Min.	Max.	
Control in (ULPI_DIR) setup time	t_{SC}	-	2.0	ns
Control in (ULPI_NXT) setup time		-	1.5	
Control in (ULPI_DIR, ULPI_NXT) hold time	t_{HC}	0	-	
Data in setup time	t_{SD}	-	2.0	
Data in hold time	t_{HD}	0	-	
Control out (ULPI_STP) setup time and hold time	t_{DC}	-	9.2	
Data out available from clock rising edge	t_{DD}	-	10.7	

1. V_{DD} = 2.7 V to 3.6 V and T_A = –40 to 85 °C.

Figure 45. ULPI timing diagram



Ethernet characteristics

Unless otherwise specified, the parameters given in *Table 64*, *Table 65* and *Table 66* for SMI, RMII and MII are derived from tests performed under the ambient temperature, f_{HCLK} frequency summarized in *Table 14* and VDD supply voltage conditions summarized in *Table 63*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$.

Refer to *Section 5.3.16: I/O port characteristics* for more details on the input/output characteristics.

Table 63. Ethernet DC electrical characteristics

Symbol		Parameter	Min.(1)	Max.(1)	Unit
Input level	V_{DD}	Ethernet operating voltage	2.7	3.6	V

1. All the voltages are measured from the local ground potential.

Table 64 gives the list of Ethernet MAC signals for the SMI (station management interface) and *Figure 46* shows the corresponding timing diagram.

Figure 46. Ethernet SMI timing diagram

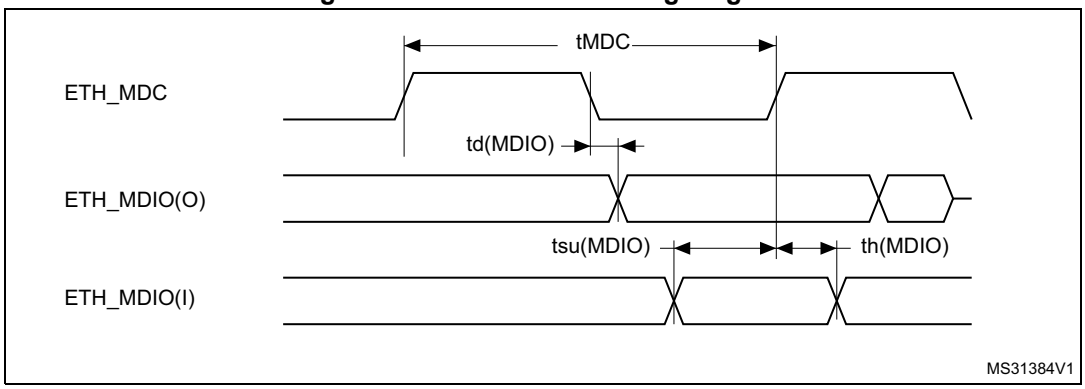


Table 64. Dynamic characteristics: Eternity MAC signals for SMI(1)

Symbol	Parameter	Min	Typ	Max	Unit
t_{MDC}	MDC cycle time(2.38 MHz)	411	420	425	ns
$T_{d(MDIO)}$	Write data valid time	6	10	13	
$t_{su(MDIO)}$	Read data setup time	12	-	-	
$t_{h(MDIO)}$	Read data hold time	0	-	-	

1. Guaranteed by characterization results, not tested in production.

Table 65 gives the list of Ethernet MAC signals for the RMII and *Figure 47* shows the corresponding timing diagram.

Figure 47. Ethernet RMII timing diagram

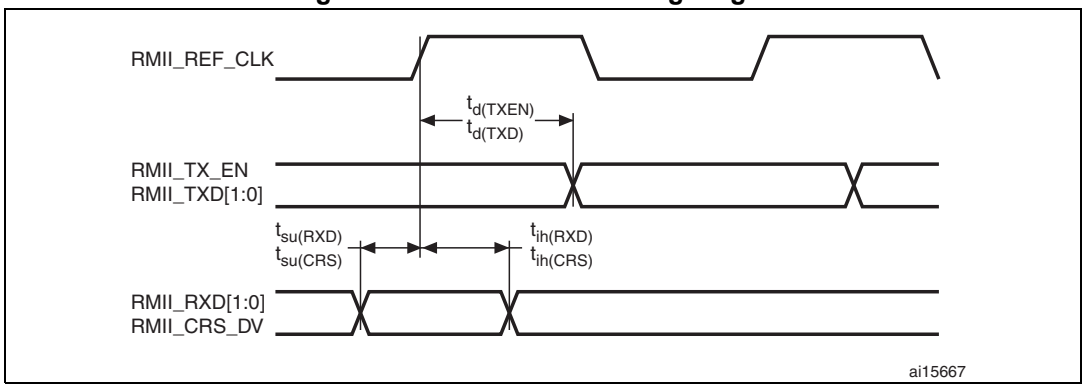


Table 65. Dynamic characteristics: Ethernet MAC signals for RMII

Symbol	Rating	Min	Typ	Max	Unit
$t_{su(RXD)}$	Receive data setup time	2	-	-	ns
$t_{ih(RXD)}$	Receive data hold time	1	-	-	ns
$t_{su(CRS)}$	Carrier sense set-up time	0.5	-	-	ns
$t_{ih(CRS)}$	Carrier sense hold time	2	-	-	ns
$t_{d(TXEN)}$	Transmit enable valid delay time	8	9.5	11	ns
$t_{d(TXD)}$	Transmit data valid delay time	8.5	10	11.5	ns

Table 66 gives the list of Ethernet MAC signals for MII and *Figure 47* shows the corresponding timing diagram.

Figure 48. Ethernet MII timing diagram

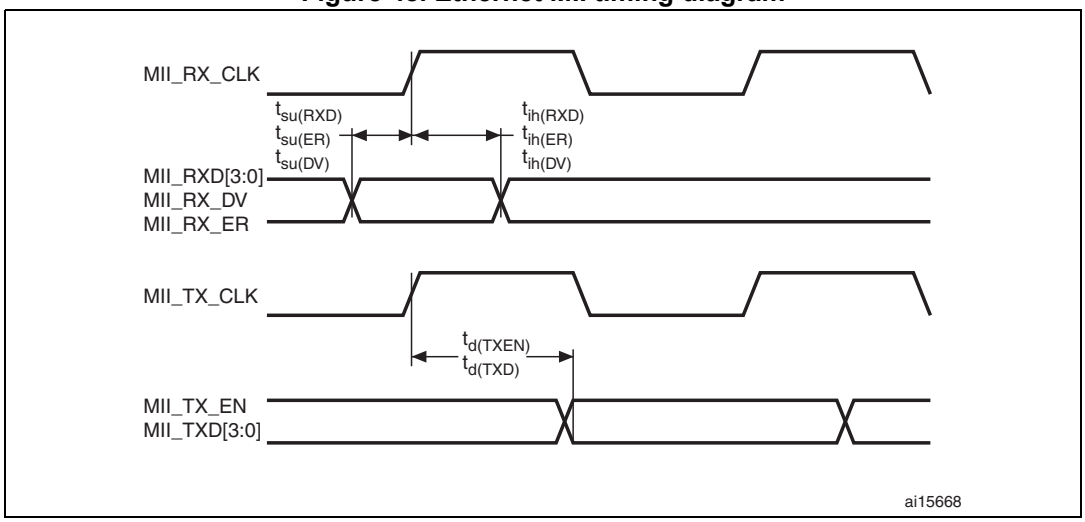


Table 66. Dynamic characteristics: Ethernet MAC signals for MII(1)

Symbol	Parameter	Min	Typ	Max	Unit
$t_{su(RXD)}$	Receive data setup time	9		-	ns
$t_{ih(RXD)}$	Receive data hold time	10		-	
$t_{su(DV)}$	Data valid setup time	9		-	
$t_{ih(DV)}$	Data valid hold time	8		-	
$t_{su(ER)}$	Error setup time	6		-	
$t_{ih(ER)}$	Error hold time	8		-	
$t_{d(TXEN)}$	Transmit enable valid delay time	0	10	14	
$t_{d(TXD)}$	Transmit data valid delay time	0	10	15	

1. Guaranteed by characterization results, not tested in production.

5.3.20 CAN (controller area network) interface

Refer to *Section 5.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (CANTX and CANRX).

5.3.21 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 67* are derived from tests performed under the ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 14*.

Table 67. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply		1.8(1)	-	3.6	V
V_{REF+}	Positive reference voltage		1.8(1)(2)(3)	-	V_{DDA}	V
f_{ADC}	ADC clock frequency	V_{DDA} = 1.8(1)(3) to 2.4 V	0.6	15	18	MHz
		V_{DDA} = 2.4 to 3.6 V(3)	0.6	30	36	MHz
f_{TRIG}(4)	External trigger frequency	f_{ADC} = 30 MHz, 12-bit resolution	-	-	1764	kHz
			-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range(5)		0 (V_{SSA} or V_{REF-} tied to ground)	-	V_{REF+}	V
R_{AIN}(4)	External input impedance	See *Equation 1* for details	-	-	50	kΩ
R_{ADC}(4)(6)	Sampling switch resistance		-	-	6	kΩ
C_{ADC}(4)	Internal sample and hold capacitor		-	4	-	pF
t_{lat}(4)	Injection trigger conversion latency	f_{ADC} = 30 MHz	-	-	0.100	µs
			-	-	3(7)	$1/f_{ADC}$

Table 67. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{latr}(4)	Regular trigger conversion latency	f_{ADC} = 30 MHz	-	-	0.067	µs
			-	-	2(7)	$1/f_{ADC}$
t_S(4)	Sampling time	f_{ADC} = 30 MHz	0.100	-	16	µs
			3	-	480	$1/f_{ADC}$
t_{STAB}(4)	Power-up time		-	2	3	µs
t_{CONV}(4)	Total conversion time (including sampling time)	f_{ADC} = 30 MHz 12-bit resolution	0.50	-	16.40	µs
		f_{ADC} = 30 MHz 10-bit resolution	0.43	-	16.34	µs
		f_{ADC} = 30 MHz 8-bit resolution	0.37	-	16.27	µs
		f_{ADC} = 30 MHz 6-bit resolution	0.30	-	16.20	µs
		9 to 492 (t_S for sampling +n-bit resolution for successive approximation)				$1/f_{ADC}$
f_S(4)	Sampling rate (f_{ADC} = 30 MHz, and t_S = 3 ADC cycles)	12-bit resolution Single ADC	-	-	2	Msps
		12-bit resolution Interleave Dual ADC mode	-	-	3.75	Msps
		12-bit resolution Interleave Triple ADC mode	-	-	6	Msps
I_{VREF+}(4)	ADC V_{REF} DC current consumption in conversion mode		-	300	500	µA
I_{VDDA}(4)	ADC V_{DDA} DC current consumption in conversion mode		-	1.6	1.8	mA

1. V_{DD}/V_{DDA} minimum value of 1.7 V is obtained when the device operates in reduced temperature range, and with the use of an external power supply supervisor (refer to *Section : Internal reset OFF*).
2. It is recommended to maintain the voltage difference between V_{REF+} and V_{DDA} below 1.8 V.
3. V_{DDA} -V_{REF+} < 1.2 V.
4. Guaranteed by characterization results, not tested in production.
5. V_{REF+} is internally connected to V_{DDA} and V_{REF-} is internally connected to V_{SSA}.
6. R_{ADC} maximum value is given for V_{DD}=1.8 V, and minimum value for V_{DD}=3.3 V.
7. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 67*.

Equation 1: R_{AIN} max formula

$$R_{AIN} = \frac{(k - 0{,}5)}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. N = 12 (from 12-bit resolution) and k is the number of sampling periods defined in the ADC_SMPR1 register.

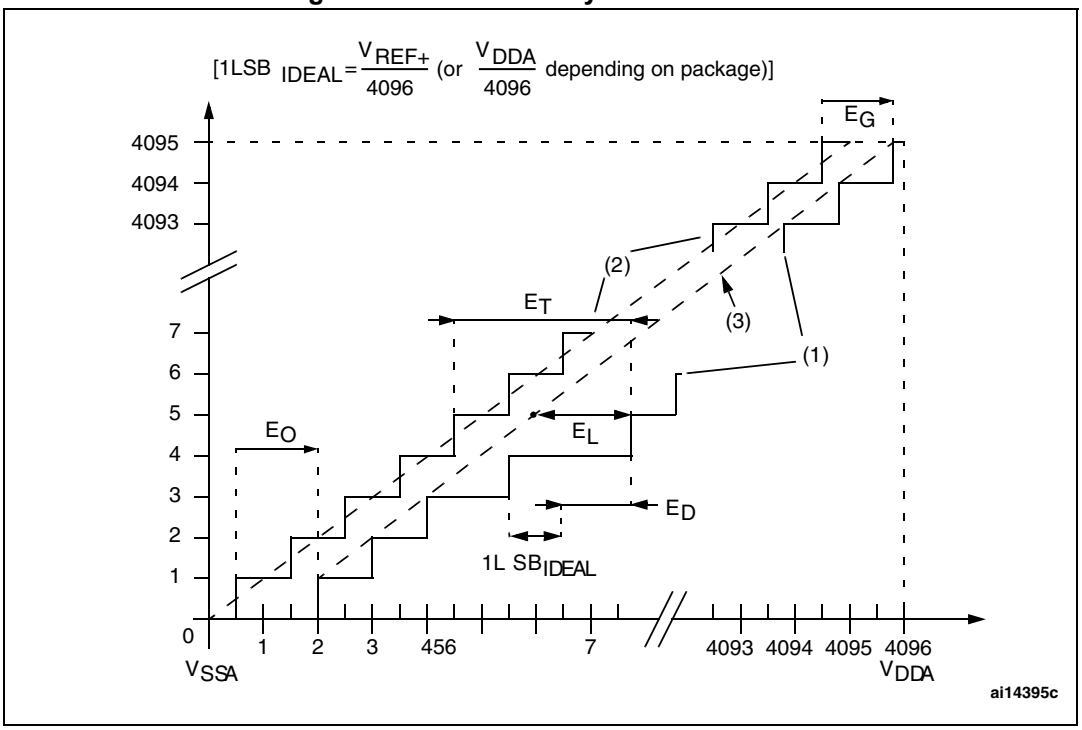
Table 68. ADC accuracy at f_{ADC} = 30 MHz(1)

Symbol	Parameter	Test conditions	Typ	Max(2)	Unit
ET	Total unadjusted error	f_{PCLK2} = 60 MHz, f_{ADC} = 30 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 1.8(3) to 3.6 V	±2	±5	LSB
EO	Offset error		±1.5	±2.5	
EG	Gain error		±1.5	±3	
ED	Differential linearity error		±1	±2	
EL	Integral linearity error		±1.5	±3	

1. Better performance could be achieved in restricted V_{DD}, frequency and temperature ranges.
2. Guaranteed by characterization results, not tested in production.
3. V_{DD}/V_{DDA} minimum value of 1.7 V is obtained when the device operates in reduced temperature range, and with the use of an external power supply supervisor (refer to *Section : Internal reset OFF*).

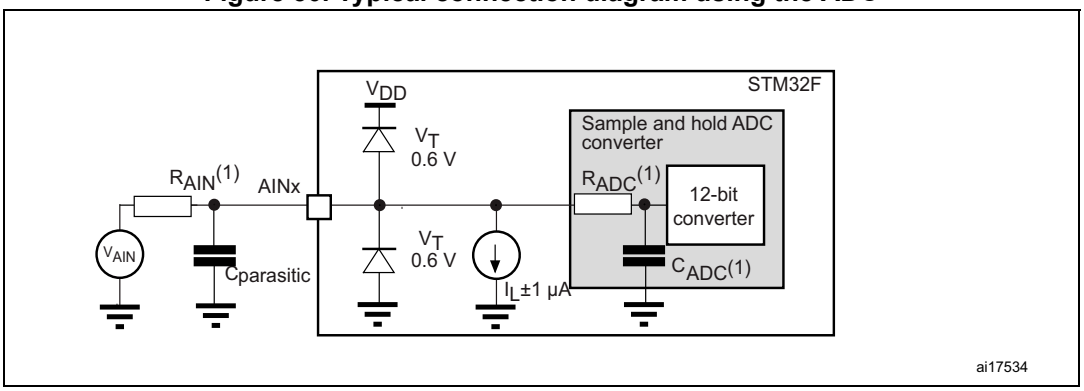
Note: ADC accuracy vs. negative injection current: injecting a negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $SI_{INJ(PIN)}$ in Section 5.3.16 does not affect the ADC accuracy.

Figure 49. ADC accuracy characteristics



1. See also *Table 68*.
2. Example of an actual transfer curve.
3. Ideal transfer curve.
4. End point correlation line.
5. E_T = Total Unadjusted Error: maximum deviation between the actual and the ideal transfer curves.
   EO = Offset Error: deviation between the first actual transition and the first ideal one.
   EG = Gain Error: deviation between the last ideal transition and the last actual one.
   ED = Differential Linearity Error: maximum deviation between actual steps and the ideal one.
   EL = Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.

Figure 50. Typical connection diagram using the ADC

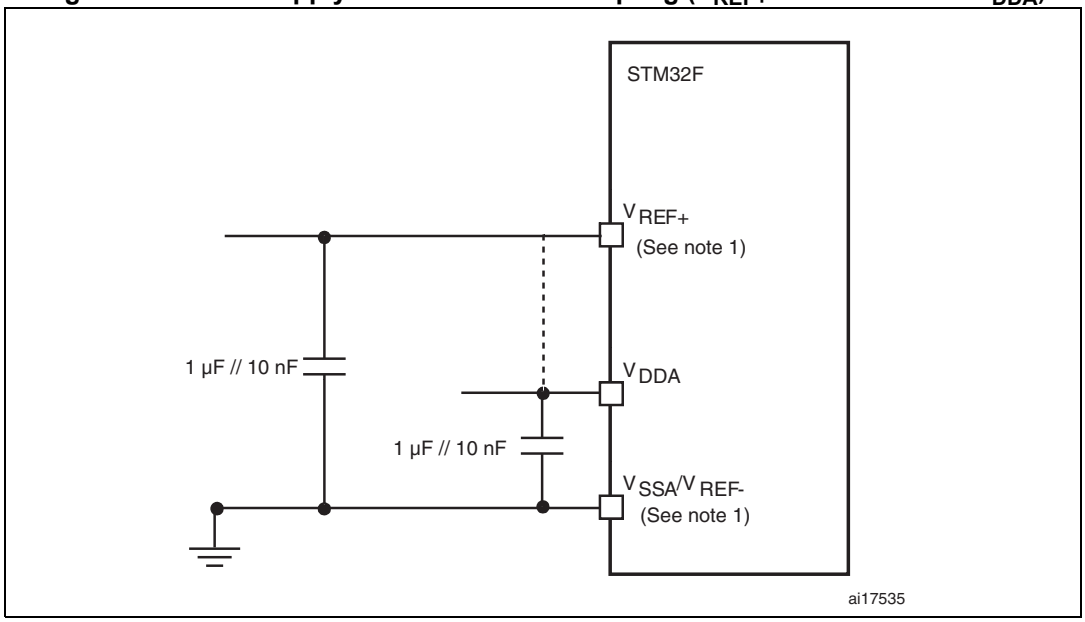


1. Refer to *Table 67* for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 5 pF). A high $C_{parasitic}$ value downgrades conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

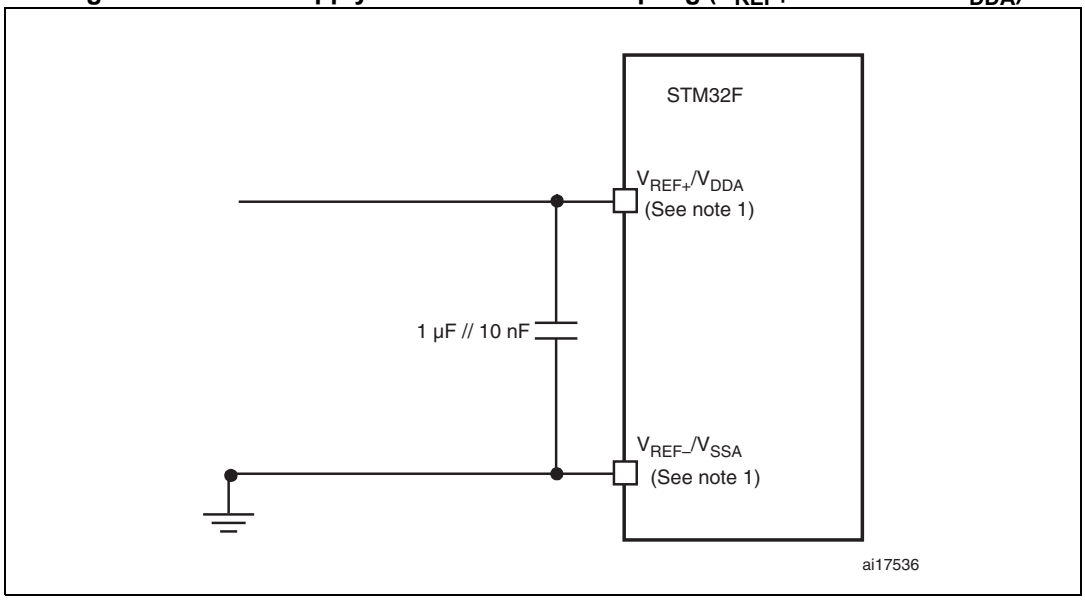
Power supply decoupling should be performed as shown in *Figure 51* or *Figure 52*, depending on whether V_{REF+} is connected to V_{DDA} or not. The 10 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

Figure 51. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are both available on UFBGA176. V_{REF+} is also available on LQFP100, LQFP144, and LQFP176. When V_{REF+} and V_{REF-} are not available, they are internally connected to V_{DDA} and V_{SSA}.

Figure 52. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are both available on UFBGA176. V_{REF+} is also available on LQFP100, LQFP144, and LQFP176. When V_{REF+} and V_{REF-} are not available, they are internally connected to V_{DDA} and V_{SSA}.

5.3.22 Temperature sensor characteristics

Table 69. Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L (1)	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope(1)	Average slope	-	2.5		mV/°C
V_{25} (1)	Voltage at 25 °C	-	0.76		V
t_{START} (2)	Startup time	-	6	10	µs
T_{S_temp} (2)	ADC sampling time when reading the temperature (1 °C accuracy)	10	-	-	µs

1. Guaranteed by characterization results, not tested in production.
2. Guaranteed by design, not tested in production.

Table 70. Temperature sensor calibration values

Symbol	Parameter	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 °C, V_{DDA}=3.3 V	0x1FFF 7A2C - 0x1FFF 7A2D
TS_CAL2	TS ADC raw data acquired at temperature of 110 °C, V_{DDA}=3.3 V	0x1FFF 7A2E - 0x1FFF 7A2F

5.3.23 V_{BAT} monitoring characteristics

Table 71. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	50	-	KΩ
Q	Ratio on V_{BAT} measurement	-	2	-	
Er(1)	Error on Q	–1	-	+1	%
T_{S_vbat} (2)(2)	ADC sampling time when reading the V_{BAT} 1 mV accuracy	5	-	-	µs

1. Guaranteed by design, not tested in production.
2. Shortest sampling time can be determined in the application by multiple iterations.

5.3.24 Embedded reference voltage

The parameters given in *Table 72* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 14*.

Table 72. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +105 °C	1.18	1.21	1.24	V
$T_{S\_vrefint}$(1)	ADC sampling time when reading the internal reference voltage		10	-	-	µs
V_{RERINT_s}(2)	Internal reference voltage spread over the temperature range	V_{DD} = 3 V	-	3	5	mV
T_{Coeff}(2)	Temperature coefficient		-	30	50	ppm/°C
t_{START}(2)	Startup time		-	6	10	µs

1. Shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design, not tested in production.

Table 73. Internal reference voltage calibration values

Symbol	Parameter	Memory address
V_{REFIN_CAL}	Raw data acquired at temperature of 30 °C, V_{DDA}=3.3 V	0x1FFF 7A2A - 0x1FFF 7A2B

5.3.25 DAC electrical characteristics

Table 74. DAC characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Comments
V_{DDA}	Analog supply voltage	1.8(1)	-	3.6	V	
V_{REF+}	Reference supply voltage	1.8(1)	-	3.6	V	$V_{REF+} \leq V_{DDA}$
V_{SSA}	Ground	0	-	0	V	
R_{LOAD}(2)	Resistive load with buffer ON	5	-	-	kΩ	
R_O(2)	Impedance output with buffer OFF	-	-	15	kΩ	When the buffer is OFF, the Minimum resistive load between DAC_OUT and V_{SS} to have a 1% accuracy is 1.5 MΩ
C_{LOAD}(2)	Capacitive load	-	-	50	pF	Maximum capacitive load at DAC_OUT pin (when the buffer is ON).
DAC_OUT min(2)	Lower DAC_OUT voltage with buffer ON	0.2	-	-	V	It gives the maximum output excursion of the DAC. It corresponds to 12-bit input code (0x0E0) to (0xF1C) at V_{REF+} = 3.6 V and (0x1C7) to (0xE38) at V_{REF+} = 1.8 V
DAC_OUT max(2)	Higher DAC_OUT voltage with buffer ON	-	-	V_{DDA} – 0.2	V	

Table 74. DAC characteristics (continued)

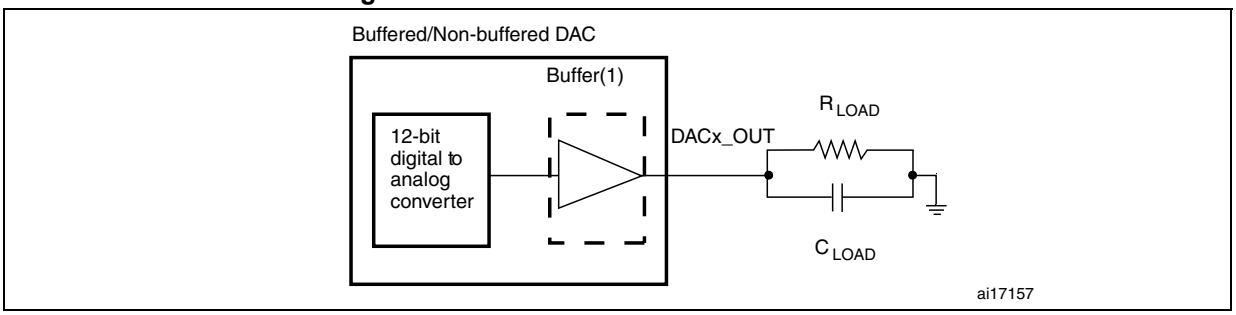
Symbol	Parameter	Min	Typ	Max	Unit	Comments
DAC_OUT min(2)	Lower DAC_OUT voltage with buffer OFF	-	0.5	-	mV	It gives the maximum output excursion of the DAC.
DAC_OUT max(2)	Higher DAC_OUT voltage with buffer OFF	-	-	V_{REF+} – 1LSB	V	
I_{VREF+}(4)	DAC DC V_{REF} current consumption in quiescent mode (Standby mode)	-	170	240	µA	With no load, worst code (0x800) at V_{REF+} = 3.6 V in terms of DC consumption on the inputs
		-	50	75		With no load, worst code (0xF1C) at V_{REF+} = 3.6 V in terms of DC consumption on the inputs
I_{DDA}(4)	DAC DC VDDA current consumption in quiescent mode(3)	-	280	380	µA	With no load, middle code (0x800) on the inputs
		-	475	625	µA	With no load, worst code (0xF1C) at V_{REF+} = 3.6 V in terms of DC consumption on the inputs
DNL(4)	Differential non linearity Difference between two consecutive code-1LSB)	-	-	±0.5	LSB	Given for the DAC in 10-bit configuration.
		-	-	±2	LSB	Given for the DAC in 12-bit configuration.
INL(4)	Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023)	-	-	±1	LSB	Given for the DAC in 10-bit configuration.
		-	-	±4	LSB	Given for the DAC in 12-bit configuration.
Offset(4)	Offset error (difference between measured value at Code (0x800) and the ideal value = V_{REF+}/2)	-	-	±10	mV	Given for the DAC in 12-bit configuration
		-	-	±3	LSB	Given for the DAC in 10-bit at V_{REF+} = 3.6 V
		-	-	±12	LSB	Given for the DAC in 12-bit at V_{REF+} = 3.6 V
Gain error(4)	Gain error	-	-	±0.5	%	Given for the DAC in 12-bit configuration
$t_{SETTLING}$(4)	Settling time (full scale: for a 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±4LSB	-	3	6	µs	$C_{LOAD} \leq$ 50 pF, $R_{LOAD} \geq$ 5 kΩ
THD(4)	Total Harmonic Distortion Buffer ON	-	-	-	dB	$C_{LOAD} \leq$ 50 pF, $R_{LOAD} \geq$ 5 kΩ

Table 74. DAC characteristics (continued)

Symbol	Parameter	Min	Typ	Max	Unit	Comments
Update rate(2)	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)	-	-	1	MS/s	$C_{LOAD} \leq$ 50 pF, $R_{LOAD} \geq 5$ kΩ
t_{WAKEUP}(4)	Wakeup time from off state (Setting the ENx bit in the DAC Control register)	-	6.5	10	µs	$C_{LOAD} \leq$ 50 pF, $R_{LOAD} \geq 5$ kΩ input code between lowest and highest possible ones.
PSRR+ (2)	Power supply rejection ratio (to V_{DDA}) (static DC measurement)	-	–67	–40	dB	No R_{LOAD}, C_{LOAD} = 50 pF

1. V_{DD}/V_{DDA} minimum value of 1.7 V is obtained when the device operates in reduced temperature range, and with the use of an external power supply supervisor (refer to *Section : Internal reset OFF*).
2. Guaranteed by design, not tested in production.
3. The quiescent mode corresponds to a state where the DAC maintains a stable output level to ensure that no dynamic consumption occurs.
4. Guaranteed by characterization results, not tested in production.

Figure 53. 12-bit buffered /non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

5.3.26 FSMC characteristics

Unless otherwise specified, the parameters given in *Table 75* to *Table 86* for the FSMC interface are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage conditions summarized in *Table 14*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to Section *Section 5.3.16: I/O port characteristics* for more details on the input/output characteristics.

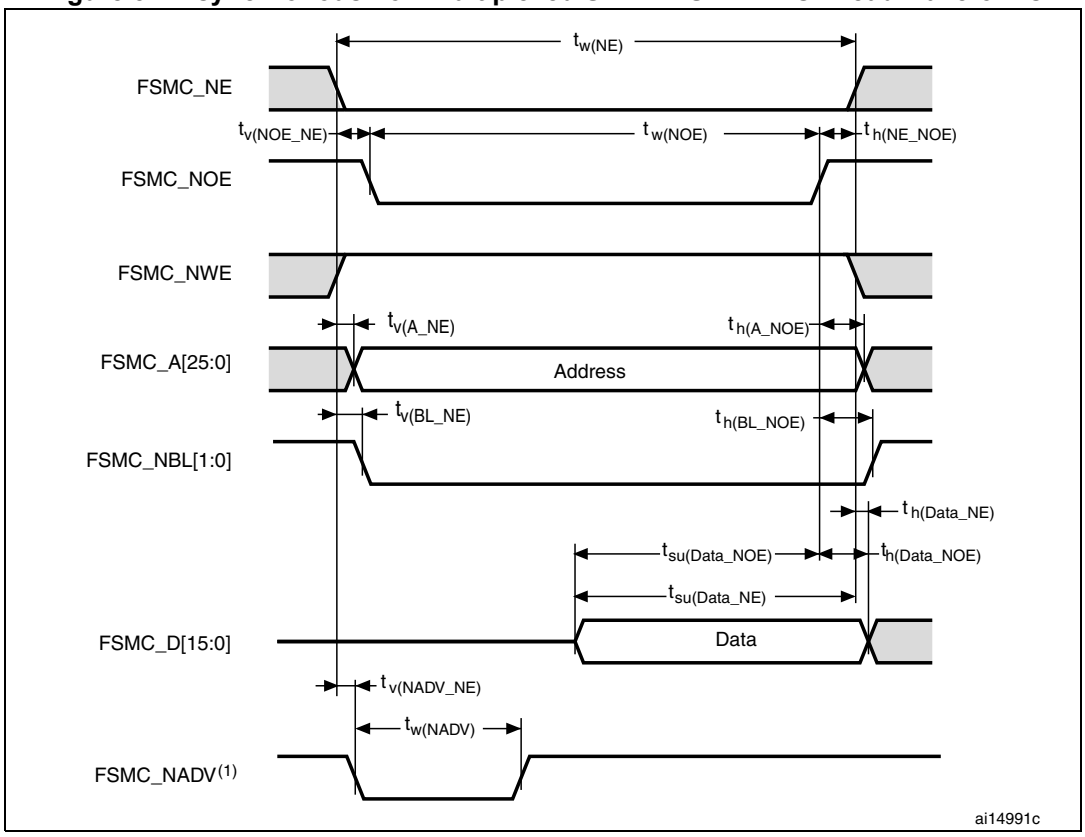
Asynchronous waveforms and timings

Figure 54 through *Figure 57* represent asynchronous waveforms and *Table 75* through *Table 78* provide the corresponding timings. The results shown in these tables are obtained with the following FSMC configuration:

- AddressSetupTime = 1
- AddressHoldTime = 0x1
- DataSetupTime = 0x1
- BusTurnAroundDuration = 0x0

In all timing tables, the T_{HCLK} is the HCLK clock period.

Figure 54. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms



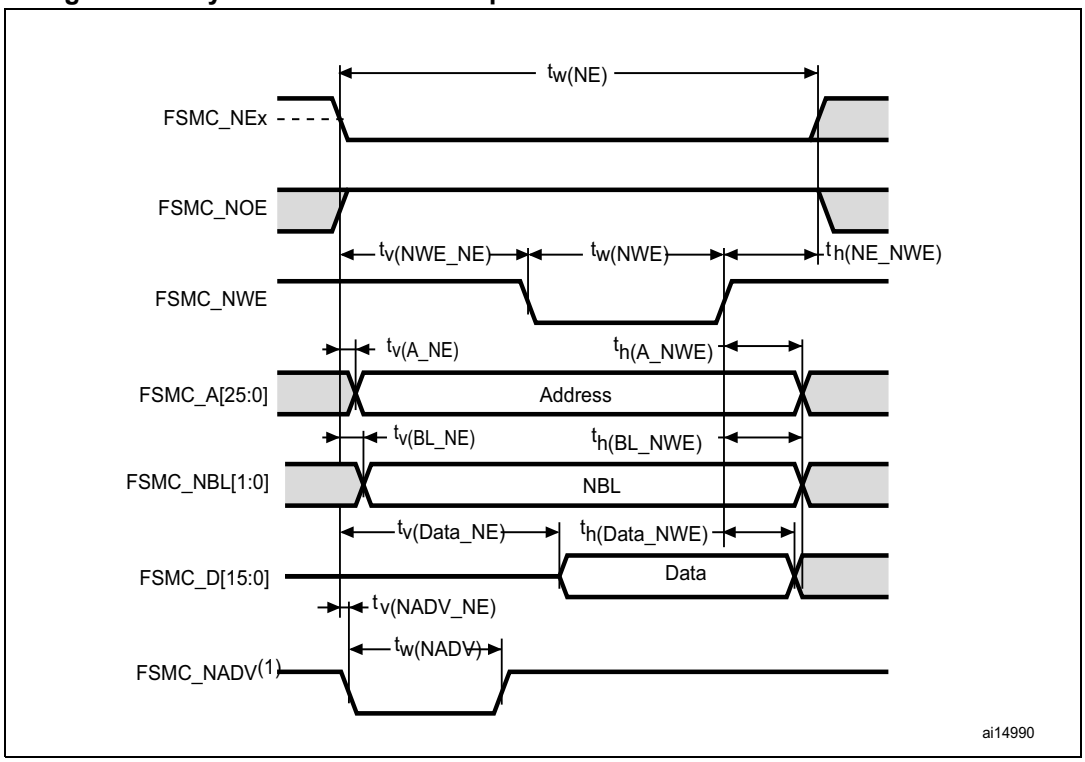
1. Mode 2/B, C and D only. In Mode 1, FSMC_NADV is not used.

Table 75. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$2T_{HCLK}–0.5$	$2\ T_{HCLK}+1$	ns
$t_{v(NOE\_NE)}$	FSMC_NEx low to FSMC_NOE low	0.5	3	ns
$t_{w(NOE)}$	FSMC_NOE low time	$2T_{HCLK}–2$	$2T_{HCLK}+ 2$	ns
$t_{h(NE\_NOE)}$	FSMC_NOE high to FSMC_NE high hold time	0	-	ns
$t_{v(A\_NE)}$	FSMC_NEx low to FSMC_A valid	-	4.5	ns
$t_{h(A\_NOE)}$	Address hold time after FSMC_NOE high	4	-	ns
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid	-	1.5	ns
$t_{h(BL\_NOE)}$	FSMC_BL hold time after FSMC_NOE high	0	-	ns
$t_{su(Data\_NE)}$	Data to FSMC_NEx high setup time	$T_{HCLK}+4$	-	ns
$t_{su(Data\_NOE)}$	Data to FSMC_NOEx high setup time	$T_{HCLK}+4$	-	ns
$t_{h(Data\_NOE)}$	Data hold time after FSMC_NOE high	0	-	ns
$t_{h(Data\_NE)}$	Data hold time after FSMC_NEx high	0	-	ns
$t_{v(NADV\_NE)}$	FSMC_NEx low to FSMC_NADV low	-	2	ns
$t_{w(NADV)}$	FSMC_NADV low time	-	T_{HCLK}	ns

1. C_L = 30 pF.
2. Guaranteed by characterization results, not tested in production.

Figure 55. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms



1. Mode 2/B, C and D only. In Mode 1, FSMC_NADV is not used.

Table 76. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$3T_{HCLK}$	$3T_{HCLK}+4$	ns
$t_{v(NWE\_NE)}$	FSMC_NEx low to FSMC_NWE low	$T_{HCLK}-0.5$	$T_{HCLK}+0.5$	ns
$t_{w(NWE)}$	FSMC_NWE low time	$T_{HCLK}-1$	$T_{HCLK}+2$	ns
$t_{h(NE\_NWE)}$	FSMC_NWE high to FSMC_NE high hold time	$T_{HCLK}-1$	-	ns
$t_{v(A\_NE)}$	FSMC_NEx low to FSMC_A valid	-	0	ns
$t_{h(A\_NWE)}$	Address hold time after FSMC_NWE high	$T_{HCLK}-2$	-	ns
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid	-	1.5	ns
$t_{h(BL\_NWE)}$	FSMC_BL hold time after FSMC_NWE high	$T_{HCLK}-1$	-	ns
$t_{v(Data\_NE)}$	Data to FSMC_NEx low to Data valid	-	$T_{HCLK}+3$	ns
$t_{h(Data\_NWE)}$	Data hold time after FSMC_NWE high	$T_{HCLK}-1$	-	ns
$t_{v(NADV\_NE)}$	FSMC_NEx low to FSMC_NADV low	-	2	ns
$t_{w(NADV)}$	FSMC_NADV low time	-	$T_{HCLK}+0.5$	ns

1. C_L = 30 pF.
2. Guaranteed by characterization results, not tested in production.

Figure 56. Asynchronous multiplexed PSRAM/NOR read waveforms

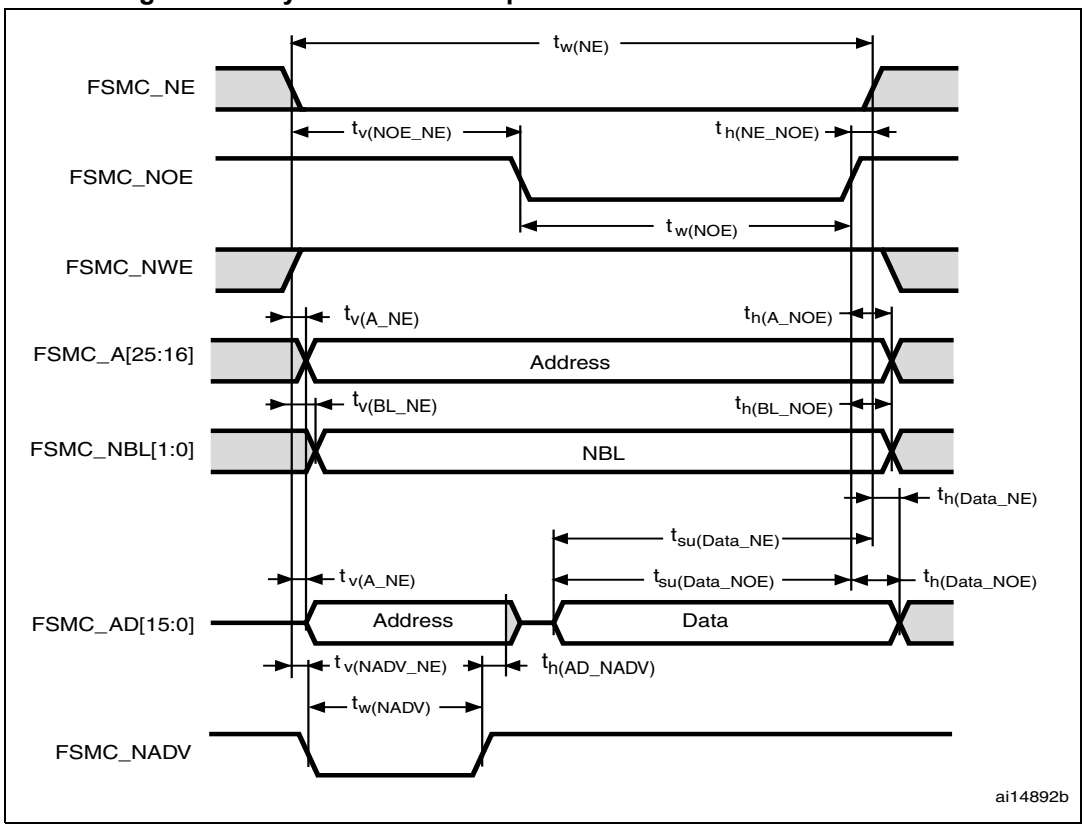


Table 77. Asynchronous multiplexed PSRAM/NOR read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$3T_{HCLK}-1$	$3T_{HCLK}+1$	ns
$t_{v(NOE\_NE)}$	FSMC_NEx low to FSMC_NOE low	$2T_{HCLK}-0.5$	$2T_{HCLK}+0.5$	ns
$t_{w(NOE)}$	FSMC_NOE low time	$T_{HCLK}-1$	$T_{HCLK}+1$	ns
$t_{h(NE\_NOE)}$	FSMC_NOE high to FSMC_NE high hold time	0	-	ns
$t_{v(A\_NE)}$	FSMC_NEx low to FSMC_A valid	-	3	ns
$t_{v(NADV\_NE)}$	FSMC_NEx low to FSMC_NADV low	1	2	ns
$t_{w(NADV)}$	FSMC_NADV low time	$T_{HCLK}-2$	$T_{HCLK}+1$	ns
$t_{h(AD\_NADV)}$	FSMC_AD(adress) valid hold time after FSMC_NADV high)	T_{HCLK}	-	ns
$t_{h(A\_NOE)}$	Address hold time after FSMC_NOE high	$T_{HCLK}-1$	-	ns
$t_{h(BL\_NOE)}$	FSMC_BL time after FSMC_NOE high	0	-	ns
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid	-	2	ns
$t_{su(Data\_NE)}$	Data to FSMC_NEx high setup time	$T_{HCLK}+4$	-	ns
$t_{su(Data\_NOE)}$	Data to FSMC_NOE high setup time	$T_{HCLK}+4$	-	ns
$t_{h(Data\_NE)}$	Data hold time after FSMC_NEx high	0	-	ns
$t_{h(Data\_NOE)}$	Data hold time after FSMC_NOE high	0	-	ns

1. C_L = 30 pF.

2. Guaranteed by characterization results, not tested in production.

Figure 57. Asynchronous multiplexed PSRAM/NOR write waveforms

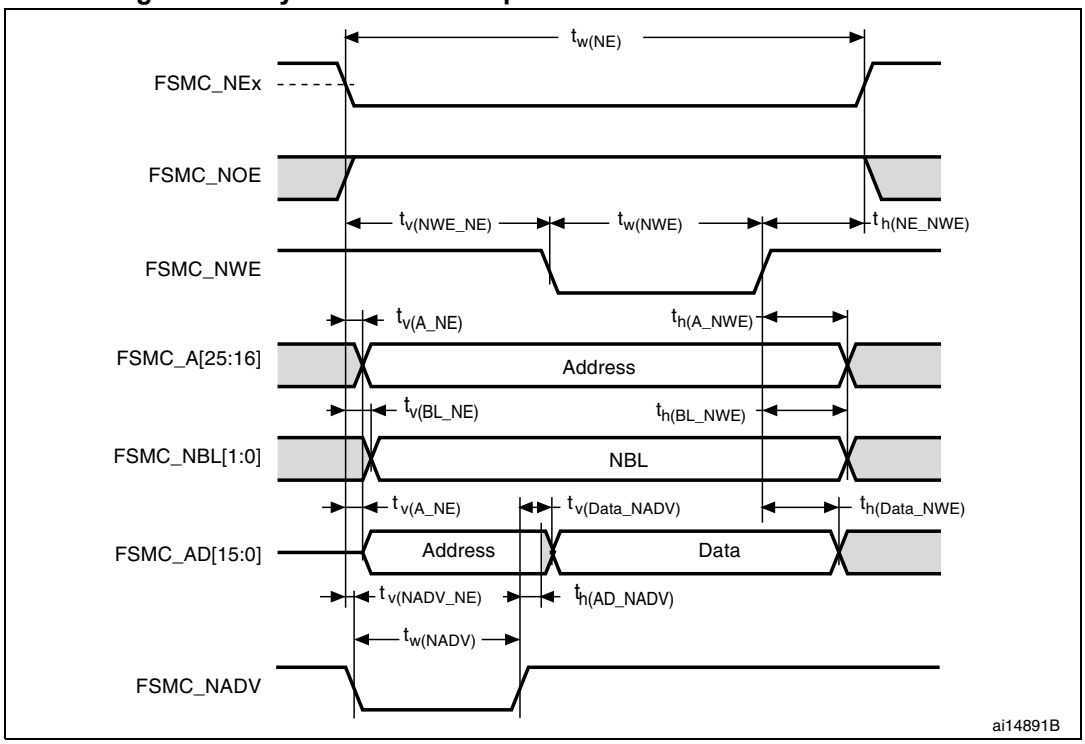


Table 78. Asynchronous multiplexed PSRAM/NOR write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$4T_{HCLK}$–0.5	$4T_{HCLK}$+3	ns
$t_{v(NWE\_NE)}$	FSMC_NEx low to FSMC_NWE low	T_{HCLK}–0.5	T_{HCLK} -0.5	ns
$t_{w(NWE)}$	FSMC_NWE low tim e	$2T_{HCLK}$–0.5	$2T_{HCLK}$+3	ns
$t_{h(NE\_NWE)}$	FSMC_NWE high to FSMC_NE high hold time	T_{HCLK}	-	ns
$t_{v(A\_NE)}$	FSMC_NEx low to FSMC_A valid	-	0	ns
$t_{v(NADV\_NE)}$	FSMC_NEx low to FSMC_NADV low	1	2	ns
$t_{w(NADV)}$	FSMC_NADV low time	T_{HCLK}– 2	T_{HCLK}+ 1	ns
$t_{h(AD\_NADV)}$	FSMC_AD(address) valid hold time after FSMC_NADV high)	T_{HCLK}–2	-	ns
$t_{h(A\_NWE)}$	Address hold time after FSMC_NWE high	T_{HCLK}	-	ns
$t_{h(BL\_NWE)}$	FSMC_BL hold time after FSMC_NWE high	T_{HCLK}–2	-	ns
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid	-	1.5	ns
$t_{v(Data\_NADV)}$	FSMC_NADV high to Data valid	-	T_{HCLK}–0.5	ns
$t_{h(Data\_NWE)}$	Data hold time after FSMC_NWE high	T_{HCLK}	-	ns

1. C_L = 30 pF.
2. Guaranteed by characterization results, not tested in production.

Synchronous waveforms and timings

Figure 58 through *Figure 61* represent synchronous waveforms and *Table 80* through *Table 82* provide the corresponding timings. The results shown in these tables are obtained with the following FSMC configuration:

- BurstAccessMode = FSMC_BurstAccessMode_Enable;
- MemoryType = FSMC_MemoryType_CRAM;
- WriteBurst = FSMC_WriteBurst_Enable;
- CLKDivision = 1; (0 is not supported, see the STM32F40xxx/41xxx reference manual)
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM

In all timing tables, the T_{HCLK} is the HCLK clock period (with maximum FSMC_CLK = 60 MHz).

Figure 58. Synchronous multiplexed NOR/PSRAM read timings

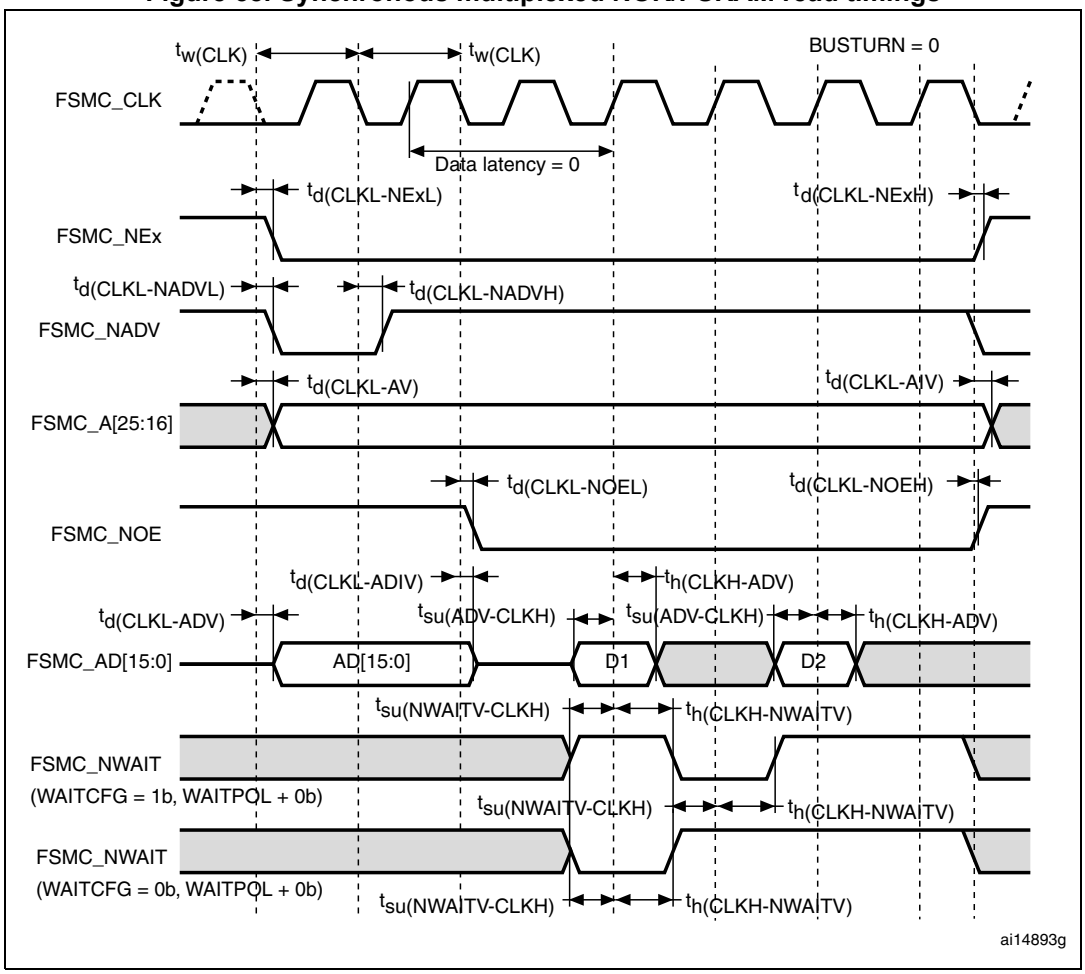


Table 79. Synchronous multiplexed NOR/PSRAM read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	$2T_{HCLK}$	-	ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x=0..2)	-	0	ns
$t_{d(CLKL-NExH)}$	FSMC_CLK low to FSMC_NEx high (x= 0…2)	2	-	ns
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low	-	2	ns
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	2	-	ns
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x=16…25)	-	0	ns
$t_{d(CLKL-AIV)}$	FSMC_CLK low to FSMC_Ax invalid (x=16…25)	0	-	ns
$t_{d(CLKL-NOEL)}$	FSMC_CLK low to FSMC_NOE low	-	0	ns
$t_{d(CLKL-NOEH)}$	FSMC_CLK low to FSMC_NOE high	2	-	ns
$t_{d(CLKL-ADV)}$	FSMC_CLK low to FSMC_AD[15:0] valid	-	4.5	ns
$t_{d(CLKL-ADIV)}$	FSMC_CLK low to FSMC_AD[15:0] invalid	0	-	ns
$t_{su(ADV-CLKH)}$	FSMC_A/D[15:0] valid data before FSMC_CLK high	6	-	ns
$t_{h(CLKH-ADV)}$	FSMC_A/D[15:0] valid data after FSMC_CLK high	0	-	ns
$t_{su(NWAIT-CLKH)}$	FSMC_NWAIT valid before FSMC_CLK high	4	-	ns
$t_{h(CLKH-NWAIT)}$	FSMC_NWAIT valid after FSMC_CLK high	0	-	ns

1. C_L = 30 pF.
2. Guaranteed by characterization results, not tested in production.

Figure 59. Synchronous multiplexed PSRAM write timings

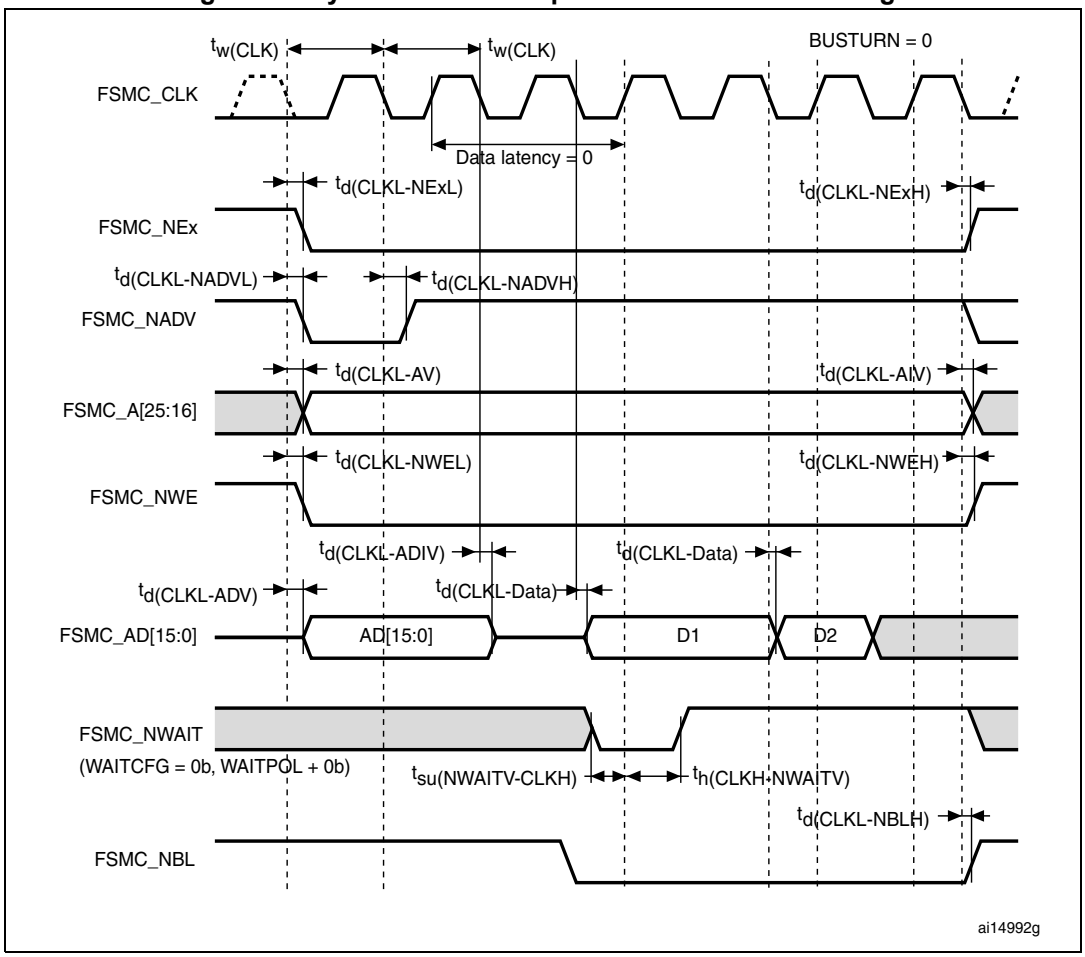


Table 80. Synchronous multiplexed PSRAM write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	$2T_{HCLK}$	-	ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x=0..2)	-	1	ns
$t_{d(CLKL-NExH)}$	FSMC_CLK low to FSMC_NEx high (x= 0…2)	1	-	ns
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low	-	0	ns
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	0	-	ns
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x=16…25)	-	0	ns
$t_{d(CLKL-AIV)}$	FSMC_CLK low to FSMC_Ax invalid (x=16…25)	8	-	ns
$t_{d(CLKL-NWEL)}$	FSMC_CLK low to FSMC_NWE low	-	0.5	ns
$t_{d(CLKL-NWEH)}$	FSMC_CLK low to FSMC_NWE high	0	-	ns
$t_{d(CLKL-ADIV)}$	FSMC_CLK low to FSMC_AD[15:0] invalid	0	-	ns
$t_{d(CLKL-DATA)}$	FSMC_A/D[15:0] valid data after FSMC_CLK low	-	3	ns

Table 80. Synchronous multiplexed PSRAM write timings(1)(2) (continued)

Symbol	Parameter	Min	Max	Unit
$t_{d(CLKL-NBLH)}$	FSMC_CLK low to FSMC_NBL high	0	-	ns
$t_{su(NWAIT-CLKH)}$	FSMC_NWAIT valid before FSMC_CLK high	4	-	ns
$t_{h(CLKH-NWAIT)}$	FSMC_NWAIT valid after FSMC_CLK high	0	-	ns

1. C_L = 30 pF.
2. Guaranteed by characterization results, not tested in production.

Figure 60. Synchronous non-multiplexed NOR/PSRAM read timings

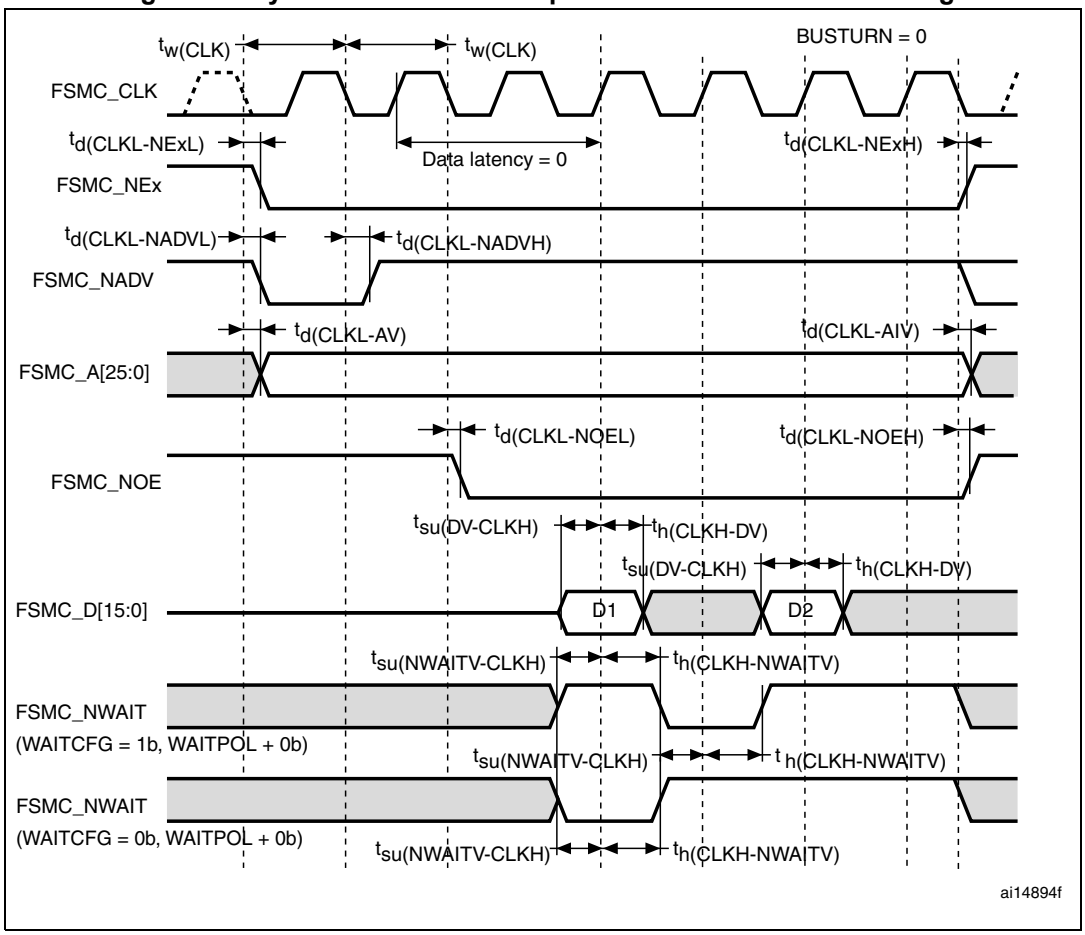


Table 81. Synchronous non-multiplexed NOR/PSRAM read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	$2T_{HCLK}$ –0.5	-	ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x=0..2)	-	0.5	ns
$t_{d(CLKL-NExH)}$	FSMC_CLK low to FSMC_NEx high (x= 0…2)	0	-	ns
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low	-	2	ns
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	3	-	ns
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x=16…25)	-	0	ns
$t_{d(CLKL-AIV)}$	FSMC_CLK low to FSMC_Ax invalid (x=16…25)	2	-	ns
$t_{d(CLKL-NOEL)}$	FSMC_CLK low to FSMC_NOE low	-	0.5	ns
$t_{d(CLKL-NOEH)}$	FSMC_CLK low to FSMC_NOE high	1.5	-	ns
$t_{su(DV-CLKH)}$	FSMC_D[15:0] valid data before FSMC_CLK high	6	-	ns
$t_{h(CLKH-DV)}$	FSMC_D[15:0] valid data after FSMC_CLK high	3	-	ns
$t_{su(NWAIT-CLKH)}$	FSMC_NWAIT valid before FSMC_CLK high	4	-	ns
$t_{h(CLKH-NWAIT)}$	FSMC_NWAIT valid after FSMC_CLK high	0	-	ns

1. C_L = 30 pF.
2. Guaranteed by characterization results, not tested in production.

Figure 61. Synchronous non-multiplexed PSRAM write timings

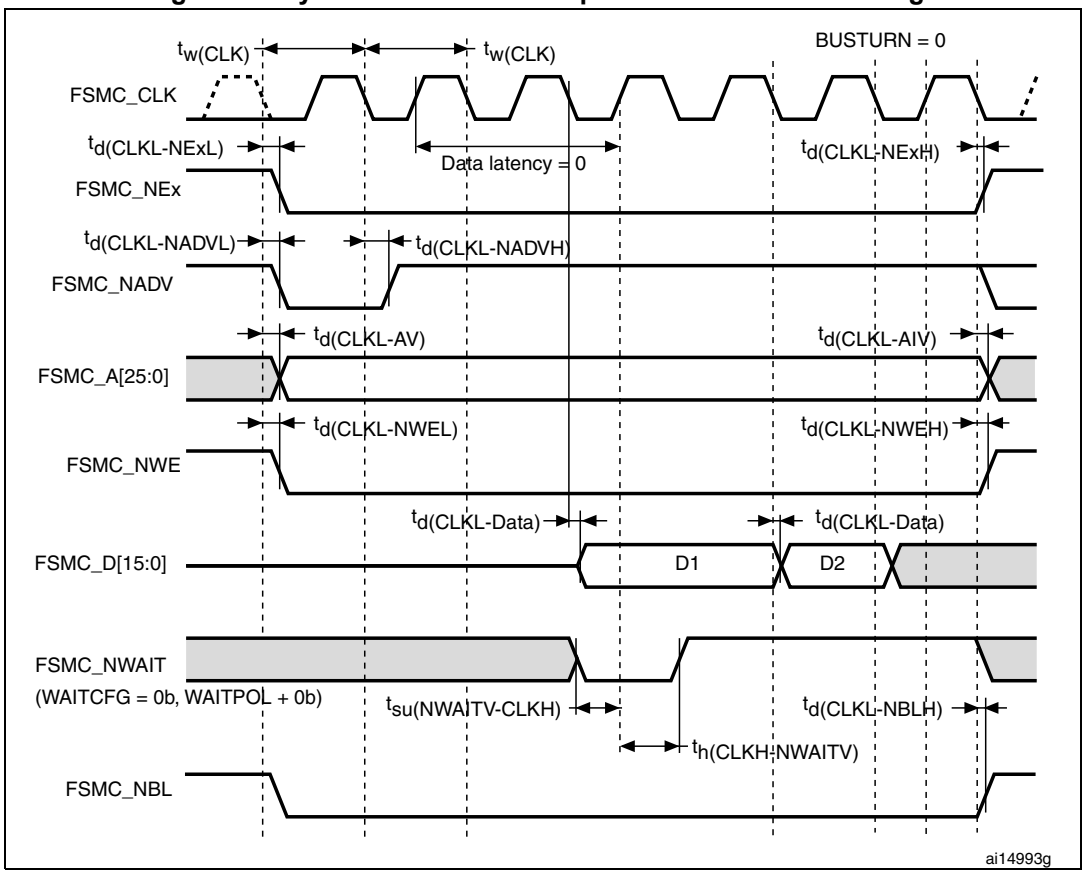


Table 82. Synchronous non-multiplexed PSRAM write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	$2T_{HCLK}$	-	ns
$t^{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x=0..2)	-	1	ns
$t_{d(CLKL-NExH)}$	FSMC_CLK low to FSMC_NEx high (x= 0…2)	1	-	ns
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low	-	7	ns
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	6	-	ns
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x=16…25)	-	0	ns
$t_{d(CLKL-AIV)}$	FSMC_CLK low to FSMC_Ax invalid (x=16…25)	6	-	ns
$t_{d(CLKL-NWEL)}$	FSMC_CLK low to FSMC_NWE low	-	1	ns
$t_{d(CLKL-NWEH)}$	FSMC_CLK low to FSMC_NWE high	2	-	ns
$t_{d(CLKL-Data)}$	FSMC_D[15:0] valid data after FSMC_CLK low	-	3	ns
$t_{d(CLKL-NBLH)}$	FSMC_CLK low to FSMC_NBL high	3	-	ns
$t_{su(NWAIT-CLKH)}$	FSMC_NWAIT valid before FSMC_CLK high	4	-	ns
$t_{h(CLKH-NWAIT)}$	FSMC_NWAIT valid after FSMC_CLK high	0	-	ns

1. C_L = 30 pF.
2. Guaranteed by characterization results, not tested in production.

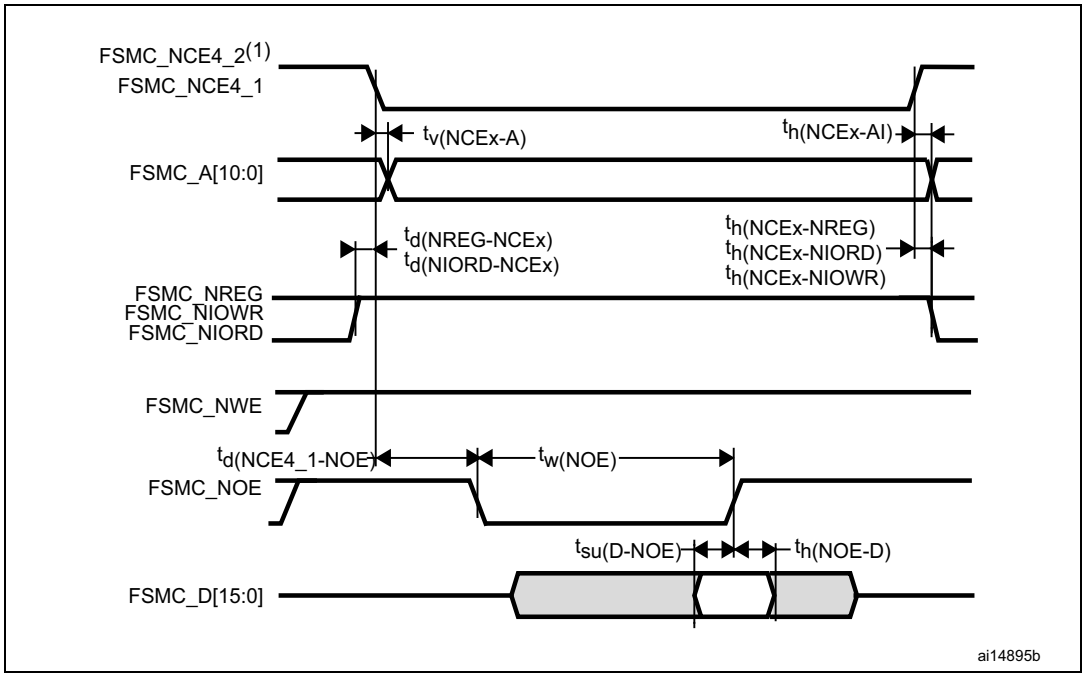
PC Card/CompactFlash controller waveforms and timings

Figure 62 through *Figure 67* represent synchronous waveforms, and *Table 83* and *Table 84* provide the corresponding timings. The results shown in this table are obtained with the following FSMC configuration:

- COM.FSMC_SetupTime = 0x04;
- COM.FSMC_WaitSetupTime = 0x07;
- COM.FSMC_HoldSetupTime = 0x04;
- COM.FSMC_HiZSetupTime = 0x00;
- ATT.FSMC_SetupTime = 0x04;
- ATT.FSMC_WaitSetupTime = 0x07;
- ATT.FSMC_HoldSetupTime = 0x04;
- ATT.FSMC_HiZSetupTime = 0x00;
- IO.FSMC_SetupTime = 0x04;
- IO.FSMC_WaitSetupTime = 0x07;
- IO.FSMC_HoldSetupTime = 0x04;
- IO.FSMC_HiZSetupTime = 0x00;
- TCLRSetupTime = 0;
- TARSetupTime = 0.

In all timing tables, the T_{HCLK} is the HCLK clock period.

Figure 62. PC Card/CompactFlash controller waveforms for common memory read access



1. FSMC_NCE4_2 remains high (inactive during 8-bit access.

Figure 63. PC Card/CompactFlash controller waveforms for common memory write access

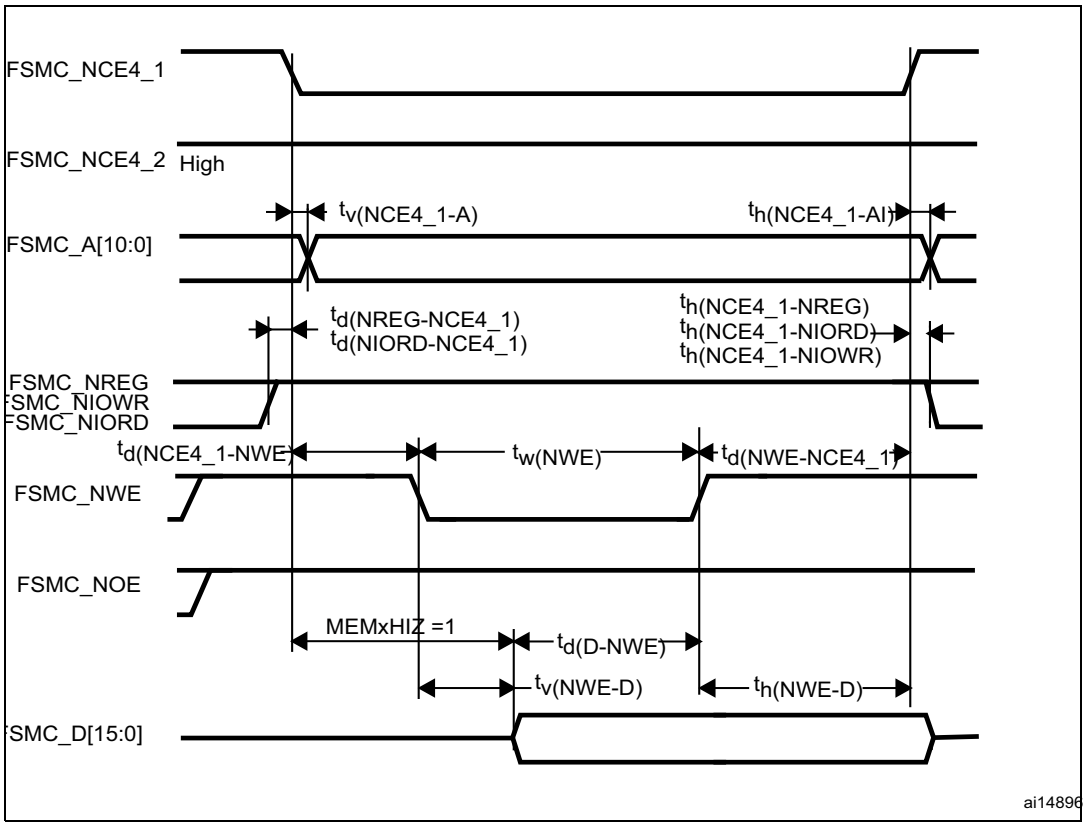
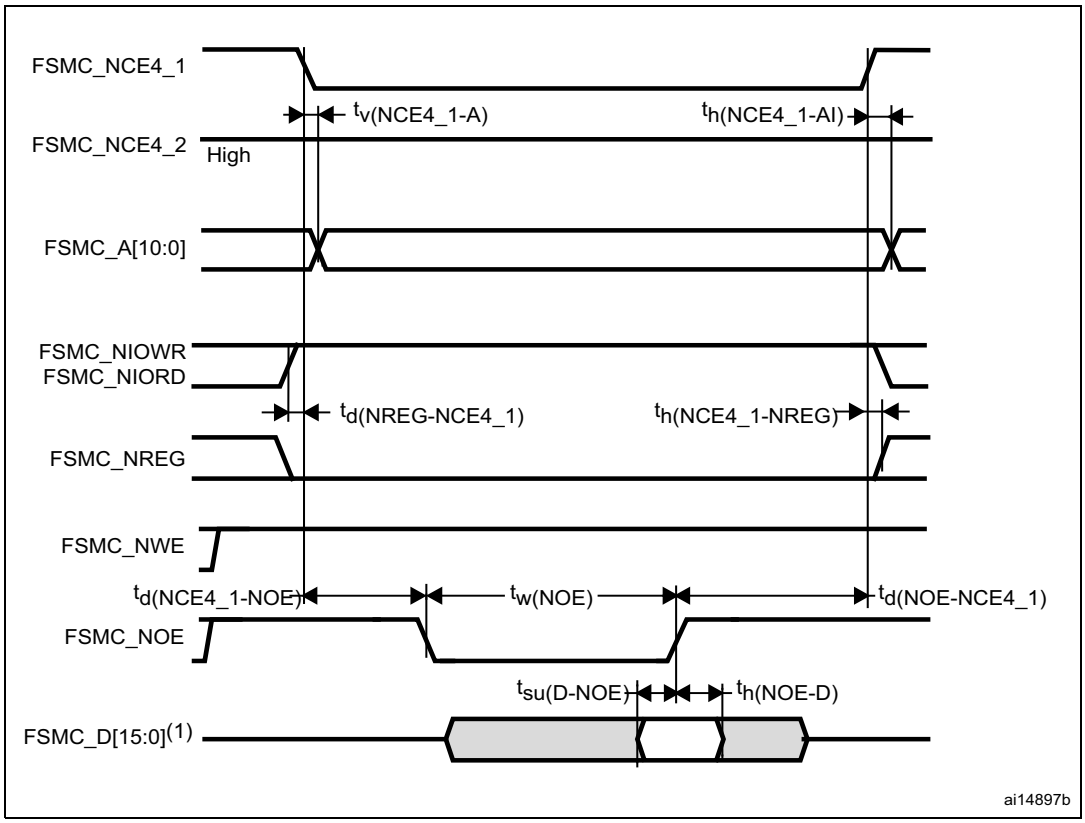
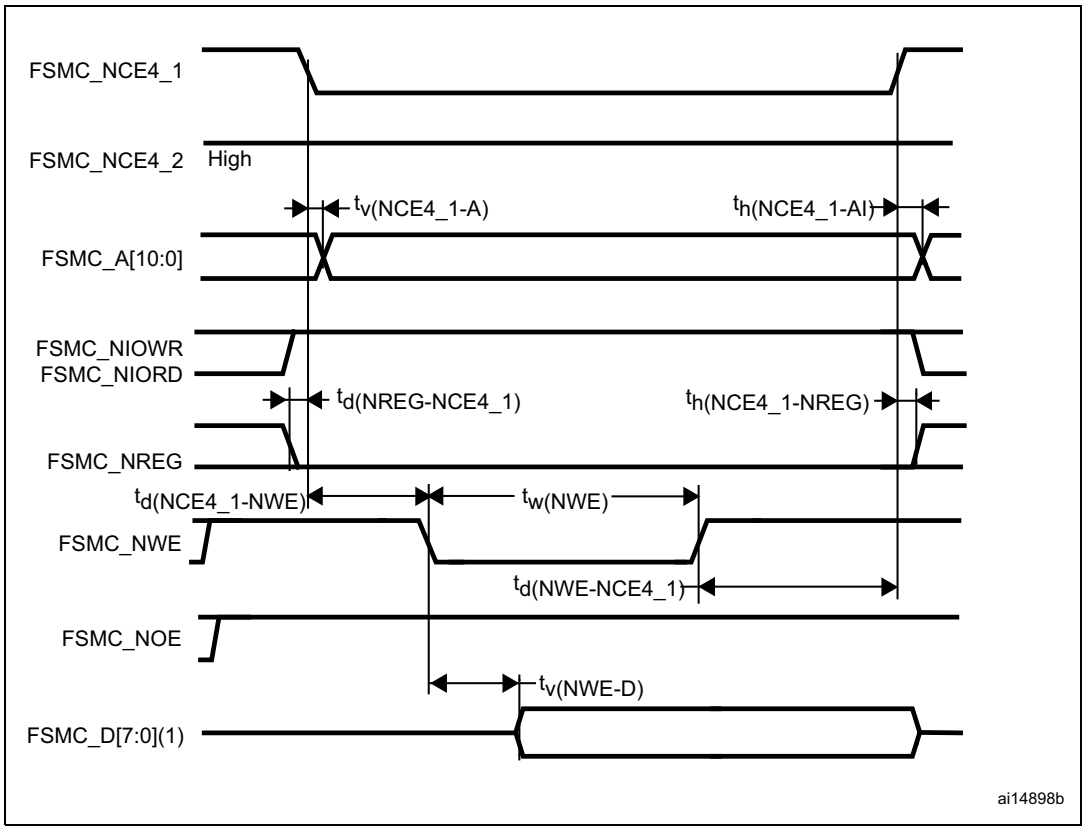


Figure 64. PC Card/CompactFlash controller waveforms for attribute memory read access



1. Only data bits 0...7 are read (bits 8...15 are disregarded).

Figure 65. PC Card/CompactFlash controller waveforms for attribute memory write access



1. Only data bits 0...7 are driven (bits 8...15 remains Hi-Z).

Figure 66. PC Card/CompactFlash controller waveforms for I/O space read access

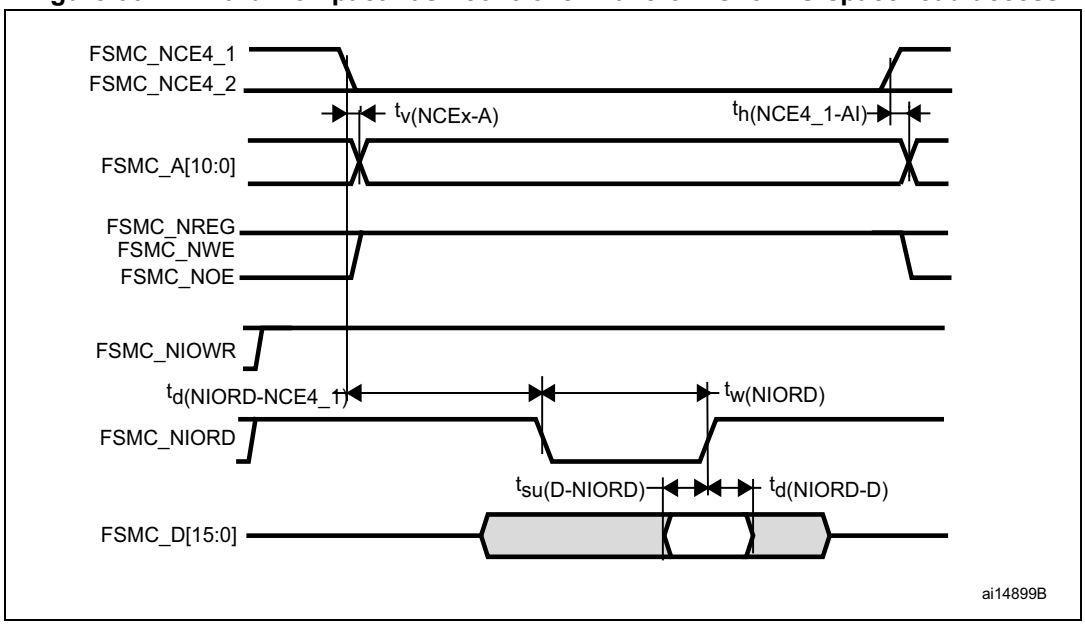


Figure 67. PC Card/CompactFlash controller waveforms for I/O space write access

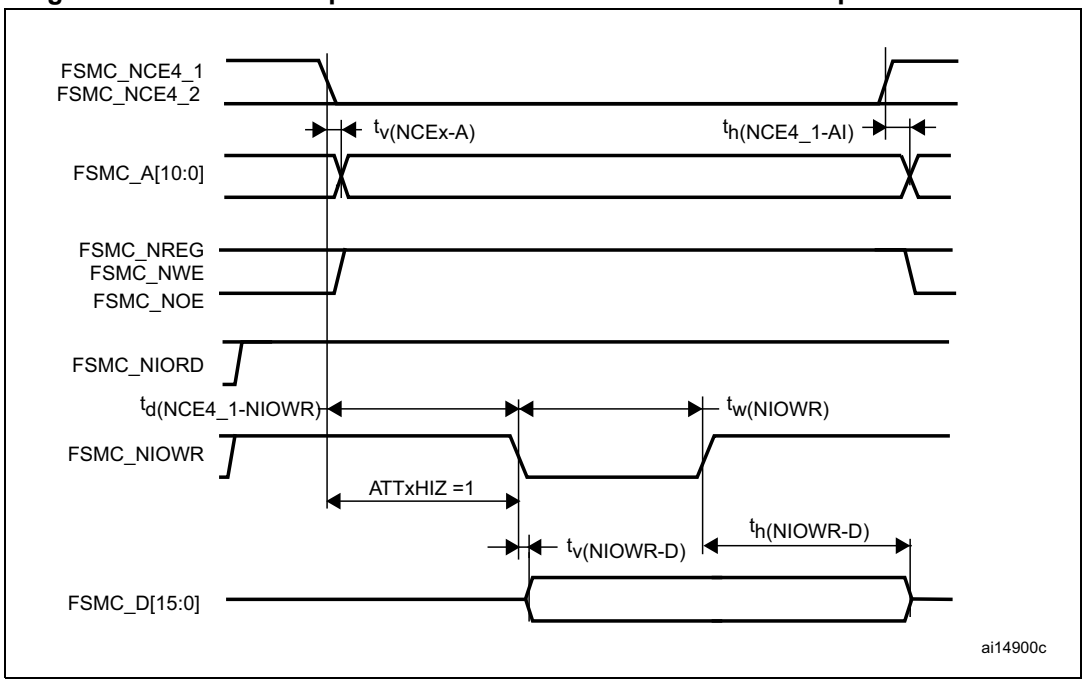


Table 83. Switching characteristics for PC Card/CF read and write cycles in attribute/common space(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{v(NCEx-A)}$	FSMC_Ncex low to FSMC_Ay valid	-	0	ns
$t_{h(NCEx\_AI)}$	FSMC_NCEx high to FSMC_Ax invalid	4	-	ns
$t_{d(NREG-NCEx)}$	FSMC_NCEx low to FSMC_NREG valid	-	3.5	ns
$t_{h(NCEx-NREG)}$	FSMC_NCEx high to FSMC_NREG invalid	T_{HCLK}+4	-	ns
$t_{d(NCEx-NWE)}$	FSMC_NCEx low to FSMC_NWE low	-	$5T_{HCLK}$+0.5	ns
$t_{d(NCEx-NOE)}$	FSMC_NCEx low to FSMC_NOE low	-	$5T_{HCLK}$ +0.5	ns
$t_{w(NOE)}$	FSMC_NOE low width	$8T_{HCLK}$–1	$8T_{HCLK}$+1	ns
$t_{d(NOE\_NCEx)}$	FSMC_NOE high to FSMC_NCEx high	$5T_{HCLK}$+2.5	-	ns
$t_{su\ (D-NOE)}$	FSMC_D[15:0] valid data before FSMC_NOE high	4.5	-	ns
$t_{h(N0E-D)}$	FSMC_N0E high to FSMC_D[15:0] invalid	3	-	ns
$t_{w(NWE)}$	FSMC_NWE low width	$8T_{HCLK}$–0.5	$8T_{HCLK}$+ 3	ns
$t_{d(NWE\_NCEx)}$	FSMC_NWE high to FSMC_NCEx high	$5T_{HCLK}$–1	-	ns
$t_{d(NCEx-NWE)}$	FSMC_NCEx low to FSMC_NWE low	-	$5T_{HCLK}$+ 1	ns
$t_{v(NWE-D)}$	FSMC_NWE low to FSMC_D[15:0] valid	-	0	ns
t_h (NWE-D)	FSMC_NWE high to FSMC_D[15:0] invalid	$8T_{HCLK}$ –1	-	ns
t_d (D-NWE)	FSMC_D[15:0] valid before FSMC_NWE high	$13T_{HCLK}$ –1	-	ns

1. C_L = 30 pF.
2. Guaranteed by characterization results, not tested in production.

Table 84. Switching characteristics for PC Card/CF read and write cycles in I/O space(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NIOWR)}$	FSMC_NIOWR low width	$8T_{HCLK}$ –1	-	ns
$t_{v(NIOWR-D)}$	FSMC_NIOWR low to FSMC_D[15:0] valid	-	$5T_{HCLK}$– 1	ns
$t_{h(NIOWR-D)}$	FSMC_NIOWR high to FSMC_D[15:0] invalid	$8T_{HCLK}$– 2	-	ns
$t_{d(NCE4\_1-NIOWR)}$	FSMC_NCE4_1 low to FSMC_NIOWR valid	-	$5T_{HCLK}$+ 2.5	ns
$t_{h(NCEx-NIOWR)}$	FSMC_NCEx high to FSMC_NIOWR invalid	$5T_{HCLK}$–1.5	-	ns
$t_{d(NIORD-NCEx)}$	FSMC_NCEx low to FSMC_NIORD valid	-	$5T_{HCLK}$+ 2	ns
$t_{h(NCEx-NIORD)}$	FSMC_NCEx high to FSMC_NIORD) valid	$5T_{HCLK}$– 1.5	-	ns
$t_{w(NIORD)}$	FSMC_NIORD low width	$8T_{HCLK}$–0.5	-	ns
$t_{su(D-NIORD)}$	FSMC_D[15:0] valid before FSMC_NIORD high	9	-	ns
$t_{d(NIORD-D)}$	FSMC_D[15:0] valid after FSMC_NIORD high	0	-	ns

1. C_L = 30 pF.
2. Guaranteed by characterization results, not tested in production.

NAND controller waveforms and timings

Figure 68 through *Figure 71* represent synchronous waveforms, and *Table 85* and *Table 86* provide the corresponding timings. The results shown in this table are obtained with the following FSMC configuration:

- COM.FSMC_SetupTime = 0x01;
- COM.FSMC_WaitSetupTime = 0x03;
- COM.FSMC_HoldSetupTime = 0x02;
- COM.FSMC_HiZSetupTime = 0x01;
- ATT.FSMC_SetupTime = 0x01;
- ATT.FSMC_WaitSetupTime = 0x03;
- ATT.FSMC_HoldSetupTime = 0x02;
- ATT.FSMC_HiZSetupTime = 0x01;
- Bank = FSMC_Bank_NAND;
- MemoryDataWidth = FSMC_MemoryDataWidth_16b;
- ECC = FSMC_ECC_Enable;
- ECCPageSize = FSMC_ECCPageSize_512Bytes;
- TCLRSetupTime = 0;
- TARSetupTime = 0.

In all timing tables, the T_{HCLK} is the HCLK clock period.

Figure 68. NAND controller waveforms for read access

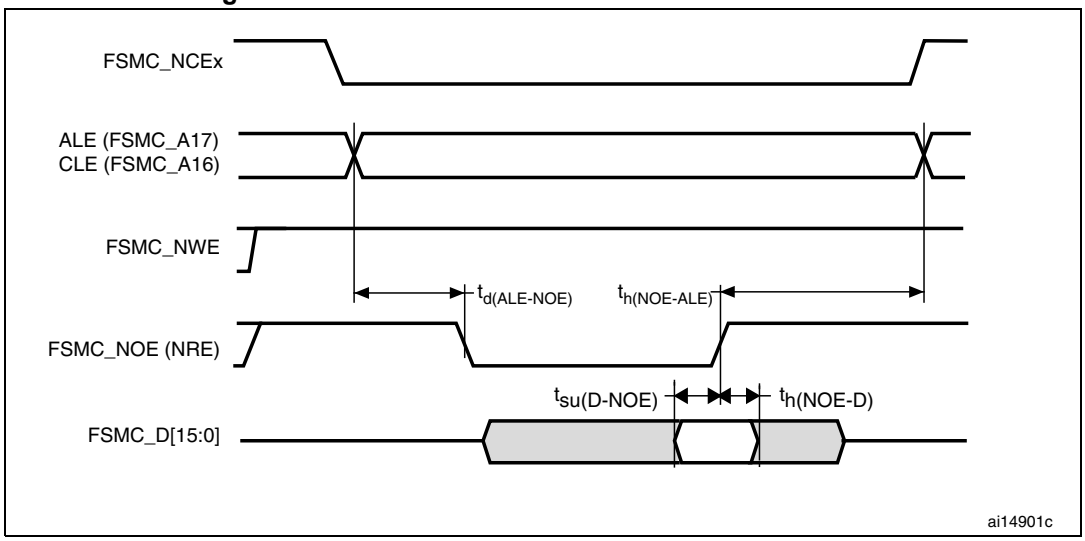


Figure 69. NAND controller waveforms for write access

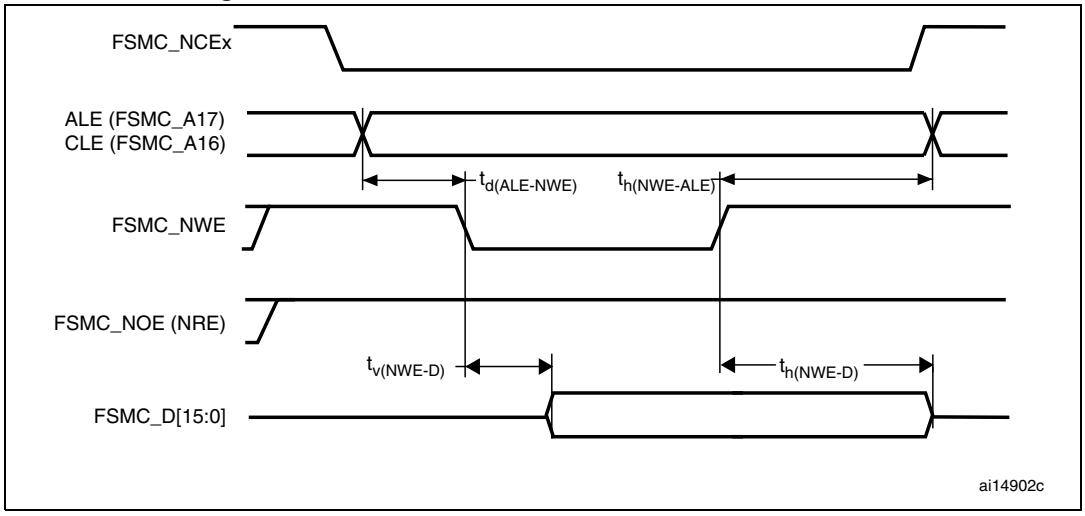


Figure 70. NAND controller waveforms for common memory read access

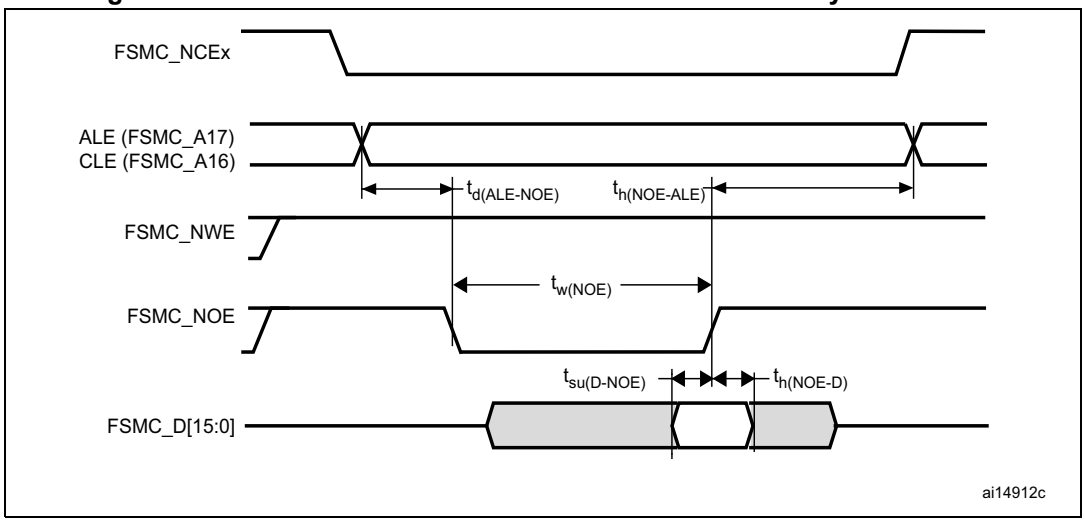


Figure 71. NAND controller waveforms for common memory write access

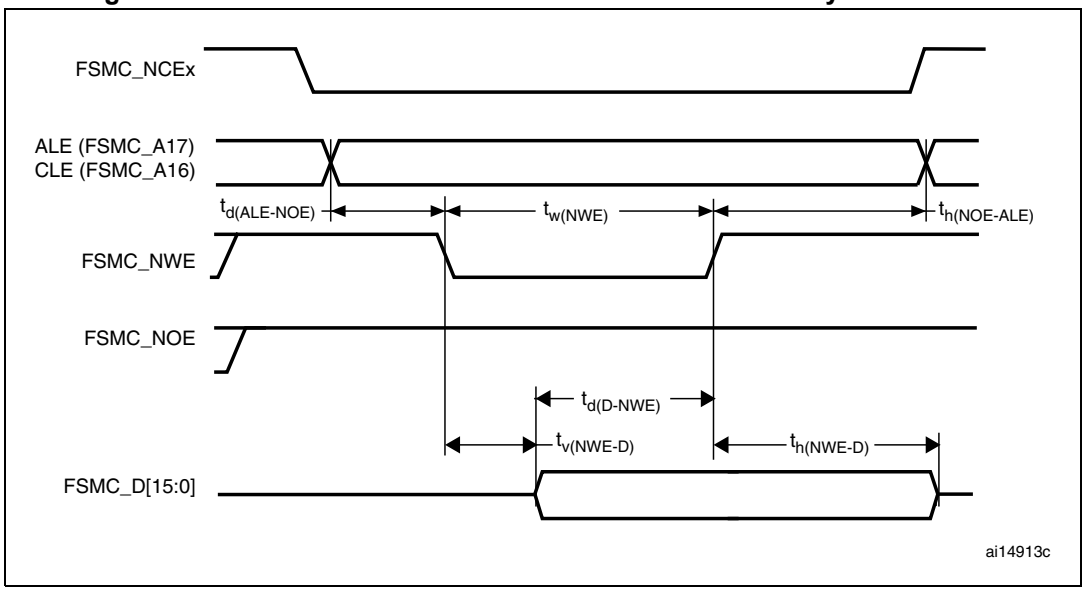


Table 85. Switching characteristics for NAND Flash read cycles(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(N0E)}$	FSMC_NOE low width	$4T_{HCLK}-0.5$	$4T_{HCLK}+3$	ns
$t_{su(D-NOE)}$	FSMC_D[15-0] valid data before FSMC_NOE high	10	-	ns
$t_{h(NOE-D)}$	FSMC_D[15-0] valid data after FSMC_NOE high	0	-	ns
$t_{d(ALE-NOE)}$	FSMC_ALE valid before FSMC_NOE low	-	$3T_{HCLK}$	ns
$t_{h(NOE-ALE)}$	FSMC_NWE high to FSMC_ALE invalid	$3T_{HCLK}-2$	-	ns

1. C_L = 30 pF.

Table 86. Switching characteristics for NAND Flash write cycles(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NWE)}$	FSMC_NWE low width	$4T_{HCLK}-1$	$4T_{HCLK}+3$	ns
$t_{v(NWE-D)}$	FSMC_NWE low to FSMC_D[15-0] valid	-	0	ns
$t_{h(NWE-D)}$	FSMC_NWE high to FSMC_D[15-0] invalid	$3T_{HCLK}-2$	-	ns
$t_{d(D-NWE)}$	FSMC_D[15-0] valid before FSMC_NWE high	$5T_{HCLK}-3$	-	ns
$t_{d(ALE-NWE)}$	FSMC_ALE valid before FSMC_NWE low	-	$3T_{HCLK}$	ns
$t_{h(NWE-ALE)}$	FSMC_NWE high to FSMC_ALE invalid	$3T_{HCLK}-2$	-	ns

1. C_L = 30 pF.

5.3.27 Camera interface (DCMI) timing specifications

Unless otherwise specified, the parameters given in *Table 87* for DCMI are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage summarized in *Table 13*, with the following configuration:

- PCK polarity: falling
- VSYNC and HSYNC polarity: high
- Data format: 14 bits

Figure 72. DCMI timing diagram

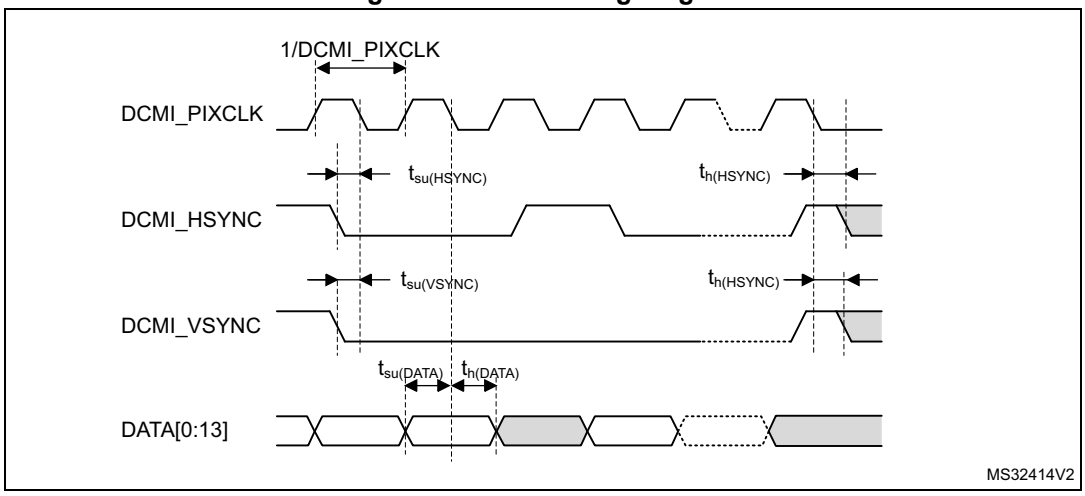


Table 87. DCMI characteristics(1)

Symbol	Parameter	Min	Max	Unit
	Frequency ratio DCMI_PIXCLK/f_{HCLK}	-	0.4	
DCMI_PIXCLK	Pixel clock input	-	54	MHz
D_{pixel}	Pixel clock input duty cycle	30	70	%

Table 87. DCMI characteristics(1) (continued)

Symbol	Parameter	Min	Max	Unit
$t_{su(DATA)}$	Data input setup time	2.5	-	ns
$t_{h(DATA)}$	Data hold time	1	-	
$t_{su(HSYNC)}$, $t_{su(VSYNC)}$	HSYNC/VSYNC input setup time	2	-	
$t_{h(HSYNC)}$, $t_{h(VSYNC)}$	HSYNC/VSYNC input hold time	0.5	-	

1. Guaranteed by characterization results, not tested in production.

5.3.28 SD/SDIO MMC card host interface (SDIO) characteristics

Unless otherwise specified, the parameters given in *Table 88* are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 14* with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 5.3.16: I/O port characteristics* for more details on the input/output characteristics.

Figure 73. SDIO high-speed mode

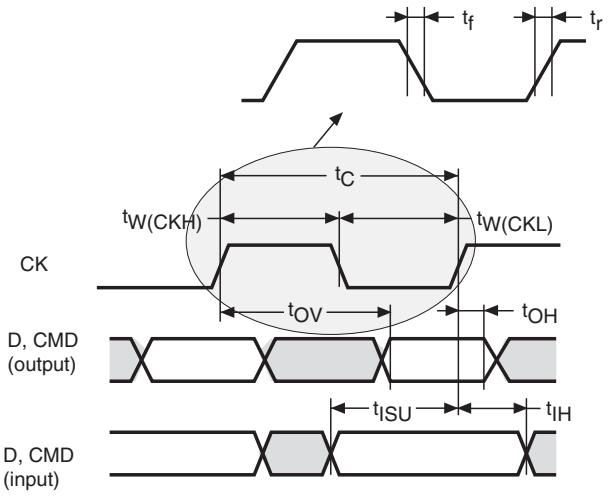


Figure 74. SD default mode

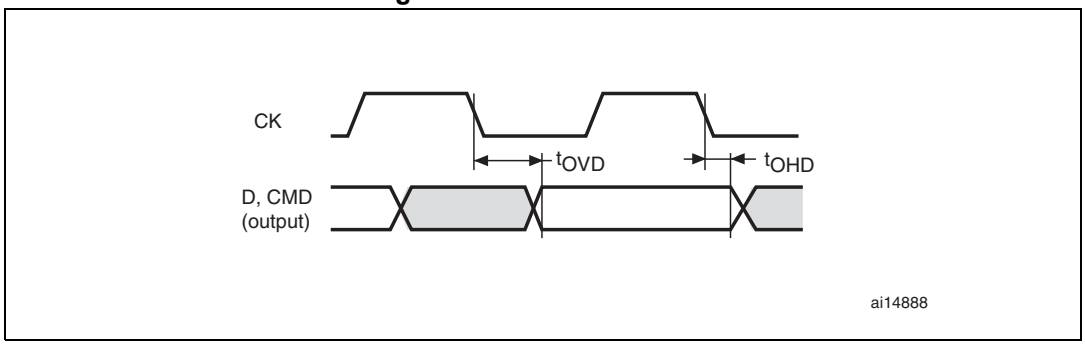


Table 88. Dynamic characteristics: SD / MMC characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode		0		48	MHz
	SDIO_CK/f_{PCLK2} frequency ratio		-	-	8/3	-
$t_{W(CKL)}$	Clock low time	f_{PP} = 48 MHz	8.5	9	-	ns
$t_{W(CKH)}$	Clock high time	f_{PP} = 48 MHz	8.3	10	-	
CMD, D inputs (referenced to CK) in MMC and SD HS mode						
t_{ISU}	Input setup time HS	f_{PP} = 48 MHz	3	-	-	ns
t_{IH}	Input hold time HS	f_{PP} = 48 MHz	0	-	-	
CMD, D outputs (referenced to CK) in MMC and SD HS mode						
t_{OV}	Output valid time HS	f_{PP} = 48 MHz	-	4.5	6	ns
t_{OH}	Output hold time HS	f_{PP} = 48 MHz	1	-	-	
CMD, D inputs (referenced to CK) in SD default mode						
t_{ISUD}	Input setup time SD	f_{PP} = 24 MHz	1.5	-	-	ns
t_{IHD}	Input hold time SD	f_{PP} = 24 MHz	0.5	-	-	
CMD, D outputs (referenced to CK) in SD default mode						
t_{OVD}	Output valid default time SD	f_{PP} = 24 MHz	-	4.5	7	ns
t_{OHD}	Output hold default time SD	f_{PP} = 24 MHz	0.5	-	-	

1. Guaranteed by characterization results, not tested in production.

5.3.29 RTC characteristics

Table 89. RTC characteristics

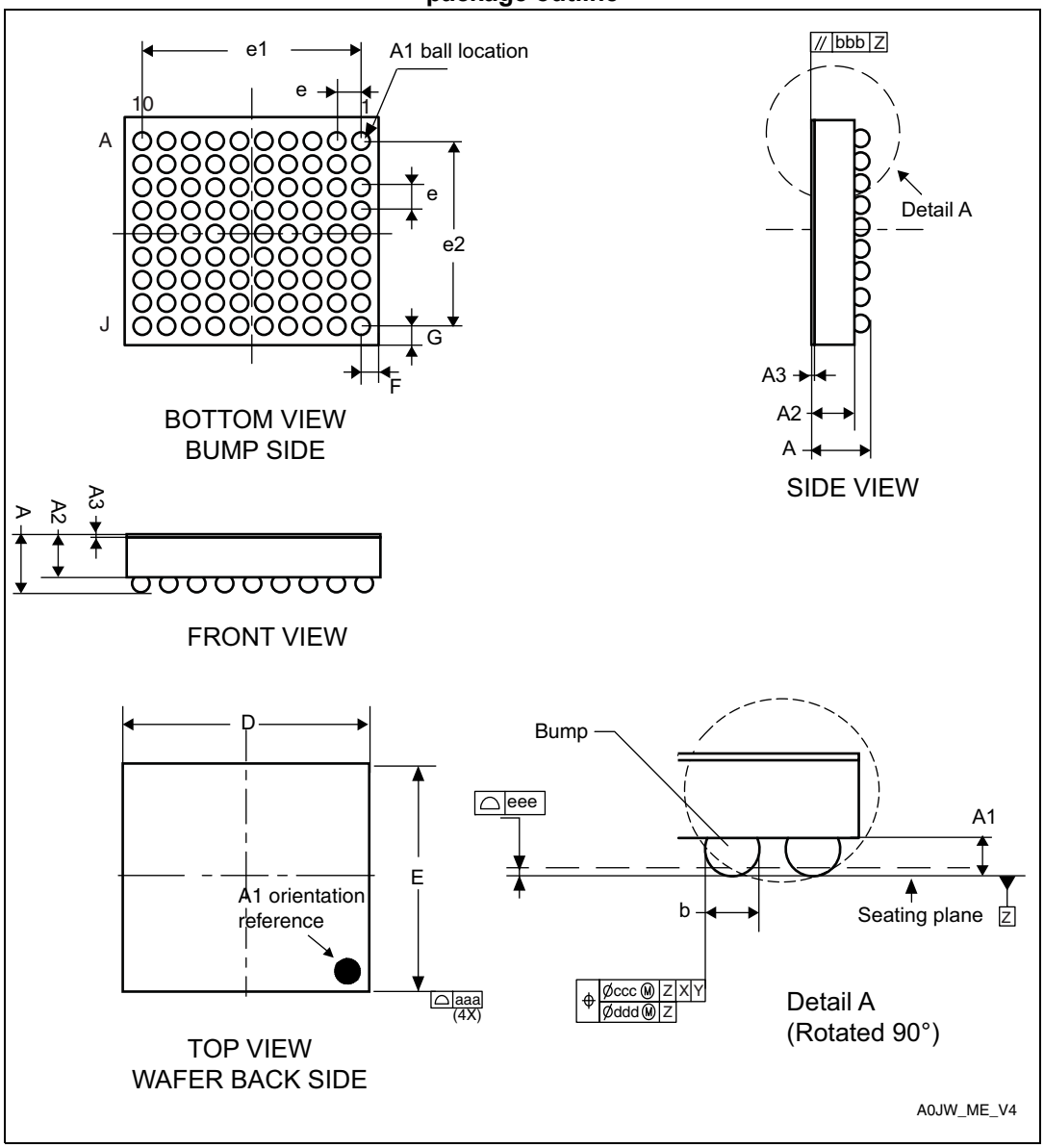
Symbol	Parameter	Conditions	Min	Max
-	f_{PCLK1}/RTCCLK frequency ratio	Any read/write operation from/to an RTC register	4	-

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

6.1 WLCSP90 package information

Figure 75. WLCSP90 - 4.223 x 3.969 mm, 0.400 mm pitch wafer level chip scale package outline



1. Drawing is not to scale.

Table 90. WLCSP90 - 4.223 x 3.969 mm, 0.400 mm pitch wafer level chip scale package mechanical data

Symbol	millimeters			inches[1]		
	Typ	Min	Max	Typ	Min	Max
A	0.540	0.600	0.585	0.0207	0.0219	0.0230
A1	-	0.190	-	-	0.0069	-
A2	-	0.380	-	-	0.0150	-
A3[2]	-	0.025	-	-	0.0010	-
b[3]	0.240	0.270	0.300	0.0087	0.0098	0.0110
D	4.188	4.223	4.258	0.1008	0.1022	0.1036
E	3.934	3.969	4.004	0.1115	0.1129	0.1143
e	-	0.400	-	-	0.0157	-
e1	-	3.600	-	-	0.0787	-
e2	-	3.200	-	-	0.0787	-
F	-	0.3115	-	-	0.0117	-
G	-	0.3845	-	-	0.0171	-
aaa	-	-	0.100	-	-	0.0039
bbb	-	-	0.100	-	-	0.0039
ccc	-	-	0.100	-	-	0.0039
ddd	-	-	0.050	-	-	0.0020
eee	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Back side coating.
3. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

Figure 76. WLCSP90 - 4.223 x 3.969 mm, 0.400 mm pitch wafer level chip scale recommended footprint

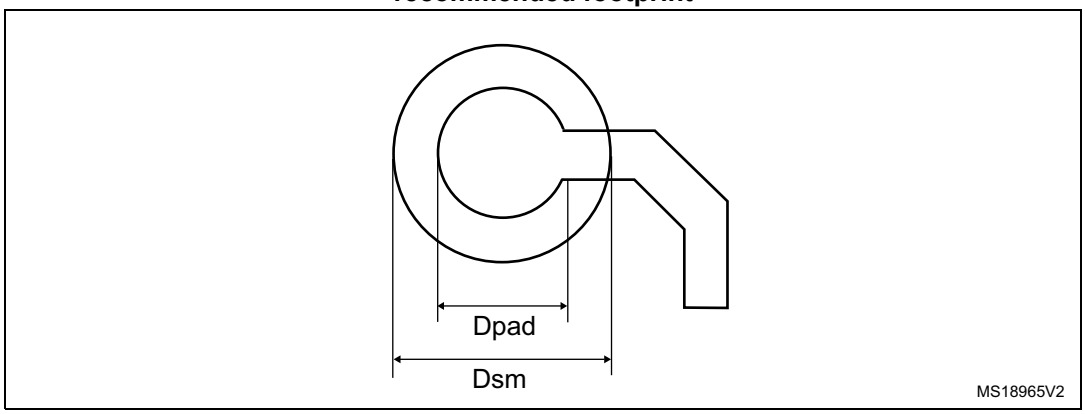


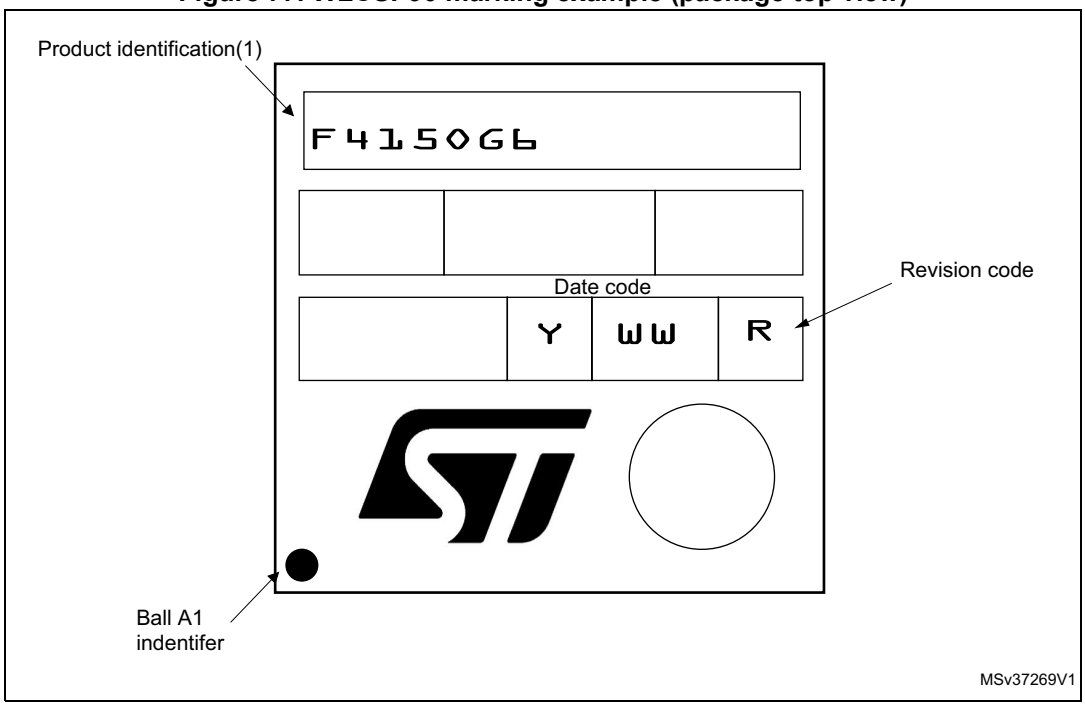
Table 91. WLCSP90 recommended PCB design rules

Dimension	Recommended values
Pitch	0.4 mm
Dpad	260 µm max. (circular) 220 µm recommended
Dsm	300 µm min. (for 260 µm diameter pad)
PCB pad design	Non-solder mask defined via underbump allowed

Device marking for WLCSP90

The following figure gives an example of topside marking and ball A1 position identifier location.

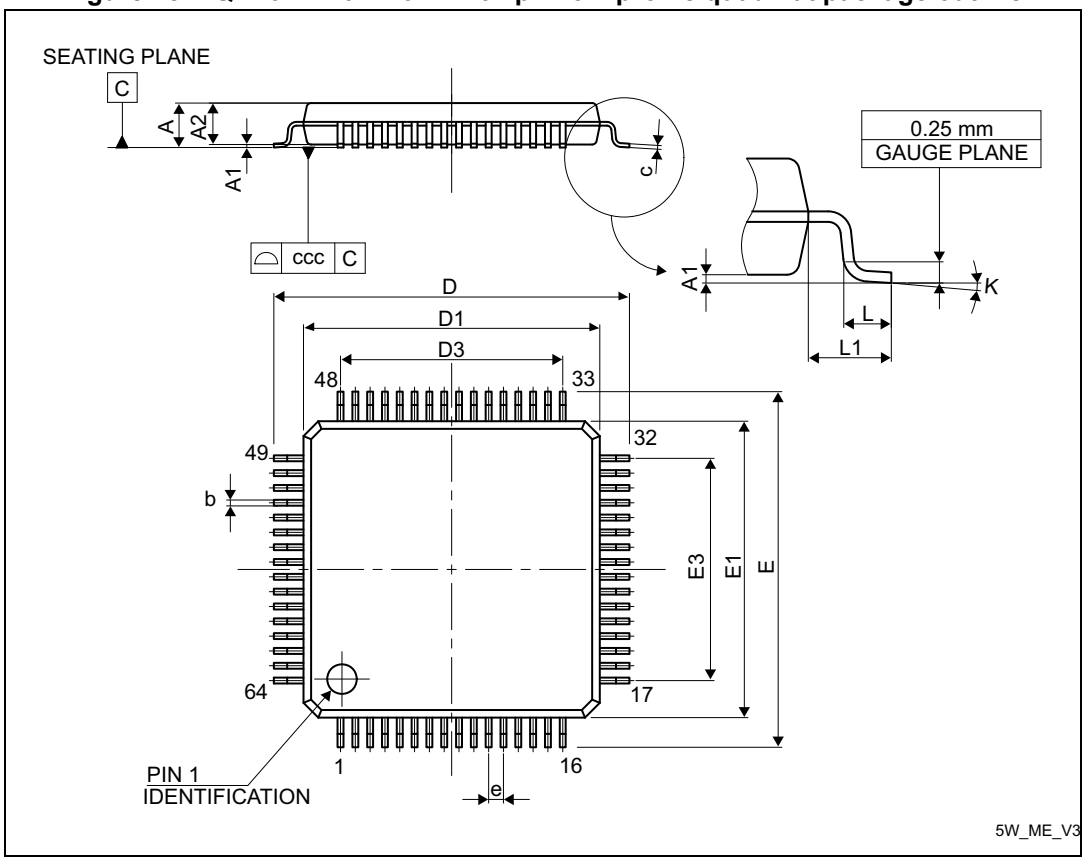
Figure 77. WLCSP90 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

6.2 LQFP64 package information

Figure 78. LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline



1. Drawing is not to scale.

Table 92. LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package mechanical data

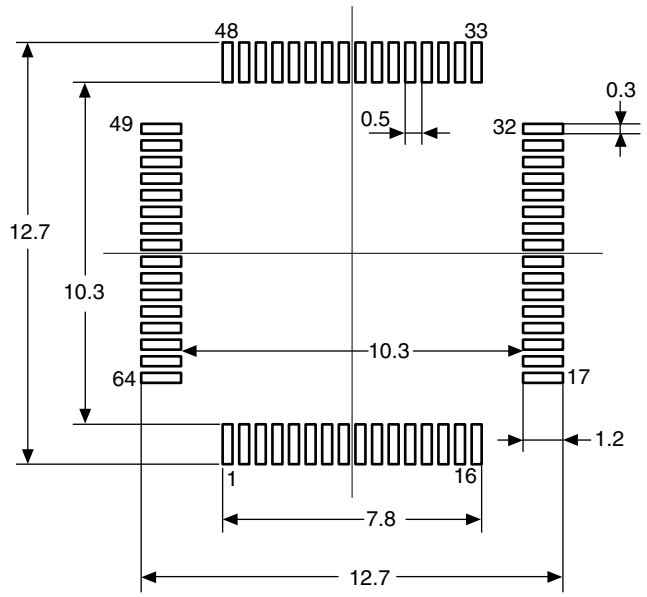
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-

Table 92. LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 79. LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package recommended footprint

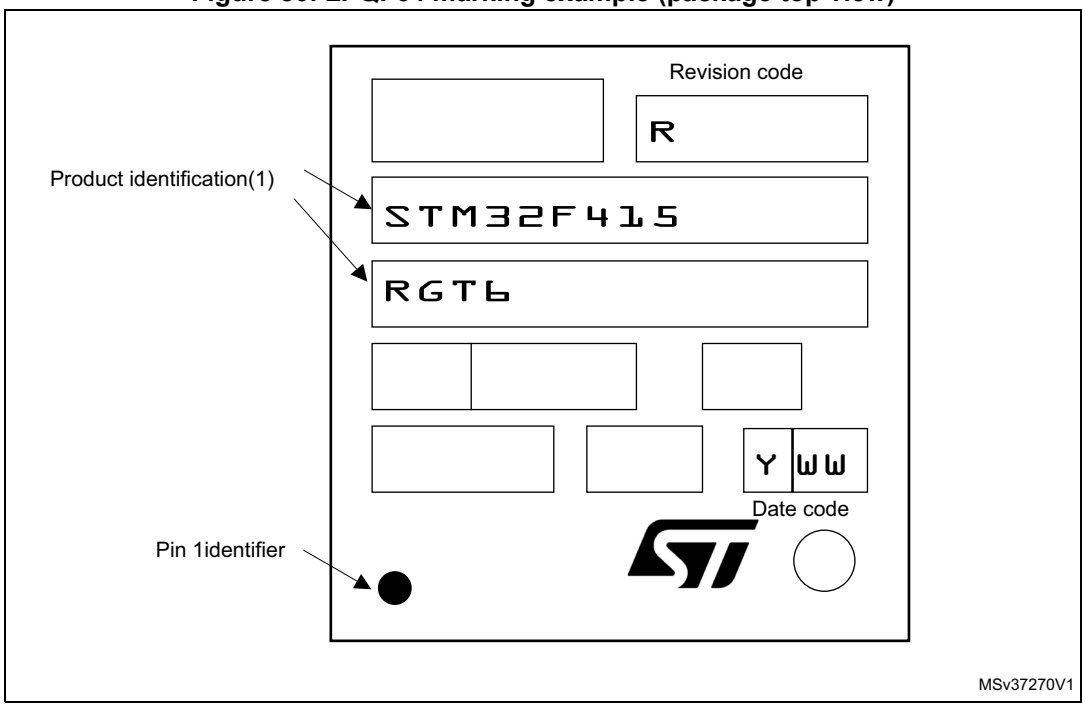


1. Drawing is not to scale.
2. Dimensions are in millimeters.

Device marking for LQFP64

The following figure gives an example of topside marking and pin 1 position identifier location.

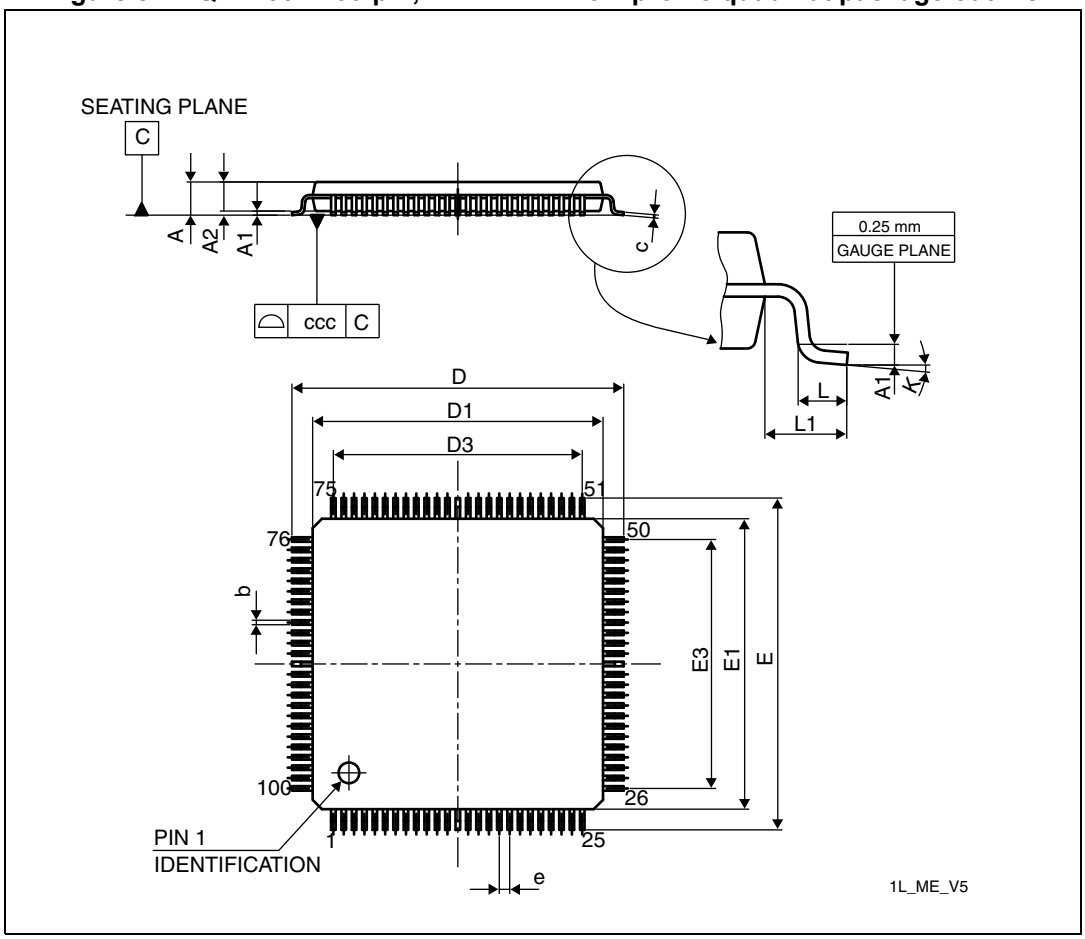
Figure 80. LPQF64 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

6.3 LQPF100 package information

Figure 81. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat package outline



1. Drawing is not to scale.

Table 93. LQPF100 – 100-pin, 14 x 14 mm low-profile quad flat package mechanical data(1)

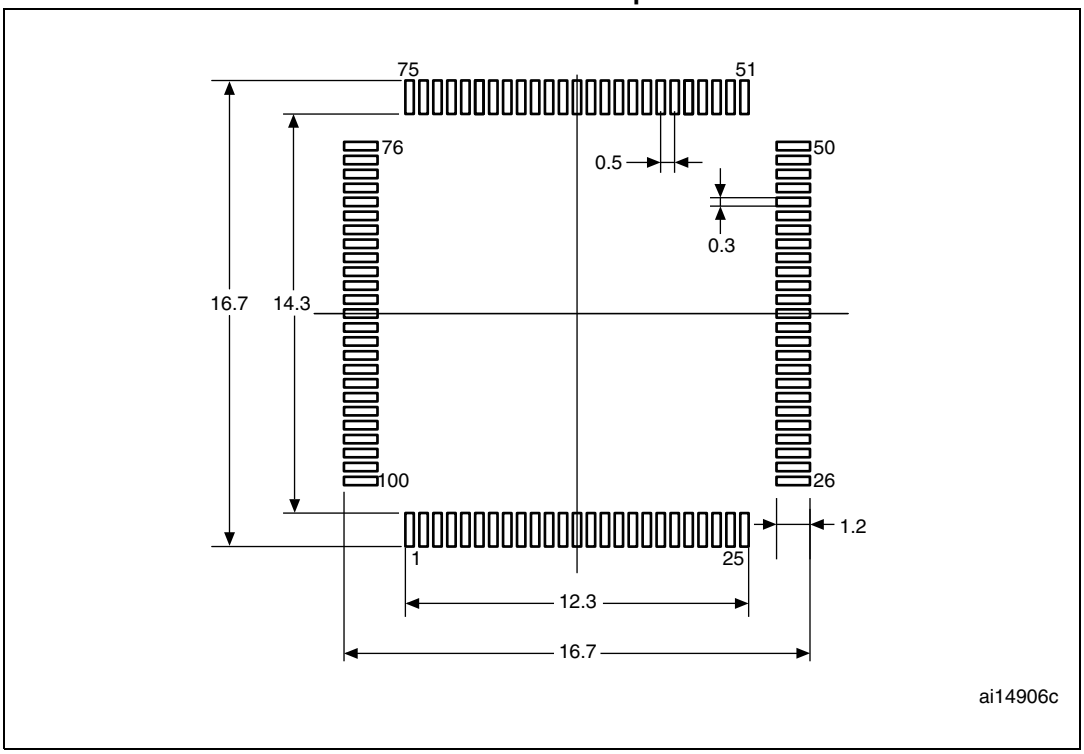
Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
E	15.80	16.000	16.200	0.6220	0.6299	0.6378

Table 93. LQPF100 – 100-pin, 14 x 14 mm low-profile quad flat package mechanical data(1) (continued)

Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 82. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint

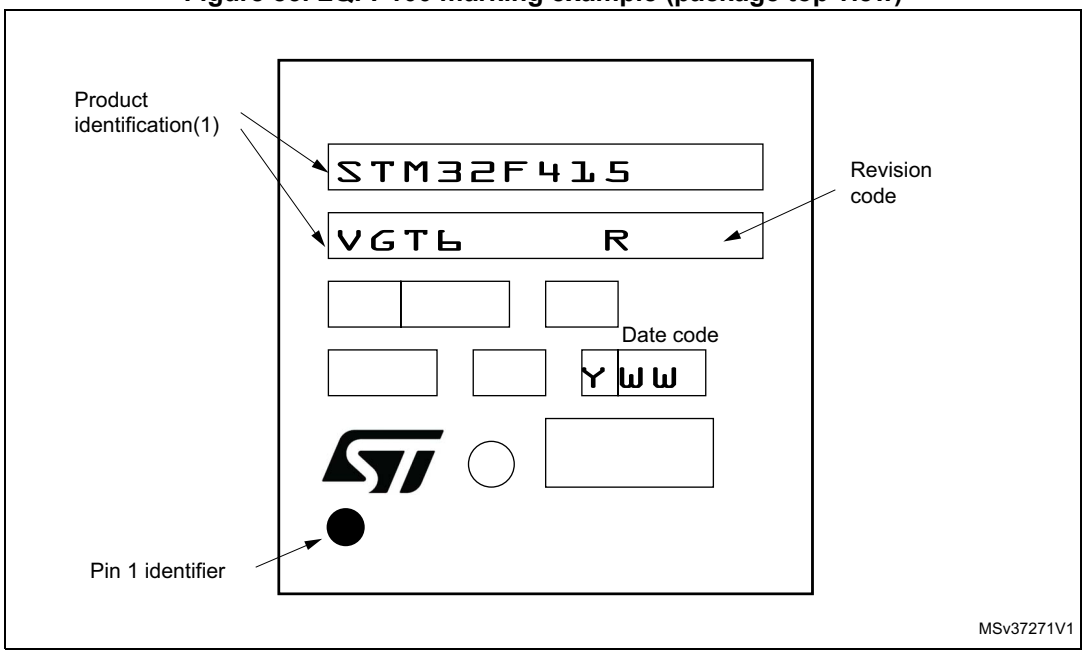


1. Drawing is not to scale.
2. Dimensions are in millimeters.

Device marking for LFP100

The following figure gives an example of topside marking and pin 1 position identifier location.

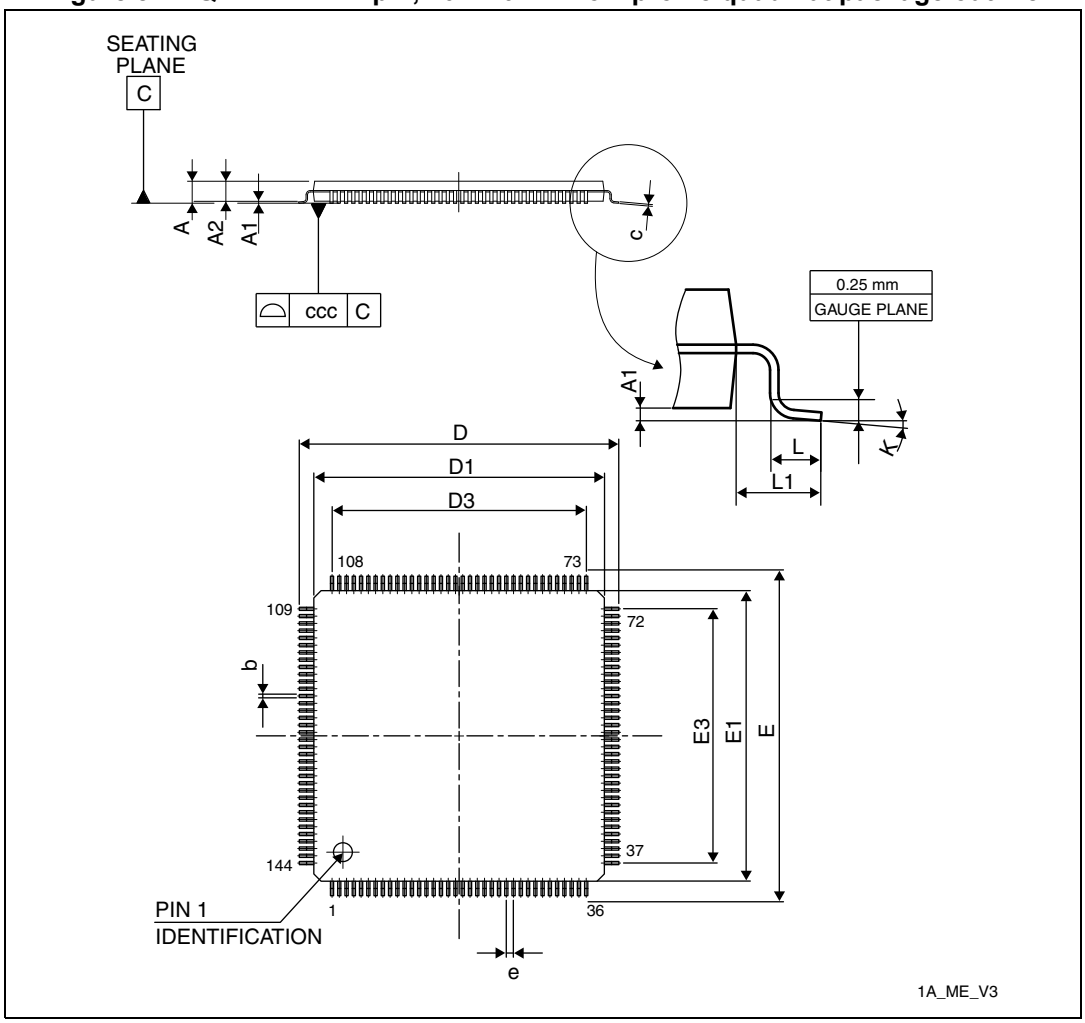
Figure 83. LQFP100 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

6.4 LQFP144 package information

Figure 84. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package outline



1. Drawing is not to scale.

Table 94. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package mechanical data

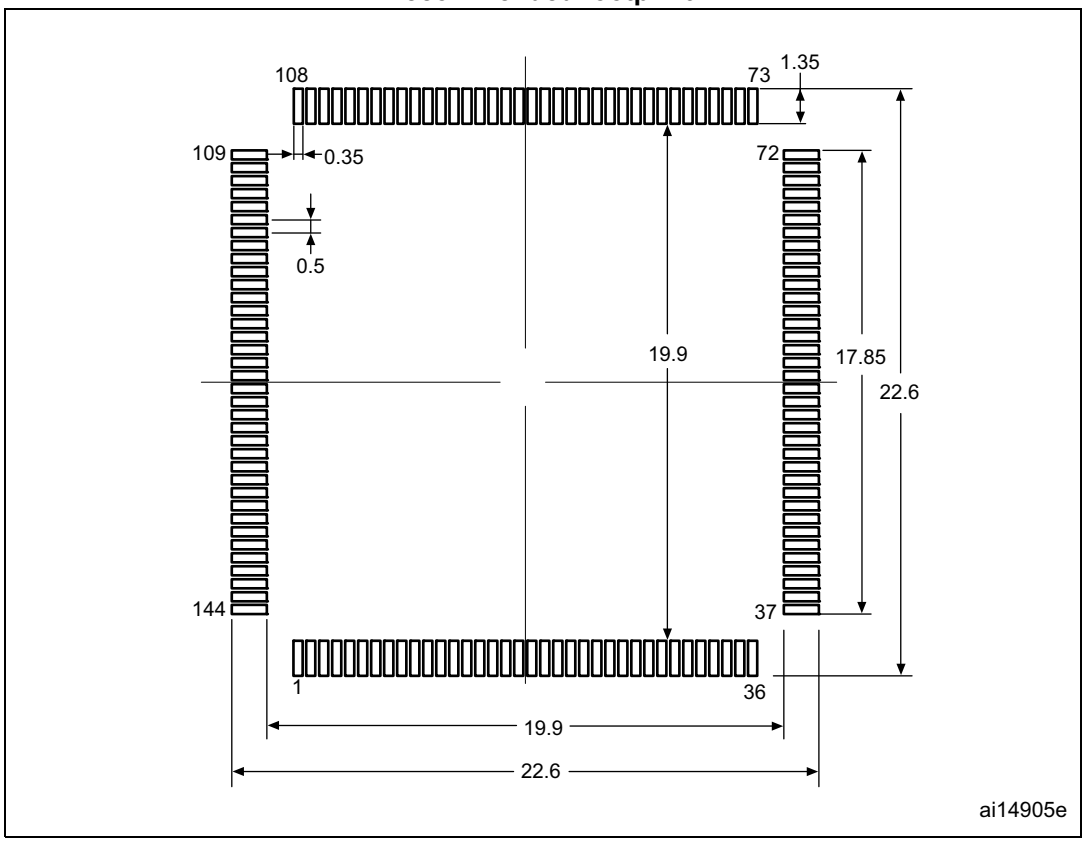
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	21.800	22.000	22.200	0.8583	0.8661	0.874
D1	19.800	20.000	20.200	0.7795	0.7874	0.7953

Table 94. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
D3	-	17.500	-	-	0.689	-
E	21.800	22.000	22.200	0.8583	0.8661	0.8740
E1	19.800	20.000	20.200	0.7795	0.7874	0.7953
E3	-	17.500	-	-	0.6890	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 85. LQFP144 - 144-pin,20 x 20 mm low-profile quad flat package recommended footprint

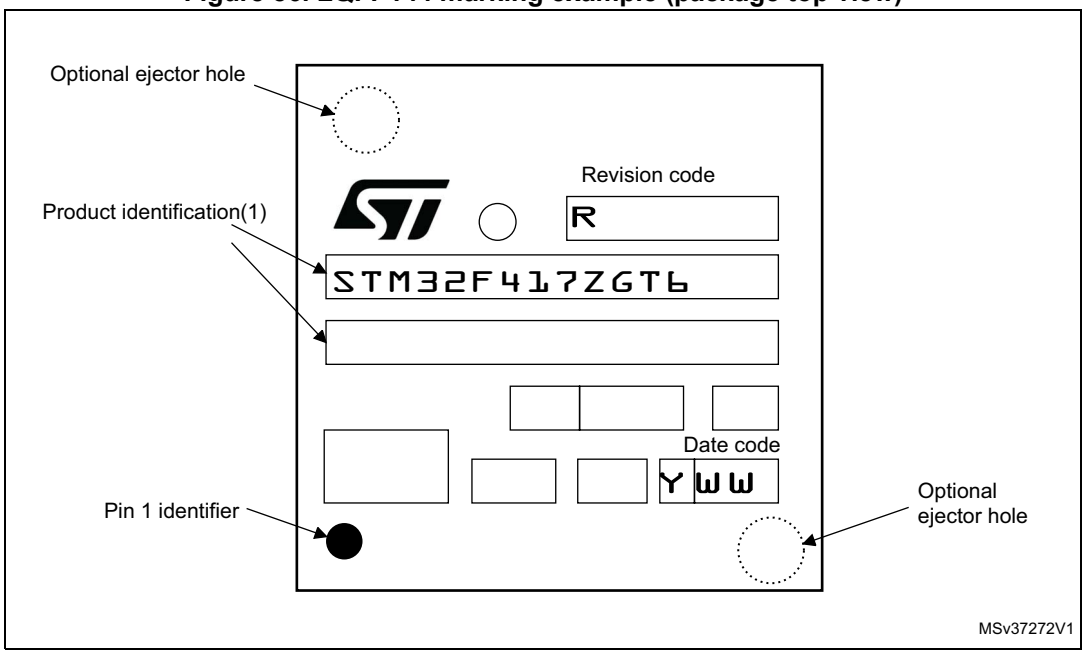


1. Drawing is not to scale.
2. Dimensions are in millimeters.

Device marking for LQPF144

The following figure gives an example of topside marking and pin 1 position identifier location.

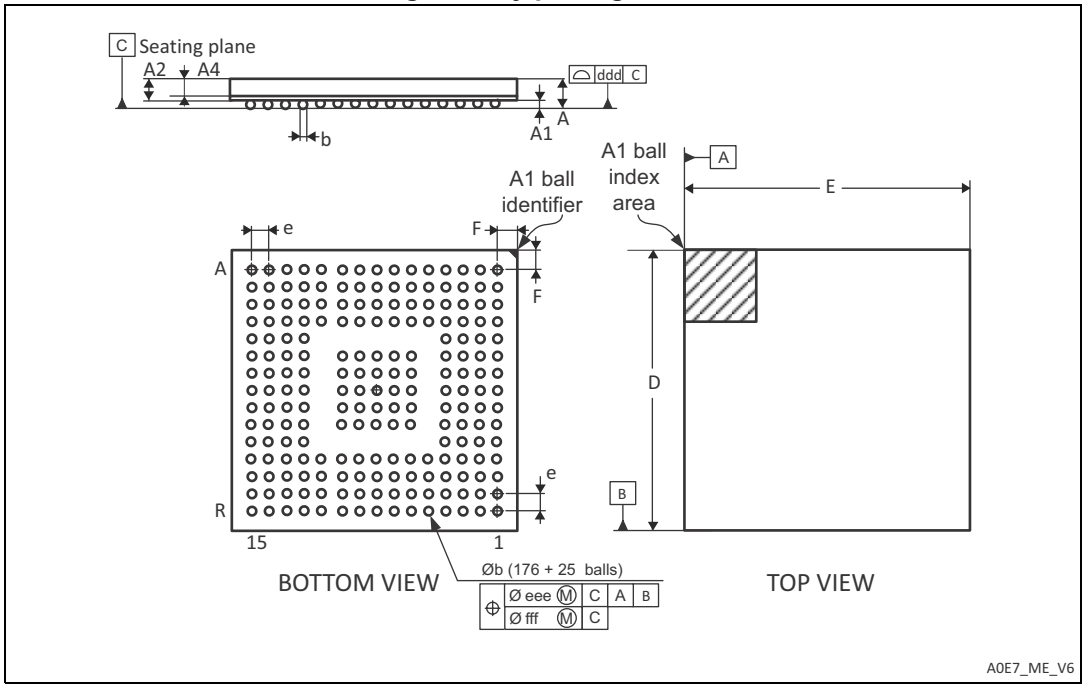
Figure 86. LQFP144 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

6.5 UFBGA176+25 package information

Figure 87. UFBGA176+25 - 201-ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package outline



1. Drawing is not to scale.

Table 95. UFBGA176+25 - 201-ball, 10 × 10 × 0.65 mm pitch, ultra thin fine pitch ball grid array mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.460	0.530	0.600	0.0181	0.0209	0.0236
A1	0.050	0.080	0.110	0.0020	0.0031	0.0043
A2	0.400	0.450	0.500	0.0157	0.0177	0.0197
A4	0.270	0.320	0.370	0.0106	0.0126	0.0146
b	0.230	0.280	0.330	0.0091	0.0110	0.0130
D	9.950	10.000	10.050	0.3917	0.3937	0.3957
E	9.950	10.000	10.050	0.3917	0.3937	0.3957
e	-	0.650	-	-	0.0256	-
F	0.400	0.450	0.500	0.0157	0.0177	0.0197
ddd	-	-	0.080	-	-	0.0031
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 88. UFBGA176+25 - 201-ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array recommended footprint

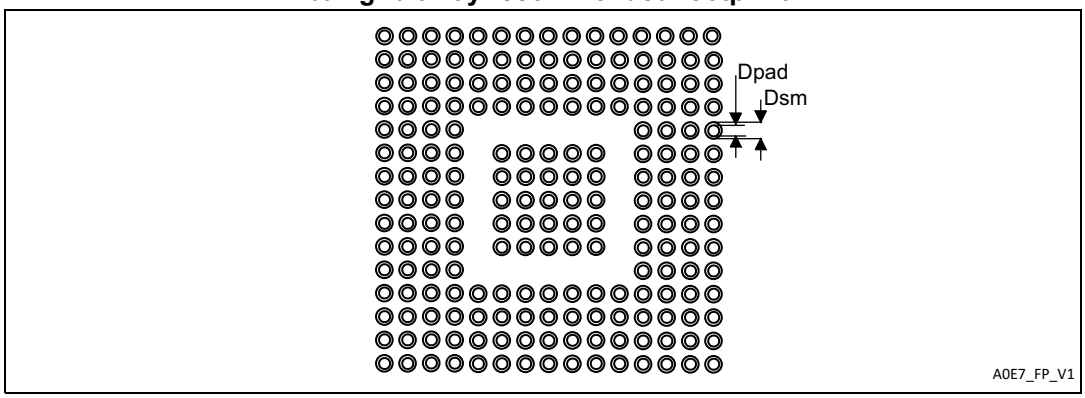


Table 96. UFBGA176+2 recommended PCB design rules (0.65 mm pitch BGA)

Dimension	Recommended values
Pitch	0.65
Dpad	0.300 mm
Dsm	0.400 mm typ. (depends on the soldermask registration tolerance)

Note: Non solder mask defined (NSMD) pads are recommended.

4 to 6 mils solder paste screen printing process.

Stencil opening is 0.300 mm.

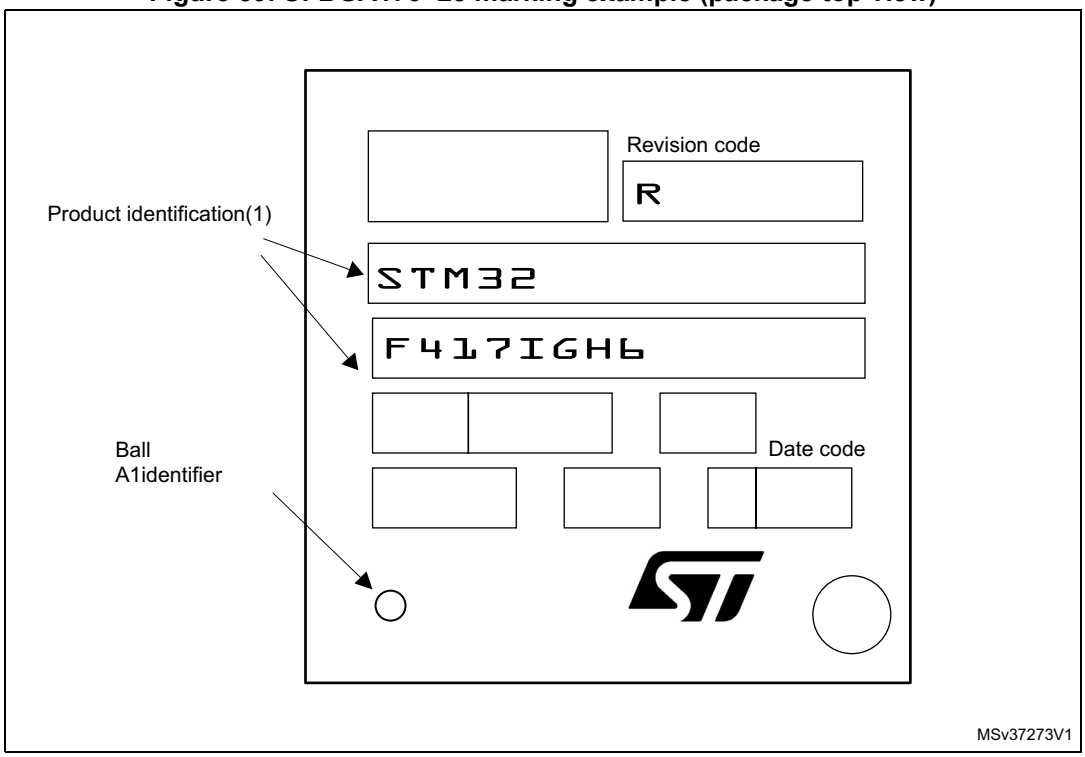
Stencil thickness is between 0.100 mm and 0.125 mm.

Pad trace width is 0.100 mm.

Device marking for UFBGA176+25

The following figure gives an example of topside marking and ball A 1 position identifier location.

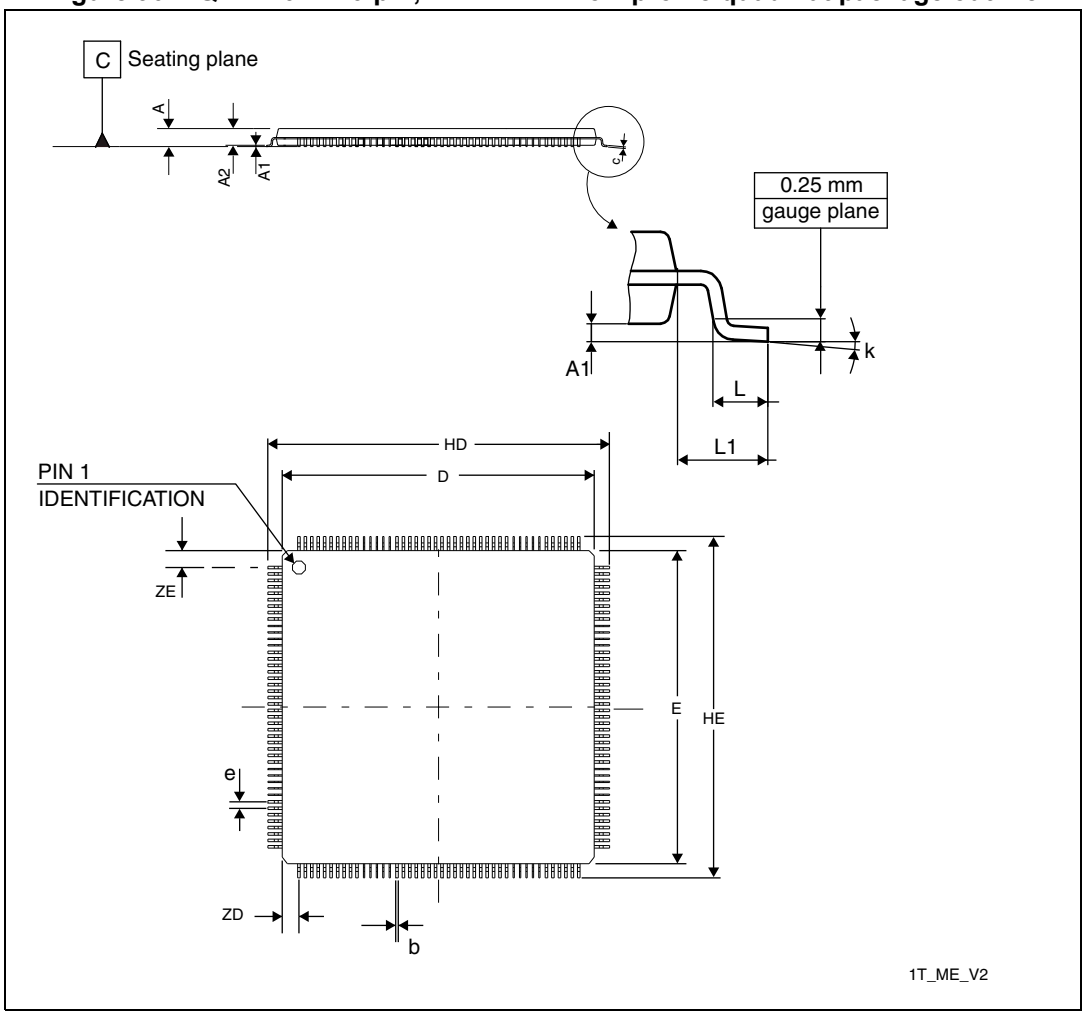
Figure 89. UFBGA176+25 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

6.6 LQFP176 package information

Figure 90. LQFP176 - 176-pin, 24 x 24 mm low profile quad flat package outline



1. Drawing is not to scale.

Table 97. LQFP176 - 176-pin, 24 x 24 mm low profile quad flat package mechanical data

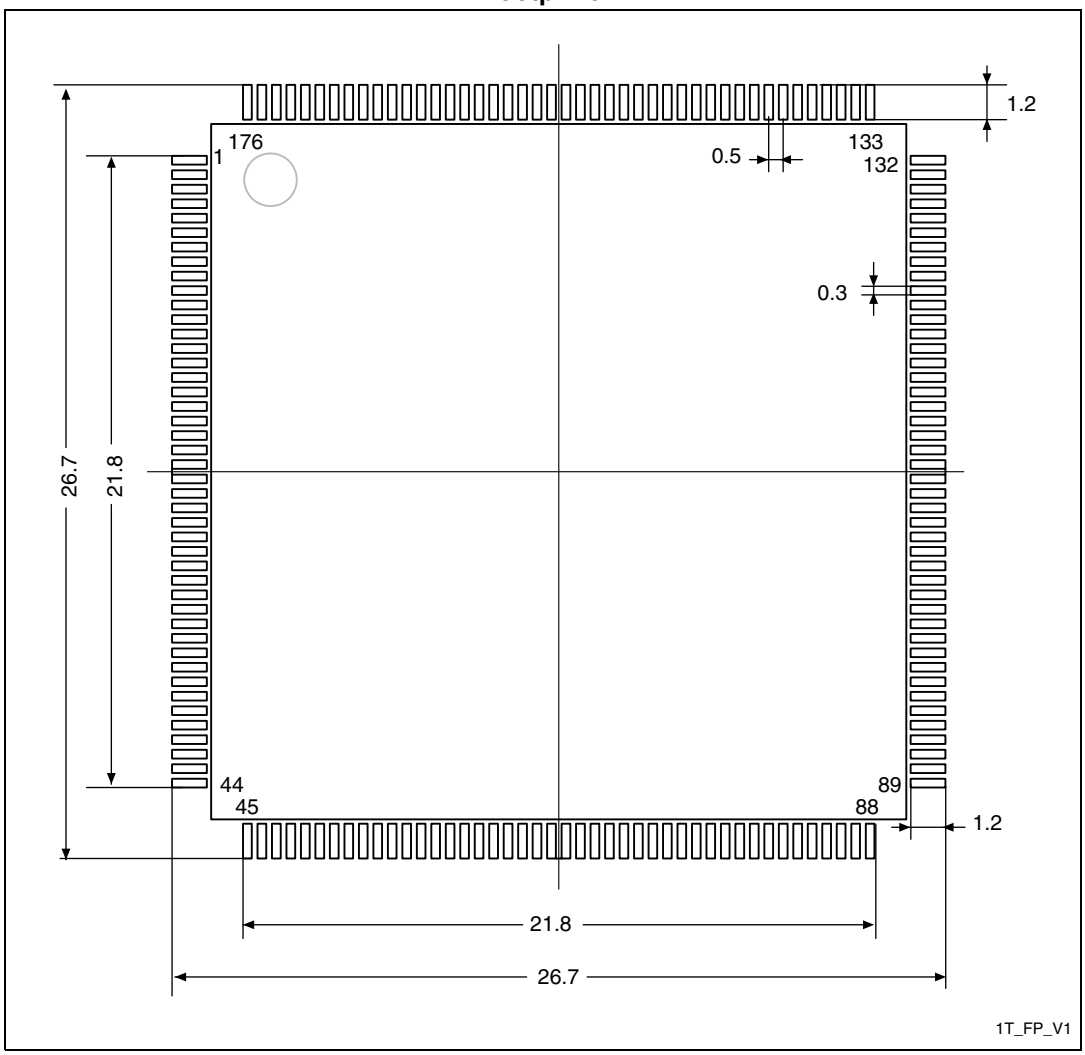
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	-	1.450	0.0531	-	0.0571
b	0.170	-	0.270	0.0067	-	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	23.900	-	24.100	0.9409	-	0.9488
HD	25.900	-	26.100	1.0197	-	1.0276

Table 97. LQFP176 - 176-pin, 24 x 24 mm low profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
ZD	-	1.250	-	-	0.0492	-
E	23.900	-	24.100	0.9409	-	0.9488
HE	25.900	-	26.100	1.0197	-	1.0276
ZE	-	1.250	-	-	0.0492	-
e	-	0.500	-	-	0.0197	-
L[2]	0.450	-	0.750	0.0177	-	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	-	7°	0°	-	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. L dimension is measured at gauge plane at 0.25 mm above the seating plane.

Figure 91. LQFP176 - 176-pin, 24 x 24 mm low profile quad flat recommended footprint

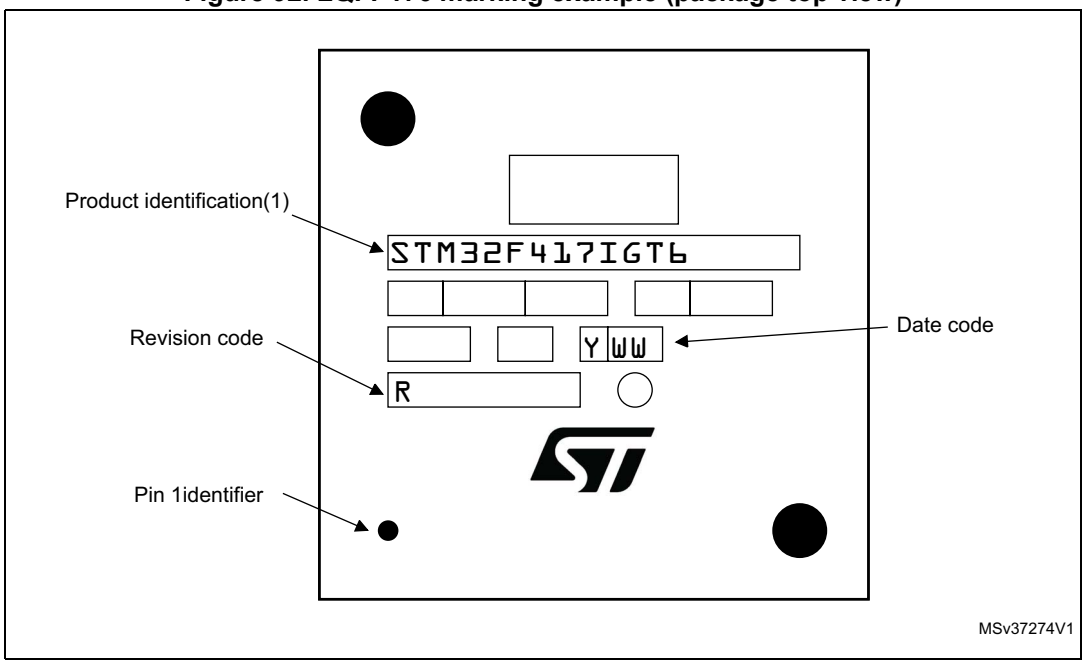


1. Dimensions are expressed in millimeters.

Device marking for LQFP176

The following figure gives an example of topside marking and pin 1 position identifier location.

Figure 92. LQFP176 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

6.7 Thermal characteristics

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

T_J max = T_A max + (P_D max x Θ_{JA})

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$P_{I/O}$ max = Σ (V_{OL} × I_{OL}) + Σ((V_{DD} – V_{OH}) × I_{OH}),

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 98. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LQFP64 - 10 × 10 mm / 0.5 mm pitch	46	°C/W
	Thermal resistance junction-ambient LQFP100 - 14 × 14 mm / 0.5 mm pitch	43	
	Thermal resistance junction-ambient LQFP144 - 20 × 20 mm / 0.5 mm pitch	40	
	Thermal resistance junction-ambient LQFP176 - 24 × 24 mm / 0.5 mm pitch	38	
	Thermal resistance junction-ambient UFBGA176 - 10× 10 mm / 0.65 mm pitch	39	
	Thermal resistance junction-ambient WLCSP90 - 0.400 mm pitch	38.1	

Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.

7 Part numbering

Table 99. Ordering information scheme

Example: STM32 F 415 R E T 6 xxx

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

F = general-purpose

Device subfamily

415 = STM32F41xxx, connectivity, cryptographic acceleration

417= STM32F41xxx, connectivity, camera interface, Ethernet cryptographic acceleration

Pin count

R = 64 pins

O = 90 pins

V = 100 pins

Z = 144 pins

I = 176 pins

Flash memory size

E = 512 Kbytes of Flash memory

G = 1024 Kbytes of Flash memory

Package

T = LQFP

H = UFBGA

Y = WLCSP

Temperature range

6 = Industrial temperature range, –40 to 85 °C.

7 = Industrial temperature range, –40 to 105 °C.

Options

xxx = programmed parts

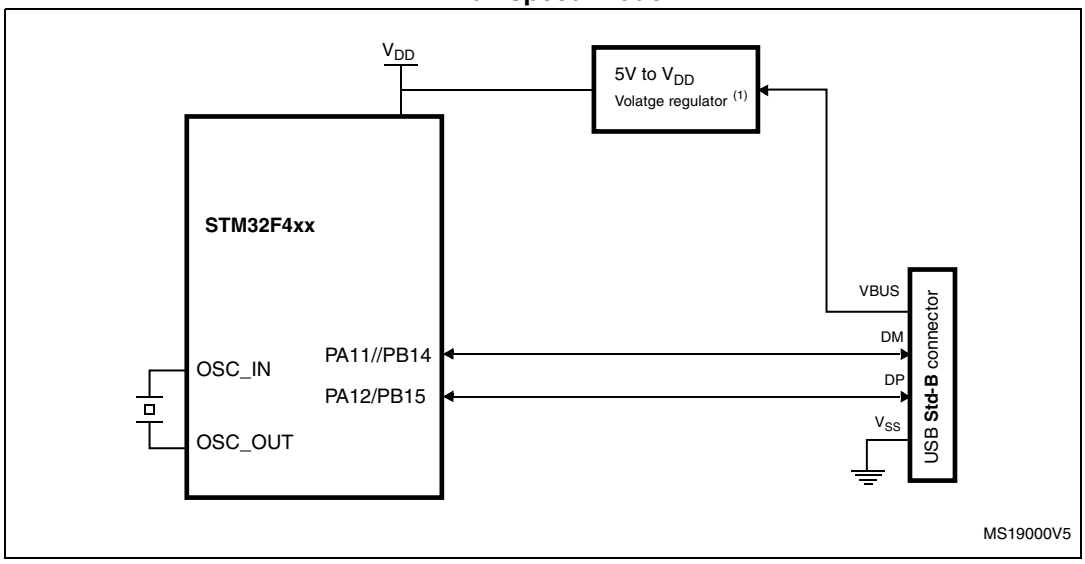
TR = tape and reel

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

Appendix A Application block diagrams

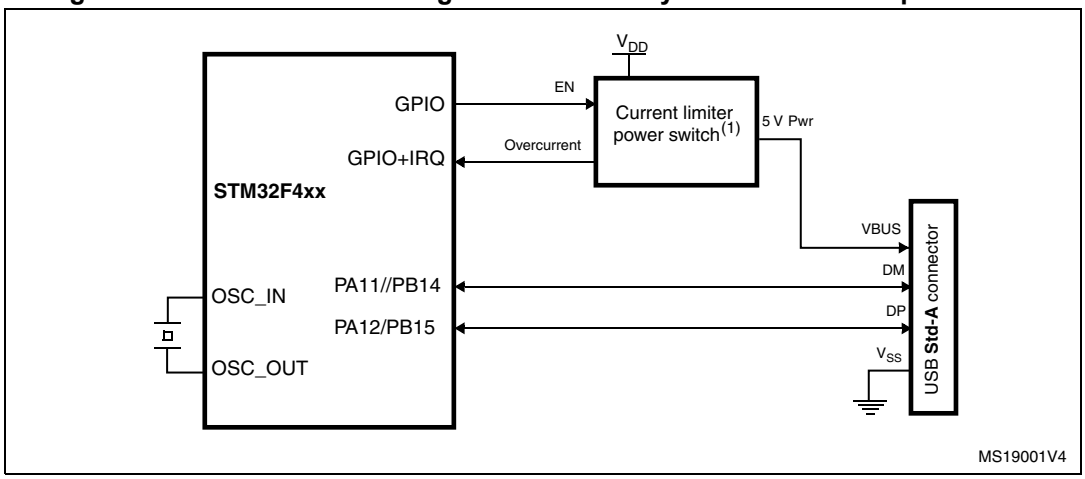
A.1 USB OTG full speed (FS) interface solutions

Figure 93. USB controller configured as peripheral-only and used in Full speed mode



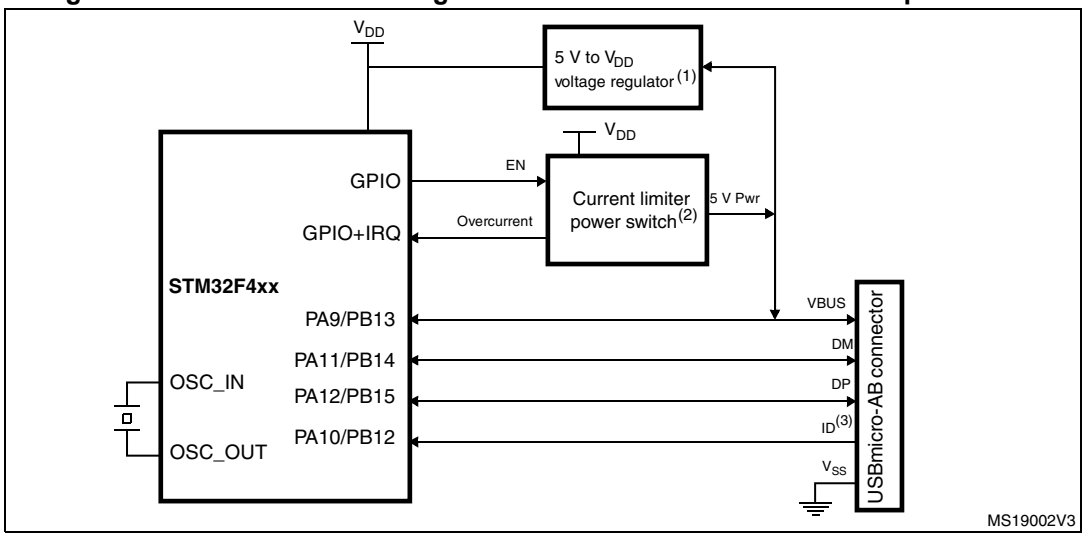
1. External voltage regulator only needed when building a V_{BUS} powered device.
2. The same application can be developed using the OTG HS in FS mode to achieve enhanced performance thanks to the large Rx/Tx FIFO and to a dedicated DMA controller.

Figure 94. USB controller configured as host-only and used in full speed mode



1. The current limiter is required only if the application has to support a V_{BUS} powered device. A basic power switch can be used if 5 V are available on the application board.
2. The same application can be developed using the OTG HS in FS mode to achieve enhanced performance thanks to the large Rx/Tx FIFO and to a dedicated DMA controller.

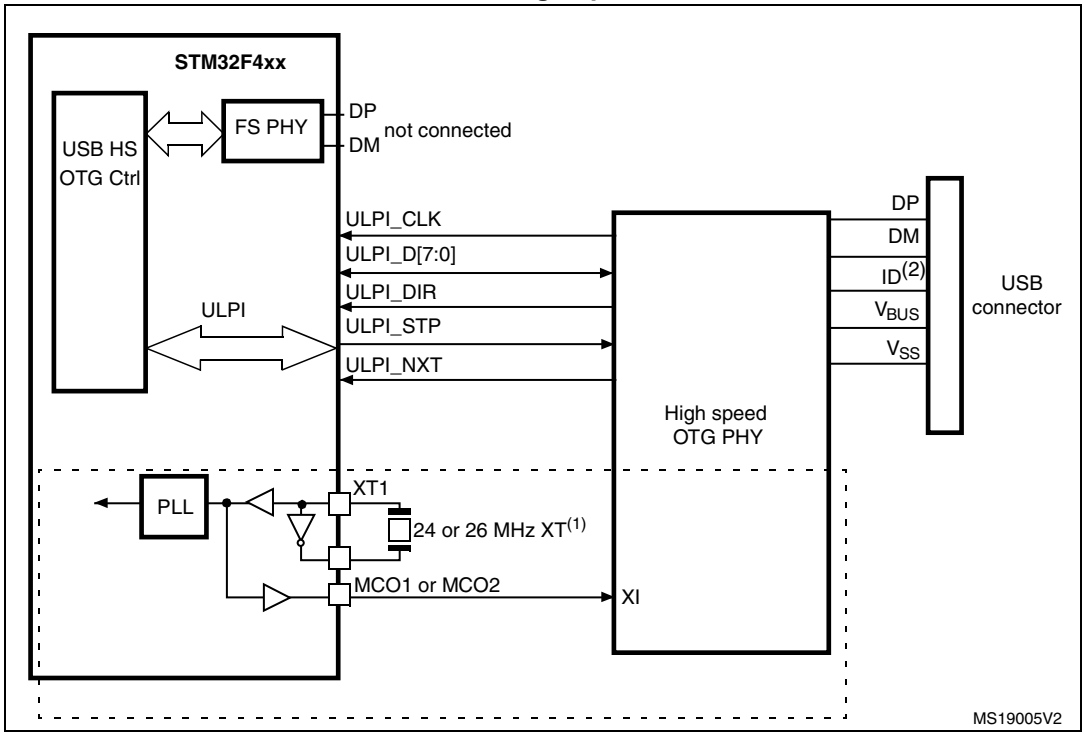
Figure 95. USB controller configured in dual mode and used in full speed mode



1. External voltage regulator only needed when building a V_{BUS} powered device.
2. The current limiter is required only if the application has to support a V_{BUS} powered device. A basic power switch can be used if 5 V are available on the application board.
3. The ID pin is required in dual role only.
4. The same application can be developed using the OTG HS in FS mode to achieve enhanced performance thanks to the large Rx/Tx FIFO and to a dedicated DMA controller.

A.2 USB OTG high speed (HS) interface solutions

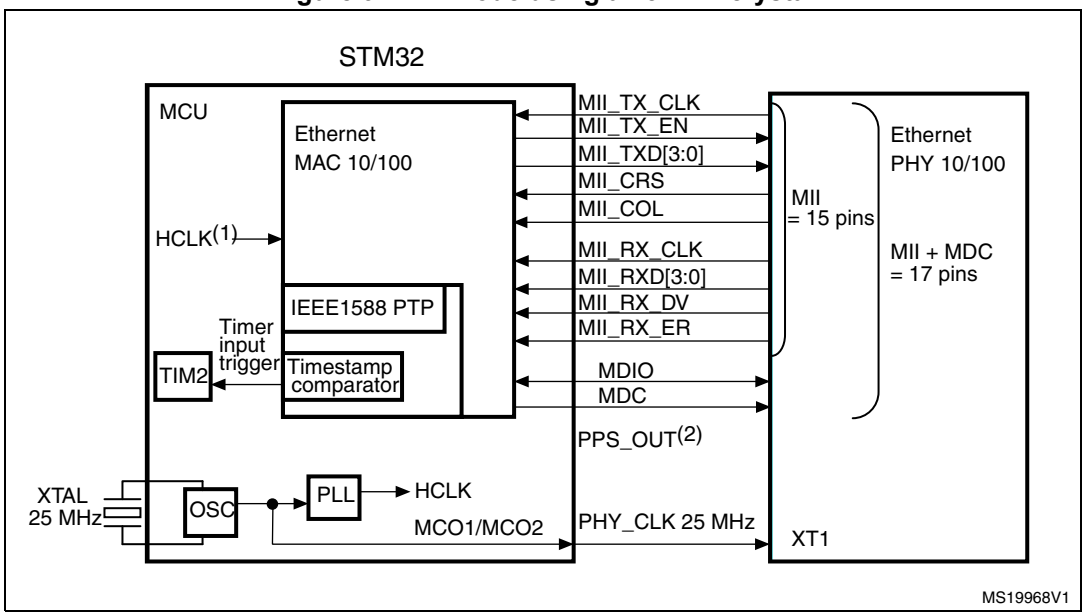
Figure 96. USB controller configured as peripheral, host, or dual-mode and used in high speed mode



1. It is possible to use MCO1 or MCO2 to save a crystal. It is however not mandatory to clock the STM32F41xxx with a 24 or 26 MHz crystal when using USB HS. The above figure only shows an example of a possible connection.
2. The ID pin is required in dual role only.

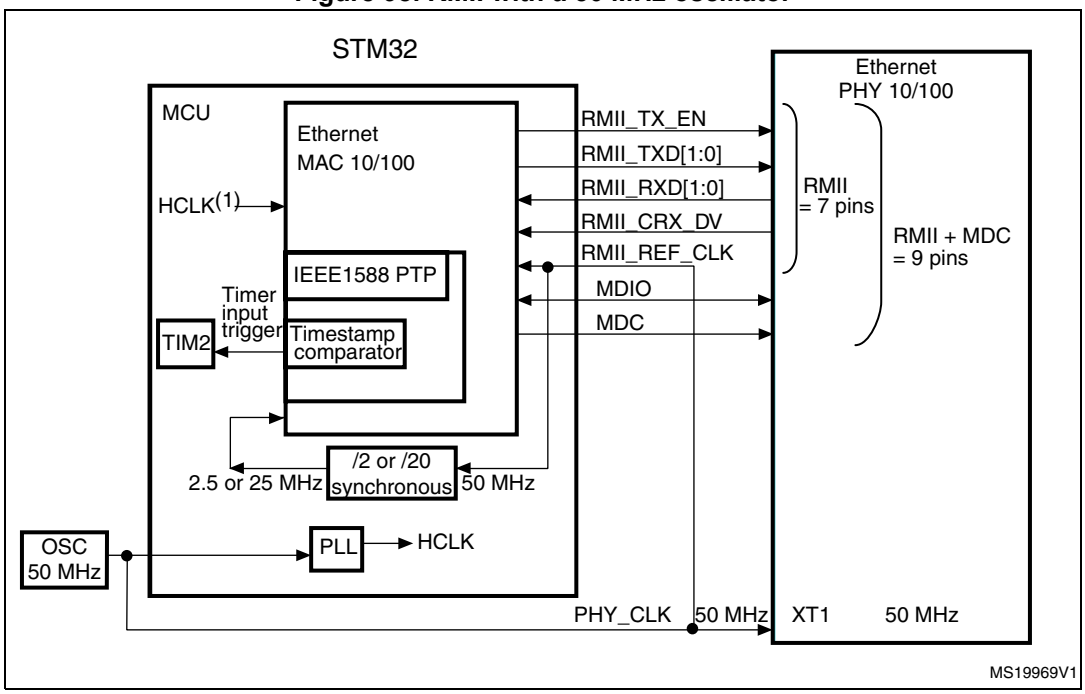
A.3 Ethernet interface solutions

Figure 97. MII mode using a 25 MHz crystal



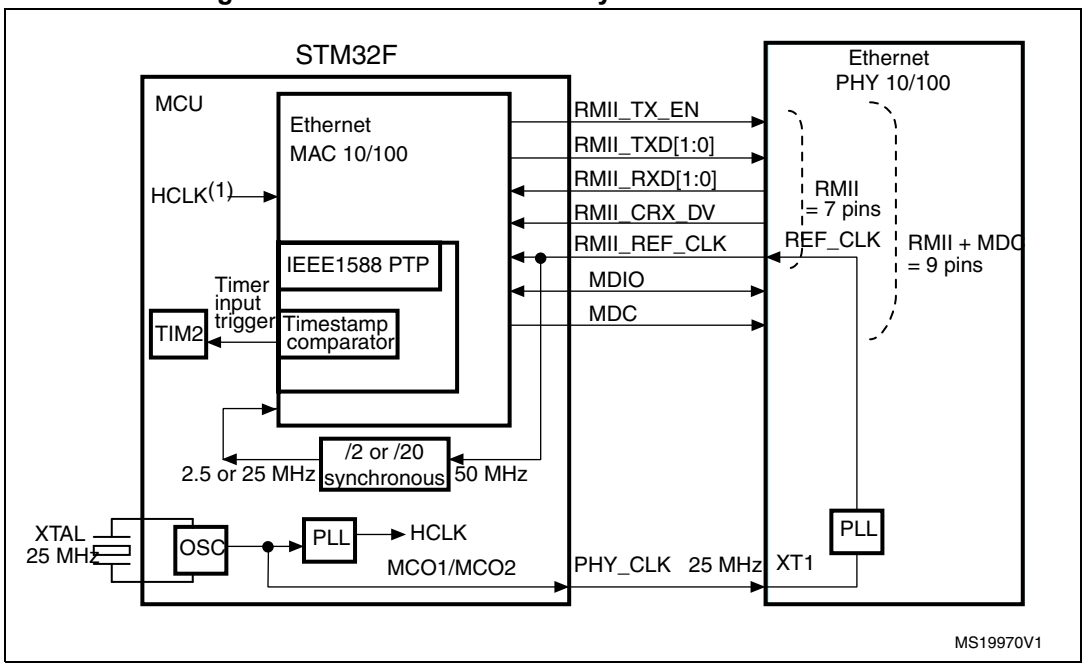
1. f_{HCLK} must be greater than 25 MHz.
2. Pulse per second when using IEEE1588 PTP optional signal.

Figure 98. RMII with a 50 MHz oscillator



1. f_{HCLK} must be greater than 25 MHz.

Figure 99. RMII with a 25 MHz crystal and PHY with PLL



1. f_{HCLK} must be greater than 25 MHz.
2. The 25 MHz (PHY_CLK) must be derived directly from the HSE oscillator, before the PLL block.

8 Revision history

Table 100. Document revision history

Date	Revision	Changes
15-Sep-2011	1	Initial release.
24-Jan-2012	2	Added WLCSP90 package on cover page. Renamed USART4 and USART5 into UART4 and UART5, respectively. Updated number of USB OTG HS and FS in *Table 2: STM32F415xx and STM32F417xx: features and peripheral counts*. Updated *Figure 3: Compatible board design between STM32F10xx/STM32F2/STM32F41xxx for LQFP144 package* and *Figure 4: Compatible board design between STM32F2 and STM32F41xxx for LQFP176 and BGA176 packages*, and removed note 1 and 2. Updated *Section 2.2.9: Flexible static memory controller (FSMC)*. Modified I/Os used to reprogram the Flash memory for CAN2 and USB OTG FS in *Section 2.2.13: Boot modes*. Updated note in *Section 2.2.14: Power supply schemes*. PDR_ON no more available on LQFP100 package. Updated *Section 2.2.16: Voltage regulator*. Updated condition to obtain a minimum supply voltage of 1.7 V in the whole document. Renamed USART4/5 to UART4/5 and added LIN and IrDA feature for UART4 and UART5 in *Table 5: USART feature comparison*. Removed support of I2C for OTG PHY in *Section 2.2.30: Universal serial bus on-the-go full-speed (OTG_FS)*. Added *Table 6: Legend/abbreviations used in the pinout table*. *Table 7: STM32F41xxx pin and ball definitions*: replaced V_{SS}_3, V_{SS}_4, and V_{SS}_8 by V_{SS}; reformatted *Table 7: STM32F41xxx pin and ball definitions* to better highlight I/O structure, and alternate functions versus additional functions; signal corresponding to LQFP100 pin 99 changed from PDR_ON to V_{SS}; EVENTOUT added in the list of alternate functions for all I/Os; ADC3_IN8 added as alternate function for PF10; FSMC_CLE and FSMC_ALE added as alternate functions for PD11 and PD12, respectively; PH10 alternate function TIM15_CH1_ETR renamed TIM5_CH1; updated PA4 and PA5 I/O structure to TTa. Removed OTG_HS_SCL, OTG_HS_SDA, OTG_FS_INTN in *Table 7: STM32F41xxx pin and ball definitions* and *Table 9: Alternate function mapping*. Changed TCM data RAM to CCM data RAM in *Figure 18: STM32F41xxx memory map*. Added I_{VDD} and I_{VSS} maximum values in *Table 12: Current characteristics*. Added *Note 1* related to f_{HCLK}, updated *Note 2* in *Table 14: General operating conditions*, and added maximum power dissipation values. Updated *Table 15: Limitations depending on the operating power supply range*.

Table 100. Document revision history (continued)

Date	Revision	Changes
24-Jan-2012	2 (continued)	Added V_{12} in *Table 19: Embedded reset and power control block characteristics*. Updated *Table 21: Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator disabled)* and *Table 20: Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator enabled) or RAM*. Added *Figure* , *Figure 25*, *Figure 26*, and *Figure 27*. Updated *Table 22: Typical and maximum current consumption in Sleep mode* and removed Note 1. Updated *Table 23: Typical and maximum current consumptions in Stop mode* and *Table 24: Typical and maximum current consumptions in Standby mode*, *Table 25: Typical and maximum current consumptions in VBAT mode*, and *Table 27: Switching output I/O current consumption*. *Section : On-chip peripheral current consumption*: modified conditions, and updated *Table 28: Peripheral current consumption* and *Note 2*. Changed f_{HSE_ext} to 50 MHz and $t_{r(HSE)}/t_{f(HSE)}$ maximum value in *Table 30: High-speed external user clock characteristics*. Added $C_{in(LSE)}$ in *Table 31: Low-speed external user clock characteristics*. Updated maximum PLL input clock frequency, removed related note, and deleted jitter for MCO for RMII Ethernet typical value in *Table 36: Main PLL characteristics*. Updated maximum PLLI2S input clock frequency and removed related note in *Table 37: PLLI2S (audio PLL) characteristics*. Updated *Section : Flash memory* to specify that the devices are shipped to customers with the Flash memory erased. Updated *Table 39: Flash memory characteristics*, and added t_{ME} in *Table 40: Flash memory programming*. Updated *Table 43: EMS characteristics*, and *Table 44: EMI characteristics*. Updated *Table 56: I2S dynamic characteristics* Updated *Figure 45: ULPI timing diagram* and *Table 62: ULPI timing*. Added $t_{COUNTER}$ and t_{MAX_COUNT} in *Table 52: Characteristics of TIMx connected to the APB1 domain* and *Table 53: Characteristics of TIMx connected to the APB2 domain*. Updated *Table 65: Dynamic characteristics: Ethernet MAC signals for RMII*. Removed USB-IF certification in *Section : USB OTG FS characteristics*.

Table 100. Document revision history (continued)

Date	Revision	Changes
24-Jan-2012	2 (continued)	Updated *Table 61: USB HS clock timing parameters* Updated *Table 67: ADC characteristics*. Updated *Table 68: ADC accuracy at fADC = 30 MHz*. Updated *Note 1* in *Table 74: DAC characteristics*. *Section 5.3.26: FSMC characteristics*: updated *Table 75* to *Table 86*, changed C_L value to 30 pF, and modified FSMC configuration for asynchronous timings and waveforms. Updated *Figure 59: Synchronous multiplexed PSRAM write timings*. Updated *Table 98: Package thermal characteristics*. Appendix *A.1: USB OTG full speed (FS) interface solutions*: modified *Figure 93: USB controller configured as peripheral-only and used in Full speed mode* added *Note 2*, updated *Figure 94: USB controller configured as host-only and used in full speed mode* and added *Note 2*, changed *Figure 95: USB controller configured in dual mode and used in full speed mode* and added *Note 3*. Appendix *A.2: USB OTG high speed (HS) interface solutions*: removed figures *USB OTG HS device-only connection in FS mode* and *USB OTG HS host-only connection in FS mode, and updated Figure 96: USB controller configured as peripheral, host, or dual-mode and used in high speed mode* and added *Note 2*. Added Appendix *A.3: Ethernet interface solutions*.

Table 100. Document revision history (continued)

Date	Revision	Changes
31-May-2012	3	Updated *Figure 5: STM32F41xxx block diagram* and *Figure 7: Power supply supervisor interconnection with internal reset OFF* Added SDIO, added notes related to FSMC and SPI/I2S in *Table 2: STM32F415xx and STM32F417xx: features and peripheral counts*. Starting from Silicon revision Z, USB OTG full-speed interface is now available for all STM32F415xx devices. Added full information on WLCSP90 package together with corresponding part numbers. Changed number of AHB buses to 3. Modified available Flash memory sizes in *Section 2.2.4: Embedded Flash memory*. Modified number of maskable interrupt channels in *Section 2.2.10: Nested vectored interrupt controller (NVIC)*. Updated case of Regulator ON/internal reset ON, Regulator ON/internal reset OFF, and Regulator OFF/internal reset ON in *Section 2.2.16: Voltage regulator*. Updated standby mode description in *Section 2.2.19: Low-power modes*. Added *Note 1* below *Figure 16: STM32F41xxx UFBGA176 ballout*. Added *Note 1* below *Figure 17: STM32F41xxx WLCSP90 ballout*. Updated *Table 7: STM32F41xxx pin and ball definitions*. Added *Table 8: FSMC pin definition*. Removed OTG_HS_INTN alternate function in *Table 7: STM32F41xxx pin and ball definitions* and *Table 9: Alternate function mapping*. Removed I2S2_WS on PB6/AF5 in *Table 9: Alternate function mapping*. Replaced JTRST by NJTRST, removed ETH_RMII _TX_CLK, and modified I2S3ext_SD on PC11 in *Table 9: Alternate function mapping*. Added *Table 10: STM32F41x register boundary addresses*. Updated *Figure 18: STM32F41xxx memory map*. Updated V_{DDA} and V_{REF+} decoupling capacitor in *Figure 21: Power supply scheme*. Added power dissipation maximum value for WLCSP90 in *Table 14: General operating conditions*. Updated $V_{POR/PDR}$ in *Table 19: Embedded reset and power control block characteristics*. Updated notes in *Table 21: Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator disabled)*, *Table 20: Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator enabled) or RAM*, and *Table 22: Typical and maximum current consumption in Sleep mode*. Updated maximum current consumption at T_A = 25 °n *Table 23: Typical and maximum current consumptions in Stop mode*.

Table 100. Document revision history (continued)

Date	Revision	Changes
31-May-2012	3 (continued)	Removed f_{HSE_ext} typical value in *Table 30: High-speed external user clock characteristics*. Updated *Table 32: HSE 4-26 MHz oscillator characteristics* and *Table 33: LSE oscillator characteristics (fLSE = 32.768 kHz)*. Added f_{PLL48_OUT} maximum value in *Table 36: Main PLL characteristics*. Modified equation 1 and 2 in *Section 5.3.11: PLL spread spectrum clock generation (SSCG) characteristics*. Updated *Table 39: Flash memory characteristics*, *Table 40: Flash memory programming*, and *Table 41: Flash memory programming with VPP*. Updated *Section : Output driving current*. *Table 56: I^2C characteristics*: *Note 4* updated and applied to $t_{h(SDA)}$ in Fast mode, and removed note 4 related to $t_{h(SDA)}$ minimum value. Updated *Table 67: ADC characteristics*. Updated note concerning ADC accuracy vs. negative injection current below *Table 68: ADC accuracy at fADC = 30 MHz*. Added WLCSP90 thermal resistance in *Table 98: Package thermal characteristics*. Updated *Table 90: WLCSP90 - 4.223 x 3.969 mm, 0.400 mm pitch wafer level chip scale package mechanical data*. Updated *Figure 87: UFBGA176+25 - 201-ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package outline* and *Table 95: UFBGA176+25 - 201-ball, 10 × 10 × 0.65 mm pitch, ultra thin fine pitch ball grid array mechanical data*. Added *Figure 91: LQFP176 - 176-pin, 24 x 24 mm low profile quad flat recommended footprint*. Removed 256 and 768 Kbyte Flash memory density from *Table 99: Ordering information scheme*.

Table 100. Document revision history (continued)

Date	Revision	Changes
04-Jun-2013	4	Modified *Note 1* below *Table 2: STM32F415xx and STM32F417xx: features and peripheral counts*. Updated *Figure 4* title. Updated *Note 3* below *Figure 21: Power supply scheme*. Changed simplex mode into half-duplex mode in *Section 2.2.25: Inter-integrated sound (I2S)*. Replaced DAC1_OUT and DAC2_OUT by DAC_OUT1 and DAC_OUT2, respectively. Updated pin 36 signal in *Figure 15: STM32F41xxx LQFP176 pinout*. Changed pin number from F8 to D4 for PA13 pin in *Table 7: STM32F41xxx pin and ball definitions*. Replaced TIM2_CH1/TIM2_ETR by TIM2_CH1_ETR for PA0 and PA5 pins in *Table 9: Alternate function mapping*. Changed system memory into System memory + OTP in *Figure 18: STM32F41xxx memory map*. Added *Note 1* below *Table 16: VCAP_1/VCAP_2 operating conditions*. Updated I_{DDA} description in *Table 74: DAC characteristics*. Removed PA9/PB13 connection to VBUS in *Figure 93: USB controller configured as peripheral-only and used in Full speed mode* and *Figure 94: USB controller configured as host-only and used in full speed mode*. Updated SPI throughput on front page and *Section 2.2.24: Serial peripheral interface (SPI)* Updated operating voltages in *Table 2: STM32F415xx and STM32F417xx: features and peripheral counts* Updated note in *Section 2.2.14: Power supply schemes* Updated *Section 2.2.15: Power supply supervisor* Updated “Regulator ON” paragraph in *Section 2.2.16: Voltage regulator* Removed note in *Section 2.2.19: Low-power modes* Corrected wrong reference manual in *Section 2.2.28: Ethernet MAC interface with dedicated DMA and IEEE 1588 support* Updated *Table 15: Limitations depending on the operating power supply range* Updated *Table 24: Typical and maximum current consumptions in Standby mode* Updated *Table 25: Typical and maximum current consumptions in VBAT mode* Updated *Table 37: PLLI2S (audio PLL) characteristics* Updated *Table 44: EMI characteristics* Updated *Table 49: Output voltage characteristics* Updated *Table 51: NRST pin characteristics* Updated *Table 55: SPI dynamic characteristics* Updated *Table 56: I2S dynamic characteristics* Deleted Table 59 Updated *Table 62: ULPI timing* Updated *Figure 46: Ethernet SMI timing diagram*

Table 100. Document revision history (continued)

Date	Revision	Changes
04-Jun-2013	4 (continued)	Updated *Figure 87: UFBGA176+25 - 201-ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package outline* Updated *Table 95: UFBGA176+25 - 201-ball, 10 × 10 × 0.65 mm pitch, ultra thin fine pitch ball grid array mechanical data* Updated *Figure 5: STM32F41xxx block diagram* Updated *Section 2: Description* Updated footnote (3) in *Table 2: STM32F415xx and STM32F417xx: features and peripheral counts* Updated *Figure 3: Compatible board design between STM32F10xx/STM32F2/STM32F41xxx for LQFP144 package* Updated *Figure 4: Compatible board design between STM32F2 and STM32F41xxx for LQFP176 and BGA176 packages* Updated *Section 2.2.14: Power supply schemes* Updated *Section 2.2.15: Power supply supervisor* Updated *Section 2.2.16: Voltage regulator*, including figures. Updated *Table 14: General operating conditions*, including footnote (2). Updated *Table 15: Limitations depending on the operating power supply range*, including footnote (3). Updated footnote (1) in *Table 67: ADC characteristics*. Updated footnote (3) in *Table 68: ADC accuracy at fADC = 30 MHz*. Updated footnote (1) in *Table 74: DAC characteristics*. Updated *Figure 9: Regulator OFF*. Updated *Figure 7: Power supply supervisor interconnection with internal reset OFF*. Added *Section 2.2.17: Regulator ON/OFF and internal reset ON/OFF availability*. Updated footnote (2) of *Figure 21: Power supply scheme*. Replaced respectively “I2S3S_WS" by "I2S3_WS”, “I2S3S_CK” by “I2S3_CK” and “FSMC_BLN1” by “FSMC_NBL1” in *Table 9: Alternate function mapping*. Added “EVENTOUT” as alternate function “AF15” for pin PC13, PC14, PC15, PH0, PH1, PI8 in *Table 9: Alternate function mapping* Replaced “DCMI_12” by “DCMI_D12” in *Table 7: STM32F41xxx pin and ball definitions*. Removed the following sentence from *Section : I2C interface characteristics*: ”Unless otherwise specified, the parameters given in *Table 56* are derived from tests performed under the ambient temperature, f_{PCLK1} frequency and V_{DD} supply voltage conditions summarized in *Table 14*.”. In *Table 7: STM32F41xxx pin and ball definitions on page 47*: – For pin PC13, replaced “RTC_AF1” by “RTC_OUT, RTC_TAMP1, RTC_TS” – for pin PI8, replaced “RTC_AF2” by “RTC_TAMP1, RTC_TAMP2, RTC_TS”. – for pin PB15, added RTC_REFIN in Alternate functions column. In *Table 9: Alternate function mapping on page 62*, for port PB15, replaced “RTC_50Hz” by “RTC_REFIN”.

Table 100. Document revision history (continued)

Date	Revision	Changes
04-Jun-2013	4 (continued)	Updated *Figure 6: Multi-AHB matrix*. Updated *Figure 7: Power supply supervisor interconnection with internal reset OFF* Changed 1.2 V to V_{12} in *Section : Regulator OFF* Updated LQFP176 pin 48. Updated *Section 1: Introduction*. Updated *Section 2: Description*. Updated operating voltage in *Table 2: STM32F415xx and STM32F417xx: features and peripheral counts*. Updated *Note 1*. Updated *Section 2.2.15: Power supply supervisor*. Updated *Section 2.2.16: Voltage regulator*. Updated *Figure 9: Regulator OFF*. Updated *Table 3: Regulator ON/OFF and internal reset ON/OFF availability*. Updated *Section 2.2.19: Low-power modes*. Updated *Section 2.2.20: VBAT operation*. Updated *Section 2.2.22: Inter-integrated circuit interface (I²C)* . Updated pin 48 in *Figure 15: STM32F41xxx LQFP176 pinout*. Updated *Table 6: Legend/abbreviations used in the pinout table*. Updated *Table 7: STM32F41xxx pin and ball definitions*. Updated *Table 14: General operating conditions*. Updated *Table 15: Limitations depending on the operating power supply range*. Updated *Section 5.3.7: Wakeup time from low-power mode*. Updated *Table 34: HSI oscillator characteristics*. Updated *Section 5.3.15: I/O current injection characteristics*. Updated *Table 48: I/O static characteristics*. Updated *Table 51: NRST pin characteristics*. Updated *Table 56: I^2C characteristics*. Updated *Figure 39: I^2C bus AC waveforms and measurement circuit*. Updated *Section 5.3.19: Communications interfaces*. Updated *Table 67: ADC characteristics*. Added *Table 70: Temperature sensor calibration values*. Added *Table 73: Internal reference voltage calibration values*. Updated *Section 5.3.26: FSMC characteristics*. Updated *Section 5.3.28: SD/SDIO MMC card host interface (SDIO) characteristics*. Updated *Table 23: Typical and maximum current consumptions in Stop mode*. Updated *Section : SPI interface characteristics* included *Table 55*. Updated *Section : I2S interface characteristics* included *Table 56*. Updated *Table 64: Dynamic characteristics: Eternity MAC signals for SMI*. Updated *Table 66: Dynamic characteristics: Ethernet MAC signals for MII*.

Table 100. Document revision history (continued)

Date	Revision	Changes
04-Jun-2013	4 (continued)	Updated *Table 64: Dynamic characteristics: Eternity MAC signals for SMI*. Updated *Table 66: Dynamic characteristics: Ethernet MAC signals for MII*. Updated *Table 79: Synchronous multiplexed NOR/PSRAM read timings*. Updated *Table 80: Synchronous multiplexed PSRAM write timings*. Updated *Table 81: Synchronous non-multiplexed NOR/PSRAM read timings*. Updated *Table 82: Synchronous non-multiplexed PSRAM write timings*. Updated *Section 5.3.27: Camera interface (DCMI) timing specifications* including *Table 87: DCMI characteristics* and addition of *Figure 72: DCMI timing diagram*. Updated *Section 5.3.28: SD/SDIO MMC card host interface (SDIO) characteristics* including *Table 88*. Updated *Chapter Figure 9.*

Table 100. Document revision history (continued)

Date	Revision	Changes
06-Mar-2015	5	Replace Cortex-M4F by Cortex-M4 with FPU throughout the document. Updated *Section : Regulator OFF* and *Table 3: Regulator ON/OFF and internal reset ON/OFF availability* for LQFP176. Updated *Figure 15: STM32F41xxx LQFP176 pinout* and *Table 7: STM32F41xxx pin and ball definitions*. Updated *Figure 6: Multi-AHB matrix*. Added note 1 below *Figure 12: STM32F41xxx LQFP64 pinout*, *Figure 13: STM32F41xxx LQFP100 pinout*, *Figure 14: STM32F41xxx LQFP144 pinout* and *Figure 15: STM32F41xxx LQFP176 pinout*. Updated I_{VDD} and I_{VSS} in *Table 12: Current characteristics*. Updated PLS[2:0]=101 (falling edge) configuration in *Table 19: Embedded reset and power control block characteristics*. Added *Section : Additional current consumption*. Updated *Section : On-chip peripheral current consumption*. Updated *Table 29: Low-power mode wakeup timings*. Updated *Table 32: HSE 4-26 MHz oscillator characteristics* and *Table 33: LSE oscillator characteristics (fLSE = 32.768 kHz)*. Changed condition related to $V_{ESD(CDM)}$ in *Table 45: ESD absolute maximum ratings*. Updated *Table 47: I/O current injection susceptibility*, *Table 48: I/O static characteristics*, *Table 49: Output voltage characteristics* conditions, *Table 50: I/O AC characteristics* and *Figure 37: I/O AC characteristics definition*. Updated *Section : I2C interface characteristics*. Remove note 3 in *Table 69: Temperature sensor characteristics*. Updated *Figure 72: DCMI timing diagram*. Modified *Figure 75: WLCSP90 - 4.223 x 3.969 mm, 0.400 mm pitch wafer level chip scale package outline* and *Table 90: WLCSP90 - 4.223 x 3.969 mm, 0.400 mm pitch wafer level chip scale package mechanical data*. Added *Figure 76: WLCSP90 - 4.223 x 3.969 mm, 0.400 mm pitch wafer level chip scale recommended footprint* and *Table 91: WLCSP90 recommended PCB design rules*. / Modified *Figure 78: LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline* and *Table 92: LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package mechanical data*. Updated *Figure 87: UFBGA176+25 - 201-ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package outline* and *Table 95: UFBGA176+25 - 201-ball, 10 × 10 × 0.65 mm pitch, ultra thin fine pitch ball grid array mechanical data*. Added *Figure 88: UFBGA176+25 - 201-ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array recommended footprint* and *Table 96: UFBGA176+2 recommended PCB design rules (0.65 mm pitch BGA)*. Updated *Figure 90: LQFP176 - 176-pin, 24 x 24 mm low profile quad flat package outline*. Added *Section : Device marking for WLCSP90*, *Section : Device marking for LQFP64*, *Section : Device marking for LFP100*, *Section : Device marking for LQPF144*, *Section : Device marking for UFBGA176+25* and *Section : Device marking for LQFP176*.

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