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FDH50N50 / FDA50N50 N-Channel UniFET<sup>TM</sup> MOSFET 500 V, 48 A, 105 m $\Omega$ 

## May 2014

#### **Features**

- $R_{DS(on)}$  = 89 m $\Omega$  (Typ.) @  $V_{GS}$  = 10 V,  $I_D$  = 24 A
- Low Gate Charge (Typ. 105 nC)
- Low C<sub>rss</sub> (Typ. 45 pF)
- · 100% Avalanche Tested
- · Improved dv/dt Capability

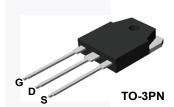
### **Applications**

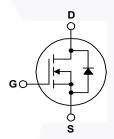
- · Lighting
- · Uninterruptible Power Supply
- AC-DC Power Supply

### **Description**

UniFET<sup>TM</sup> MOSFET is Fairchild Semiconductor's high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on-state resistance, and to provide better switching performance and higher avalanche energy strength. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.







## **Absolute Maximum Ratings** $T_C = 25^{\circ}C$ unless otherwise noted.

Symbol		Parameter	FDH50N50_F133 / FDA50N50	Unit
V <sub>DSS</sub>	Drain-Source Voltage		500	V
I <sub>D</sub>	Drain Current	- Continuous (T <sub>C</sub> = 25°C) - Continuous (T <sub>C</sub> = 100°C)	48 30.8	A A
I <sub>DM</sub>	Drain Current	- Pulsed (Note	1) 192	Α
V <sub>GSS</sub>	Gate-Source voltage		±20	V
E <sub>AS</sub>	Single Pulsed Avalanche	Energy (Note	2) 1868	mJ
I <sub>AR</sub>	Avalanche Current (Note 1)		1) 48	Α
E <sub>AR</sub>	Repetitive Avalanche Energy (Note 1)		62.5	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		3) 20	V/ns
$P_{D}$	Power Dissipation	(T <sub>C</sub> = 25°C) - Derate Above 25°C	625 5	W W/°C
T <sub>J,</sub> T <sub>STG</sub>	Operating and Storage Te	emperature Range	-55 to +150	°C
T <sub>L</sub>	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds		300	°C

#### **Thermal Characteristics**

Symbol	Parameter	FDH50N50_F133 / FDA50N50	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	0.2	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max. 40		C/VV

## **Package Marking and Ordering Information**

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDH50N50_F133	FDH50N50	TO-247	Tube	N/A	N/A	30 units
FDA50N50	FDA50N50	TO-3PN	Tube	N/A	N/A	30 units

## $\textbf{Electrical Characteristics} \quad \textbf{T}_{C} = 25^{\circ} \text{C unless otherwise noted}.$

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
Off Charac	cteristics					
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS}$ = 0 V, $I_{D}$ = 250 $\mu$ A	500			V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C		0.5		V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 500 V, V <sub>GS</sub> = 0 V V <sub>DS</sub> = 400 V, T <sub>C</sub> = 125°C			25 250	μ <b>Α</b> μ <b>Α</b>
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 20 V, V <sub>DS</sub> = 0 V			100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = -20 V, V <sub>DS</sub> = 0 V			-100	nA
On Charac	teristics					
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	3.0		5.0	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 24 A		0.089	0.105	Ω
9 <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 40 V, I <sub>D</sub> = 48 A		20		S
Dynamic C	Characteristics				•	
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, f = 1 MHz		4979	6460	pF
C <sub>oss</sub>	Output Capacitance			760	1000	pF
C <sub>rss</sub>	Reverse Transfer Capacitance			50	65	pF
C <sub>oss</sub>	Output Capacitance	V <sub>DS</sub> = 400 V, V <sub>GS</sub> = 0 V, f = 1 MHz		161		pF
C <sub>oss(eff.)</sub>	Effective Output Capacitance	V <sub>DS</sub> = 0 V to 400 V, V <sub>GS</sub> = 0 V		342		pF
Switching	Characteristics					
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 250 V, I <sub>D</sub> = 48 A,		105	220	ns
t <sub>r</sub>	Turn-On Rise Time	$V_{GS}$ = 10 V, $R_{G}$ = 25 $\Omega$ (Note 4)		360	730	ns
t <sub>d(off)</sub>	Turn-Off Delay Time			225	460	ns
t <sub>f</sub>	Turn-Off Fall Time			230	470	ns
Qg	Total Gate Charge	V <sub>DS</sub> = 400 V, I <sub>D</sub> = 48 A	/	105	137	nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>GS</sub> = 10 V		33	/	nC
Q <sub>gd</sub>	Gate-Drain Charge (Note 4			45		nC
Drain-Soul	rce Diode Characteristics and Maximur	n Ratings				
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current				48	Α
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode F	orward Current			192	Α
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 48 A	-		1.4	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 48 A, dI <sub>F</sub> /dt =100 A/µs		580		ns
Q <sub>rr</sub>	Reverse Recovery Charge			10		μС

#### Notes:

 $<sup>{\</sup>it 1. Repetitive\ rating: pulse-width\ limited\ by\ maximum\ junction\ temperature.}$ 

<sup>2.</sup> L = 1.46 mH, I  $_{AS}$  = 48 A, V  $_{DD}$  = 50 V, R  $_{G}$  = 25  $\Omega,$  starting T  $_{J}$  = 25  $^{\circ}C.$ 

<sup>3.</sup>  $I_{SD} \le 48$  A, di/dt  $\le 200$  A/µs,  $V_{DD} \le BV_{DSS}$ , starting  $T_J$  = 25°C.

 $<sup>{\</sup>bf 4.} \ {\bf Essentially \ independent \ of \ operating \ temperature \ typical \ characteristics.}$ 

### **Typical Performance Characteristics**

Figure 1. On-Region Characteristics

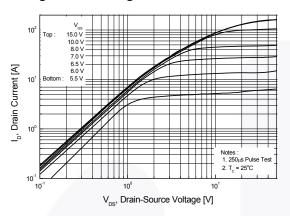


Figure 3. On-Resistance Variation vs.
Drain Current and Gate Voltage

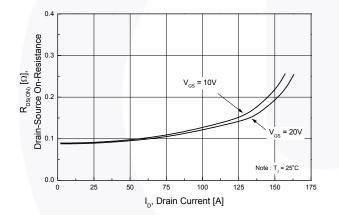
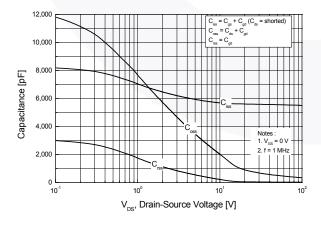


Figure 5. Capacitance Characteristics



**Figure 2. Transfer Characteristics** 

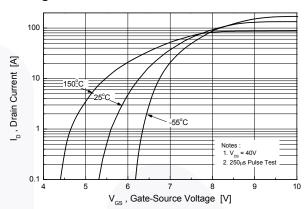


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperatue

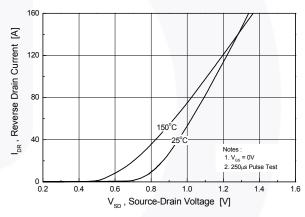
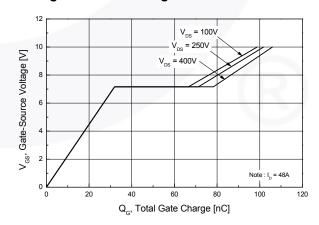


Figure 6. Gate Charge Characteristics



## **Typical Performance Characteristics** (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

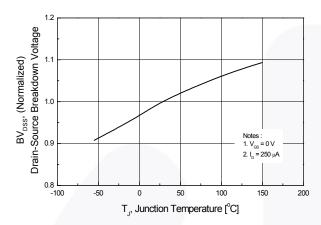


Figure 8. On-Resistance Variation vs. Temperature

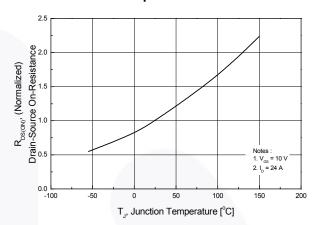


Figure 9. Maximum Safe Operating Area

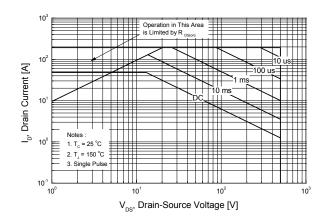


Figure 10. Maximum Drain Current vs. Case Temperature

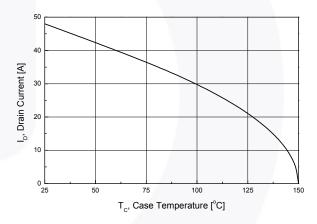


Figure 11. Typical Drain Current Slope vs. Gate Resistance

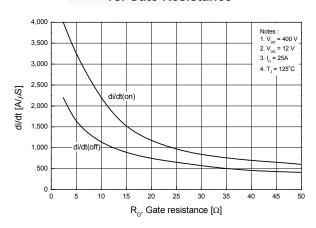
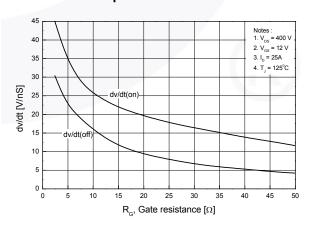


Figure 12. Typical Drain-Source Voltage Slope vs. Gate Resistance



### **Typical Performance Characteristics** (Continued)

Figure 13. Typical Switching Losses vs. Gate Resistance

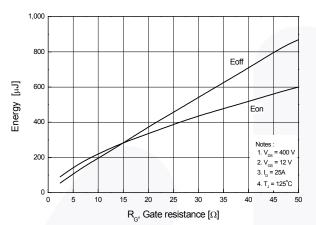


Figure 14. Unclamped Inductive Switching Capability

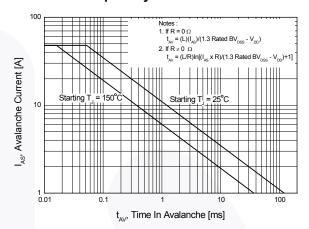
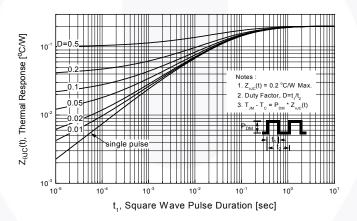


Figure 15. Transient Thermal Resistance Curve



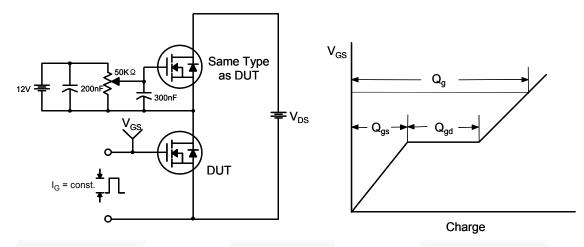


Figure 16. Gate Charge Test Circuit & Waveform

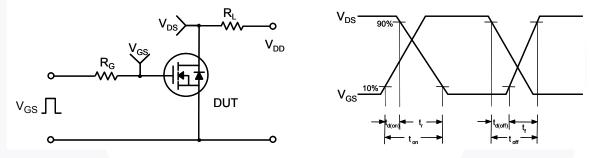


Figure 17. Resistive Switching Test Circuit & Waveforms

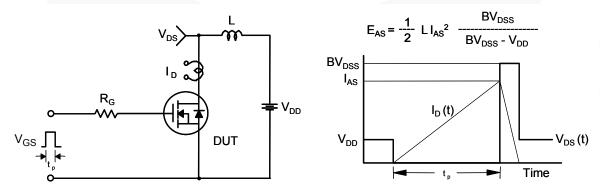


Figure 18. Unclamped Inductive Switching Test Circuit & Waveforms

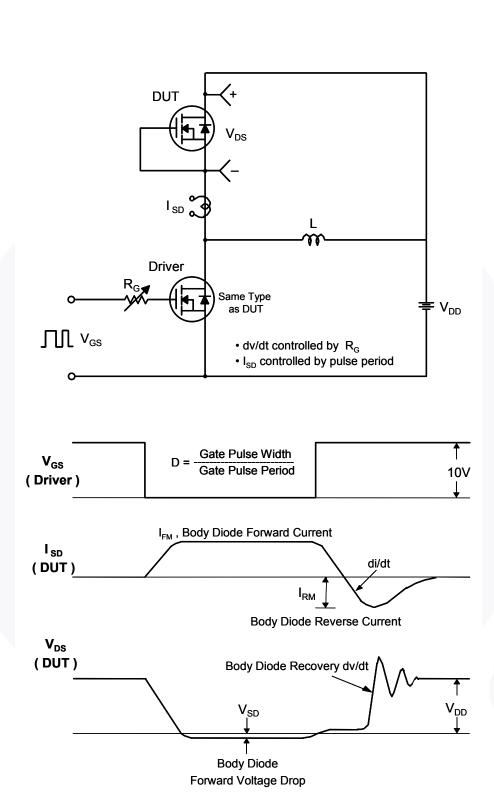
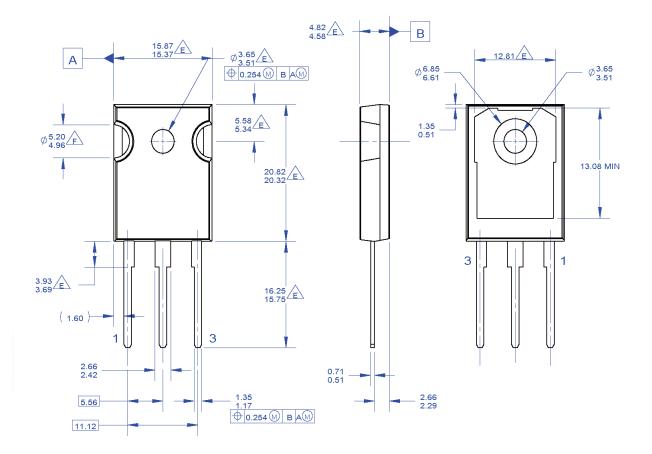


Figure 19. Peak Diode Recovery dv/dt Test Circuit & Waveforms

#### **Mechanical Dimensions**



NOTES: UNLESS OTHERWISE SPECIFIED.

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- D. DRAWING CONFORMS TO ASME Y14.5 1994

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G. DRAWING FILENAME: MKT-TO247A03\_REV03

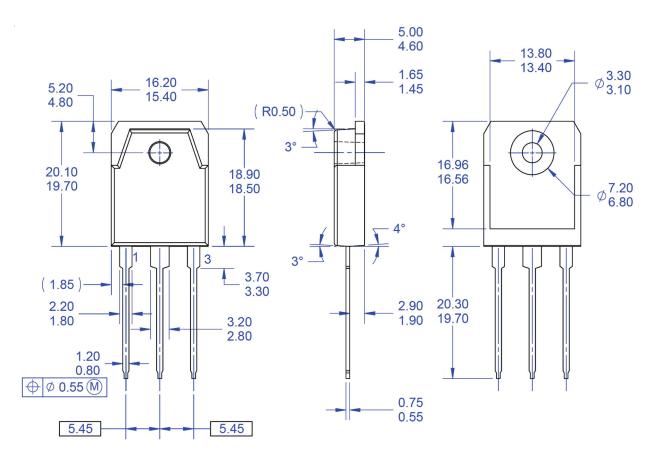
#### Figure 20. TO-247, Molded, 3-Lead, Jedec Variation AB

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#### **Mechanical Dimensions**



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Rev. 168

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