

# Complete Low Cost 12-Bit D/A Converters

# ADDAC80/ADDAC85/ADDAC87

#### **FEATURES**

Single Chip Construction On-Board Output Amplifier Low Power Dissipation: 300 mW Monotonicity Guaranteed over Temperature Guaranteed for Operation with 12 V Supplies Improved Replacement for Standard DAC80, DAC800 HI-5680 High Stability, High Current Output Buried Zener Reference Laser Trimmed to High Accuracy 1/2 LSB Max Nonlinearity Low Cost Plastic Packaging

#### PRODUCT DESCRIPTION

The ADDAC80 Series is a family of low cost 12-bit digital-toanalog converters with both a high stability voltage reference and output amplifier combined on a single monolithic chip. The ADDAC80 Series is recommended for all low cost 12-bit D/A converter applications where reliability and cost are of paramount importance.

Advanced circuit design and precision processing techniques result in significant performance advantages over conventional DAC80 devices. Innovative circuit design reduces the total power consumption to 300 mW, which not only improves reliability, but also improves long term stability.

The ADDAC80 incorporates a fully differential, nonsaturating precision current switching cell structure which provides greatly increased immunity to supply voltage variation. This same structure also reduces nonlinearities due to thermal transients as the various bits are switched; nearly all critical components operate at constant power dissipation. High stability, SiCr thin film resistors are trimmed with a fine resolution laser, resulting in lower differential nonlinearity errors. A low noise, high stability, subsurface Zener diode is used to produce a reference voltage with excellent long term stability, high external current capability and temperature drift characteristics which challenge the best discrete Zener references.

The ADDAC80 Series is available in three performance grades and three package types. The ADDAC80 is specified for use over the 0°C to 70°C temperature range and is available in both plastic and ceramic DIP packages. The ADDAC85 and ADDAC87 are available in hermetically sealed ceramic packages and are specified for the  $-25^{\circ}$ C to  $+85^{\circ}$ C and  $-55^{\circ}$ C to  $+125^{\circ}$ C temperature ranges.

#### REV. B

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#### FUNCTIONAL BLOCK DIAGRAM



#### **PRODUCT HIGHLIGHTS**

- 1. The ADDAC80 series of D/A converters directly replaces all other devices of this type with significant increases in performance.
- 2. Single chip construction and low power consumption provides the optimum choice for applications where low cost and high reliability are major considerations.
- 3. The high speed output amplifier has been designed to settle within 1/2 LSB for a 10 V full scale transition in 2.0  $\mu$ s, when properly compensated.
- 4. The precision buried Zener reference can supply up to 2.5 mA for use elsewhere in the application.
- 5. The low TC binary ladder guarantees that all units are monotonic over the specified temperature range.
- 6. System performance upgrading is possible without redesign.

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# ADDAC80/ADDAC85/ADDAC87—SPECIFICATIONS (T<sub>A</sub> = 25°C, rated power supplies unless otherwise noted.)

Model	Al Min	DDAC8 Typ	0 Max	A Min	DDAC8 Typ	5 Max	A Min	DDAC8 Typ	7 Max	Unit
TECHNOLOGY	Ν	Ionolithi	с	Ν	Aonolithi	c	N	Monolithi	с	
$\label{eq:constraint} \hline \begin{array}{c} \mbox{DIGITAL INPUT} \\ \mbox{Binary-CBI} \\ \mbox{BCD-CCD} \\ \mbox{Logic Levels (TTL Compatible)} \\ \mbox{V}_{IH} (Logic "1") \\ \mbox{V}_{IL} (Logic "0") \\ \mbox{I}_{IH} (V_{IH} = 5.5 \mbox{ V}) \\ \mbox{I}_{IL} (V_{IL} = 0.8 \mbox{ V}) \end{array}$	2.0 0		12 5.5 0.8 250 100	2.0 0		12 5.5 0.8 250 100	2.0 0		12 5.5 0.8 250 100	Bits Digits V V μΑ μΑ
$\begin{array}{c} \text{TRANSFER CHARACTERISTICS} \\ \text{ACCURACY} \\ \text{Linearity Error @ 25°C} \\ \text{CBI} \\ \text{CCD} \\ \text{T}_{A} @ \text{T}_{\text{MIN}} \text{ to } \text{T}_{\text{MAX}} \\ \text{Differential Linearity Error @ 25°C} \\ \text{CBI} \\ \text{CCD} \\ \text{T}_{A} @ \text{T}_{\text{MIN}} \text{ to } \text{T}_{\text{MAX}} \\ \text{Gain Error}^2 \\ \text{Offset Error}^2 \\ \text{Temperature Range for Guaranteed} \\ \text{Monotonicity} \\ \text{DRIFT (T}_{\text{MIN}} \text{ to } \text{T}_{\text{MAX}}) \\ \text{Total Bipolar Drift, max (includes gain, offset, and linearity drifts)} \\ \text{Total Bipolar Drift, to } \text{T}_{\text{MAX}})^4 \\ \text{Unipolar} \\ \text{Bipolar} \\ \text{Gain Including Internal Reference} \\ \text{Gain Excluding Internal Reference} \\ \text{Gain Excluding Internal Reference} \\ \text{Unipolar Offset} \\ \text{Bipolar Offset} \\ \end{array}$	0	$\pm 1/4$ $\pm 0.1$ $\pm 0.05$ $\pm 0.06$ $\pm 15$ $\pm 4$ $\pm 1$ $\pm 5$	$\begin{array}{c} \pm 1/2 \\ \pm 1/2 \\ \pm 3/4 \\ \pm 0.3 \\ \pm 0.15 \\ +70 \\ \pm 20 \\ \pm 0.15 \\ \pm 0.10 \\ \pm 30 \\ \pm 7 \\ \pm 3 \\ \pm 10 \end{array}$	-25	$\pm 1/4$ $\pm 0.1$ $\pm 0.05$ $\pm 0.12$ $\pm 0.08$	$\pm 1/2$ $\pm 1/2$ $\pm 3/4$ $\pm 1$ $\pm 0.2$ $\pm 0.1$ $\pm 85$ $\pm 20$ $\pm 0.2$ $\pm 0.12$ $\pm 20$ $\pm 10$ $\pm 3$ $\pm 10$	-55	$\pm 1/2$ $\pm 0.1$ $\pm 0.05$ $\pm 0.18$ $\pm 0.14$	$\pm 1/2$ $\pm 3/4$ $\pm 1$ $\pm 0.2$ $\pm 0.1$ $\pm 125$ $\pm 30$ $\pm 0.3$ $\pm 0.24$ $\pm 20$ $\pm 10$ $\pm 3$ $\pm 10$	LSB <sup>1</sup> LSB LSB LSB LSB %FSR <sup>3</sup> %FSR <sup>3</sup> °C ppm of FSR/°C % of FSR % of FSR ppm of FSR/°C ppm of FSR/°C ppm of FSR/°C ppm of FSR/°C
$\begin{tabular}{ c c c c } \hline CONVERSION SPEED & & & & & & & & & & & & & & & & & & $	10	3 2 1	4 3	10	3 2 1	4 3	10	3 2 1	4 3	μs μs μs V/μs
ANALOG OUTPUT Voltage Models Ranges–CBI –CCD Output Current Output Impedance (dc) Short Circuit Current Internal Reference Voltage (V <sub>R</sub> ) Output Impedance Max External Current <sup>6</sup> Tempco of Drift	±5 6.23	$\pm 2.5, \pm \pm 10, \pm 10, \pm 10$ 0.05 6.3 1.5 $\pm 10$	5, 5, 6.37 2.5 ±20	±5 6.23	$\pm 2.5, \pm \pm 10, \pm 10$ 0.05 6.3 1.5 $\pm 10$	5, 5, 6.37 2.5 ±20	±5 6.23	$\pm 2.5, \pm \pm 10, \pm 10$ 0.05 6.3 1.5	5, 5, 6.37 2.5 ±10	V V V W MA $\Omega$ mA V Q mA ppm of V <sub>R</sub> /°C
POWER SUPPLY SENSITIVITY $\pm 15 \text{ V} \pm 10\%$ , 5 V supply when applicable $\pm 12 \text{ V} \pm 5\%$			±0.002 ±0.002			±0.002 ±0.002			±0.002 ±0.002	% of FSR/%V <sub>S</sub> % of FSR/%V <sub>S</sub>
POWER SUPPLY REQUIREMENTS Rated Voltages Range Analog Supplies Logic Supplies Supply Drain +12 V, +15 V	$\pm 11.4^{7}$	±15	±16.5	$\pm 11.4^{7}$	±15	±16.5	$\pm 11.4^{7}$	±15	±16.5	V V V mA
-12 v, -13 v		14	20		14	20		14	20	шл

	ADDA		0	A	ADDAC85			ADDAC		
Model	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
TEMPERATURE RANGE										
Specifications	0		+70	-25		+85	-55		+125	°C
Operating	-25		+85	-55		+125	-55		+125	°C
Storage	-25		+125	-65		+150	-65		+150	°C

NOTES

<sup>1</sup>Least Significant Bit.

<sup>2</sup>Adjustable to zero with external trim potentiometer. <sup>3</sup>FSR means "Full Scale Range" and is 20 V for the  $\pm 10$  V range and 10 V for the  $\pm 5$  V range.

<sup>4</sup>Gain and offset errors adjusted to zero at 25°C.

 ${}^{5}C_{F} = 0$ , see Figure 3a.

<sup>6</sup>Maximum with no degradation of specification, must be a constant load.

<sup>7</sup>A minimum of  $\pm 12.3$  V is required for a  $\pm 10$  V full scale output and  $\pm 11.4$  V is required for all other voltage ranges.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Specifications subject to change without notice.

Model	A Min	ADDAC8 Typ	0 Max	A Min	ADDAC85 Typ	Max	Min	ADDAC8 Typ	7 Max	Unit
TECHNOLOGY		Hybrid			Hybrid			Hybrid		
$\label{eq:constraint} \hline \\ \hline DIGITAL INPUT \\ Binary-CBI \\ BCD-CCD \\ Logic Levels (TTL Compatible) \\ V_{IH} (Logic "1") \\ V_{IL} (Logic "0") \\ I_{IH} (V_{IH} = 5.5 \ V) \\ I_{IL} (V_{IL} = 0.8 \ V) \\ \hline \end{array}$	2.0 0	250 -100	12 3 5.5 0.8	2.0 0	250 -100	12 3 5.5 0.8	2.0 0	250 -100	12 3 5.5 0.8	Bits Digits V V µA µA
TRANSFER CHARACTERISTICS ACCURACY Linearity Error @ 25°C CBI CCD $T_A$ @ $T_{MIN}$ to $T_{MAX}$ Differential Linearity Error @ 25°C CBI CCD $T_A$ @ $T_{MIN}$ to $T_{MAX}$ Gain Error <sup>2</sup> Offset Error <sup>2</sup> Temperature Range for Guaranteed Monotonicity DRIFT ( $T_{MIN}$ to $T_{MAX}$ ) Total Bipolar Drift, max (includes gain, offset, and linearity drifts) Total Error ( $T_{MIN}$ to $T_{MAX}$ ) <sup>4</sup> Unipolar Bipolar Gain Including Internal Reference Excluding Internal Reference Unipolar Offset	0	$\begin{array}{c} \pm 1/4 \\ \pm 1/8 \\ \pm 1/4 \\ \pm 1/2 \\ \pm 1/4 \\ \pm 0.1 \\ \pm 0.05 \\ \\ \pm 0.06 \\ \pm 15 \\ \pm 5 \\ \pm 1 \\ \pm 5 \\ \pm 1 \\ \pm 5 \\ \pm 1 \end{array}$	$\begin{array}{c} \pm 1/2 \\ \pm 1/4 \\ \pm 1/2 \\ \pm 3/4 \\ \pm 1/2 \\ \pm 1 \\ \pm 0.3 \\ \pm 0.15 \\ \pm 70 \\ \pm 20 \\ \pm 0.15 \\ \pm 0.10 \\ \pm 30 \\ \pm 7 \\ \pm 30 \\ \pm 7 \\ \pm 30 \\ \pm 10 \end{array}$	0	$\pm 1/4$ $\pm 1/2$ $\pm 1/2$ $\pm 0.1$ $\pm 0.05$ $\pm 1$	<pre>±1/2 ±1/4 ±1/2 ±1 +70 </pre>	-25	$\pm 1/2$ $\pm 1/2$ $\pm 1/2$ $\pm 0.1$ $\pm 0.05$ $\pm 1$	<pre>±1/2 ±1/4 ±1/2 ±1 +85 ±20 ±10 </pre>	LSB <sup>1</sup> LSB LSB LSB LSB KFSR <sup>3</sup> %FSR <sup>3</sup> °C ppm of FSR/°C ppm of FSR/°C ppm of FSR/°C ppm of FSR/°C
Support Onset         Support Onset         CONVERSION SPEED         Voltage Model (V) <sup>5</sup> Settling Time to $\pm 0.01\%$ of FSR for         FSR Change (2 kΩ  500 pF load)         with 10 kΩ Feedback         with 10 kΩ Feedback         with 5 kΩ Feedback         For LSB Change         Slew Rate         Current Model (I)         Settling time to $\pm 0.01\%$ of FSR for         FSR Change         10.0 Load	10	5 3 1.5 15	10		5 3 1.5 20			5 3 1.5 20	10	μs μs μs V/μs
for 1 k $\Omega$		1			1			1		μs

# ADDAC80/ADDAC85/ADDAC87—SPECIFICATIONS (continued)

Model	Min	ADDAC Typ	80 Max	A Min	ADDAC Typ	85 Max	A Min	ADDACS Typ	87 Max	Unit
ANALOG OUTPUT										
Voltage Models										
Ranges–CBI		±2.5,±	:5,		±2.5, :	±5,		±2.5, ±	:5,	
		±10,+	5,		±10,+	-5,		±10,+	5,	
		+10			+10			+10		V
Ranges-CCD		$\pm 10$			+10			+10		V
Output Current	±5			±5			±5			mA
Output Impedance (dc)		0.05			0.05			0.05		Ω
Short Circuit Duration	Indefini	ite to Con	nmon	Indefini	te to Cor	nmon	Indefini	ite to Con	nmon	
Current Models										
Ranges–Unipolar		-2.0			-2.0			-2.0		mA
Ranges-Bipolar		$\pm 1.0$			$\pm 1.0$			$\pm 1.0$		mA
Output Impedance										
Bipolar		3.2			3.2			3.2		kΩ
Unipolar		6.6			6.6			6.6		kΩ
Compliance		-1.5, +	10		-2.5, +	+10		-2.5, +	10	V
Internal Reference Voltage (V <sub>R</sub> )	6.17	6.3	6.43	6.17	6.3	6.43	6.17	6.3	6.43	V
Output Impedance		1.5			1.5			1.5		Ω
Max External Current <sup>6</sup>			2.5			2.5			2.5	mA
Tempco of Drift		$\pm 10$	$\pm 20$		$\pm 10$	$\pm 20$		$\pm 10$	$\pm 20$	ppm of $V_R / ^{\circ}C$
POWER SUPPLY SENSITIVITY										
$\pm 15 \text{ V} \pm 10\%$ , 5 V Supply When Applicable		$\pm 0.002$	2		±0.002	2		$\pm 0.002$	2	% of FSR/%V <sub>S</sub>
POWER SUPPLY REQUIREMENTS			_			_			_	
Rated Voltages Range		±15,+	5		±15,+	-5		±15,+	5	V
Analog Supplies	±14		$\pm 16$	±14.5		±15.5	±14.5		±15.5	V
Logic Supplies	4.5		16	4.5		15.5	4.5		15.5	V
Supply Drain <sup>7</sup>										
+15 V		10	20		15	20		15	20	mA
–15 V		20	35		25	30		25	30	mA
+5 V <sup>8</sup>		8	20		15	20		15	20	mA
TEMPERATURE RANGE										
Specifications	0		+70	0		+70	-25		+85	°C
Operating	-25		+85	-25		+85	-55		+125	°C
Storage	-55		+130	-65		+150	-65		+150	υ°C

NOTES

<sup>1</sup>Least Significant Bit.

<sup>2</sup>Adjustable to zero with external trim potentiometer.

<sup>3</sup>FSR means "Full Scale Range" and is 20 V for the  $\pm 10$  V range and 10 V for the  $\pm 5$  V range. <sup>4</sup>Gain and offset errors adjusted to zero at 25°C.

 ${}^{5}C_{F} = 0$ , see Figure 3a.

<sup>6</sup>Maximum with no degradation of specification, must be a constant load. <sup>7</sup>Including 5 mA load.

<sup>8</sup>5 V supply required only for CCD versions.

Specifications subject to change without notice.

	AD	DAC85L	.D	AD	DAC85N	ul.	A	ADDAC8	7	<b>T</b> T <b>1</b> .
Model	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
TECHNOLOGY		Hybrid			Hybrid			Hybrid		
DIGITAL INPUT Binary-CBI BCD-CCD			12			12			12	Bits Digits
Logic Levels (11L Compatible) $V_{IH}$ (Logic "1") $V_{IL}$ (Logic "0") $I_{IH}$ ( $V_{IH}$ = 5.5 V) $I_{IL}$ ( $V_{IL}$ = 0.8 V)	2.0 0	250 -100	5.5 0.8	2.0 0	250 -100	5.5 0.8	2.0 0	250 -100	5.5 0.8	V V μΑ μΑ
TRANSFER CHARACTERISTICS ACCURACY										
Linearity Error @ 25°C CBI CCD T <sub>A</sub> @ T <sub>MIN</sub> to T <sub>MAX</sub>			$\pm 1/2$ $\pm 1/2$			±1/2 ±3/4		$\pm 1/4$	±1/2 ±3/4	LSB <sup>1</sup> LSB LSB
Differential Linearity Error @ 25°C CBI CCD		$\pm 1/2$			$\pm 1/2$			$\pm 1/2$		LSB LSB
$T_A @ T_{MIN}$ to $T_{MAX}$ Gain Error <sup>2</sup> Offset Error <sup>2</sup>		±0.1 ±0.05	±1		$\pm 0.1$ $\pm 0.05$	±1		±0.1 ±0.05	$^{\pm 1}_{\pm 0.2}_{\pm 0.1}$	LSB %FSR <sup>3</sup> %FSR <sup>3</sup>
Monotonicity DRIFT (T <sub>MIN</sub> to T <sub>MAX</sub> ) Total Binolar Drift, max (includes gain.	-25		+85	-55		+125	-55		+125	°C
offset, and linearity drifts) Total Error $(T_{MIN} \text{ to } T_{MAX})^4$								±15	±30	ppm of FSR/°C
Bipolar Gain								±0.13 ±0.12	±0.24	% of FSR
Including Internal Reference Excluding Internal Reference Unipolar Offset Bipolar Offset		±1	±10 ±5		±2	±20 ±10		$\pm 10 \\ \pm 5 \\ \pm 1 \\ \pm 5$	$\pm 25 \\ \pm 10 \\ \pm 3 \\ \pm 10$	ppm of FSR/°C ppm of FSR/°C ppm of FSR/°C ppm of FSR/°C
CONVERSION SPEED Voltage Model (V) <sup>5</sup> Settling Time to $\pm 0.01\%$ of FSR for FSR change (2 kΩ $\parallel$ 500 pF load) with 10 kΩ Feedback		5			5			5		ЦS
with 5 k $\Omega$ Feedback For LSB Change Slew Rate Current Model (I) Settling Time to $\pm 0.01\%$ of FSR		3 1.5 20			3 1.5 20			3 1.5 20		μs μs V/μs
for FSR Change $10 \Omega$ to $100 \Omega$ Load for $1 k\Omega$		300 1			300 1			300 1		ns μs
ANALOG OUTPUT Voltage Models Ranges–CBI		±2.5, ± ±10, + +10	:5, 5,		±2.5, ± ±10, +9 +10	5, 5,		$\pm 2.5, \pm \pm 10, \pm 2$ +10	5, 5,	V
-CCD Output Current Output Impedance (dc) Short Circuit Duration Current Models	±5 Indefin	0.05 ite to Corr	nmon	±5 Indefin	0.05 ite to Com	imon	±5 Indefin	0.05 ite to Com	imon	V mA Ω
Ranges–Unipolar –Bipolar Output Impedance		$^{-2.0}_{\pm 1.0}$			$^{-2.0}_{\pm 1.0}$			$^{-2.0}_{\pm 1.0}$		mA mA
Bipolar Unipolar Compliance Internal Reference Voltage (V <sub>R</sub> ) Output Impedance Max External Current <sup>6</sup> Tempco of Drift	6.17	3.2 6.6 -2.5, + 6.3 1.5 $\pm 10$	$10 \\ 6.43 \\ 2.5 \\ \pm 20$	6.17	3.2 6.6 -2.5, + 6.3 1.5 $\pm 10$	$10 \\ 6.43 \\ 2.5 \\ \pm 20$	2.5 5.0 6.17	3.2 6.6 -1.5, + 6.3 1.5 $\pm 5$	$\begin{array}{c} 4.1 \\ 8.2 \\ 10 \\ 6.43 \\ 2.5 \\ \pm 10 \end{array}$	$k\Omega$ $k\Omega$ V Q mA $ppm of V_{P}/^{\circ}C$
POWER SUPPLY SENSITIVITY ±15 V± 10%, 5 V supply when applicable		±0.002			±0.002			±0.002	±0.003	% of FSR/%V <sub>s</sub>

# ADDAC80/ADDAC85/ADDAC87—SPECIFICATIONS (continued)

	AD	DAC85I	.D	AD	DAC85N	MIL	A	DDAC8	7	
Model	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
POWER SUPPLY REQUIREMENTS										
Rated Voltages		±15,5			±15, 5			±15,5		V
Range										
Analog Supplies	±14.5		±15.5	±14.5		±15.5	±13.5		±16.5	V
Logic Supplies	+4.5		±15.5	+4.5		+15.5	+4.5		±16.5	V
Supply Drain <sup>7</sup>										
+15 V		15	20		15	20		10	20	mA
–15 V		25	30		25	30		20	35	mA
+5 V <sup>8</sup>		15	20		15	20		10	20	mA
TEMPERATURE RANGE										
Specification	-25		+85	-55		+125	-55		+125	°C
Operating	-55		+125	-55		+125	-55		+125	°C
Storage	-55		+125	-55		+125	-65		+150	°C

NOTES

<sup>1</sup>Least Significant Bit.

<sup>2</sup>Adjustable to zero with external trim potentiometer.

 $^3FSR$  means "Full-Scale Range" and is 20 V for the  $\pm 10$  V range and 10 V for the  $\pm 5$  V range.

<sup>4</sup>Gain and offset errors adjusted to zero at 25°C.

 ${}^{5}C_{F} = 0$ , see Figure 3a.

<sup>6</sup>Maximum with no degradation of specification, must be a constant load.

<sup>7</sup>Including 5 mA load.

<sup>8</sup>5 V supply required only for CCD versions.

Specifications subject to change without notice.

#### ABSOLUTE MAXIMUM RATINGS

$+V_S$ to Power Ground 0 V to $+18$ V
$-V_S$ to Power Ground
Digital Inputs (Pins 1 to 12) to Power Ground
-1.0 V to +7 V
Ref In to Reference Ground ±12 V
Bipolar Offset to Reference Ground ±12 V
10 V Span R to Reference Ground ±12 V
20 V Span R to Reference Ground ±24 V
Ref Out Indefinite Short to Power Ground or $+V_8$



Figure 1. Voltage Model Function Diagram and Pin Configuration



*Figure 2. Current Model Functional Diagram and Pin Configuration* 

Model	Input Code	Output Mode	Technology	Temperature Range	Linearity Error	Package Option <sup>1</sup>
ADDAC80N-CBI-V	Binary	Voltage	Monolithic	0°C to 70°C	±1/2 LSB	N-24A
ADDAC80D-CBI-V	Binary	Voltage	Monolithic	0°C to 70°C	±1/2 LSB	D-24
ADDAC85D-CBI-V	Binary	Voltage	Monolithic	–25°C to +85°C	±1/2 LSB	D-24
ADDAC87D-CBI-V	Binary	Voltage	Monolithic	–55°Cto +125°C	±1/2 LSB	D-24
ADDAC80-CBI-V	Binary	Voltage	Hybrid	0°C to 70°C	$\begin{array}{c} \pm 1/2 \text{ LSB} \\ \pm 1/2 \text{ LSB} \\ \pm 1/4 \text{ LSB} \\ \pm 1/4 \text{ LSB} \\ \pm 1/4 \text{ LSB} \\ \pm 1/2 \text{ LSB} \\ \pm 1/2 \text{ LSB} \\ \pm 1/4 \text{ LSB} \\ \end{array}$	DH-24A
ADDAC80-CBI-I	Binary	Current	Hybrid	0°C to 70°C		DH-24A
ADDAC80-CCD-V	Binary Coded Decimal	Voltage	Hybrid	0°C to 70°C		DH-24A
ADDAC80-CCD-I	Binary Coded Decimal	Current	Hybrid	0°C to 70°C		DH-24A
ADDAC80Z-CBI-V <sup>2</sup>	Binary	Voltage	Hybrid	0°C to 70°C		DH-24A
ADDAC80Z-CBI-I <sup>2</sup>	Binary	Current	Hybrid	0°C to 70°C		DH-24A
ADDAC80Z-CCD-V <sup>2</sup>	Binary Coded Decimal	Voltage	Hybrid	0°C to 70°C		DH-24A
ADDAC80Z-CCD-I <sup>2</sup>	Binary Coded Decimal	Current	Hybrid	0°C to 70°C	±1/4 LSB	DH-24A
ADDAC85C-CBI-V <sup>3</sup>	Binary	Voltage	Hybrid	0°C to 70°C	±1/2 LSB	DH-24A
ADDAC85C-CBI-I ADDAC85-CBI-V <sup>3</sup> ADDAC85-CBI-I <sup>3</sup>	Binary Binary Binary	Current Voltage	Hybrid Hybrid Hybrid	0°C to 70°C -25°C to +85°C -25°C to +85°C	±1/2 LSB ±1/2 LSB +1/2 LSB	DH-24A DH-24A DH-24A
ADDAC85-CBI-I ADDAC85LD-CBI-V <sup>3</sup> ADDAC85LD-CBI-I <sup>3</sup>	Binary Binary	Voltage Current	Hybrid Hybrid Hybrid	-25°C to +85°C -25°C to +85°C -25°C to +85°C	$\pm 1/2 \text{ LSB}$ $\pm 1/2 \text{ LSB}$ $\pm 1/2 \text{ LSB}$	DH-24A DH-24A DH-24A
ADDAC85MIL-CBI-V <sup>3</sup>	Binary	Voltage	Hybrid	–55°C to +125°C	±1/2 LSB	DH-24A
ADDAC85MIL-CBI-I <sup>3</sup>	Binary	Current	Hybrid	–55°C to +125°C	±1/2 LSB	DH-24A
ADDAC85C-CCD-V <sup>3</sup>	Binary Coded Decimal	Voltage	Hybrid	0°C to 70°C	±1/4 LSB	DH-24A
ADDAC85C-CCD-I <sup>3</sup>	Binary Coded Decimal	Current	Hybrid	0°C to 70°C	± 1/4 LSB	DH-24A
ADDAC85-CCD-V <sup>3</sup>	Binary Coded Decimal	Voltage	Hybrid	-25°C to +85°C	± 1/4 LSB	DH-24A
ADDAC85-CCD-I <sup>3</sup>	Binary Coded Decimal	Current	Hybrid	–25°C to +85°C	±1/4 LSB	DH-24A
ADDAC85MILCBII8	Binary	Current	Hybrid	–55°C to +125°C	±1/2 LSB	DH-24A
ADDAC85MILCBIV8	Binary	Voltage	Hybrid	–55°C to +125°C	±1/2 LSB	DH-24A
ADDAC87-CBI-V <sup>3</sup> ADDAC87-CBI-I <sup>3</sup> ADDAC87-CBI883 ADDAC87-CBIV883	Binary Binary Binary Binary	Voltage Current Current Voltage	Hybrid Hybrid Hybrid Hybrid	-55°C to +125°C -55°C to +125°C -55°C to +125°C -55°C to +125°C -55°C to +125°C	$\pm 1/2$ LSB $\pm 1/2$ LSB $\pm 1/2$ LSB $\pm 1/2$ LSB $\pm 1/2$ LSB	DH-24A DH-24A DH-24A DH-24A

#### **ORDERING GUIDE**

NOTES

<sup>1</sup>For outline information see Package Information section.

 $^{2}$ Z-Suffix devices guarantee performance of 0 V to +5 V and ±5 V spans with minimum supply voltages of ±11.4 V.

<sup>3</sup>These models have been discontinued. This is for historical information only.

#### **PRODUCT OFFERING**

Analog Devices has developed a number of technologies to support products within the data acquisition market. In serving the market new products are implemented with the technology best suited to the application. The DAC80 series of products was first implemented in hybrid form and now it is available in a single monolithic chip. We will provide both the hybrid and monolithic versions of the family so that in existing designs changes to documentation or product qualification will not have to be done. Specifications and ordering information for both versions are delineated in this data sheet.

#### **DIGITAL INPUT CODES**

The ADDAC80 Series accepts complementary digital input code in binary (CBI) format. The CBI model may be connected by the user for anyone of three complementary codes: CSB, COB or CTC.

#### Table I. Digital Input Codes

Digital Input	Analog Input							
MSB LSB	CSB	COB	CTC*					
	Compl.	Compl.	Compl.					
	Straight	Offset	Two's					
	Binary	Binary	Compl.					
00000000000	+Full-Scale	+Full-Scale	-1 LSB					
01111111111	+1/2 Full-Scale	Zero	-Full-Scale					
100000000000	Midscale	-1 LSB	+Full-Scale					
111111	Zero	-Full-Scale	Zero					

\*Invert the MSB of the COB code with an external inverter to obtain CTC code.

#### ACCURACY

Accuracy error of a D/A converter is the difference between the analog output that is expected when a given digital code is applied and the output that is actually measured with that code applied to the converter. Accuracy error can be caused by gain error, zero error, linearity error, or any combination of the three. Of these three specifications, the linearity error specification is the most important since it cannot be corrected. Linearity error is specified over its entire temperature range. This means that the analog output will not vary by more than its maximum specification, from an ideal straight line drawn between the end points (inputs all "1"s and all "0"s) over the specified temperature range.

Differential linearity error of a D/A converter is the deviation from an ideal 1 LSB voltage change from one adjacent output state to the next. A differential linearity error specification of  $\pm 1/2$  LSB means that the output voltage step sizes can range from 1/2 LSB to 1 1/2 LSB when the input changes from one adjacent input state to the next.

#### DRIFT

#### **Gain Drift**

A measure of the change in the full scale range output over temperature expressed in parts per million of full scale range per °C (ppm of FSR/°C). Gain drift is established by: 1) testing the end point differences for each ADDAC80 model at the lowest operating temperature,  $25^{\circ}$ C and the highest operating temperature; 2) calculating the gain error with respect to the  $25^{\circ}$ C value and; 3) dividing by the temperature change.

#### **Offset Drift**

A measure of the actual change in output with all "1"s on the input over the specified temperature range. The maximum change in offset is referenced to the offset at 25°C and is divided by the temperature range. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

#### SETTLING TIME

Settling time for each model is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input.

#### **Voltage Output Models**

Three settling times are specified to 0.01% of full scale range (FSR); two for maximum full scale range changes of 20 V, 10 V and one for a 1 LSB change. The 1 LSB change is measured at the major carry (0 1 1 1 . . . 1 1 to 1 0 0 0 . . . 0 0), the point at which the worst case settling time occurs. The settling time characteristic depends on the compensation capacitor selected, the optimum value is 25 pF as shown in Figure 3a.

#### **Current Output Models**

Two settling times are specified to  $\pm 0.01\%$  of FSR. Each is given for current models connected with two different resistive loads:  $10 \Omega$  to  $100 \Omega$  and  $1000 \Omega$  to  $1875 \Omega$ . Internal resistors are provided for connecting nominal load resistances of approximately  $1000 \Omega$ to  $1800 \Omega$  for output voltage ranges of  $\pm 1$  V and 0 V to -2 V.



Figure 3a. Voltage Model Settling Time Circuit



Figure 3b. Voltage Model Settling Time  $C_F = 25 \text{ pF}$ 

#### POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a percent of FSR per percent of change in either the positive or negative supplies about the nominal power supply voltages.

#### **REFERENCE SUPPLY**

All models are supplied with an internal 6.3 V reference voltage supply. This voltage (Pin 24) is accurate to  $\pm 1\%$  and must be connected to the Reference Input (Pin 16) for specified operation. This reference may also be used externally with external current drain limited to 2.5 mA. An external buffer amplifier is recommended if this reference is to be used to drive other system components. Otherwise, variations in the load driven by the reference will result in gain variations. All gain adjustments should be made under constant load conditions.

# ANALYZING DEVICE ACCURACY OVER THE TEMPERATURE RANGE

For the purposes of temperature drift analysis, the major device components are shown in Figure 4. The reference element and buffer amplifier drifts are combined to give the total reference temperature coefficient. The input reference current to the DAC,  $I_{REF}$ , is developed from the internal reference and will show the same drift rate as the reference voltage. The DAC output current,  $I_{DAC}$ , which is a function of the digital input codes, is designed to track  $I_{REF}$ ; if there is a slight mismatch in these currents over temperature, it will contribute to the gain T.C. The bipolar offset resistor,  $R_{BP}$ , and gain setting resistor,  $R_{GAIN}$ , also have temperature coefficients that contribute to system drift errors. The input offset voltage drift of the output amplifier, OA, also contributes a small error.



#### Figure 4. Bipolar Configuration

There are three types of drift errors over temperature: offset, gain, and linearity. Offset drift causes a vertical translation of the entire transfer curve; gain drift is a change in the slope of the curve; and linearity drift represents a change in the shape of the curve. The combination of these three drifts results in the complete specification for total error over temperature.

Total error is defined as the deviation from a true straight line transfer characteristic from exactly zero at a digital input that calls for zero output to a point that is defined as full-scale. A specification for total error over temperature assumes that both the zero and full-scale points have been trimmed for zero error at 25°C. Total error is normally expressed as a percentage of the full-scale range. In the bipolar situation, this means the total range from  $-V_{FS}$  to  $+V_{FS}$ .

Several new design concepts not previously used in DAC80-type devices contribute to a reduction in all the error factors over temperature. The incorporation of low temperature coefficient silicon-chromium thin-film resistors deposited on a single chip, a patented, fully differential, emitter weighted, precision current steering cell structure, and a T.C. trimmed buried Zener diode reference element results in superior wide temperature range performance. The gain setting resistors and bipolar offset resistor are also fabricated on the chip with the same SiCr material as the ladder network, resulting in low gain and offset drift.

#### MONOTONICITY AND LINEARITY

The initial linearity error of  $\pm 1/2$  LSB max and the differential linearity error of  $\pm 3/4$  LSB max guarantee monotonic performance over the specified range. It can therefore be assumed that linearity errors are insignificant in computation of total temperature errors.

#### **UNIPOLAR ERRORS**

Temperature error analysis in the unipolar mode is straightforward: there is an offset drift and a gain drift. The offset drift (which comes from leakage currents and drift in the output amplifier (OA)) causes a linear shift in the transfer curve as shown in Figure 5. The gain drift causes a change in the slope of the curve and results from reference drift, DAC drift, and drift in  $R_{GAIN}$  relative to the DAC resistors.

#### **BIPOLAR RANGE ERRORS**

The analysis is slightly more complex in the bipolar mode. In this mode  $R_{BP}$  is connected to the summing node of the output amplifier (see Figure 4) to generate a current that exactly balances the current of the MSB so that the output voltage is zero with only the MSB on.

## ADDAC80/ADDAC85/ADDAC87

Note that if the DAC and application resistors track perfectly, the bipolar offset drift will be zero even if the reference drifts. A change in the reference voltage, which causes a shift in the bipolar offset, will also cause an equivalent change in  $I_{REF}$  and thus  $I_{DAC}$ , so that  $I_{DAC}$  will always be exactly balanced by  $I_{BP}$  with the MSB turned on. This effect is shown in Figure 5. The net effect of the reference drift then is simply to cause a rotation in the transfer around bipolar zero. However, consideration of second order effects (which are often overlooked) reveals the errors in the bipolar mode. The unipolar offset drifts previously discussed will have the same effect on the bipolar offset. A mismatch of  $R_{BP}$  to the DAC resistors is usually the largest component of bipolar drift, but in the ADDAC80 this error is held to 10 ppm/°C max. Gain drift in the DAC also contributes to bipolar offset drift, as well as full-scale drift, but again is held to 10 ppm/°C max.



Figure 5. Unipolar and Bipolar Drifts

#### USING THE ADDAC80 SERIES POWER SUPPLY CONNECTIONS

For optimum performance power supply decoupling capacitors should be added as shown in the connection diagrams. These capacitors (1  $\mu$ F electrolytic recommended) should be located close to the ADDAC80. Electrolytic capacitors, if used, should be paralleled with 0.01  $\mu$ F ceramic capacitors for optimum high frequency performance.

#### EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and gain may be trimmed by installing external OFFSET and GAIN potentiometers. These potentiometers should be connected as shown in the block diagrams and adjusted as described below. TCR of the potentiometers should be 100 ppm/°C or less. The 3.9 M $\Omega$  and 10 M $\Omega$  resistors (20% carbon or better) should be located close to the ADDAC80 to prevent noise pickup. If it is not convenient to use these high-value resistors, a functionally equivalent "T" network, as shown in Figure 8 may be substituted in each case. The gain adjust (Pin 23) is a high impedance point and a 0.01 µF ceramic capacitor should be connected from this pin to common to prevent noise pickup.



Figure 6. External Adjustment and Voltage Supply Connection Diagram, Current Model

#### **Offset Adjustment**

For unipolar (CSB) configurations, apply the digital input code that should produce zero potential output and adjust the OFFSET potentiometer for zero output. For bipolar (COB, CTC) configurations, apply the digital input code that should produce the maximum negative output voltage. Example: If the FULL SCALE RANGE is connected for 20 V, the maximum negative output voltage is –10 V. See Table II for corresponding codes.

#### Gain Adjustment

For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive voltage output. Adjust the GAIN potentiometer for this positive full-scale voltage. See Table II for positive full-scale voltages.



Figure 7. External Adjustment and Voltage Supply Connection Diagram, Voltage Model



Figure 8. Equivalent Resistances

Digital Input	Analog Output								
12-Bit Resolution	Voltag	ge*	Current						
MSB         LSB           0 0 0 0 0 0 0 0 0 0 0 0 0 0         0 0 0           0 1 1 1 1 1 1 1 1 1 1         1 1 1           1 0 0 0 0 0 0 0 0 0 0 0 0         0 0	<b>0 to +10 V</b>	<b>±10 V</b>	<b>0 to -2 mA</b>	<b>±1 mA</b>					
	+9.9976 V	+9.9951 V	-1.9995 mA	-0.9995 mA					
	+5.0000 V	0.0000 V	-1.0000 mA	0.0000 mA					
	+4.9976 V	4.88 mV	-0.9995 mA	+0.0005 mA					
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	0.0000 V	–10.0000 V	0.0000 mA	–1.00 mA					
	2.44 mV	–0.0049 V	0.488 μA	0.488 μA					

Table II. Digital Input Analog Output

\*To obtain values for other binary ranges 0 to 5 V range: divide 0 to 10 values by 2;  $\pm$ 5 V range: divide  $\pm$ 10 V range values by 2;  $\pm$ 2.5 V range: divide  $\pm$ 10 V range values by 4.

#### **VOLTAGE OUTPUT MODELS**

Internal scaling resistors provided in the ADDAC80 may be connected to produce bipolar output voltage ranges of  $\pm 10$  V,  $\pm 5$  V or  $\pm 2.5$  V or unipolar output voltage ranges of 0 V to  $\pm 5$  V or 0 V to  $\pm 10$  V (see Figure 9).



Figure 9. Output Amplifier Voltage Range Scaling Circuit

Gain and offset drift are minimized in the ADDAC80 because of the thermal tracking of the scaling resistors with other device components. Connections for various output voltage ranges are shown in Table III. Settling time is specified for a full-scale range change: 4  $\mu$ s for a 10 k $\Omega$  feedback resistor; 3  $\mu$ s for a 5 k $\Omega$ feedback resistor when using the compensation capacitor shown in Figure 3a.

The equivalent resistive scaling network and output circuit of the current model are shown in Figures 10 and 11. External  $R_{LS}$  resistors are required to produce exactly 0 V to -2 V or  $\pm 1$  V output. TCR of these resistors should be  $\pm 100$  ppm/°C or less to maintain the ADDAC80 output specifications. If exact output ranges are not required, the external resistors are not needed.



Figure 10. Internal Scaling Resistors



Figure 11. ADDAC80 Current Model Equivalent Output Circuit

Internal resistors are provided to scale an external op amp or to configure a resistive load to offer two output voltage ranges of  $\pm 1$  V or 0 V to -2 V. These resistors ( $R_{LI}$  TCR = 20 ppm/°C) are an integral part of the ADDAC80 and maintain gain and bipolar offset drift specifications. If the internal resistors are not used, external  $R_L$  (or  $R_F$ ) resistors should have a TCR of  $\pm 25$  ppm/°C or less to minimize drift. This will typically add  $\pm 50$  ppm/°C + the TCR of  $R_L$  (or  $R_F$ ) to the total drift.

Output Range	Digital Input Codes	Connect Pin 15 to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10 V	COB or CTC	19	20	15	24
±5 V	COB or CTC	18	20	NC	24
±2.5 V	COB or CTC	18	20	20	24
0 V to 10 V	CSB	18	21	NC	24
0 V to 5 V	CSB	18	21	20	24
0 V to 10 V	CCD	19	NC	15	24

 Table III. Output Voltage Range Connections, Voltage Model ADDAC80

NC = No Connect

#### DRIVING A RESISTIVE LOAD UNIPOLAR

A load resistance,  $R_L = R_{LI}$ , +  $R_{LS}$ , connected as shown in Figure 12 will generate a voltage range,  $V_{OUT}$ , determined by:

$$V_{OUT} = -2 \ mA\left(\frac{6.6 \ k\Omega \times R_L}{6.6 \ k\Omega + R_L}\right) \tag{1}$$

where  $R_L \max = 1.54 \text{ k}\Omega$  and  $V_{OUT} \max = -2.5 \text{ V}$ 

To achieve specified drift, connect the internal scaling resistor  $(R_{LI})$  as shown in Table IV to an external metal film trim resistor  $(R_{LS})$  to provide full scale output voltage range of 0 V to -2 V. With  $R_{LS} = 0$  V,  $V_{OUT} = -1.69$  V.



Figure 12. Equivalent Circuit ADDAC80-CBI-I Connected for Unipolar Voltage Output with Resistive Load

#### DRIVING A RESISTOR LOAD BIPOLAR

The equivalent output circuit for a bipolar output voltage range is shown in Figure 13,  $R_L = R_{LI} + R_{LS}$ .  $V_{OUT}$  is determined by:

$$V_{OUT} = \pm 1 \, mA \left( \frac{R_L \times 3.22 \, k\Omega}{R_L + 3.22 \, k\Omega} \right) \tag{2}$$

where  $R_L \max = 11.18 \text{ k}\Omega$  and  $V_{OUT} \max = \pm 2.5 \text{ V}$ 

To achieve specified drift, connect the internal scaling resistors  $(R_{LI})$  as shown in Table IV for the COB or CTC codes and add an external metal film resistor  $(R_{LS})$  in series to obtain a full scale output range of  $\pm 1$  V. In this configuration, with  $R_{LS}$  equal to zero, the full scale range will be  $\pm 0.874$  V.



Figure 13. ADDAC80-CBI-I Connected for Bipolar Output Voltage with Resistive Load

#### DRIVING AN EXTERNAL OP AMP

The current model ADDAC80 will drive the summing junction of an op amp used as a current to voltage converter to produce an output voltage. As seen in Figure 14,

$$V_{OUT} = I_{OUT} \times R_F \tag{3}$$

where  $I_{OUT}$  is the ADDAC80 output current and  $R_F$  is the feedback resistor. Using the internal feedback resistors of the current model ADDAC80 provides output voltage ranges the same as the voltage model ADDAC80. To obtain the desired output voltage range when connecting an external op amp, refer to Table V and Figure 14.



\*FOR FAST SETTLING TIME

Figure 14. External Op Amp Using Internal Feedback Resistors

#### **OUTPUT LARGER THAN 20 V RANGE**

For output voltage ranges larger than  $\pm 10$  V, a high voltage op amp may be employed with an external feedback resistor. Use  $I_{OUT}$  values of  $\pm 1$  mA for bipolar voltage ranges and -2 mA for unipolar voltage ranges (see Figure 15). Use protection diodes when a high voltage op amp is used.

The feedback resistor,  $R_F$ , should have a temperature coefficient as low as possible. Using an external feedback resistor, overall drift of the circuit increases due to the lack of temperature tracking between  $R_F$  and the internal scaling resistor network. This will typically add 50 ppm/°C +  $R_F$  drift to total drift.



\*FOR OUTPUT VOLTAGE SWINGS UP TO 140V p-p

Figure 15. External Op Amp Using External Feedback Resistors

		<b>T</b> , <b>1</b>	1% Metal Film	R	<sub>LI</sub> Connectio	ns	Reference	Bipolar Offset	
Digital Input Codes	Output Range	Resistance $R_{LI}(k\Omega)$	Resistance R <sub>LS</sub>	Connect Pin 15 to	Connect Pin 18 to	Connect Pin 20 to	Connect Pin 16 to	Connect Pin 17 to	R <sub>LS</sub>
CSB	0 to -2 V	0.968	210 Ω	20	19 and $R_{LS}$	15	24	Com (21)	Between Pin 18 and Com (21)
COB or CTC	±1 V	1.2	249 Ω	18	19	R <sub>LS</sub>	24	15	Between Pin 20 and Com (21)
CCD	0 to $\pm 2$ V	3	N/A	NC	21	NC	24	NC	N/A

Table IV. Current Model/Resistive Load Connections

Output Range	Digital Input Codes	Connect A to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10 V	COB or CTC	19	15	A	24
±5 V	COB or CTC	18	15	NC	24
±2.5 V	COB or CTC	18	15	15	24
0 V to 10 V	CSB	18	21	NC	24
0 V to 5 V	CSB	18	21	15	24

Table V. External Op Amp Voltage Mode Connections

#### **OUTLINE DIMENSIONS**

Dimensions shown in inches and (mm).





CONTROLLING DIMENSIONS ARE IN MILLIMETERS: INCH DIMENSIONS ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN





NOTES

- 1. INDEX AREA; A NOTCH OR A LEAD ONE IDENTIFICATION MARK IS LOCATED ADJACENT TO LEAD ONE.
- 2 THE MINIMUM LIMIT FOR DIMENSION MAY BE 0.023" (0.58 mm) FOR ALL FOUR CORNER LEADS ONLY. DIMENSION SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
- 3. THIS DIMENSION ALLOWS FOR OFF-CENTER LID, MENISCUS AND GLASS OVERRUN. APPLIES TO ALL FOUR CORNERS. 4.

5.

ALL LEADS — INCREASE MAXIMUM LIMIT BY 0.003" (0.08 mm) MEASURED AT THE CENTER OF THE FLAT, WHEN HOT SOLDER DIP LEAD FINISH IS APPLIED. 6.

7. TWENTY TWO SPACES.

CONTROLLING DIMENSIONS ARE IN MILLIMETERS. INCH DIMENSIONS ARE ROUNDED-OFF MILLIMETER 8. EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

#### **OUTLINE DIMENSIONS**

Dimensions shown in inches and (mm).

#### 24-Lead Side Brazed Ceramic DIP for Hybrid (DH-24A)



NOTES

- NOTES 1. INDEX AREA; A NOTCH OR A LEAD ONE IDENTIFICATION MARK IS LOCATED ADJACENT TO LEAD ONE. 2. THE MINIMUM LIMIT FOR DIMENSION MAY BE 0.023" (0.58 mm) FOR ALL FOUR CORNER LEADS ONLY. 3. DIMENSION SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE. 4. THE BASIC PIN SPACING IS 0.100" (2.54 mm) BETWEEN CENTERLINES. 5. APPLIES TO ALL FOUR CORNERS. 6. SHALL BE MEASURED AT THE CENTERLINE OF THE LEADS. 7. TWENTY TWO SPACES. 8. CONTROLLING DIMENSIONS ARE IN MILLIMETERS: INCH DIMENSIONS ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

# **Revision History**

Location

Page

Data Sheet changed from REV. A to REV. B.
Update OUTLINE DIMENSION drawings

C00381-0-1/02(B)



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