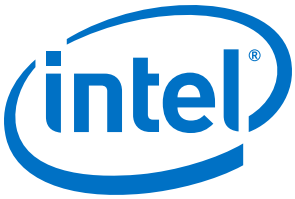

Intel® Stratix® 10 SX SoC Development Kit User Guide

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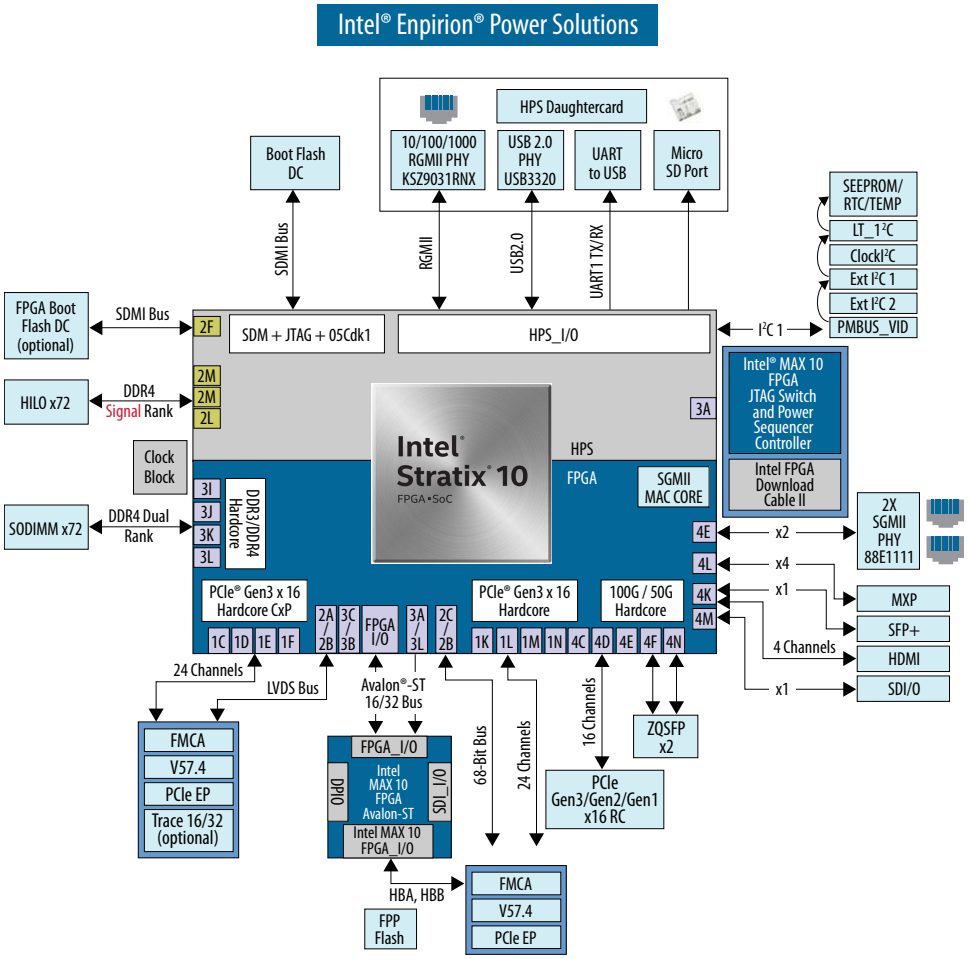
1. Overview

This document describes the features of the Intel® Stratix® 10 SoC development kit, including detailed pin-out and component reference information required to create custom FPGA designs that interface with all components of the board.

1.1. General Development Kit Description

The Intel Stratix 10 SoC development board provides a hardware platform for developing and prototyping low-power, high-performance and logic-intensive designs using Intel Stratix 10 SoC. The board provides a wide range of peripherals and memory interfaces to facilitate the development of Intel Stratix 10 SoC designs.

Figure 1. Intel Stratix 10 SoC Development Kit Block Diagram



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1.2. Recommended Operating Conditions

- Recommended ambient operating temperature range: 0 °C to 45 °C
- Maximum ICC load current: 190 A
- Maximum ICC load transient percentage: 30%
- FPGA maximum power supported by the supplied heatsink/fan: 300 W

1.3. Handling the Development Kit

When handling the board, it is important to observe static discharge precautions.

Caution: Without proper anti-static handling, the board can be damaged. Therefore, use anti-static handling precautions when touching the board.

Caution: You must not operate this development kit in a vibration environment.

2. Getting Started

2.1. Installing Quartus Prime Software

The Intel Quartus® Prime design software is a multiplatform design environment that easily adapts to your specific needs in all phases of FPGA, CPLD, and SoC designs. The Intel Quartus Prime software delivers the highest performance and productivity for Intel FPGAs, CPLDs, and SoCs.

Design software must enable dramatically increased design productivity in order to take advantage of devices with multi-million logic elements with increased capabilities that provide designers with an ideal platform to meet next-generation design opportunities.

The new Intel Quartus Prime Design Suite design software includes everything needed to design for Intel FPGAs, SoCs and CPLDs from design entry and synthesis to optimization, verification and simulation. The Intel Quartus Prime Design Suite software includes an additional Spectra-Q® engine that is optimized for Intel Stratix 10 and future devices. The Spectra-Q engine enables new levels of design productivity for next generation programmable devices with a set of faster and more scalable algorithms, a hierarchical database infrastructure and a unified compiler technology.

Intel Quartus Prime

The Intel Quartus Prime Design Suite software is available in three editions based on specific design requirements: Pro, Standard, and Lite Edition.

The Intel Quartus Prime Pro Edition is optimized to support the advanced features in Intel's next generation FPGAs and SoCs and requires a paid license.

Intel Quartus Prime Standard Edition includes the most extensive support for Altera's latest device families and requires paid license.

Intel Quartus Prime Lite Edition provides an ideal entry point to Altera's high-volume device families and is available as a free download with no license file required.

Included in the Intel Quartus Prime Pro Edition are the Intel Quartus Prime software, Nios® II EDS and the MegaCore IP Library.

To install Intel's development tools, download the Intel Quartus Prime Pro Edition software from the Quartus Prime Pro Edition page in the Download Center of Intel's website.

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2.2. Installing the Intel FPGA Download Cable

The Intel Stratix 10 SoC Development Kit includes embedded Intel FPGA Download Cable circuits for FPGA and Intel MAX® 10 programming. However, for the host computer and board to communicate, you must install the Intel FPGA Download Cable driver on the host computer.

Installation instructions for the Intel FPGA Download Cable driver for your operating system are available on the Intel website.

On the Intel website, navigate to the Cable and Adapter Drivers Information link to locate the table entry for your configuration and click the link to access the instructions.

2.3. Installing the Intel SoC Embedded Development Suite (EDS)

The Intel SoC EDS is a comprehensive software tool suite for embedded software development on Intel SoC devices. It contains development tools, utility programs, run-time software, and application examples to expedite firmware and application software of SoC embedded systems.

As a part of the Intel SoC EDS, the Arm* Development Studio 5 (DS-5) Intel SoC FPGA Edition Toolkit provides a comprehensive set of embedded development tools for Intel's SoC FPGAs.

For more information and steps to install the SoC EDS Tool Suite refer to the links below.

Related Information

- Arm Development Studio 5 (DS-5) Intel SoC FPGA Edition
- Intel SoC FPGA Embedded Development Suite User Guide

2.4. Installing the Intel Stratix 10 SX SoC Development Kit Package

The Intel Stratix 10 SX SoC Development Kit offers a quick and simple approach for developing custom Arm processor-based SoC designs. The Intel Stratix 10 SX SoCs offer full software compatibility with previous generation SoCs, a broad ecosystem of Arm software and tools, and the enhanced FPGA and digital signal processing (DSP) hardware design flow.

Intel Stratix 10 SX SoC Development Kit Package Installer is a single installation file contains that Intel Stratix 10 SX SoC Development Kit board design files, documents, and examples including the Board Test System (BTS) installation files.

Download and unzip Intel Stratix 10 SX SoC Development Kit Package Installer first. Install the Intel Stratix 10 SX SoC Board Test System.

Note: To view the the layout `*.brd` files in the board package, you can download the Cadence® Allegro®/OrCAD® Free Viewer from Cadence's website.

For additional information, refer to the Intel Stratix 10 SX SoC Development Kit webpage on Intel's website using the link provided at the end of this section.

Related Information

- Intel Stratix 10 SX SoC Development Kit
- Cadence Allegro Downloads

3. Development Kit Setup

The instructions in this chapter explain how to setup the Intel Stratix 10 SoC Development Board.

3.1. Inspect the Development Kit

To inspect the board, perform the following steps:

1. Place the board on an anti-static surface and inspect it to ensure that it has not been damaged during shipment.
2. Verify that all components on the board appear in place and intact.

Caution: Without proper anti-static handling, you could damage the board.

Table 1. Stratix 10 SoC Development Kit Contents

Item	Quantity
Intel Stratix 10 SoC Development Board	1
USB Cable	2
USB Cable Micro	1
Ethernet Cable	1
HPS IO48 OOBE Daughter Card	1
HPS IO48 NAND Daughter Card	1
DDR4 HILO Memory Card	1
SODIMM Memory Card	1
QSPI Flash	1
SD Micro Flash	1
Linear Dongle	1
Intel Intel Enpirion® Dongle EVI-EM2COMIF	1

Related Information

- Thermal Management for FPGAs
- Intel Intel Enpirion Digital Power Configurator Graphical User Interface (GUI)

3.2. Default Setup of the Development Kit

This development kit ships with its board switches preconfigured to support the design examples in the kit.

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1. Power up the development board by using the included power supply.
2. When configuration is complete, the configuration done green LED (D22) illuminates, signaling that the Intel Stratix 10 device is configured successfully.

Caution: Use only the provided power supply. Power regulation circuits on the board can be damaged by power supplies with greater voltage and a lower-rated power supply may not be able to provide enough power for the board.

Table 2. Default Setup

Checkpoint	Name	Reference	Description
1	Power Switch	SW7	Power is turn off at left position
2	Power Adapter connector	J25, J55	Both connectors can be used to connect the power adapter
3	Intel Intel Enpirion	J29	You can install Intel Enpirion dongle to monitor the board power rails. Switch 8 is at off position.
4	JTAG Dongle connector	J1	You can install Intel JTAG dongle to access FPGA
5	JTAG Switch	SW1	Default Setup from bit 1 to bit 8 is "off, off, on, on, on, on, on, on": Intel Stratix 10 SoC and Intel MAX 10 are on the JTAG chain
6	USB JTAG Port	J57	You need connect Micro USB cable to access Intel Stratix 10 SoC
7	12V Fan Connector	J16	You need use it to connect thermal Fan
8	Boot Switch	SW4	Default set up from bit 1 to Bit 4 is "on, off, on, off" FPGA/HPS I^2C is enabled. Daughter card power is on
9	MSEL Switch	SW2	Default Setup is "on on on on": JTAG mode

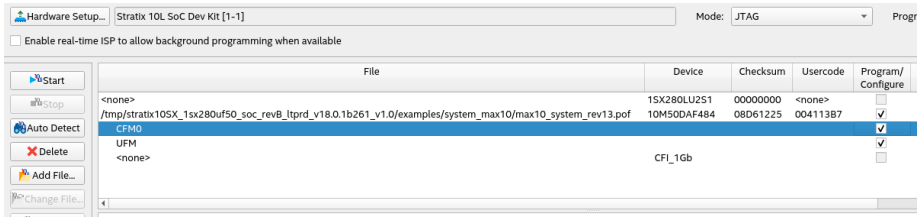
3.3. Intel MAX 10 System Controller Updates

The Intel MAX 10 System Controller manages several features on the Intel Stratix 10 SX SoC Development kit, including clocks, I^2C, and some configuration signals. In certain situations, it may be necessary to ensure the Intel MAX 10 System Controller internal flash contains the latest available design. This may include the Intel Stratix 10 device failing to configure from `OSC_CLK_1`, or when other unexpected issues arise. The latest System Controller design is included in the Intel Stratix 10 SX Soc Development Kit Installer Package, in the "`system_max10`" folder inside the "`examples`" folder.

To update the internal flash, follow the steps outlined in the procedure below:

1. Power off the Intel Stratix 10 SX SoC Development Kit.
2. Ensure **SW1** and **SW2** are set to the default settings so the System Intel MAX 10 is on the JTAG chain and the Intel Stratix 10 device does not automatically configure itself.
3. Connect a micro USB cable to **J57** for JTAG access and power on the board.
4. Open the Intel Quartus Prime Programmer and scan the device chain.

5. Right click on the Intel MAX 10 and select "**Change File**". Navigate to the "`system_max10`" folder and select the `.pof` file, for example, "`max10_system_rev13.pof`".
6. Check the **Program/Verify** box in the row with the `.pof` and the Intel MAX 10 Device. The **Program/Verify** boxes in the immediately following rows, **CFM0** and **UFM**, will auto-check as well. Refer to the following screenshot:



7. Click **Start** and wait for the programming cycle to finish.
8. Power off the board and reset **SW1** and **SW2** to prior settings, if any.

4. Development Kit Components

This chapter introduces the major components on the Intel Stratix 10 Development Board. The board overview figure illustrates the component locations and the board components table provides a brief description of all component features of the board.

4.1. Development Kit Feature Summary

Table 3. Intel Stratix 10 SoC Development Kit Feature Summary

Feature	Description
Programmable Logic	• 1SX280LU2F50E2VGS2 Intel Stratix 10 SoC FPGA • 10M04SCU169C8G Intel MAX 10 CPLD as the Intel FPGA Download Cable and JTAG switch device • 10M16SAU169C8G Intel MAX 10 CPLD as the Power manager and sequencer device • 10M50DAF484I7G Intel MAX 10 CPLD as the IO level translator, IO MUX and Passive AVST-16 FPGA controller device
HPS memory	1066 MHz 4 GB 72-bit HILO memory card
HPS Boot Flash (Flash Card)	• Boot Codes for QSPI, SD Micro • QSPI Flash: 256 MB (MT25QU02GCBB8E12-0SIT) • SD Micro Flash Card: 16 GB (Kingston)
HPS IO48 OOBE Daughter Card	• One HPS IO48 60-pin Samtec Connector • One RGMII 10/100/1000 Mbps Ethernet port: Standard RJ-45 • One UART port: Standard USB Mini-B Receptacle • One Micro SD Card Connector: Standard Micro SD Card Socket • One USB 2.0 port: Standard USB Micro-AB Receptacle • One Mictor 38-pin connector (JTAG only without Trace signals) — Two JTAG targets selected by the resistors MUX: FPGA JTAG chain (optional) and HPS JTAG Port (default) • I^2C: HPS I^2C port • GPIO — 2 Push buttons — 3 LEDs — 1 Ethernet Interrupt from Ethernet PHY — 1 USB over-current indicator • HPS Clock: 25 MHz oscillator
HPS IO48 NAND Flash Daughter Card	• One HPS IO48 60-pin Samtec connector • One RGMII 10/100/1000 Mbps Ethernet port: Standard RJ-45 • One UART port: Standard USB Mini-B Receptacle • NAND Flash (x16): 8 Gb • eMMC (x8): 8 GB 5.0 compliant eMMC

continued...

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Feature	Description
	• I^2C: HPS I^2C port • GPIO — 2 Push Buttons — 3 LEDs — 1 Ethernet Interrupt from Ethernet PHY • HPS Clock: 25 MHz oscillator
FPGA memory	1200 MHz 16 GB DDR4 SO-DIMM MTA18ASF2G72HZ – 2G6
FPGA File Flash (Flash Card)	• NAND Flash (x8): 1 GB • QSPI Flash: 256 MB • SD Micro Flash Card: 16 GB (Kingston)
Two V57.4 High Pin Count FMC+ Slots	• 28 Gbps signals: Insertion loss less than 5 dB, return loss less than 10 dB • FMC+ PCIe* Gen3 x16 cable • FMCPCIe Gen3 x8 cable • 16/32 bit trace
FPGA PCIe Gen 1/2/3 x16 RC Slot	• 75 W Power • Meets PCIe specifications
FPGA Communication Ports	• Two 28 Gbps ZQSFP+ Ports: 100/50 Gbps IP, Insertion loss less than 5 dB, return loass less than 10 dB • One 10 Gbps SFP+ Port: 10 Gbps Ethernet IP • SMA Test Port: Up to four 28 Gbps channels, inseertion loss less than 5 dB, return loss less than 10 dB, one external reference clock • One DB-9 RS-232 Port (MAX3221)
FPGA Debug Ports	Intel FPGA Download Cable Direct Port & JTAG
FPGA Reference Clocks	• Clock Cleaner — 122.88 MHz (Network) — 644.5312 MHz (Network) — 297 MHz (SDI) — 245 MHz (SDI) • Clock Generators — LMH1983 (27 MHz, 148.5 MHz) — Si5388 (133.33 MHz) — PCIe (100 MHz) — Si5338 (148 MHz, 100 MHz, 27 MHz, 100 MHz) — Si5341 (155.52 MHz, 644.53125 MHz, 135 MHz, 156.25 MHz, 625 MHz, 100 MHz, 125 MHz, 125 MHz)
I^2C Devices	• 4 KB SEEPROM • Real Time Clock • Silicon Labs™ Clock Generators • FMC+ Slots • PCIe Slots • SFP+ • ZQSFP • Clock Cleaner • Power Supplies
Intel MAX 10 Controller I/O CPLD Features	• System Reset Controller • FPGA PS AVST Configuration Controller • I^2C Master Controller • UART Level Shifter • FPGA I/O MUX • SDI/HDMI/QSFP/SFP+ I/O level shift

continued...

Feature	Description
Intel MAX 10 Power CPLD Sequencer	FPGA, PCIe, FMC+ slots power sequencer, Reset.
Intel MAX 10 CPLD Features	• Intel FPGA Download Cable II • JTAG Switch — Input JTAG Sources (Intel FPGA Download Cable II, 10-pin Program Header, FMCA+, FMCB+, Mictor JTAG) — Output JTAG Sources (Intel MAX 10 A JTAG, MAX10B JTAG, Intel Stratix 10 JTAG, FMCA+, FMCB+, PCIe) — JTAG Program — User I/O
User I/O	• 4 Push Buttons • 4-bit Dipswitch • 4 User LEDs • 2-pin I/O Header • System Intel MAX 10 LEDs and 4-bit switch
Power	• Volgen KTPS200-12160, 12V, 24A • ATX-Power
Mechanical	• 8.5" x 14.5" Rectangular Form Factor • Liquid cool thermal heat sink (300W @ 35C)
System Monitor	Power, Voltage, Current

4.2. Board Components

Figure 2. Board Picture (Top View)

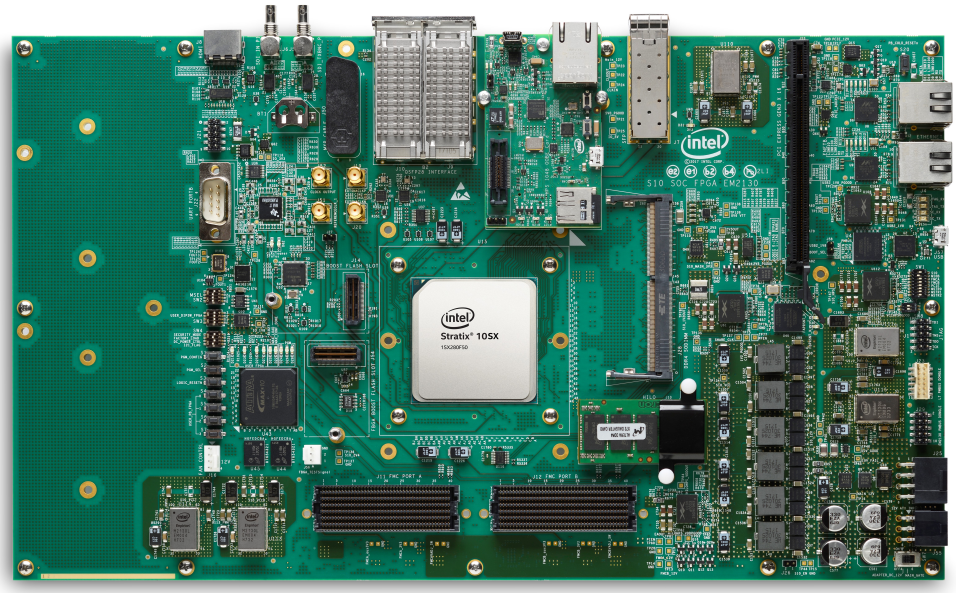
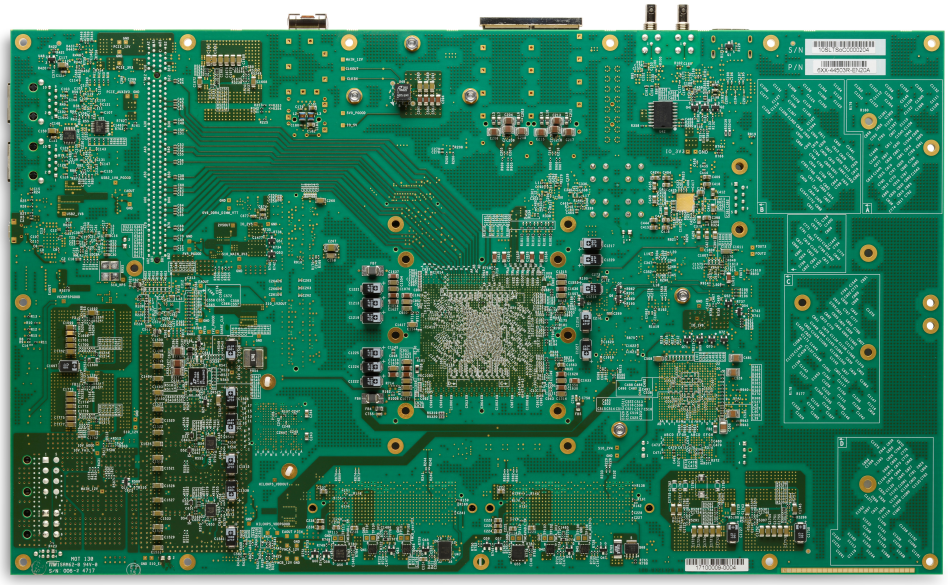


Figure 3. Board Picture (Bottom View)



Board Components Table

Table 4. Intel Stratix 10 SoC Board Components Table

Board Reference	Type	Description
Featured Device		
U15	FPGA	Intel Stratix 10 SoC 1SX280LU2F50E2VGS2 FPGA
U43	CPLD	Intel MAX 10 10M50DAF484I7G System Controller
U46	CPLD	Intel MAX 10 10M16SAU169C8G Power Manager CPLD
Configuration, Status and Setup Elements		
J1	JTAG chain header	Provides access to the JTAG chain and disables the on-board Intel FPGA Download Cable II when using an external JTAG debugger such as an Intel FPGA Download Cable II
SW1	JTAG chain control DIP switch	Remove or include devices in the active JTAG chain
SW2	MSEL DIP Switch	Controls the configuration scheme on the board. MSEL pin 0,1,2 connect to the DIP Switch
J57	Micro-USB Header	USB interface to on-board Intel FPGA Download Cable II JTAG for programming and debugging HPS, FPGA orIntel MAX 10 CPLD through a type-B Micro-USB cable.
SW4	Function DIP Switch	Selects I^2C master, controls PCIe slot power and selects FPGA image source
SW8	Power Switch	ON position: Power GUI

continued...

Board Reference	Type	Description
		OFF position: Intel Enpirion dongle
S2	Program select push button	Toggles the program select LEDs which selects the program image that loads from flash memory to the FPGA
S1	Configure push button	Load image from flash memory to the FPGA based on the settings of the program select LEDs
D22	Configuration done LED	Illuminates when the FPGA is configured
D20	Load LED	Illuminates when the Intel MAX 10 CPLD System Controller
D19	Error LED	Illuminates when the FPGA configuration from flash memory fails
D31	Power LED	Illuminates when 3.3V power is present
D1, D2	JTAG TX/RX LEDs	Indicates the transmit or receive activity of the JTAG chain. The TX and RX LEDs flicker if the link is in use and active. The LEDs are either off when not in use or on when in use but idle
D24, D26, D28	Program select LEDs	Illuminates to show which flash memory image loads to the FPGA when you press the program select push button
D29, D30	FMC port present LEDs	Illuminates when a daughtercard is plugged into the FMC port
Clock Circuits		
U26	Multi-output oscillator	Si5338A quad-output fixed oscillator with 148.5 MHz, 100 MHz, 27 MHz and 100 MHz outputs
U29	50-MHz oscillator	50 MHz crystal oscillator for general purpose logic
U25	Multi-output oscillator	Two 100 MHz outputs for PCIe application
J19, J20	Clock input SMA connector	External clock inputs for the transceiver test port
U33	Multi-output oscillator	Si5341 ten-output fixed oscillator
U31	Multi-output oscillator	Si5338A quad-output fixed oscillator with four 133.33 MHz outputs
U34	Multi-output clock cleaner	LMK05028 Clock Cleaner
General User Input/Output		
D21, D23, D25, D27	User LEDs	Four user LEDs. Illuminate when driven high.
SW3	User DIP Switch	User DIP switch. When the switch is ON, a logic 0 is selected
S3	FPGA Reset Push Button	Reset the FPGA logic
S4, S5, S6, S7	General user push buttons	Four user push buttons. Driven low when pressed
S20	HPS Reset Push Buttons	HPS cold/warm reset push buttons
Memory Connectors		
J134	HPS HILO Memory Connector	HPS memory card include DDR3 HILO memory card and DDR4 HILO memory card
J14	Boot Flash Connector	Boot flash card options include QSPI flash card, SD micro flash card and NAND flash card

continued...

Board Reference	Type	Description
J28	SO-DIMM	16 GB SO-DIMM DDR4 Memory Card
U41	I^2C EEPROM	32 Kb I^2C serial EEPROM
Communication Ports		
J53	PCIe socket	Gen3 x16 Socket
J11, J12	FMC Port	J29 is a V57.4 compatible FMC connector. J19 is a FMC connector defined by Intel 16 transceivers specification
J7	SFP+ Port	One SFP+ Ports
J3	Gigabit Ethernet Port	SGMII Gigabit Ethernet port through FPGA transceiver
J4	Gigabit Ethernet Port	SGMII Gigabit Ethernet Port through FPGA transciever
J57, U2	USB-UART Port	Mini-B USB interface to USB-to-UART bridge for serial UART interface
J22	DB9 UART Port	DB9 RS-232 UART Port
U42	Real-time clock	DS1339 device with built-in power sense circuit that detects power failures and automatically switches to backup battery supply, maintaining time keeping even when the board is not powered
Video and Display Ports		
J8	HDMI Port	Display Port interface
J5, U13	SDI Video Output Port	HDBNC 75-Ohm SDI video TX interface
J6, U14	SDI Video Input Port	HDBNC 75-Ohm SDI video RX interface
J29	Power GUI Connector	Intel Enpirion Power GUI Connector
Power Supply		
J25, J55	DC input jack	Accepts 12 V DC power supply
SW7	Power Switch	Switch to power on or off the board when power is supplied from the DC input jack

4.3. Intel Stratix 10 SoC Device Overview

Intel's 14-nm Intel Stratix 10 SX SoCs deliver 2x core performance and up to 70% lower power over previous generation high-performance SoCs. Featuring several groundbreaking innovations, including the all new Intel Hyperflex™ core architecture, this device family enables you to meet the demand for ever-increasing bandwidth and processing performance in you most advanced applications, while meeting your power budget.

Featuring several groundbreaking innovations, including the all new HyperFlex™ core architecture, this device family enables you to meet the demand for ever-increasing bandwidth and processing performance in your most advanced applications, while meeting your power budget.

With an embedded hard processor system (HPS) based on a quad-core 64-bit ARM® Cortex®-A53, the Stratix 10 SoC devices deliver power efficient, application-class processing and allow designers to extend hardware virtualization into the FPGA fabric.

Stratix 10 SoC devices demonstrate Intel's commitment to high-performance SoCs and extend Intel's leadership in programmable devices featuring an ARM-based processor system.

Important innovations in Stratix 10 FPGAs and SoCs include:

- All new HyperFlex core architecture delivering 2X the core performance compared to previous generation high-performance FPGAs
- Industry leading Intel 14-nm Tri-Gate (FinFET) technology
- Heterogeneous 3D System-in-Package (SiP) technology
- Monolithic core fabric with up to 5.5 million logic elements (LEs)
- Up to 96 full duplex transceiver channels on heterogeneous 3D SiP transceiver tiles
- Transceiver data rates up to 28.3 Gbps chip-to-chip/module and backplane performance
- Embedded eSRAM (45 Mbit) and M20K (20 kbit) internal SRAM memory blocks
- Fractional synthesis and ultra-low jitter LC tank based transmit phase locked loops (PLLs)
- Hard PCI Express® Gen3 x16 intellectual property (IP) blocks
- Hard 10GBASE-KR/40GBASE-KR4 Forward Error Correction (FEC) in every transceiver channel
- Hard memory controllers and PHY supporting DDR4 rates up to 2666 Mbps per pin
- Hard fixed-point and IEEE 754 compliant hard floating-point variable precision digital signal processing (DSP) blocks with up to 10 TFLOPS compute performance with a power efficiency of 80 GFLOPS per Watt
- Quad-core 64-bit ARM Cortex-A53 embedded processor running up to 1.5 GHz in SoC family variants
- Programmable clock tree synthesis for flexible, low power, low skew clock trees
- Dedicated secure device manager (SDM) for:
  - Enhanced device configuration and security
  - AES-256, SHA-256/384 and ECDSA-256/384 encrypt/decrypt accelerators and authentication
  - Multi-factor authentication
  - Physically Unclonable Function (PUF) service and software programmable device configuration capability
- Comprehensive set of advanced power saving features delivering up to 70% lower power compared to previous generation high-performance FPGAs
- Non-destructive register state readback and writeback, to support ASIC prototyping and other applications

With these capabilities, Stratix 10 FPGAs and SoCs are ideally suited for the most demanding applications in diverse markets such as:

- **Compute and Storage**—for custom servers, cloud computing and data center acceleration
- **Networking**—for Terabit, 400G and multi-100G bridging, aggregation, packet processing and traffic management
- **Optical Transport Networks**—for OTU4, 2xOTU4, 4xOTU4
- **Broadcast**—for high-end studio distribution, headend encoding/decoding, edge quadrature amplitude modulation (QAM)
- **Military**—for radar, electronic warfare, and secure communications
- **Medical**—for diagnostic scanners and diagnostic imaging
- **Test and Measurement**—for protocol and application testers
- **Wireless**—for next-generation 5G networks
- **ASIC Prototyping**—for designs that require the largest monolithic FPGA fabric with the highest I/O count

Intel Stratix 10 SX SoC devices have a feature set that is identical to the Intel Stratix 10 FPGA devices, with the addition of an embedded quad-core 64-bit Arm Cortex A53 Hard Processor System.

Common to all Stratix 10 family variants is a high-performance fabric based on the new HyperFlex core architecture that includes additional Hyper-Registers throughout the interconnect routing and at the inputs of all functional blocks. The core fabric also contains an enhanced logic array utilizing Intel's adaptive logic module (ALM) and a rich set of high performance building blocks including:

To clock these building blocks, Stratix 10 devices use programmable clock tree synthesis, which uses dedicated clock tree routing to synthesize only those branches of the clock trees required for the application. All devices support in-system, fine-grained partial reconfiguration of the logic array, allowing logic to be added and subtracted from the system while it is operating.

All family variants also contain high speed serial transceivers, containing both the physical medium attachment (PMA) and the physical coding sublayer (PCS), which can be used to implement a variety of industry standard and proprietary protocols. In addition to the hard PCS, Stratix 10 devices contain multiple instantiations of PCI Express hard IP that supports Gen1/Gen2/Gen3 rates in x1/x2/x4/x8/x16 lane configurations, and hard 10GBASE-KR/40GBASE-KR4 FEC for every transceiver. The hard PCS, FEC, and PCI Express IP free up valuable core logic resources, save power, and increase your productivity.

Table 5. Stratix 10 FPGA and SoC Common Device Features

Feature	Description
Technology	• 14-nm Intel Tri-Gate (FinFET) process technology • SmartVoltage ID (VID) controlled standard V_{CC} option • 0.8 V and 0.85 V optional V_{CC} core voltage
Low power serial transceivers	• Up to 96 total transceivers available • Continuous operating range of 1 Gbps to 28.3 Gbps for Stratix 10 GX/SX devices • Backplane support up to 28.3 Gbps for Stratix 10 GX/SX devices

continued...

Feature	Description
	• Extended range down to 125 Mbps with oversampling • ATX transmit PLLs with user-configurable fractional synthesis capability • XFP, SFP+, QSFP/QSFP28, CFP/CFP2/CFP4 optical module support • Adaptive linear and decision feedback equalization • Transmit pre-emphasis and de-emphasis • Dynamic partial reconfiguration of individual transceiver channels • On-chip instrumentation (EyeQ non-intrusive data eye monitoring)
General purpose I/Os	• Up to 1640 total GPIO available • 1.6 Gbps LVDS—every pair can be configured as an input or output • 1333 MHz/2666 Mbps DDR4 external memory interface • 1067 MHz/2133 Mbps DDR3 external memory interface • 1.2 V to 3.0 V single-ended LVCMOS/LVTTL interfacing • On-chip termination (OCT)
Embedded hard IP	• PCIe Gen1/Gen2/Gen3 complete protocol stack, x1/x2/x4/x8/x16 end point and root port • DDR4/DDR3/LPDDR3 hard memory controller (RLDRAM3/QDR II+/QDR IV using soft memory controller) • Multiple hard IP instantiations in each device • Single Root I/O Virtualization (SR-IOV)
Transceiver hard IP	• 10GBASE-KR/40GBASE-KR4 Forward Error Correction (FEC) • 10G Ethernet PCS • PCI Express PIPE interface • Interlaken PCS • Gigabit Ethernet PCS • Deterministic latency support for Common Public Radio Interface (CPRI) PCS • Fast lock-time support for Gigabit Passive Optical Networking (GPON) PCS • 8B/10B, 64B/66B, 64B/67B encoders and decoders • Custom mode support for proprietary protocols
Power management	• SmartVoltage ID controlled standard V_{CC} option • Low static power device options • Intel Quartus Prime Pro Edition integrated power analysis
High performance monolithic core fabric	• HyperFlex core architecture with Hyper-Registers throughout the interconnect routing and at the inputs of all functional blocks • Monolithic fabric minimizes compile times and increases logic utilization • Enhanced adaptive logic module (ALM) • Improved multi-track routing architecture reduces congestion and improves compile times • Hierarchical core clocking architecture with programmable clock tree synthesis • Fine-grained partial reconfiguration
Internal memory blocks	• eSRAM - 45-Mbit with hard ECC support • M20K—20-Kbit with hard ECC support • MLAB—640-bit distributed LUTRAM
Variable precision DSP blocks	• IEEE 754-compliant hard single-precision floating point capability • Supports signal processing with precision ranging from 18x19 up to 54x54 • Native 27x27 and 18x19 multiply modes • 64-bit accumulator and cascade for systolic FIRs • Internal coefficient memory banks • Pre-adder/subtractor improves efficiency • Additional pipeline register increases performance and reduces power

continued...

Feature	Description
Phase locked loops (PLL)	• Fractional synthesis PLLs (fPLL) support both fractional and integer modes • Fractional mode with third-order delta-sigma modulation • Precision frequency synthesis • Integer PLLs adjacent to general purpose I/Os, support external memory, and LVDS interfaces, clock delay compensation, zero delay buffering
Core clock networks	• 1 GHz fabric clocking • 667 MHz external memory interface clocking, supports 2666 Mbps DDR4 interface • 800 MHz LVDS interface clocking, supports 1600 Mbps LVDS interface • Programmable clock tree synthesis, backwards compatible with global, regional and peripheral clock networks • Clocks only synthesized where needed, to minimize dynamic power
Configuration	• Dedicated Secure Device Manager • Software programmable device configuration • Serial and parallel flash interface • Configuration via protocol (CvP) using PCI Express Gen1/Gen2/Gen3 • Fine-grained partial reconfiguration of core fabric • Dynamic reconfiguration of transceivers and PLLs • Comprehensive set of security features including AES-256, SHA-256/384, and ECDSA-256/384 accelerators, and multi-factor authentication • Physically Unclonable Function (PUF) service
Packaging	• Intel Embedded Multi-die Interconnect Bridge (EMIB) packaging technology • Multiple devices with identical package footprints allows seamless migration across different device densities • 1.0 mm ball-pitch FBGA packaging • Lead and lead-free package options
Software and tools	• Intel Quartus Prime Pro Edition design suite with new Spectra-Q engine and Hyper-Aware design flow • Fast Forward compiler to allow HyperFlex architecture performance exploration • Transceiver toolkit • Qsys system integration tool • DSP Builder advanced blockset • OpenCL™ support • SoC Embedded Design Suite (EDS)

Table 6. Stratix 10 SoC Specific Device Features

SoC Subsystem	Feature	Description
Hard Processor System	Multi-processor unit (MPU) core	• Quad-core ARM Cortex-A53 MPCore processor with ARM CoreSight debug and trace technology • Scalar floating-point unit supporting single and double precision • ARM NEON media processing engine for each processor
	System Controllers	• System Memory Management Unit (SMMU) • Cache Coherency Unit (CCU)
	Layer 1 Cache	• 32 KB L1 instruction cache with parity • 32 KB L1 data cache with ECC
	Layer 2 Cache	• 1 MB Shared L2 Cache with ECC
	On-Chip Memory	• 256 KB On-Chip RAM
	Direct memory access (DMA) controller	• 8-Channel DMA

continued...

SoC Subsystem	Feature	Description
	Ethernet media access controller (EMAC)	• Three 10/100/1000 EMAC with integrated DMA
	USB On-The-Go controller (OTG)	• 2 USB OTG with integrated DMA
	UART controller	• 2 UART 16550 compatible
	Serial Peripheral Interface (SPI) controller	• 4 SPI
	I^2C controller	• 5 I^2C controllers
	SD/SDIO/MMC controller	• 1 eMMC version 4.5 with DMA and CE-ATA support • SD, including eSD, version 3.0 • SDIO, including eSDIO, verion 3.0 • CE-ATA - version 1.1
	NAND flash controller	• 1 ONFI 1.0, 8- and 16-bit support
	General-purpose I/O (GPIO)	• Maximum of 48 software programmable GPIO
	Timers	• 4 general-purpose timers • 4 watchdog timers
Secure Device Manager	Security	• Secure boot • Advanced Encryption Standard (AES) and authentication (SHA/ECDSA)
External Memory Interface	External Memory Interface	• Hard Memory Controller with DDR4 and DDR3, and LPDDR3

For further information , please refer to the Intel Stratix 10 GX/SX Device Overview available on the Intel website.

Related Information

Stratix 10 GX/SX Device Overview

4.4. Intel MAX 10 System Controller Overview

Intel MAX 10 devices are single-chip, non-volatile low-cost programmable logic devices (PLDs) to integrate the optimal set of system components.

Intel MAX 10 devices are the ideal solution for system management, I/O expansion, communication control planes, industrial, automotive, and consumer applications.

The highlights of the Intel MAX 10 devices include:

- Internally stored dual configuration flash
- User flash memory
- Instant on support
- Integrated analog-to-digital converters (ADCs)
- Single-chip Nios II soft core processor support

Table 7. Summary of Features for Intel MAX 10 Devices

Feature	Description
Technology	55 nm TSMC Embedded Flash (Flash + SRAM) process technology
Packaging	• Low cost, small form factor packages—support multiple packaging technologies and pin pitches • Multiple device densities with compatible package footprints for seamless migration between different device densities • RoHS6-compliant
Core architecture	• 4-input look-up table (LUT) and single register logic element (LE) • LEs arranged in logic array block (LAB) • Embedded RAM and user flash memory • Clocks and PLLs • Embedded multiplier blocks • General purpose I/Os
Internal memory blocks	• M9K—9 kilobits (Kb) memory blocks • Cascadable blocks to create RAM, dual port, and FIFO functions
User flash memory (UFM)	• User accessible non-volatile storage • High speed operating frequency • Large memory size • High data retention • Multiple interface option
Embedded multiplier blocks	• One 18 × 18 or two 9 × 9 multiplier modes • Cascadable blocks enabling creation of filters, arithmetic functions, and image processing pipelines
ADC	• 12-bit successive approximation register (SAR) type • Up to 17 analog inputs • Cumulative speed up to 1 million samples per second (MSPS) • Integrated temperature sensing capability
Clock networks	• Global clocks support • High speed frequency in clock network
Internal oscillator	Built-in internal ring oscillator
PLLs	• Analog-based • Low jitter • High precision clock synthesis • Clock delay compensation • Zero delay buffering • Multiple output taps
General-purpose I/Os (GPIOs)	• Multiple I/O standards support • On-chip termination (OCT) • Up to 830 megabits per second (Mbps) LVDS receiver, 800 Mbps LVDS transmitter
External memory interface (EMIF) (1)	Supports up to 600 Mbps external memory interfaces: • DDR3, DDR3L, DDR2, LPDDR2 (on 10M16, 10M25, 10M40 and 10M50) • SRAM (Hardware support only)

continued...

(1) EMIF is only supported in selected MAX 10 device density and package combinations. Refer to the *External Memory Interface User Guide* for more information.

Feature	Description
	Note: For 600 Mbps performance, –6 device speed grade is required. Performance varies according to device grade (commercial, industrial, or automotive) and device speed grade (–6 or –7). Refer to the *MAX 10 Device Data Sheet* or *External Memory Interface Spec Estimator* for more details.
Configuration	• Internal configuration • JTAG • Advanced Encryption Standard (AES) 128-bit encryption and compression options • Flash memory data retention of 20 years at 85 °C
Flexible power supply schemes	• Single- and dual-supply device options • Dynamically controlled input buffer power down • Sleep mode for dynamic power reduction

4.5. FPGA Configuration

This development kit supports the following FPGA configurations:

- QSPI Configuration
- SDMMC x4 Configuration
- JTAG Only

A 4-bit DIP Switch (SW2) is used to select the FPGA configuration mode.

Table 8. DIP Switch Bits

Switch Bit	Name
1	MSEL0
2	MSEL1
3	MSEL2
4	Not Used

Table 9. DIP Switch Bit Description

MSEL2	MSEL1	MSEL0	Mode
OFF	OFF	ON	QSPI
ON	OFF	OFF	SDMMC x4, SDMMC x8
ON	ON	ON	JTAG

Note: The default setting is JTAG mode. The default bit position is "ON, ON, ON, ON"

4.6. General User Input/Output

Table 10. User I/O Pin Map

Pin Name	Schematic Signal Name	Description
PIN_A24	USER_LED_FPGA0	USER_LED0
PIN_B24	USER_LED_FPGA2	USER_LED1

continued...

Pin Name	Schematic Signal Name	Description
PIN_F22	USER_LED_FPGA1	USER_LED2
PIN_E22	USER_LED_FPGA3	USER_LED3
PIN_A26	USER_PB_FPGA0	USER_PB0
PIN_A25	USER_PB_FPGA1	USER_PB1
PIN_D23	USER_PB_FPGA2	USER_PB2
PIN_D24	USER_PB_FPGA3	USER_PB3
PIN_B23	USER_DIPSW_FPGA0	USER_DPSW0
PIN_C23	USER_DIPSW_FPGA1	USER_DPSW1
PIN_E23	USER_DIPSW_FPGA2	USER_DPSW2
PIN_E24	USER_DIPSW_FPGA3	USER_DPSW3

4.7. Connectors and Interfaces

The FPGA portion of this development kit includes 96 transceivers.

Table 11. Channel Assignment for Transceiver Applications

Applications	Channel (Bank, Number)
FMC+ A	1C (1C, 0-5), 1D (1D, 0-5), 1E (1E, 0-3), 1F (PCIE EP x16)
SFP+ Port	(4C, 0)
PCIE RC x16	(4K, 0-5), (4L, 0-5), (4M, 0-3)
SGMII Port 1 and Port 2	(4M, 4), (4M, 5)
FMC+ B	1K (1K, 0-5), 1L (1L, 0-5), 1M (1M, 0-3), 1N (PCIE EPx16)
MXP Test Ports	(4D, 0, 1, 3, 4)
SDI Port	TX (4E,1), RX (4F, 0)
HDMI	(4C, 2-5)
ZQSFP+ B	(4F, (0,1,3,4))
ZQSFP+ A	(4N, (0,1,3,4))

4.7.1. PCIe Slot

The PCIe root port is a PCIe Gen3 x16 port. This port is assigned to 4K, 4L and 4M Banks. The transceiver I/O bank power is connected to 1.8 V.

PCIE_PRSNT2n, PCIE_PERSTn and PCIE_WAKE_N 3V3 signals are mapped to the dedicated trasnceiver I/O bank (IO4) in the Intel MAX 10. The system performance of the PCIe root port should meet the PCIe 3.0 specifications.

Table 12. PCIE Root Port FPGA Pin Map

Pin Name	Schematic Signal Name	Direction	Description
PIN_V12	PCIE_REFCLK_QR0_P	Input	REFCLK_GXBR4K_CHTP
PIN_V13	PCIE_REFCLK_QR0_N	Input	REFCLK_GXBR4K_CHTN
PIN_L4	PCIE_TX_N15	Output	GXBR4M_TX_CH3N
PIN_L3	PCIE_TX_P15	Output	GXBR4M_TX_CH3P
PIN_H6	PCIE_RX_N15	Input	GXBR4M_RX_CH3N
PIN_H5	PCIE_RX_P15	Input	GXBR4M_RX_CH3P
PIN_K2	PCIE_TX_N14	Output	GXBR4M_TX_CH2N
PIN_K1	PCIE_TX_P14	Output	GXBR4M_TX_CH2P
PIN_L8	PCIE_RX_N14	Input	GXBR4M_RX_CH2N
PIN_L7	PCIE_RX_P14	Input	GXBR4M_RX_CH2P
PIN_N4	PCIE_TX_N13	Output	GXBR4M_TX_CH1N
PIN_N3	PCIE_TX_P13	Output	GXBR4M_TX_CH1P
PIN_K6	PCIE_RX_N13	Input	GXBR4M_RX_CH1N
PIN_K5	PCIE_RX_P13	Input	GXBR4M_RX_CH1P
PIN_M2	PCIE_TX_N12	Output	GXBR4M_TX_CH0N
PIN_M1	PCIE_TX_P12	Output	GXBR4M_TX_CH0P
PIN_N8	PCIE_RX_N12	Input	GXBR4M_RX_CH0N
PIN_N7	PCIE_RX_P12	Input	GXBR4M_RX_CH0P
PIN_R4	PCIE_TX_N11	Output	GXBR4L_TX_CH5N
PIN_R3	PCIE_TX_P11	Output	GXBR4L_TX_CH5P
PIN_M6	PCIE_RX_N11	Input	GXBR4L_RX_CH5N
PIN_M5	PCIE_RX_P11	Input	GXBR4L_RX_CH5P
PIN_P2	PCIE_TX_N10	Output	GXBR4L_TX_CH4N
PIN_P1	PCIE_TX_P10	Output	GXBR4L_TX_CH4P
PIN_R8	PCIE_RX_N10	Input	GXBR4L_RX_CH4N
PIN_R7	PCIE_RX_P10	Input	GXBR4L_RX_CH4P
PIN_T2	PCIE_TX_N9	Output	GXBR4L_TX_CH3N
PIN_T1	PCIE_TX_P9	Output	GXBR4L_TX_CH3P
PIN_P6	PCIE_RX_N9	Input	GXBR4L_RX_CH3N
PIN_P5	PCIE_RX_P9	Input	GXBR4L_RX_CH3P
PIN_U4	PCIE_TX_N8	Output	GXBR4L_TX_CH2N
PIN_U3	PCIE_TX_P8	Output	GXBR4L_TX_CH2P
PIN_T6	PCIE_RX_N8	Input	GXBR4L_RX_CH2N

continued...

Pin Name	Schematic Signal Name	Direction	Description
PIN_T5	PCIE_RX_P8	Input	GXBR4L_RX_CH2P
PIN_V2	PCIE_TX_N7	Output	GXBR4L_TX_CH1N
PIN_V1	PCIE_TX_P7	Output	GXBR4L_TX_CH1P
PIN_U8	PCIE_RX_N7	Input	GXBR4L_RX_CH1N
PIN_U7	PCIE_RX_P7	Input	GXBR4L_RX_CH1P
PIN_Y2	PCIE_TX_N6	Output	GXBR4L_TX_CH0N
PIN_Y1	PCIE_TX_P6	Output	GXBR4L_TX_CH0P
PIN_V6	PCIE_RX_N6	Input	GXBR4L_RX_CH0N
PIN_V5	PCIE_RX_P6	Input	GXBR4L_RX_CH0P
PIN_W4	PCIE_TX_N5	Output	GXBR4K_TX_CH5N
PIN_W3	PCIE_TX_P5	Output	GXBR4K_TX_CH5P
PIN_Y6	PCIE_RX_N5	Input	GXBR4K_RX_CH5N
PIN_Y5	PCIE_RX_P5	Input	GXBR4K_RX_CH5P
PIN_AB2	PCIE_TX_N4	Output	GXBR4K_TX_CH4N
PIN_AB1	PCIE_TX_P4	Output	GXBR4K_TX_CH4P
PIN_W8	PCIE_RX_N4	Input	GXBR4K_RX_CH4N
PIN_W7	PCIE_RX_P4	Input	GXBR4K_RX_CH4P
PIN_AA4	PCIE_TX_N3	Output	GXBR4K_TX_CH3N
PIN_AA3	PCIE_TX_P3	Output	GXBR4K_TX_CH3P
PIN_AB6	PCIE_RX_N3	Input	GXBR4K_RX_CH3N
PIN_AB5	PCIE_RX_P3	Input	GXBR4K_RX_CH3P
PIN_AD2	PCIE_TX_N2	Output	GXBR4K_TX_CH2N
PIN_AD1	PCIE_TX_P2	Output	GXBR4K_TX_CH2P
PIN_AA8	PCIE_RX_N2	Input	GXBR4K_RX_CH2N
PIN_AA7	PCIE_RX_P2	Input	GXBR4K_RX_CH2P
PIN_AC4	PCIE_TX_N1	Output	GXBR4K_TX_CH1N
PIN_AC3	PCIE_TX_P1	Output	GXBR4K_TX_CH1P
PIN_AD6	PCIE_RX_N1	Input	GXBR4K_RX_CH1N
PIN_AD5	PCIE_RX_P1	Input	GXBR4K_RX_CH1P
PIN_AE4	PCIE_TX_N0	Output	GXBR4K_TX_CH0N
PIN_AE3	PCIE_TX_P0	Output	GXBR4K_TX_CH0P
PIN_AC8	PCIE_RX_N0	Input	GXBR4K_RX_CH0N
PIN_AC7	PCIE_RX_P0	Input	GXBR4K_RX_CH0P

4.7.2. ZQSFP+

The ZQSFP+ 0/1 ports meet SFF8665 and QSFP28 industrial standards. The connector part number is Molex 170432-001. The cage part number is TE 2227103-2. The PCB trace insertion loss is less than -5 dB and return loss is less than -10 dB. The ZQSFP+ signals (`Modesl`, `RESETL`, `MOdPrsl`, `LPmode`, `int`) are mapped to the dedicated I/O in System Intel MAX 10. The BC25, BC26 pins in 2F bank are I^2C interface. The user needs this interface to access ZQSFP.

Table 13. ZQSFP+ 0/1 Ports FPGA Pin Map

Pin Name	Schematic Signal Name	Direction	Description
PIN_P9	CLEARNER_XVR_644.53125 MHZ_P	Input	REFCLK_GXBR4N_CHTP
PIN_P10	CLEARNER_XVR_644.53125 MHZ_N	Input	REFCLK_GXBR4N_CHTN
PIN_C4	ZQSFP0_TXN3	Output	GXBR4N_TX_CH3N
PIN_C3	ZQSFP0_TXP3	Output	GXBR4N_TX_CH3P
PIN_A8	ZQSFP0_RXN3	Input	GXBR4N_RX_CH3N
PIN_A7	ZQSFP0_RXP3	Input	GXBR4N_RX_CH3P
PIN_E4	ZQSFP0_TXN2	Output	GXBR4N_TX_CH2N
PIN_E3	ZQSFP0_TXP2	Output	GXBR4N_TX_CH2P
PIN_C8	ZQSFP0_RXN2	Input	GXBR4N_RX_CH2N
PIN_C7	ZQSFP0_RXP2	Input	GXBR4N_RX_CH2P
PIN_G4	ZQSFP0_TXN1	Output	GXBR4N_TX_CH1N
PIN_G3	ZQSFP0_TXP1	Output	GXBR4N_TX_CH1P
PIN_D6	ZQSFP0_RXN1	Input	GXBR4N_RX_CH1N
PIN_D5	ZQSFP0_RXP1	Input	GXBR4N_RX_CH1P
PIN_F2	ZQSFP0_TXN0	Output	GXBR4N_TX_CH0N
PIN_F1	ZQSFP0_TXP0	Output	GXBR4N_TX_CH0P
PIN_G8	ZQSFP0_RXN0	Input	GXBR4N_RX_CH0N
PIN_G7	ZQSFP0_RXP0	Input	GXBR4N_RX_CH0P
PIN_T9	REFCLK0_P	Input	REFCLK_GXBR4N_CHBP
PIN_T10	REFCLK0_N	Input	REFCLK_GXBR4N_CHBN
PIN_AF2	ZQSFP1_TXN3	Output	GXBR4F_TX_CH3N
PIN_AF1	ZQSFP1_TXP3	Output	GXBR4F_TX_CH3P
PIN_AG8	ZQSFP1_RXN3	Input	GXBR4F_RX_CH3N
PIN_AG7	ZQSFP1_RXP3	Input	GXBR4F_RX_CH3P
PIN_AJ4	ZQSFP1_TXN2	Output	GXBR4F_TX_CH2N
PIN_AJ3	ZQSFP1_TXP2	Output	GXBR4F_TX_CH2P

continued...

Pin Name	Schematic Signal Name	Direction	Description
PIN_AF6	ZQSFP1_RXN2	Input	GXBR4F_RX_CH2N
PIN_AF5	ZQSFP1_RXP2	Input	GXBR4F_RX_CH2P
PIN_AL4	ZQSFP1_TXN1	Output	GXBR4F_TX_CH1N
PIN_AL3	ZQSFP1_TXP1	Output	GXBR4F_TX_CH1P
PIN_AH6	ZQSFP1_RXN1	Input	GXBR4F_RX_CH1N
PIN_AH5	ZQSFP1_RXP1	Input	GXBR4F_RX_CH1P
PIN_AK2	ZQSFP1_TXN0	Output	GXBR4F_TX_CH0N
PIN_AK1	ZQSFP1_TXP0	Output	GXBR4F_TX_CH0P
PIN_AL8	ZQSFP1_RXN0	Input	GXBR4F_RX_CH0N
PIN_AL7	ZQSFP1_RXP0	Input	GXBR4F_RX_CH0P
PIN_AM12	REFCLK_QSFP1_P	Input	REFCLK_GXBR4F_CHBP
PIN_AM13	REFCLK_QSFP1_N	Input	REFCLK_GXBR4F_CHBN

4.7.3. SFP+

The SFP+ Port meets SFF-8431 Industrial Standard. The connector part number is Samtec MECT-110-01-M-D-RA1. The cage part number is Molex 74754-0101. The PCB trace insertion loss is less than -5 dB and return loss less than -10 dB.

SFP+ signals (TX_disable, RS0/1, MOD_ABS, LOS, Fault) are mapped to the dedicated transceiver I/O in Intel MAX 10.

Table 14. SFP+ Port FPGA Pin Map

Pin Name	Schematic Signal Name	Direction	Description
PIN_BJ5	SFPA_TX_N	Output	GXBR4C_TX_CH0N
PIN_BJ4	SFPA_TX_P	Output	GXBR4C_TX_CH0P
PIN_BH10	SFPA_RX_N	Input	GXBR4C_RX_CH0N
PIN_BH9	SFPA_RX_P	Input	GXBR4C_RX_CH0P
PIN_AT9	REFCLK_SFPA_P	Input	REFCLK_GXBR4C_CHBP
PIN_AT10	REFCLK_SFPA_N	Input	REFCLK_GXBR4C_CHBN

4.7.4. HDMI

Table 15. HDMI Port FPGA Pin Map

Pin Name	Schematic Signal Name	Direction	Description
PIN_AP9	HDMIREFCLK_P	Input	REFCLK_GXBR4C_CHTP
PIN_AP10	HDMIREFCLK_N	Input	REFCLK_GXBR4C_CHTN
PIN_BC4	HDMI_LANE_CLKN	Output	GXBR4C_TX_CH5N
PIN_BC3	HDMI_LANE_CLKP	Output	GXBR4C_TX_CH5P

continued...

Pin Name	Schematic Signal Name	Direction	Description
PIN_BF2	HDMI_LANE_N2	Output	GXBR4C_TX_CH4N
PIN_BF1	HDMI_LANE_P2	Output	GXBR4C_TX_CH4P
PIN_BE4	HDMI_LANE_N1	Output	GXBR4C_TX_CH3N
PIN_BE3	HDMI_LANE_P1	Output	GXBR4C_TX_CH3P
PIN_BG4	HDMI_LANE_N0	Output	GXBR4C_TX_CH2N
PIN_BG3	HDMI_LANE_P0	Output	GXBR4C_TX_CH2P

4.7.5. SDI Port

Table 16. SDI Port FPGA Pin Map

Pin Name	Schematic Signal Name	Direction	Description
PIN_AF9	CLEARNER_SDI_245MHZ_P	Input	REFCLK_GXBL4E_CHTP
PIN_AF10	CLEARNER_SDI_245MHZ_N	Input	REFCLK_GXBL4E_CHTN
PIN_AR4	SDI_TX_N	Output	GXBR4E_TX_CH1N
PIN_AR3	SDI_TX_P	Output	GXBR4E_TX_CH1P
PIN_AR8	SDI_RX_N	Input	GXBR4E_RX_CH0N
PIN_AR7	SDI_RX_P	Input	GXBR4E_RX_CH0P
PIN_AK12	CLEARNER_SDI_297MHZ_P	Input	REFCLK_GXBL4F_CHTP
PIN_AK13	CLEARNER_SDI_297MHZ_N	Input	REFCLK_GXBL4F_CHTN

4.7.6. MXP

The MXP Test Port is a MXP Coaxial Print Connectors. The PCB trace insertion loss is less than -5 dB and return loss is less than -10 dB. You can use it for 100 Gbps applications.

Table 17. MXP Port FPGA Pin Map

Pin Name	Schematic Signal Name	Direction	Description
PIN_AK9	REFCLK_SMA_P	Input	REFCLK_GXBR4D_CHTP
PIN_AK10	REFCLK_SMA_N	Input	REFCLK_GXBR4D_CHTN
PIN_AY2	MXP_TXN3	Output	GXBR4D_TX_CH3N
PIN_AY1	MXP_TXP3	Output	GXBR4D_TX_CH3P
PIN_AU8	MXP_RXN3	Input	GXBR4D_RX_CH3N
PIN_AU7	MXP_RXP3	Input	GXBR4D_RX_CH3P
PIN_AW4	MXP_TXN2	Output	GXBR4D_TX_CH2N
PIN_AW3	MXP_TXP2	Output	GXBR4D_TX_CH2P
PIN_AY6	MXP_RXN2	Input	GXBR4D_RX_CH2N
PIN_AY5	MXP_RXP2	Input	GXBR4D_RX_CH2P

continued...

Pin Name	Schematic Signal Name	Direction	Description
PIN_BA4	MXP_TXN1	Output	GXBR4D_TX_CH1N
PIN_BA3	MXP_TXP1	Output	GXBR4D_TX_CH1P
PIN_BB6	MXP_RXN1	Input	GXBR4D_RX_CH1N
PIN_BB5	MXP_RXP1	Input	GXBR4D_RX_CH1P
PIN_BD2	MXP_TXN0	Output	GXBR4D_TX_CH0N
PIN_BD1	MXP_TXP0	Output	GXBR4D_TX_CH0P
PIN_BA8	MXP_RXN0	Input	GXBR4D_RX_CH0N
PIN_BA7	MXP_RXP0	Input	GXBR4D_RX_CH0P

4.7.7. Intel FPGA Download Cable Direct Port (Debug Port)

The Direct Port is connected to the 3B bank.

Table 18. Debug Port FPGA Pin Map

Pin Name	Schematic Signal Name	Description
PIN_AP16	USB0	USB Debug Data
PIN_AP15	USB1	USB Debug Data
PIN_AU13	USB2	USB Debug Data
PIN_AV13	USB3	USB Debug Data
PIN_AU12	USB4	USB Debug Data
PIN_AT12	USB5	USB Debug Data
PIN_AR13	USB6	USB Debug Data
PIN_AP12	USB7	USB Debug Data
PIN_AP14	USB_RDN	USB Debug Control Signal
PIN_AP13	USB_WRN	USB Debug Control Signal
PIN_AT14	USB_OEN	USB Debug Control Signal
PIN_AR14	USB_RESETN	USB Debug Control Signal
PIN_AR18	USB_EMPTY	USB Debug Control Signal
PIN_AP18	USB_FULL	USB Debug Control Signal
PIN_AU14	USB_SDA	USB Debug I^2C
PIN_AU15	USB_SCL	USB Debug I^2C

4.7.8. FMC+ A/B Slot

Table 19. FMC+ A Slot FPGA Pin Map

Pin Name	Schematic Signal Name	Direction	Description
PIN_AP41	FAGBTCLK0M2CP	Input	REFCLK_GXBL1C_CHTP
PIN_AP40	FAGBTCLK0M2CN	Input	REFCLK_GXBL1C_CHTN
PIN_BC46	FAD5C2MN	Output	GXBR1C_TX_CH5N
PIN_BC47	FAD5C2MP	Output	GXBR1C_TX_CH5P
PIN_BD44	FAD5M2CN	Input	GXBR1C_RX_CH5N
PIN_BD45	FAD5M2CP	Input	GXBR1C_RX_CH5P
PIN_BF48	FAD4C2MN	Output	GXBR1C_TX_CH4N
PIN_BF49	FAD4C2MP	Output	GXBR1C_TX_CH4P
PIN_BC42	FAD4M2CN	Input	GXBR1C_RX_CH4N
PIN_BC43	FAD4M2CP	Input	GXBR1C_RX_CH4P
PIN_BE46	FAD3C2MN	Output	GXBR1C_TX_CH3N
PIN_BE47	FAD3C2MP	Output	GXBR1C_TX_CH3P
PIN_BE42	FAD3M2CN	Input	GXBR1C_RX_CH3N
PIN_BE43	FAD3M2CP	Input	GXBR1C_RX_CH3P
PIN_BG46	FAD2C2MN	Output	GXBR1C_TX_CH2N
PIN_BG47	FAD2C2MP	Output	GXBR1C_TX_CH2P
PIN_BG42	FAD2M2CN	Input	GXBR1C_RX_CH2N
PIN_BG43	FAD2M2CP	Input	GXBR1C_RX_CH2P
PIN_BF44	FAD1C2MN	Output	GXBR1C_TX_CH1N
PIN_BF45	FAD1C2MP	Output	GXBR1C_TX_CH1P
PIN_BJ42	FAD1M2CN	Input	GXBR1C_RX_CH1N
PIN_BJ43	FAD1M2CP	Input	GXBR1C_RX_CH1P
PIN_BJ45	FAD0C2MN	Output	GXBR1C_TX_CH0N
PIN_BJ46	FAD0C2MP	Output	GXBR1C_TX_CH0P
PIN_BH40	FAD0M2CN	Input	GXBR1C_RX_CH0N
PIN_BH41	FAD0M2CP	Input	GXBR1C_RX_CH0P
PIN_AT41	CLEARNER_XVRR_122.88MHZ_P	Input	REFCLK_GXBL1C_CHBP
PIN_AT40	CLEARNER_XVRR_122.88MHZ_N	Input	REFCLK_GXBL1C_CHBN
PIN_AK41	FAGBTCLK1M2CP	Input	REFCLK_GXB1D_CHTP
PIN_AK40	FAGBTCLK1M2CN	Input	REFCLK_GXB1D_CHTN
PIN_AU46	FAD11C2MN	Output	GXBR1D_TX_CH5N

continued...

Pin Name	Schematic Signal Name	Direction	Description
PIN_AU47	FAD11C2MP	Output	GXBR1D_TX_CH5P
PIN_AV44	FAD11M2CN	Input	GXBR1D_RX_CH5N
PIN_AV45	FAD11M2CP	Input	GXBR1D_RX_CH5P
PIN_AY48	FAD10C2MN	Output	GXBR1D_TX_CH4N
PIN_AY49	FAD10C2MP	Output	GXBR1D_TX_CH4P
PIN_AU42	FAD10M2CN	Input	GXBR1D_RX_CH4N
PIN_AU43	FAD10M2CP	Input	GXBR1D_RX_CH4P
PIN_AW46	FAD9C2MN	Output	GXBR1D_TX_CH3N
PIN_AW47	FAD9C2MP	Output	GXBR1D_TX_CH3P
PIN_AY44	FAD9M2CN	Input	GXBR1D_RX_CH3N
PIN_AY45	FAD9M2CP	Input	GXBR1D_RX_CH3P
PIN_BB48	FAD8C2MN	Output	GXBR1D_TX_CH2N
PIN_BB49	FAD8C2MP	Output	GXBR1D_TX_CH2P
PIN_AW42	FAD8M2CN	Input	GXBR1D_RX_CH2N
PIN_AW43	FAD8M2CP	Input	GXBR1D_RX_CH2P
PIN_BA46	FAD7C2MN	Output	GXBR1D_TX_CH1N
PIN_BA47	FAD7C2MP	Output	GXBR1D_TX_CH1P
PIN_BB44	FAD7M2CN	Input	GXBR1D_RX_CH1N
PIN_BB45	FAD7M2CP	Input	GXBR1D_RX_CH1P
PIN_BD48	FAD6C2MN	Output	GXBR1D_TX_CH0N
PIN_BD49	FAD6C2MP	Output	GXBR1D_TX_CH0P
PIN_BA42	FAD6M2CN	Input	GXBR1D_RX_CH0N
PIN_BA43	FAD6M2CP	Input	GXBR1D_RX_CH0P
PIN_AM41	FAGBTCLK3M2CP	Input	REFCLK_GXBL1D_CHBP
PIN_AM40	FAGBTCLK3M2CN	Input	REFCLK_GXBL1D_CHBN
PIN_AF41	FAGBTCLK2M2CP	Input	REFCLK_GXBL1E_CHBP
PIN_AF40	FAGBTCLK2M2CN	Input	REFCLK_GXBL1E_CHBN
PIN_AM48	FAD17C2MN	Output	GXBR1E_TX_CH5N
PIN_AM49	FAD17C2MP	Output	GXBR1E_TX_CH5P
PIN_AK44	FAD17M2CN	Input	GXBR1E_RX_CH5N
PIN_AK45	FAD17M2CP	Input	GXBR1E_RX_CH5P
PIN_AN46	FAD16C2MN	Output	GXBR1E_TX_CH4N
PIN_AN47	FAD16C2MP	Output	GXBR1E_TX_CH4P
PIN_AM44	FAD16M2CN	Input	GXBR1E_RX_CH4N

continued...

Pin Name	Schematic Signal Name	Direction	Description
PIN_AM45	FAD16M2CP	Input	GXBR1E_RX_CH4P
PIN_AP48	FAD15C2MN	Output	GXBR1E_TX_CH3N
PIN_AP49	FAD15C2MP	Output	GXBR1E_TX_CH3P
PIN_AN42	FAD15M2CN	Input	GXBR1E_RX_CH3N
PIN_AN43	FAD15M2CP	Input	GXBR1E_RX_CH3P
PIN_AT48	FAD14C2MN	Output	GXBR1E_TX_CH2N
PIN_AT49	FAD14C2MP	Output	GXBR1E_TX_CH2P
PIN_AP44	FAD14M2CN	Input	GXBR1E_RX_CH2N
PIN_AP45	FAD14M2CP	Input	GXBR1E_RX_CH2P
PIN_AR46	FAD13C2MN	Output	GXBR1E_TX_CH1N
PIN_AR47	FAD13C2MP	Output	GXBR1E_TX_CH1P
PIN_AT44	FAD13M2CN	Input	GXBR1E_RX_CH1N
PIN_AT45	FAD13M2CP	Input	GXBR1E_RX_CH1P
PIN_AV48	FAD12C2MN	Output	GXBR1E_TX_CH0N
PIN_AV49	FAD12C2MP	Output	GXBR1E_TX_CH0P
PIN_AR42	FAD12M2CN	Input	GXBR1E_RX_CH0N
PIN_AR43	FAD12M2CP	Input	GXBR1E_RX_CH0P
PIN_AH41	FAGBTCLK4M2CP	Input	REFCLK_GXBL1E_CHBP
PIN_AH40	FAGBTCLK4M2CN	Input	REFCLK_GXBL1E_CHBN
PIN_AK38	FAGBTCLK5M2CP	Input	REFCLK_GXBL1F_CHTP
PIN_AK37	FAGBTCLK5M2CN	Input	REFCLK_GXBL1F_CHTN
PIN_AG46	FAD23C2MN	Output	GXBR1F_TX_CH5N
PIN_AG47	FAD23C2MP	Output	GXBR1F_TX_CH5P
PIN_AE42	FAD23M2CN	Input	GXBR1F_RX_CH5N
PIN_AE43	FAD23M2CP	Input	GXBR1F_RX_CH5P
PIN_AF48	FAD22C2MN	Output	GXBR1F_TX_CH4N
PIN_AF49	FAD22C2MP	Output	GXBR1F_TX_CH4P
PIN_AG42	FAD22M2CN	Input	GXBR1F_RX_CH4N
PIN_AG43	FAD22M2CP	Input	GXBR1F_RX_CH4P
PIN_AJ46	FAD21C2MN	Output	GXBR1F_TX_CH3N
PIN_AJ47	FAD21C2MP	Output	GXBR1F_TX_CH3P
PIN_AF44	FAD21M2CN	Input	GXBR1F_RX_CH3N
PIN_AF45	FAD21M2CP	Input	GXBR1F_RX_CH3P
PIN_AH48	FAD20C2MN	Output	GXBR1F_TX_CH2N

continued...

Pin Name	Schematic Signal Name	Direction	Description
PIN_AH49	FAD20C2MP	Output	GXBR1F_TX_CH2P
PIN_AJ42	FAD20M2CN	Input	GXBR1F_RX_CH2N
PIN_AJ43	FAD20M2CP	Input	GXBR1F_RX_CH2P
PIN_AL46	FAD19C2MN	Output	GXBR1F_TX_CH1N
PIN_AL47	FAD19C2MP	Output	GXBR1F_TX_CH1P
PIN_AH44	FAD19M2CN	Input	GXBR1F_RX_CH1N
PIN_AH45	FAD19M2CP	Input	GXBR1F_RX_CH1P
PIN_AK48	FAD18C2MN	Output	GXBR1F_TX_CH0N
PIN_AK49	FAD18C2MP	Output	GXBR1F_TX_CH0P
PIN_AL42	FAD18M2CN	Input	GXBR1F_RX_CH0N
PIN_AL43	FAD18M2CP	Input	GXBR1F_RX_CH0P
PIN_AM38	REFCLK0_FMC_P	Input	REFCLKI_GXBL1F_CHBP
PIN_AM37	REFCLK0_FMC_N	Input	REFCLKI_GXBL1F_CHBN

Table 20. FMC+ B Slot FPGA Pin Map

Pin Name	Schematic Signal Name	Direction	Description
PIN_V38	FBGBTCLK0M2CP	Input	REFCLK_GXBL1K_CHTP
PIN_V37	FBGBTCLK0M2CN	Input	REFCLK_GXBL1K_CHTN
PIN_W46	FBD5C2MN	Output	GXBR1K_TX_CH5N
PIN_W47	FBD5C2MP	Output	GXBR1K_TX_CH5P
PIN_Y44	FBD5M2CN	Input	GXBR1K_RX_CH5N
PIN_Y45	FBD5M2CP	Input	GXBR1K_RX_CH5P
PIN_AB48	FBD4C2MN	Output	GXBR1K_TX_CH4N
PIN_AB49	FBD4C2MP	Output	GXBR1K_TX_CH4P
PIN_W42	FBD4M2CN	Input	GXBR1K_RX_CH4N
PIN_W43	FBD4M2CP	Input	GXBR1K_RX_CH4P
PIN_AA46	FBD3C2MN	Output	GXBR1K_TX_CH3N
PIN_AA47	FBD3C2MP	Output	GXBR1K_TX_CH3P
PIN_AB44	FBD3M2CN	Input	GXBR1K_RX_CH3N
PIN_AB45	FBD3M2CP	Input	GXBR1K_RX_CH3P
PIN_AD48	FBD2C2MN	Output	GXBR1K_TX_CH2N
PIN_AD49	FBD2C2MP	Output	GXBR1K_TX_CH2P
PIN_AA42	FBD2M2CN	Input	GXBR1K_RX_CH2N
PIN_AA43	FBD2M2CP	Input	GXBR1K_RX_CH2P
PIN_AC46	FBD1C2MN	Output	GXBR1K_TX_CH1N

continued...

Pin Name	Schematic Signal Name	Direction	Description
PIN_AC47	FBD1C2MP	Output	GXBR1K_TX_CH1P
PIN_AD44	FBD1M2CN	Input	GXBR1K_RX_CH1N
PIN_AD45	FBD1M2CP	Input	GXBR1K_RX_CH1P
PIN_AE46	FBD0C2MN	Output	GXBR1K_TX_CH0N
PIN_AE47	FBD0C2MP	Output	GXBR1K_TX_CH0P
PIN_AC42	FBD0M2CN	Input	GXBR1K_RX_CH0N
PIN_AC43	FBD0M2CP	Input	GXBR1K_RX_CH0P
PIN_Y38	CLEARNER_XVRL_122.88MHZ_P	Input	REFCLK_GXBL1K_CHBP
PIN_Y37	CLEARNER_XVRL_122.88MHZ_N	Input	REFCLK_GXBL1K_CHBN
PIN_AB41	FBGBTCLK1M2CP	Input	REFCLK_GXB1L_CHTP
PIN_AB40	FBGBTCLK1M2CN	Input	REFCLK_GXB1L_CHTN
PIN_R46	FBD11C2MN	Output	GXBR1L_TX_CH5N
PIN_R47	FBD11C2MP	Output	GXBR1L_TX_CH5P
PIN_M44	FBD11M2CN	Input	GXBR1L_RX_CH5N
PIN_M45	FBD11M2CP	Input	GXBR1L_RX_CH5P
PIN_P48	FBD10C2MN	Output	GXBR1L_TX_CH4N
PIN_P49	FBD10C2MP	Output	GXBR1L_TX_CH4P
PIN_R42	FBD10M2CN	Input	GXBR1L_RX_CH4N
PIN_R43	FBD10M2CP	Input	GXBR1L_RX_CH4P
PIN_T48	FBD9C2MN	Output	GXBR1L_TX_CH3N
PIN_T49	FBD9C2MP	Output	GXBR1L_TX_CH3P
PIN_P44	FBD9M2CN	Input	GXBR1L_RX_CH3N
PIN_P45	FBD9M2CP	Input	GXBR1L_RX_CH3P
PIN_U46	FBD8C2MN	Output	GXBR1L_TX_CH2N
PIN_U47	FBD8C2MP	Output	GXBR1L_TX_CH2P
PIN_T44	FBD8M2CN	Input	GXBR1L_RX_CH2N
PIN_T45	FBD8M2CP	Input	GXBR1L_RX_CH2P
PIN_V48	FBD7C2MN	Output	GXBR1L_TX_CH1N
PIN_V49	FBD7C2MP	Output	GXBR1L_TX_CH1P
PIN_U42	FBD7M2CN	Input	GXBR1L_RX_CH1N
PIN_U43	FBD7M2CP	Input	GXBR1L_RX_CH1P
PIN_Y48	FBD6C2MN	Output	GXBR1L_TX_CH0N
PIN_Y49	FBD6C2MP	Output	GXBR1L_TX_CH0P

continued...

Pin Name	Schematic Signal Name	Direction	Description
PIN_V44	FBD6M2CN	Input	GXBR1L_RX_CH0N
PIN_V45	FBD6M2CP	Input	GXBR1L_RX_CH0P
PIN_AD41	FBGBTCLK5M2CP	Input	REFCLK_GXBL1L_CHBP
PIN_AD40	FBGBTCLK5M2CN	Input	REFCLK_GXBL1L_CHBN
PIN_V41	FBGBTCLK2M2CP	Input	REFCLK_GXBL1M_CHBP
PIN_V40	FBGBTCLK2M2CN	Input	REFCLK_GXBL1M_CHBN
PIN_J46	FBD17C2MN	Output	GXBR1M_TX_CH5N
PIN_J47	FBD17C2MP	Output	GXBR1M_TX_CH5P
PIN_F44	FBD17M2CN	Input	GXBR1M_RX_CH5N
PIN_F45	FBD17M2CP	Input	GXBR1M_RX_CH5P
PIN_H48	FBD16C2MN	Output	GXBR1M_TX_CH4N
PIN_H49	FBD16C2MP	Output	GXBR1M_TX_CH4P
PIN_J42	FBD16M2CN	Input	GXBR1M_RX_CH4N
PIN_J43	FBD16M2CP	Input	GXBR1M_RX_CH4P
PIN_L46	FBD15C2MN	Output	GXBR1M_TX_CH3N
PIN_L47	FBD15C2MP	Output	GXBR1M_TX_CH3P
PIN_H44	FBD15M2CN	Input	GXBR1M_RX_CH3N
PIN_H45	FBD15M2CP	Input	GXBR1M_RX_CH3P
PIN_K48	FBD14C2MN	Output	GXBR1M_TX_CH2N
PIN_K49	FBD14C2MP	Output	GXBR1M_TX_CH2P
PIN_L42	FBD14M2CN	Input	GXBR1M_RX_CH2N
PIN_L43	FBD14M2CP	Input	GXBR1M_RX_CH2P
PIN_N46	FBD13C2MN	Output	GXBR1M_TX_CH1N
PIN_N47	FBD13C2MP	Output	GXBR1M_TX_CH1P
PIN_K44	FBD13M2CN	Input	GXBR1M_RX_CH1N
PIN_K45	FBD13M2CP	Input	GXBR1M_RX_CH1P
PIN_M48	FBD12C2MN	Output	GXBR1M_TX_CH0N
PIN_M49	FBD12C2MP	Output	GXBR1M_TX_CH0P
PIN_N42	FBD12M2CN	Input	GXBR1M_RX_CH0N
PIN_N43	FBD12M2CP	Input	GXBR1M_RX_CH0P
PIN_Y41	FBGBTCLK4M2CP	Input	REFCLK_GXBL1N_CHBP
PIN_Y40	FBGBTCLK4M2CN	Input	REFCLK_GXBL1N_CHBN
PIN_P41	FBGBTCLK3M2CP	Input	REFCLK_GXBL1N_CHTP
PIN_P40	FBGBTCLK3M2CN	Input	REFCLK_GXBL1N_CHTN

continued...

Pin Name	Schematic Signal Name	Direction	Description
PIN_B44	FBD23C2MN	Output	GXBR1N_TX_CH5N
PIN_B45	FBD23C2MP	Output	GXBR1N_TX_CH5P
PIN_B40	FBD23M2CN	Input	GXBR1N_RX_CH5N
PIN_B41	FBD23M2CP	Input	GXBR1N_RX_CH5P
PIN_C46	FBD22C2MN	Output	GXBR1N_TX_CH4N
PIN_C47	FBD22C2MP	Output	GXBR1N_TX_CH4P
PIN_A42	FBD22M2CN	Input	GXBR1N_RX_CH4N
PIN_A43	FBD22M2CP	Input	GXBR1N_RX_CH4P
PIN_E46	FBD21C2MN	Output	GXBR1N_TX_CH3N
PIN_E47	FBD21C2MP	Output	GXBR1N_TX_CH3P
PIN_C42	FBD21M2CN	Input	GXBR1N_RX_CH3N
PIN_C43	FBD21M2CP	Input	GXBR1N_RX_CH3P
PIN_D48	FBD20C2MN	Output	GXBR1N_TX_CH2N
PIN_D49	FBD20C2MP	Output	GXBR1N_TX_CH2P
PIN_E42	FBD20M2CN	Input	GXBR1N_RX_CH2N
PIN_E43	FBD20M2CP	Input	GXBR1N_RX_CH2P
PIN_G46	FBD19C2MN	Output	GXBR1N_TX_CH1N
PIN_G47	FBD19C2MP	Output	GXBR1N_TX_CH1P
PIN_D44	FBD19M2CN	Input	GXBR1N_RX_CH1N
PIN_D45	FBD19M2CP	Input	GXBR1N_RX_CH1P
PIN_F48	FBD18C2MN	Output	GXBR1N_TX_CH0N
PIN_F49	FBD18C2MP	Output	GXBR1N_TX_CH0P
PIN_G42	FBD18M2CN	Input	GXBR1N_RX_CH0N
PIN_G43	FBD18M2CP	Input	GXBR1N_RX_CH0P
PIN_T41	REFCLK1_FMC_P	Input	REFCLK_GXBL1N_CHBP
PIN_T40	REFCLK1_FMC_N	Input	REFCLK_GXBL1N_CHBN

4.7.9. FMC+ A/B LVDS Interfaces (LPC Pins)

All LVDS interface signals except the LAP/N33, LAP/N32 signals from FMC+ A are directly connected to FPGA I/O ports. For the PCIE ED port application, PCIEA_EP_PERSTn and PCIEA_WAKEN are connected to System MAX10 IO through LAP/N33 signals.

LAP/N32 signals are shorted together into PCIE_present. All LA P/N except LAP/N33, LAP/N32 signals from FMC+B are directly connected to FPGA I/O ports. For a PCIE ED port application, PCIEA_EP_PERSTn and PCIEA_WAKEN are connected to System MAX10 I/O through FALP/N33 signals. LP/N32 signals are short together into PCIE_present.

Most HB and HA signals from FMC+B are connected to System MAX10 I/O. You must write the code to map these signals to the I/O ports of FPGA.

Table 21. FMC+ A/B Port FPGA Map

Pin Name	Schematic Signal Name	Description
PIN_AP21	FALAN20	FMCA LA LVDS
PIN_AN21	FALAP20	FMCA LA LVDS
PIN_BG20	FALAN25	FMCA LA LVDS
PIN_BF20	FALAP25	FMCA LA LVDS
PIN_BD18	FALAN19	FMCA LA LVDS
PIN_BE18	FALAP19	FMCA LA LVDS
PIN_BG19	FALAN21	FMCA LA LVDS
PIN_BG18	FALAP21	FMCA LA LVDS
PIN_BH21	FALAN24	FMCA LA LVDS
PIN_BH20	FALAP24	FMCA LA LVDS
PIN_BH17	FALAN18	FMCA LA LVDS
PIN_BG17	FALAP18	FMCA LA LVDS
PIN_BJ20	FALAN27	FMCA LA LVDS
PIN_BJ19	FALAP27	FMCA LA LVDS
PIN_BJ18	FALAN26	FMCA LA LVDS
PIN_BH18	FALAP26	FMCA LA LVDS
PIN_AT16	FALAN11	FMCA LA LVDS
PIN_AT15	FALAP11	FMCA LA LVDS
PIN_AN18	FALAN15	FMCA LA LVDS
PIN_AN17	FALAP15	FMCA LA LVDS
PIN_AU17	FALAN17	FMCA LA LVDS
PIN_AT17	FALAP17	FMCA LA LVDS
PIN_AU28	FALAN12	FMCA LA LVDS
PIN_AU29	FALAP12	FMCA LA LVDS
PIN_BA30	FALAN9	FMCA LA LVDS
PIN_BA31	FALAP9	FMCA LA LVDS
PIN_BC32	FALAN3	FMCA LA LVDS
PIN_BC31	FALAP3	FMCA LA LVDS
PIN_AW31	FALAN0	FMCA LA LVDS
PIN_AW30	FALAP0	FMCA LA LVDS
PIN_BD31	FA_LA_DEVCLK_N	FMCA LA LVDS

continued...

Pin Name	Schematic Signal Name	Description
PIN_BE31	FA_LA_DEVCLK_P	FMCA LA LVDS
PIN_BF30	FALAN6	FMCA LA LVDS
PIN_BF31	FALAP6	FMCA LA LVDS
PIN_BD30	FALAN4	FMCA LA LVDS
PIN_BC30	FALAP4	FMCA LA LVDS
PIN_BH30	FALAN5	FMCA LA LVDS
PIN_BG30	FALAP5	FMCA LA LVDS
PIN_BF32	FALAN7	FMCA LA LVDS
PIN_BE32	FALAP7	FMCA LA LVDS
PIN_BG32	FALAN8	FMCA LA LVDS
PIN_BH32	FALAP8	FMCA LA LVDS
PIN_BD36	FALAN31	FMCA LA LVDS
PIN_BE36	FALAP31	FMCA LA LVDS
PIN_BC35	FALAN23	FMCA LA LVDS
PIN_BC36	FALAP23	FMCA LA LVDS
PIN_BB34	FALAN10	FMCA LA LVDS
PIN_BB33	FALAP10	FMCA LA LVDS
PIN_BF35	FALAN29	FMCA LA LVDS
PIN_BF36	FALAP29	FMCA LA LVDS
PIN_BG35	FALAN32_FPGA	FMCA LA LVDS
PIN_BH35	FALAP32_FPGA	FMCA LA LVDS
PIN_BE34	FALAN33_FPGA	FMCA LA LVDS
PIN_BE33	FALAP33_FPGA	FMCA LA LVDS
PIN_BJ36	FALAN22	FMCA LA LVDS
PIN_BJ35	FALAP22	FMCA LA LVDS
PIN_AT32	FALAN14	FMCA LA LVDS
PIN_AU32	FALAP14	FMCA LA LVDS
PIN_AU35	FALAN30	FMCA LA LVDS
PIN_AV35	FALAP30	FMCA LA LVDS
PIN_AY13	FAHAN14	FMCA HA LVDS
PIN_AW13	FAHAP14	FMCA HA LVDS
PIN_AV12	FAHAN18	FMCA HA LVDS
PIN_AV11	FAHAP18	FMCA HA LVDS
PIN_AY12	FAHAN20	FMCA HA LVDS

continued...

Pin Name	Schematic Signal Name	Description
PIN_BA12	FAHAP20	FMCA HA LVDS
PIN_BA11	FAHAN21	FMCA HA LVDS
PIN_BA10	FAHAP21	FMCA HA LVDS
PIN_AW11	FAHAN17	FMCA HA LVDS
PIN_AY11	FAHAP17	FMCA HA LVDS
PIN_BB12	FAHAN0	FMCA HA LVDS
PIN_BC12	FAHAP0	FMCA HA LVDS
PIN_BB10	FAHAN1	FMCA HA LVDS
PIN_BC10	FAHAP1	FMCA HA LVDS
PIN_BB20	FAHAN2	FMCA HA LVDS
PIN_BC20	FAHAP2	FMCA HA LVDS
PIN_AY21	FAHAN11	FMCA HA LVDS
PIN_AW21	FAHAP11	FMCA HA LVDS
PIN_AW20	FAHAN10	FMCA HA LVDS
PIN_AW19	FAHAP10	FMCA HA LVDS
PIN_BA19	FAHAN15	FMCA HA LVDS
PIN_BB19	FAHAP15	FMCA HA LVDS
PIN_AU20	FAHAN19	FMCA HA LVDS
PIN_AT20	FAHAP19	FMCA HA LVDS
PIN_BD20	FAHAN6	FMCA HA LVDS
PIN_BD19	FAHAP6	FMCA HA LVDS
PIN_BB18	FAHAN23	FMCA HA LVDS
PIN_BC18	FAHAP23	FMCA HA LVDS
PIN_AV20	FAHAN16	FMCA HA LVDS
PIN_AV21	FAHAP16	FMCA HA LVDS
PIN_BF17	FAHAN22	FMCA HA LVDS
PIN_BE17	FAHAP22	FMCA HA LVDS
PIN_AV28	FAHAN12	FMCA HA LVDS
PIN_AW28	FAHAP12	FMCA HA LVDS
PIN_AV30	FAHAN5	FMCA HA LVDS
PIN_AU30	FAHAP5	FMCA HA LVDS
PIN_AY32	FAHAN9	FMCA HA LVDS
PIN_AY31	FAHAP9	FMCA HA LVDS
PIN_BE29	FAHAN7	FMCA HA LVDS

continued...

Pin Name	Schematic Signal Name	Description
PIN_BD29	FAHAP7	FMCA HA LVDS
PIN_BJ31	FAHAN13	FMCA HA LVDS
PIN_BH31	FAHAP13	FMCA HA LVDS
PIN_BB29	FAHAN3	FMCA HA LVDS
PIN_BB30	FAHAP3	FMCA HA LVDS
PIN_AV32	FAHAN4	FMCA HA LVDS
PIN_AV33	FAHAP4	FMCA HA LVDS
PIN_BF19	FAHBN1	FMCA HB LVDS
PIN_BE19	FAHBP1	FMCA HB LVDS
PIN_AR16	FAHBN16	FMCA HB LVDS
PIN_AR17	FAHBP16	FMCA HB LVDS
PIN_BB25	FAHBN6	FMCA HB LVDS
PIN_BA25	FAHBP6	FMCA HB LVDS
PIN_BB27	FAHBN19	FMCA HB LVDS
PIN_BC27	FAHBP19	FMCA HB LVDS
PIN_AW29	FAHBN2	FMCA HB LVDS
PIN_AY29	FAHBP2	FMCA HB LVDS
PIN_BB28	FAHBN3	FMCA HB LVDS
PIN_BA29	FAHBP3	FMCA HB LVDS
PIN_AT30	FAHBN0	FMCA HB LVDS
PIN_AT29	FAHBP0	FMCA HB LVDS
PIN_BB32	FAHBN5	FMCA HB LVDS
PIN_BA32	FAHBP5	FMCA HB LVDS
PIN_BG28	FAHBN15	FMCA HB LVDS
PIN_BG29	FAHBP15	FMCA HB LVDS
PIN_BE28	FAHBN10	FMCA HB LVDS
PIN_BF29	FAHBP10	FMCA HB LVDS
PIN_BJ29	FAHBN14	FMCA HB LVDS
PIN_BJ30	FAHBP14	FMCA HB LVDS
PIN_BH28	FAHBN18	FMCA HB LVDS
PIN_BJ28	FAHBP18	FMCA HB LVDS
PIN_BD35	FAHBN4	FMCA HB LVDS
PIN_BD34	FAHBP4	FMCA HB LVDS
PIN_BC33	FAHAN8	FMCA HB LVDS

continued...

Pin Name	Schematic Signal Name	Description
PIN_BD33	FAHAP8	FMCA HB LVDS
PIN_AY33	FAHBN8	FMCA HB LVDS
PIN_AW33	FAHBP8	FMCA HB LVDS
PIN_BA35	FAHBN21	FMCA HB LVDS
PIN_BB35	FAHBP21	FMCA HB LVDS
PIN_AY36	FAHBN20	FMCA HB LVDS
PIN_BA36	FAHBP20	FMCA HB LVDS
PIN_BF34	FAHBN12	FMCA HB LVDS
PIN_BG34	FAHBP12	FMCA HB LVDS
PIN_BJ34	FAHBN9	FMCA HB LVDS
PIN_BJ33	FAHBP9	FMCA HB LVDS
PIN_AT34	FAHBN11	FMCA HB LVDS
PIN_AT35	FAHBP11	FMCA HB LVDS
PIN_AR31	FAHBN7	FMCA HB LVDS
PIN_AR32	FAHBP7	FMCA HB LVDS
PIN_AU33	FAHBN17	FMCA HB LVDS
PIN_AU34	FAHBP17	FMCA HB LVDS
PIN_AT19	FACLK1M2CN	FMCA M2C Clk1N
PIN_AR19	FACLK1M2CP	FMCA M2C Clk1P
PIN_BE21	FACLK0M2CN	FMCA M2C Clk0N
PIN_BF21	FACLK0M2CP	FMCA M2C Clk0P
PIN_AY17	FACLKDIR	FMCA CLK DIR
PIN_AY40	FBLAN3	FMCB LA LVDS
PIN_BA40	FBLAP3	FMCB LA LVDS
PIN_BA39	FBLAN20	FMCB LA LVDS
PIN_BB39	FBLAP20	FMCB LA LVDS
PIN_BB40	FBLAN11	FMCB LA LVDS
PIN_BC40	FBLAP11	FMCB LA LVDS
PIN_BD38	FBLAN12	FMCB LA LVDS
PIN_BD39	FBLAP12	FMCB LA LVDS
PIN_BC38	FBLAN15	FMCB LA LVDS
PIN_BB38	FBLAP15	FMCB LA LVDS
PIN_BC37	FBLAN27	FMCB LA LVDS
PIN_BB37	FBLAP27	FMCB LA LVDS

continued...

Pin Name	Schematic Signal Name	Description
PIN_BD40	FBLAN8	FMCB LA LVDS
PIN_BE40	FBLAP8	FMCB LA LVDS
PIN_BG38	FBLAN2	FMCB LA LVDS
PIN_BG37	FBLAP2	FMCB LA LVDS
PIN_BE38	FBLAN4	FMCB LA LVDS
PIN_BE39	FBLAP4	FMCB LA LVDS
PIN_BE37	FBLAN16	FMCB LA LVDS
PIN_BF37	FBLAP16	FMCB LA LVDS
PIN_BF39	FBLAN7	FMCB LA LVDS
PIN_BF40	FBLAP7	FMCB LA LVDS
PIN_BH37	FBLAN0	FMCB LA LVDS
PIN_BH36	FBLAP0	FMCB LA LVDS
PIN_AW39	FB_LA_DEVCLK_N	FMCB LA LVDS
PIN_AW38	FB_LA_DEVCLK_P	FMCB LA LVDS
PIN_BA37	FBLAN22	FMCB LA LVDS
PIN_AY37	FBLAP22	FMCB LA LVDS
PIN_AV40	FBLAN9	FMCB LA LVDS
PIN_AW40	FBLAP9	FMCB LA LVDS
PIN_AY39	FBLAN19	FMCB LA LVDS
PIN_AY38	FBLAP19	FMCB LA LVDS
PIN_AU37	FAHBN13	FMCB LA LVDS
PIN_AU38	FAHBP13	FMCB LA LVDS
PIN_AV38	FBLAN26	FMCB LA LVDS
PIN_AV37	FBLAP26	FMCB LA LVDS
PIN_AR34	FBLAN23	FMCB LA LVDS
PIN_AP35	FBLAP23	FMCB LA LVDS
PIN_AR36	FBLAN18	FMCB LA LVDS
PIN_AP36	FBLAP18	FMCB LA LVDS
PIN_AP33	FBLAN10	FMCB LA LVDS
PIN_AN33	FBLAP10	FMCB LA LVDS
PIN_AT36	FBLAN13	FMCB LA LVDS
PIN_AT37	FBLAP13	FMCB LA LVDS
PIN_AR37	FBLAN6	FMCB LA LVDS
PIN_AT38	FBLAP6	FMCB LA LVDS

continued...

Pin Name	Schematic Signal Name	Description
PIN_AR33	FBLAN5	FMCB LA LVDS
PIN_AP34	FBLAP5	FMCB LA LVDS
PIN_AT25	FBLAN30	FMCB LA LVDS
PIN_AU25	FBLAP30	FMCB LA LVDS
PIN_AW25	FBLAN29	FMCB LA LVDS
PIN_AV25	FBLAP29	FMCB LA LVDS
PIN_AT26	FBLAN24	FMCB LA LVDS
PIN_AR26	FBLAP24	FMCB LA LVDS
PIN_AU27	FBLAN25	FMCB LA LVDS
PIN_AT27	FBLAP25	FMCB LA LVDS
PIN_AY26	FBLAN21	FMCB LA LVDS
PIN_AW26	FBLAP21	FMCB LA LVDS
PIN_AN26	FBLAN28	FMCB LA LVDS
PIN_AP26	FBLAP28	FMCB LA LVDS
PIN_AN25	FBLAN31	FMCB LA LVDS
PIN_AP25	FBLAP31	FMCB LA LVDS
PIN_AP29	FBLAN32_FPGA	FMCB LA LVDS
PIN_AP28	FBLAP32_FPGA	FMCB LA LVDS
PIN_AR27	FBLAN33_FPGA	FMCB LA LVDS
PIN_AR28	FBLAP33_FPGA	FMCB LA LVDS
PIN_AP31	FBLAN14	FMCB LA LVDS
PIN_AP30	FBLAP14	FMCB LA LVDS
PIN_BA26	FBLAN17	FMCB LA LVDS
PIN_BA27	FBLAP17	FMCB LA LVDS

4.7.10. LMK05028 Jitter Attenuator

The LMK05028 device is a high-performance clock generator, jitter cleaner, and clock synchronizer with advanced reference clock selection and hitless switching to meet the stringent requirements of communications infrastructure applications.

The ultra-low jitter reduces bit error rates (BER) in high-speed serial links and improves signal to noise ratio (SNR) when clocking high-speed data converters.

The device has two independent PLL cores that can each synchronize or lock to one of four reference clock inputs, and the LMK05028 can generate up to eight output clocks with up to six different frequencies.

You can use the FPGA I^2C port at FPGA pins BC25, BC26 to control LMK05028. LMK05028 3.3V I/O signals are connected to System MAX10 (U43) IO ports. You need to write code to connect these I/Os to FPGA 1.8V I/O ports. The J21 10-pin Header is used to connect the TI 05028 GUI port. You can use it to configure LMK05028.

Clock outputs from I/O ports (AW35, AW34, BA34, and AY34 pins) in 2B bank are connected to TI LMK05028.

The following table lists the cleaner output signal pin assignments:

Table 22. LMK05028 Clock Cleaner Output Pin Frequencies and Pin Assignments

Output	Frequency	Pin Assignments
0	245 MHz or 297/1.001 MHz	AF9, AF10 in 4E Bank
1	122.88 MHz	Y38, Y37 in 1K Bank
2	122.88 MHz	AT41, AT40 in 1C Bank
3	122.88 MHz	D8, D9 (FALAP1, FALAN1) in FMCA
4	122.88 MHz	D8, D9 (FBLAP1, FBLAN1) in FMCB
5	122.88 MHz	AK12, AK 13 in 4E Bank
6	297 MHz	AK12, AK 13 in 4E Bank
7	644.53125 MHz	P9, P10 in bank 4M

TI LMH1983 is used to generate SDI reference clocks. Four 3.3V IO signals (U43 pins: E17, F17, B21, B22) in the MAX10 system controller are connected to the LMH1983 FIN, VIN, HIN and INIT input pins. SDI users need to write code to map the four 3.3V IOs to the FGPA 1.8V IOs. The 27 MHz output clock is directly connected to clock cleaner input 2. The 148.5 MHz clock is connected to U15AN28 and An27 in IO bank 2F. The clock cleaner application can be found at this link.

Related Information

LMK05028 Network Clock Generator and Synchronizer Evaluation Module

4.7.11. FPGA-IOMAX10 Interface

The I/O signals of the transceiver I/O banks and the 14 I/O ports in 3A banks are connected to System Intel MAX 10.

The figure below illustrates the signal connections between Intel MAX 10 and Intel Stratix 10 SX SoC. You can write your own code to map User I/O to these pins.

Figure 4. Signal Connections

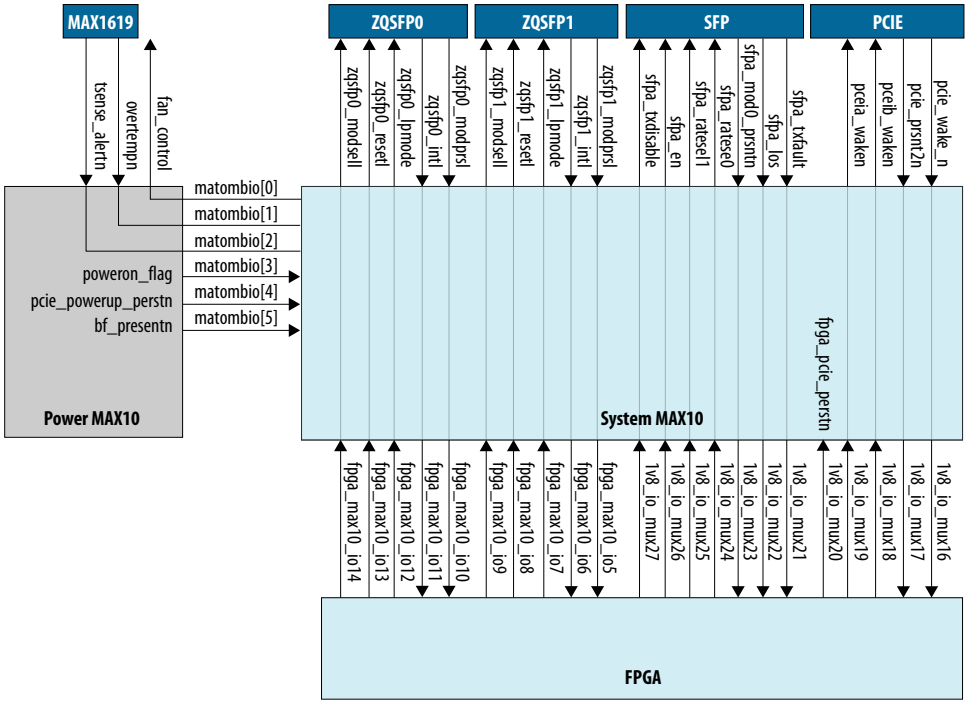


Table 23. FPGA-IOMAX10 Pin Map

Pin Name	Schematic Signal Name	Description
PIN_AJ34	NPERSTL0	System MAX10_IO
PIN_AG35	1V8_IO_MUX0	System MAX10_IO
PIN_AH33	1V8_IO_MUX1	System MAX10_IO
PIN_AF34	1V8_IO_MUX2	System MAX10_IO
PIN_AE36	1V8_IO_MUX3	System MAX10_IO
PIN_AG34	1V8_IO_MUX4	System MAX10_IO
PIN_AH32	1V8_IO_MUX5	System MAX10_IO
PIN_AJ33	1V8_IO_MUX6	System MAX10_IO
PIN_AD34	NPERSTL2	System MAX10_IO
PIN_AD35	1V8_IO_MUX7	System MAX10_IO
PIN_AC35	1V8_IO_MUX8	System MAX10_IO
PIN_AB34	1V8_IO_MUX9	System MAX10_IO
PIN_AC33	1V8_IO_MUX10	System MAX10_IO
PIN_AC36	1V8_IO_MUX11	System MAX10_IO
PIN_AB35	1V8_IO_MUX12	System MAX10_IO
PIN_AB36	1V8_IO_MUX13	System MAX10_IO

continued...

Pin Name	Schematic Signal Name	Description
PIN_AH16	NPERSTR0	System MAX10_IO
PIN_AF15	1V8_IO_MUX14	System MAX10_IO
PIN_AB12	1V8_IO_MUX15	System MAX10_IO
PIN_AF17	1V8_IO_MUX16	System MAX10_IO
PIN_AD16	1V8_IO_MUX17	System MAX10_IO
PIN_AF16	1V8_IO_MUX18	System MAX10_IO
PIN_AE16	1V8_IO_MUX19	System MAX10_IO
PIN_AH17	1V8_IO_MUX20	System MAX10_IO
PIN_AE14	NPERSTR2	System MAX10_IO
PIN_AD15	1V8_IO_MUX21	System MAX10_IO
PIN_AC15	1V8_IO_MUX22	System MAX10_IO
PIN_AC14	1V8_IO_MUX23	System MAX10_IO
PIN_AB13	1V8_IO_MUX24	System MAX10_IO
PIN_AD14	1V8_IO_MUX25	System MAX10_IO
PIN_AB15	1V8_IO_MUX26	System MAX10_IO
PIN_AB14	1V8_IO_MUX27	System MAX10_IO
PIN_BD13	AVST_D0	System MAX10_IO
PIN_BE13	AVST_D1	System MAX10_IO
PIN_BF15	AVST_D2	System MAX10_IO
PIN_BG15	AVST_D3	System MAX10_IO
PIN_BE14	AVST_D4	System MAX10_IO
PIN_BF14	AVST_D5	System MAX10_IO
PIN_BE16	AVST_D6	System MAX10_IO
PIN_BF16	AVST_D7	System MAX10_IO
PIN_BD16	AVST_D8	System MAX10_IO
PIN_BC16	AVST_D9	System MAX10_IO
PIN_BD14	AVST_D10	System MAX10_IO
PIN_BD15	AVST_D11	System MAX10_IO
PIN_BF12	AVST_D12	System MAX10_IO
PIN_BG12	AVST_D13	System MAX10_IO
PIN_BJ13	AVST_D14	System MAX10_IO
PIN_BJ14	AVST_D15	System MAX10_IO
PIN_BG13	FPGA_MAX10_IO0	System MAX10_IO
PIN_BG14	FPGA_MAX10_IO1	System MAX10_IO

continued...

Pin Name	Schematic Signal Name	Description
PIN_BH15	FPGA_MAX10_IO2	System MAX10_IO
PIN_BJ15	FPGA_MAX10_IO3	System MAX10_IO
PIN_BH12	ENETA_INTN_B	System MAX10_IO
PIN_BH13	AVST_VALID	System MAX10_IO
PIN_BH16	CLK_50M_FPGA	System MAX10_IO
PIN_BJ16	FPGA_MAX10_IO5	System MAX10_IO
PIN_AV15	FPGA_MAX10_IO6	System MAX10_IO
PIN_AW15	FPGA_MAX10_IO7	System MAX10_IO
PIN_BA15	FPGA_MAX10_IO8	System MAX10_IO
PIN_BA16	FPGA_MAX10_IO9	System MAX10_IO
PIN_AW14	FPGA_MAX10_IO10	System MAX10_IO
PIN_AY14	FPGA_MAX10_IO11	System MAX10_IO
PIN_BB14	FPGA_MAX10_IO12	System MAX10_IO
PIN_BA14	FPGA_MAX10_IO13	System MAX10_IO
PIN_BB15	FPGA_MAX10_IO14	System MAX10_IO
PIN_BC15	GLOBAL_RESETN	System MAX10_IO
PIN_BC13	FPGA_PR_REQUEST	System MAX10_IO
PIN_BA17	FPGA_PR_DONE	System MAX10_IO
PIN_AY16	FPGA_PR_ERROR	System MAX10_IO
PIN_AY19	AVST_CLK	System MAX10_IO

4.8. Daughter Cards

4.8.1. HPS IO-48 OOBE Daughter Card

This is a daughter card for the Intel Stratix 10 SoC IO48 interface. The two types of Intel Stratix 10 SoC Development Kit IO48 daughter cards are OOBE and NAND Flash. These IO48 daughter cards are plugged into the Samtec IO48 connector.

Feature Summary

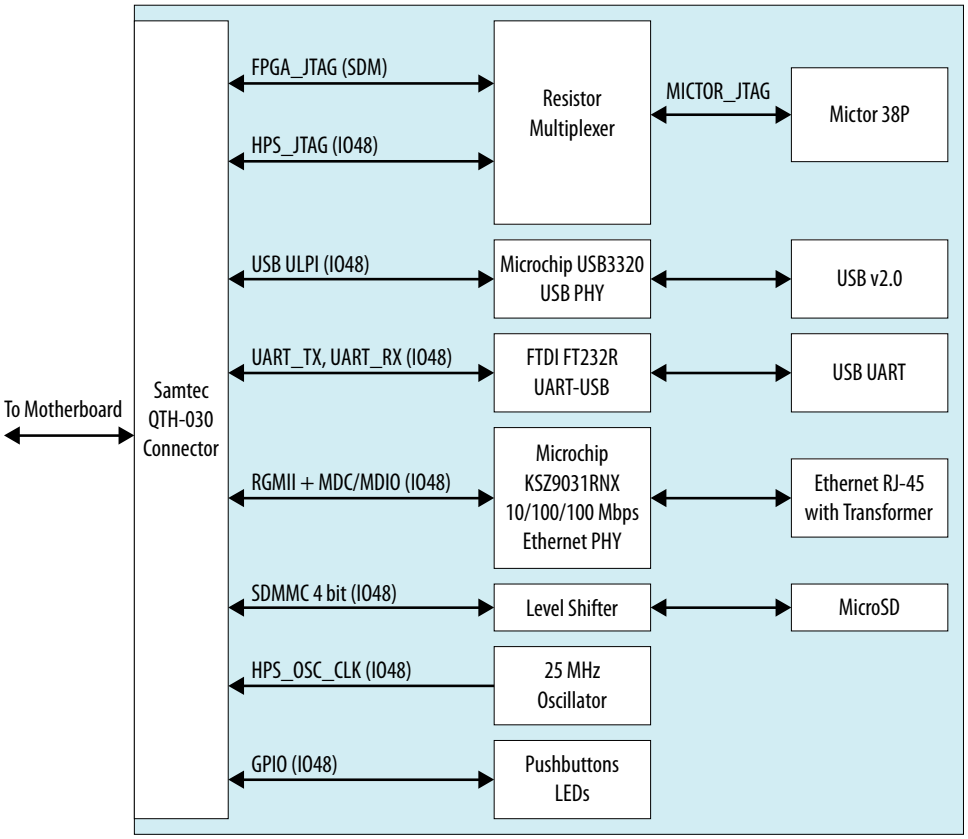
Table 24. IO48 OOBE Daughter Card Feature Summary

Feature	Description
IO48 Connector	• Samtec QTH-030 Series 60-pin connector on IO48 daughter card side • Samtec QSH-030 Series 60-pin connector on motherboard
10/100/1000 Mbps Ethernet PHY with RGMII interface	• Microchip KSZ9031RNX Ethernet PHY • RGMII MAC Interface • MDC/MDIO Management Interface • Standard RJ-45 with Integrated Ethernet Transformer

continued...

Feature	Description
UART	• FTDI FT232R UART USB Convertor • Standard USB Mini-B Receptacle
Micro-SD Card Connector	• 4-bit SD card Data Bus • Standard Micro SD Card Socket
USB 2.0	• Microchip USB3320 USB 2.0 PHY • ULPI interface connects the USB PHY to Intel Stratix 10 HPS IO48 interface • Standard USB Micro-AB Receptacle • VBUS current limitation when VBUS is sourced to peripheral device
JTAG	• Mictor 38-pin connector pinouts (JTAG only without Trace signals) • Two JTAG target with resisters MUX — FPGA chained JTAG pins in SDM — HPS dedicated JTAG pins in IO48 (by default)
I^2C	• HPS I^2C and FPGA I^2C are connected on the motherboard
GPIO	• 2 Push Buttons • 3 LEDs • 1 Ethernet Interrupt from Ethernet PHY • 1 USB over-current indicator
HPS Clock	On-board 25 MHz oscillator provides HPS clock
Mechanical	3" x 1.8" board size

Figure 5. OOBE Daughter Card Block Diagram



IO48 Interface

Stratix 10 SoC IO48 bank can be multiplexed to different peripheral interfaces. The OOBE daughter card is mulitplexed with USB 2.0, Ethernet RGMII, UART, I^2C, JTAG, MicroSD card and GPIO interfaces.

Table 25. IO48 Pinout MUX

HPS Pin Name	Peripheral Name	Signal
Q1_1	USB0	CLK
Q1_2	USB0	STP
Q1_3	USB0	DIR
Q1_4	USB0	DATA0
Q1_5	USB0	DATA1
Q1_6	USB0	NXT
Q1_7	USB0	DATA2
Q1_8	USB0	DATA3
Q1_9	USB0	DATA4
Q1_10	USB0	DATA5
Q1_11	USB0	DATA6
Q1_12	USB0	DATA7
Q2_1	EMAC0	TX_CLK
Q2_2	EMAC0	TX_CTL
Q2_3	EMAC0	RX_CLK
Q2_4	EMAC0	RX_CTL
Q2_5	EMAC0	TXD0
Q2_6	EMAC0	TXD1
Q2_7	EMAC0	RXD0
Q2_8	EMAC0	RXD1
Q2_9	EMAC0	TXD2
Q2_10	EMAC0	TXD3
Q2_11	EMAC0	RXD2
Q2_12	EMAC0	RXD3
Q3_1	GPIO1	IO0
Q3_2	GPIO1	IO1
Q3_3	UART0	TX
Q3_4	UART0	RX
Q3_5	GPIO1	IO4
Q3_6	GPIO1	IO5

continued...

HPS Pin Name	Peripheral Name	Signal
Q3_7	I2C1	SDA
Q3_8	I2C1	SCL
Q3_9	JTAG	TCK
Q3_10	JTAG	TMS
Q3_11	JTAG	TDO
Q3_12	JTAG	TDI
Q4_1	SDMMC	DATA0
Q4_2	SDMMC	CMD
Q4_3	SDMMC	CCLK
Q4_4	SDMMC	DATA1
Q4_5	SDMMC	DATA2
Q4_6	SDMMC	DATA3
Q4_7	CM	HPS_OSC_CLK
Q4_8	GPIO1	IO19
Q4_9	GPIO1	IO20
Q4_10	GPIO1	IO21
Q4_11	MDIO0	MDIO
Q4_12	MDIO0	MDC

Connector to Motherboard

To connect between the motherboard and IO48 OOBE daughter card, Samtec QSH/QTH series connectors are applied. Samtec QTH-030 60-pin connector is used on IO48 OOBE daughter card while Samtec QSH-030 60-pin connector is at the motherboard side.

10/100/1000 Mbps Ethernet PHY

This board supports copper RJ-45 10/100/1000 Mbps Ethernet using an external Ethernet PHY Microchip KSZ9031RNX. The PHY-to-MAC interface employs RGMII using Intel Stratix 10 SoC IO48 EMAC0 to transmit and receive data. For management interface, it uses MDC/MDIO interface between EMAC0 and Ethernet PHY.

Figure 6. Ethernet Block Diagram

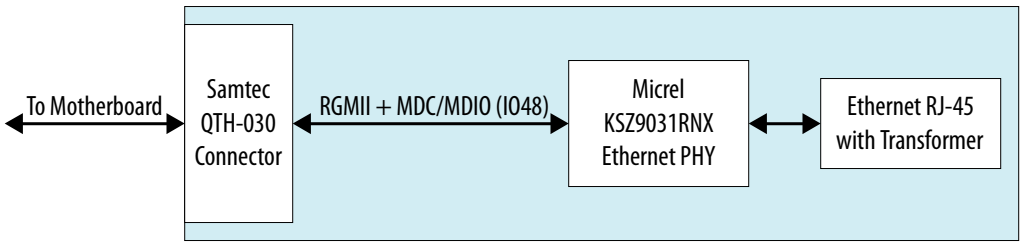


Table 26. Ethernet Signals List

Net Name	IO48 Location	Type	Description
ENET_TXD0	Q2_5	IN	RGMII Data Transmit Bit 0
ENET_TXD1	Q2_6	IN	RGMII Data Transmit Bit 1
ENET_TXD2	Q2_9	IN	RGMII Data Transmit Bit 2
ENET_TXD3	Q2_10	IN	RGMII Data Transmit Bit 3
ENET_GTX_CLK	Q2_1	IN	RGMII Transmit Reference Clock
ENET_TX_EN	Q2_2	IN	RGMII Transmit Control (TX_CTL)
ENET_RXD0	Q2_7	OUT	RGMII Data Receive Bit 0
ENET_RXD1	Q2_8	OUT	RGMII Data Receive Bit 1
ENET_RXD2	Q2_11	OUT	RGMII Data Receive Bit 2
ENET_RXD3	Q2_12	OUT	RGMII Data Receive Bit 3
ENET_RX_CLK	Q2_3	OUT	RGMII Receive Reference Clock
ENET_RX_DV	Q2_4	OUT	RGMII Receive Control (RX_CTL)
ENET_MDC	Q4_12	IN	Management Clock
ENET_MDIO	Q4_11	INOUT	Management Data
ENET_INTn	Q3_1	OUT	Ethernet PHY Interrupt Output
ENET_RESETn		IN	Ethernet PHY reset input connected to HPS_RESETn

UART

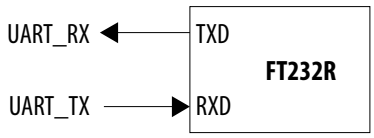
The IO48 OOBE daughter card uses a USB based UART bridge chip (FTDI FT232R) to bridge communication to a host for general UART usage. This chip uses TXD and RXD for transmission and reception of data.

Table 27. UART Signals List

Net Name	IO48 Location	Type	Description
UART_TX	Q3_3	IN	UART TX from Intel Stratix 10 HPS to FT232R
UART_RX	Q3_4	OUT	UART RX from FT232R to Intel Stratix 10 HPS
UART_RESETn		IN	FT232R Reset Input connected to HPS_RESETn

Based on signal direction, HPS IO48's UART_TX is connected to FT232R's RXD pin and HPS IO48's UART_RX is connected to FT232R's TXD.

Figure 7. UART Connection



Micro SD Connector

Intel Stratix 10 provides a Secure Digital/ Multimedia Card (SD/MMC) controller for interfacing to external SD/MMC flash cards, secure digital I/O devices and Consumer Electronics Adavnced Transport Architecture (CE-ATA) hard drives.

On IO48 OOBE daughter card, there is a standard MicroSD Memory Card connector that supports 4-bit SD memory interface.

Table 28. MicroSD Card Signal list

Net Name	IO48 Location	Type	Description
SD_DATA0	Q4_1	INOUT	Bi-directional data signal bit 0
SD_DATA1	Q4_4	INOUT	Bi-directional data signal bit 1
SD_DATA2	Q4_5	INOUT	Bi-directional data signal bit 2
SD_DATA3	Q4_6	INOUT	Bi-directional data signal bit 3
SD_CMD	Q4_2	INOUT	Bi-directional command/ response signal
SD_CLK	Q4_3	IN	Host to card clock signal
SD_POWER_ON		IN	SD card power ON/OFF control wired to HPS_RESETn

USB 2.0

Intel Stratix 10 HPS provides a USB On-the-Go (OTG) controller that supports both device and host functions. The controller supports all high-speed, full-speed and low-speed transfers in both device and host modes. Microchip USB 2.0 PHY USB3320 is used on IO48 OOBE daughter card with ULPI interface. A USB 2.0 Micro-AB receptacle to interface external USB host or device.

Table 29. USB 2.0 PHY Signal List

Net Name	IO48 Location	Type	Description
USB_DATA0	Q1_4	INOUT	ULPI bidirectional data bus bit 0
USB_DATA1	Q1_5	INOUT	ULPI bidirectional data bus bit 1
USB_DATA2	Q1_7	INOUT	ULPI bidirectional data bus bit 2
USB_DATA3	Q1_8	INOUT	ULPI bidirectional data bus bit 3

continued...

Net Name	IO48 Location	Type	Description
USB_DATA4	Q1_9	INOUT	ULPI bidirectional data bus bit 4
USB_DATA5	Q1_10	INOUT	ULPI bidirectional data bus bit 5
USB_DATA6	Q1_11	INOUT	ULPI bidirectional data bus bit 6
USB_DATA7	Q1_12	INOUT	ULPI bidirectional data bus bit 7
USB_CLK	Q1_1	OUT	ULPI clock output
USB_NXT	Q1_6	OUT	ULPI next data
USB_STP	Q1_2	IN	ULPI stop data
USB_DIR	Q1_3	OUT	ULPI data bus direction
USB_VFLAGn	Q3_2	OUT	USB over-current limit indicator to HPS IO48 GPIO pin
USB_RESETn		IN	USB3320 reset input connected to HPS_RESETn

JTAG

The JTAG interface is routed to Mictor 38-pin connector. Other trace signals are not routed to Mictor 38-pin due to the pinout limitation.

There are two JTAG sources for the HPS-JTAG: Mictor 38-pin connector, or SDM chained JTAG pins from the mother board. They are selected with on board resistor MUX by soldering suitable resistors. By default, all resistors are soldered, thus both sources can drive the HPS_JTAG pins.

If Mictor is selected to be the source, the MAX on motherboard can tri-state the FPGA_JTAG pins thus give control to the Probe on Mictor. If MAX is to be the source, no Probe can be connected to the Mictor thus MAX is the only source.

Figure 8. JTAG

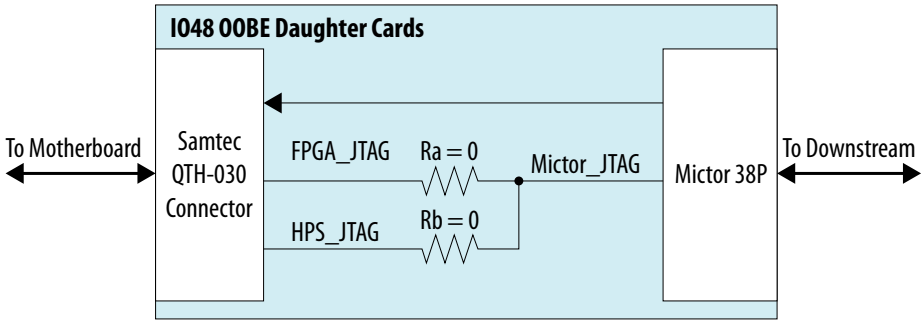


Table 30. JTAG Signal List

Net Name	IO48 Location	Type	Description
HPS_JTAG_TCK	Q3_9	OUT	HPS dedicated JTAG TCK on IO48
HPS_JTAG_TMS	Q3_10	OUT	HPS dedicated JTAG TMS on IO48
HPS_JTAG_TDO	Q3_11	IN	HPS dedicated JTAG TDO on IO48
HPS_JTAG_TDI	Q3_12	OUT	HPS dedicated JTAG TDI on IO48
FPGA_JTAG_TCK		IN	SDM chained JTAG TCK on SDM bank
FPGA_JTAG_TMS		IN	SDM chained JTAG TMS on SDM bank
FPGA_JTAG_TDO		OUT	SDM chained JTAG TDO on SDM bank
FPGA_JTAG_TDI		IN	SDM chained JTAG TDI on SDM bank
MICTOR_JTAG_TCK		IN	Mictor JTAG TCK on Mictor Connector
MICTOR_JTAG_TMS		IN	Mictor JTAG TMS on Mictor Connector
MICTOR_JTAG_TDO		OUT	Mictor JTAG TDO on Mictor Connector
MICTOR_JTAG_TDI		IN	Mictor JTAG TDI on Mictor Connector
MICTOR_JTAG_TRSTn		IN	Mictor JTAG TRSTn on Mictor Connector

I²C

The FPGA I²C and HPS I²C are connected on motherboard. HPS I²C left floating on this IO48 OOBE daughter card although it is connected to IO48 connector. A 3-pin 2.54 mm header is reserved on the OOBE daughter card with HPS I²C

GPIO

Remainder GPIO pins on IO48 are used as push buttons and LEDs.

Table 31. IO48 GPIO Signal List

Net Name	IO48 Location	Type	Description
HPS_PB0	Q3_5	OUT	Push Button 0 on daughter card
HPS_PB1	Q3_6	OUT	Push Button 1 on daughter card
HPS_LED0	Q4_9	IN	LED 0 on daughter card active high
HPS_LED1	Q4_8	IN	LED 1 on daughter card active high

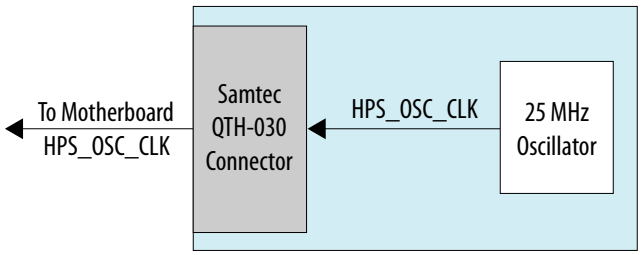
continued...

Net Name	IO48 Location	Type	Description
HPS_LED2	Q4_10	IN	LED 2 on daughter card active high
ENET_INTn	Q3_1	OUT	Ethernet PHY interrupt output
USB_VFLAGn	Q3_2	OUT	USB over-current limit indicator to HPS IO48 GPIO pin

HPS Clock

One on board oscillator provides a fixed 25 MHz single-ended clock for HPS PLL input (HPS_OSC_CLK). The OOBE card do not support clock frequency adjustment and external clock injection.

Figure 9. HPS Clock



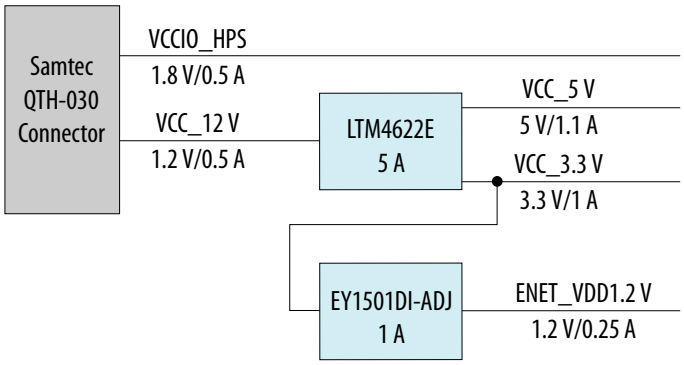
Power

There are two power rails drawn from motherboard through Samtec connector VCC_12V and VCCIO_HPS.

VCC_12V is major power source for IO48 OOBE daughter card and it will be converted to other power rails with on board regulators. It is recommended to have at least 1 A capability on VCC_12V power rail.

VCCIO_HPS is HPS I/O buffers power supply also from the motherboard. It is 1.8V nominal.

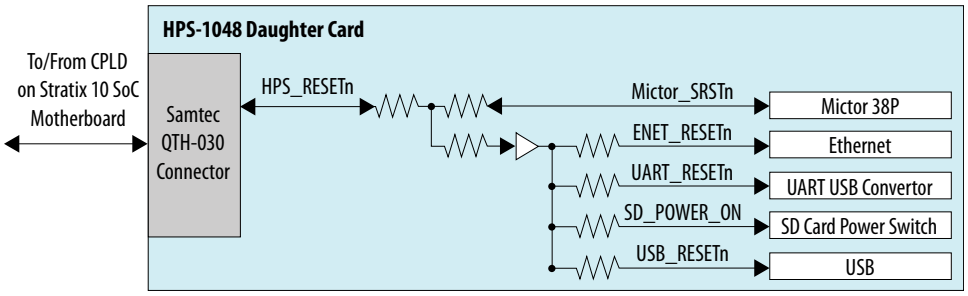
Figure 10. Power Tree



Reset

Reset is from Intel MAX 10 CPLD on the Intel Stratix 10 SoC mother board. The Intel MAX 10 controls all device's resets on the devlopment kit.

Figure 11. Reset Diagram



4.8.2. HPS IO-48 NAND Flash Daughter Card

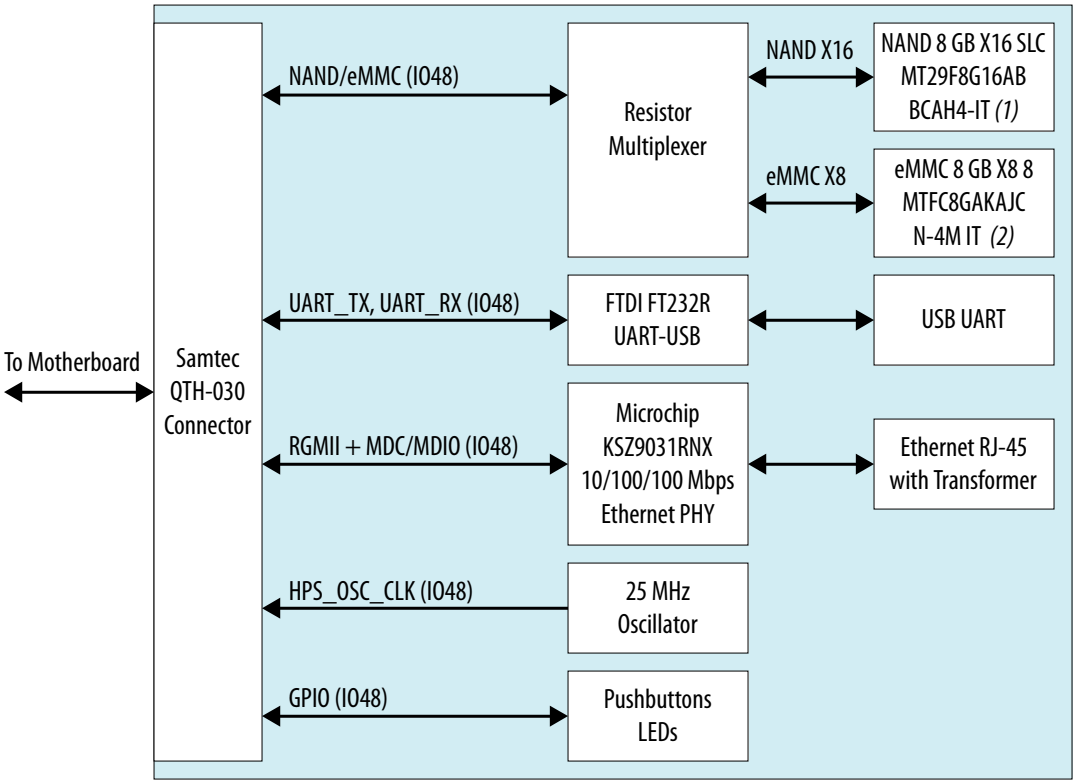
IO48 NAND Flash Feature Summary

Table 32. Feature Summary

Feature Name	Description
IO48 Connector	• Samtec QTH-030 Series 60-pin connector on IO48 daughter card side • Samtec QSH-030 Series 60-pin connector on motherboard
10/100/1000 Mbps Ethernet PHY with RGMII interface	• Microchip KSZ9031RNX Ethernet PHY • RGMII MAC Interface • MDC/MDIO Management Interface • Standard RJ-45 with integrated Ethernet Transformer
UART	• FTDI FT232R UART USB Convertor • Standard USB Mini-B Receptacle
NAND Flash	• Micron MT29F8G16ADBDAH4-AIT:D • 1.8V 8 Gb SLC ASYNC NAND Flash • x16 bit data width • VFBGA-63 Package • Multiplexed with eMMC Flash with resistor MUX (Cannot use simultaneously)
eMMC	• Micron MTFC8GAKAJCN-4M IT • 8 GB 5.0 compliant eMMC • Not support eMMC data strobe due to Intel Stratix 10 HPS limitation • VPFBGA-153 Package
I^2C	• HPS I^2C and FPGA I^2C is connected together on the motherboard
GPIO	• 2 GPIOs as Push Buttons • 3 GPIOs as LEDs • 1 GPIO as Ethernet Interrupt from Ethernet PHY
HPS Clock	• 1 On-board 25 MHz oscillator provides HPS clock
Mechanical	• Supposed 3" x 1.8" board size

Block Diagram

Figure 12. NAND Daughter Card Block Diagram



Notes:
1. You cannot use the NAND and eMMC connectors at the same time.
2. The eMMC connector is optional.

IO48 Interface

Stratix 10 SoC IO48 bank can be multiplexed to different peripheral interfaces. On NAND daughter card, IO48 bank is interfaced with Ethernet RGMII, UART, I^2C, NAND Flash, eMMC and GPIO interfaces.

Table 33. IO48 Pinout MUX

HPS Pin Name	Peripheral Name	Signal
Q1_1	NAND	ADQ0
Q1_2	NAND	ADQ1
Q1_3	NAND	WE_N
Q1_4	NAND	RE_N
Q1_5	NAND	WP_N
Q1_6	NAND	ADQ2
Q1_7	NAND	ADQ3

continued...

HPS Pin Name	Peripheral Name	Signal
Q1_8	NAND	CLE
Q1_9	NAND	ADQ4
Q1_10	NAND	ADQ5
Q1_11	NAND	ADQ6
Q1_12	NAND	ADQ7
Q2_1	NAND	ALE
Q2_2	NAND	RB
Q2_3	NAND	CE_N
Q2_4	CM	HPS_OSC_CLK
Q2_5	NAND	ADQ8
Q2_6	NAND	ADQ9
Q2_7	NAND	ADQ10
Q2_8	NAND	ADQ11
Q2_9	NAND	ADQ12
Q2_10	NAND	ADQ13
Q2_11	NAND	ADQ14
Q2_12	NAND	ADQ15
Q3_1	GPIO1	IO0
Q3_2	GPIO1	IO1
Q3_3	UART0	TX
Q3_4	UART0	RX
Q3_5	GPIO1	IO4
Q3_6	GPIO1	IO5
Q3_7	I2C1	SDA
Q3_8	I2C1	SCL
Q3_9	MDIO2	MDIO
Q3_10	MDIO2	MDC
Q3_11	GPIO1	IO10
Q3_12	GPIO1	IO11
Q4_1	EMAC2	TX_CLK
Q4_2	EMAC2	TX_CTL
Q4_3	EMAC2	RX_CLK
Q4_4	EMAC2	RX_CTL
Q4_5	EMAC2	TXD0

continued...

HPS Pin Name	Peripheral Name	Signal
Q4_6	EMAC2	TXD1
Q4_7	EMAC2	RXD0
Q4_8	EMAC2	RXD1
Q4_9	EMAC2	TXD2
Q4_10	EMAC2	TXD3
Q4_11	EMAC2	RXD2
Q4_12	EMAC2	RXD3

Connector to Motherboard

To connect between motherboard and IO48 NAND Flash daughter card, Samtec QSH/QTH series connectors are applied. Samtec QTH-030 60-pin connector is used on IO48 NAND Flash daughter card side while Samtec QSH 60-pin is at the mptherboard side.

10/100/1000 Mbps Ethernet PHY

This daughter card supports copper RJ-45 10/100/1000 Mbps Ethernet using an external Ethernet PHY Microchip KSZ9031RNX. The PHY-to-MAC interface employs RGMII using Intel Stratix 10 SoC IO48 EMAC2 to transmit and receive data. For management interface, it uses MDC/MDIO interface between EMAC2 and Ethernet PHY.

Figure 13. Ethernet PHY Block Diagram

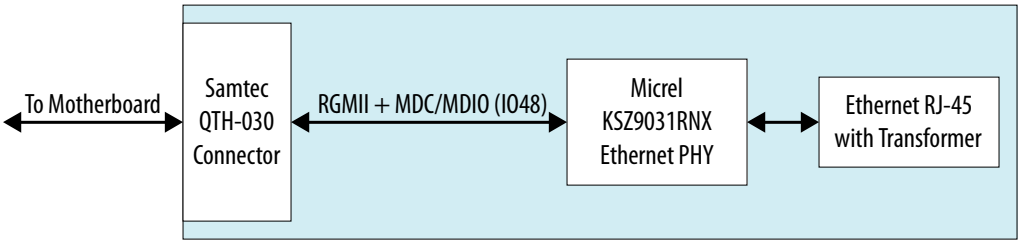


Table 34. Ethernet Signals List

Net Name	IO48 Location	Type	Description
ENET_TXD0	Q4_5	IN	RGMII Data Transmit Bit 0
ENET_TXD1	Q4_6	IN	RGMII Data Transmit Bit 1
ENET_TXD2	Q4_9	IN	RGMII Data Transmit Bit 2
ENET_TXD3	Q4_10	IN	RGMII Data Transmit Bit 3
ENET_GTX_CLK	Q4_1	IN	RGMII Transmit Reference Clock
ENET_TX_EN	Q4_2	IN	RGMII Transmit Control (TX_CTL)
ENET_RXD0	Q4_7	OUT	RGMII Data Receive Bit 0

continued...

Net Name	IO48 Location	Type	Description
ENET_RXD1	Q4_8	OUT	RGMII Data Receive Bit 1
ENET_RXD2	Q4_11	OUT	RGMII Data Receive Bit 2
ENET_RXD3	Q4_12	OUT	RGMII Data Receive Bit 3
ENET_RX_CLK	Q4_3	OUT	RGMII Receive Reference Clock
ENET_RX_DV	Q4_4	OUT	RGMII Receive Control (RX_CTL)
ENET_MDC	Q3_10	IN	Management Clock
ENET_MDIO	Q3_9	INOUT	Management Data
ENET_INTn	Q3_1	OUT	Ethernet PHY Interrupt Output

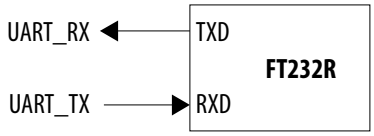
UART

Table 35. UART Signals List

Net Name	IO48 Location	Type	Description
UART_TX	Q3_3	IN	UART TX from Intel Stratix 10 HPS to FT232R
UART_RX	Q3_4	OUT	UART RX from FT232R to Intel Stratix 10 HPS
UART_RESETn		IN	FT232R reset input connected to HPS_RESETn

Based on the signal direction, HPS IO48's UART_TX is connected to FT232R's RXD pin and HPS IO48's UART_RX is connected to FT232R's TXD.

Figure 14. UART Connection



NAND Flash

The IO48 NAND flash daughter card supports a 16-bit NAND flash. Since some NAND flash pins are mutiplexed with eMMC pins, NAND flash and eMMC flash cannot be used simultaneously. There are MUX resistors to select related IO48 signals are connected to NAND flash or eMMC flash. The default setup is NAND flash.

The proposed NAND flash memory is **MT29F8G16ADBDAH4-AIT:D** manufactured by Micron. Major parameters are as listed below:

Table 36. NAND Flash Memory Parameters

Paramater	Description
Type	SLC NAND
Density	8 Gb
Data Width	16-bit
Voltage	1.8 V
Package	VFBGA-63
Operational Temperature	-40 C to +85 C

An optional NAND socket can be used for easy NAND Flash replacement when NAND flash is not soldered down. The socket vendor is Ironwood with part number SG-BGA-6367.

Table 37. NAND Flash Memory Signal List

Net Name	IO48 Location	Type	Direction
NAND_ADQ0	Q1_1	INOUT	Bidirectional data bit 0
NAND_ADQ1	Q1_2	INOUT	Bidirectional data bit 1
NAND_ADQ2	Q1_6	INOUT	Bidirectional data bit 2
NAND_ADQ3	Q1_7	INOUT	Bidirectional data bit 3
NAND_ADQ4	Q1_9	INOUT	Bidirectional data bit 4
NAND_ADQ5	Q1_10	INOUT	Bidirectional data bit 5
NAND_ADQ6	Q1_11	INOUT	Bidirectional data bit 6
NAND_ADQ7	Q1_12	INOUT	Bidirectional data bit 7
NAND_ADQ8	Q2_5	INOUT	Bidirectional data bit 8
NAND_ADQ9	Q2_6	INOUT	Bidirectional data bit 9
NAND_ADQ10	Q2_7	INOUT	Bidirectional data bit 10
NAND_ADQ11	Q2_8	INOUT	Bidirectional data bit 11
NAND_ADQ12	Q2_9	INOUT	Bidirectional data bit 12
NAND_ADQ13	Q2_10	INOUT	Bidirectional data bit 13
NAND_ADQ14	Q2_11	INOUT	Bidirectional data bit 14
NAND_ADQ15	Q2_12	INOUT	Bidirectional data bit 15
NAND_WEn	Q1_3	IN	Write Enable
NAND_REn	Q1_4	IN	Read Enable
NAND_WPn	Q1_5	IN	Write Protect
NAND_CLE	Q1_8	IN	Command Latch Enable
NAND_ALE	Q2_1	IN	Address Latch Enable
NAND_RBn	Q2_2	OUT	Ready/Busy
NAND_CEn	Q2_3	IN	Chip Enable

eMMC

The IO48 NAND flash daughter card also supports a 8-bit eMMC flash. Since the eMMC flash pins are multiplexed with NAND pins, NAND Flash and eMMC Flash cannot be used simultaneously. There are MUX resistors to select related IO48 signals are connected to NAND flash or eMMC flash. The default setup is NAND flash, not eMMC.

The proposed eMMC flash memory is **MTFC8GAKAJCN-4M IT** manufactured by Micron.

Table 38. eMMC Flash Parameters

Parameter	Description
Type	eMMC with 5.0-compliant (JESD84-B50)
Density	8 GB
Data Width	8-bit
Voltage	3.3 V VCC and 1.8 V/3.3 V VCCQ operation (VCCQ=1.8 V on this card)
Package	VFBGA-153
Operational Temperature	-40 C to +85 C

Table 39. eMMC Signal List

Net Name	IO48 Location	Type	Description
EMMC_D0	Q1_3	INOUT	eMMC bidirectional data bus bit
EMMC_D1	Q1_4	INOUT	eMMC bidirectional data bus bit
EMMC_D2	Q1_5	INOUT	eMMC bidirectional data bus bit
EMMC_D3	Q1_6	INOUT	eMMC bidirectional data bus bit
EMMC_D4	Q1_7	INOUT	eMMC bidirectional data bus bit
EMMC_D5	Q1_8	INOUT	eMMC bidirectional data bus bit
EMMC_D6	Q1_9	INOUT	eMMC bidirectional data bus bit
EMMC_D7	Q1_10	INOUT	eMMC bidirectional data bus bit
EMMC_CLK	Q1_1	IN	eMMC clock input
EMMC_CMD	Q1_2	INOUT	eMMC bi-directional command
EMMC_DS		OUT	eMMC Data Strobe. No Connection. Intel Stratix 10 does not support it.
EMMC_RSTn		IN	eMMC reset input. Connected to HPS_RESETn.

Note: Since Intel Stratix 10 HPS does not support HS400, Data Strobe pin on eMMC flash is not used. HS400 is not supported on this board.

I²C

The FPGA I²C and HPS I²C are connected together on motherboard. HPS I²C left floating on this IO48 debug daughter card although is connected to IO48 connector. A 3-pin 2.54 mm header is reserved with HPS I²C.

GPIO

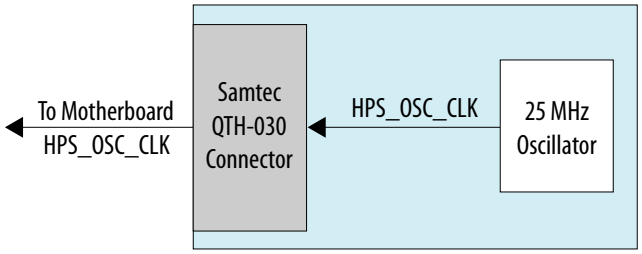
Table 40. IO48 GPIO Signals List

Net Name	IO48 Location	Type	Description
HPS_PB0	Q3_5	OUT	Push Button 0 on daughter card
HPS_PB1	Q3_6	OUT	Push Button 1 on daughter card
HPS_LED0	Q3_2	IN	LED 0 on daughter card active high
HPS_LED1	Q3_11	IN	LED 1 on daughter card active high
HPS_LED2	Q3_12	IN	LED 2 on daughter card active high
ENET_INTn	Q3_1	OUT	Ethernet PHY interrupt output

HPS Clock

One on-board oscillator provides a fixed 25 MHz single-ended clock for HPS PLL input.

Figure 15. Clock Diagram

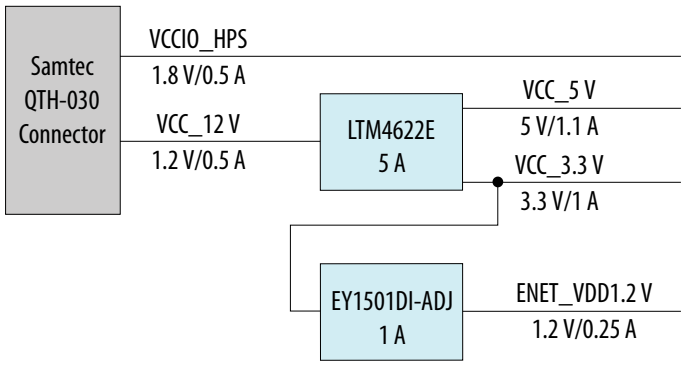


Power

There are two power rails drawn from motherboard through Samtec connector VCC_12V and VCCIO_HPS. VCC_12V is major power source and it is converted to other power rails with on-board regulators. It is recommended to have at least 1 A capabiity on VCC_12V power rail.

VCCIO_HPS is HPS I/O buffers power supply from motherboard.

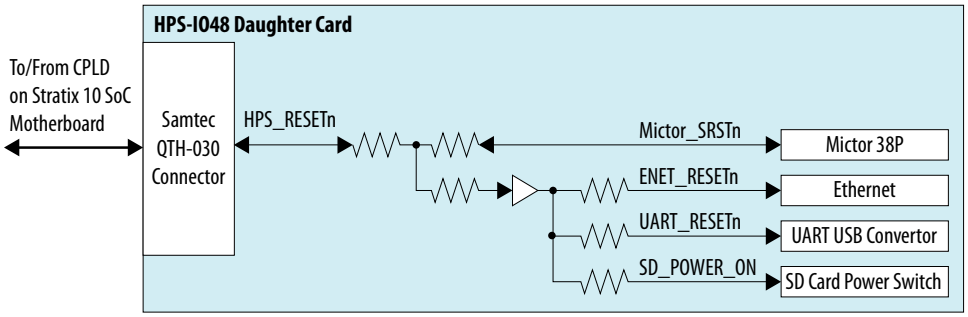
Figure 16. Power Diagram



Reset

Reset is from MAX 10 CPLD on Stratix 10 SoC motherboard. The MAX 10 controls all devices' resets on the develpment kit.

Figure 17. Reset Diagram



4.8.3. HPS Boot Flash Card

The Intel Stratix 10 SoC Boot Flash daughter cards have four independent types as listed below

- Boot QSPI Flash
- Boot MicroSD
- Boot eMMC

Attention: Boot eMMC Flash Card is sold separately and is not included in the development kit package.

These boot flash daughter cards are connected to the SDM bank of the Intel Stratix 10 FPGA. They are plugged into the Samtec SDM Flash connector.

Table 41. Feature Summary

Feature	Description
Card Connector	• Samtec QSH-030 Series 60-pin connector on Boot Flash daughter cards side • Samtec QTH-030 Series 60-pin connector on the motherboard
Boot QSPI Flash Card	• Micron 2 Gb 1.8V QSPI Flash • TPBGA-24 package • Compatible with Intel EPCQ-L devices
Boot MicroSD Card	• 4-bit SD Card Data Bus • Standard MicroSD Card Socket
Boot eMMC Card	• Micron 8 GB eMMC • VFBGA-153 package
Mechanical	• 1.5" x 1"

Connector to Motherboard

To connect between the motherboard and Boot flash daughter card, Samtec QSH/QTH series connectors are used. Samtec QSH-030 60-pin connector is used on boot flash daughter cards while Samtec QTH-030 60-pin connector is at the motherboard side.

Figure 18. Samtec QSH-030

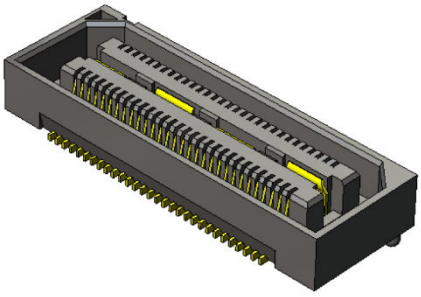
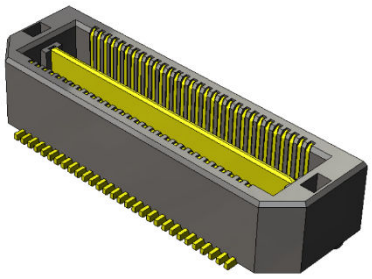


Figure 19. Samtec QTH-030



Card Identification

There is one CARD_PRSTn signal on the Boot Flash daughter cards to identify whether card is plugged in. This signal is connected to CPLD on the Intel Stratix 10 SoC development kit.

CARD_PRSTn is pulled high on the motherboard and directly tie to GND on Boot Flash daughter cards.

Table 42. Card Identification

CARD_PRSTn	Status
1	No daughter card is plugged in
0	One daughter card is plugged in

Power

There are two power rails drawn from motherboard through Samtec connector 3.3 V and 1.8 V.

Table 43. Card Identification

	Current @ 1.8 V (A)	Current @ 3.3 V (A)	Total Power (W)
MicroSD	-	0.22	1.32
QSPI Flash	0.1	-	0.18
eMMC	0.1	0.05	0.35

Note: The power of MicroSD card is estimated at SDR25 (50 MHz).

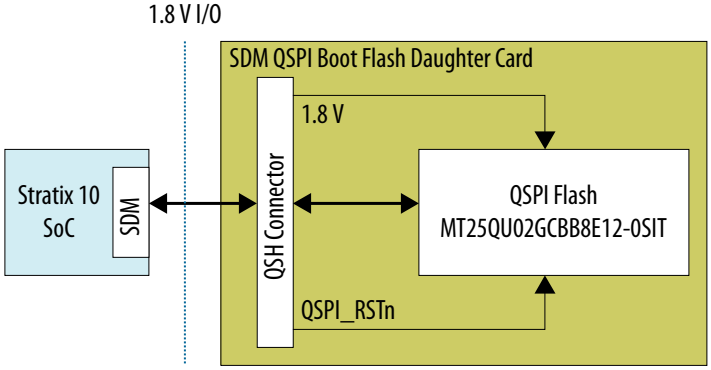
4.8.3.1. Boot QSPI Flash Daughter Card

This card supports a 2 Gb density QSPI NOR Flash manufactured by Micron. The QSPI NOR Flash uses TPBGA-24 package which is compatible with Intel EPCQ-L devices. To support EPCQ-L devices, you need to change BOM of the board.

The key features of the QSPI Flash used on this board are:

- Micron P/N: MT25QU02GCBB8E12-0SIT
- 2 Gb NOR Flash
- 1.8V QSPI I/O
- Operation Temperature: -40 C to +85 C
- TPBGA-24 package which is compatible with Intel EPCQ-L devices

Figure 20. Boot QSPI Flash Daughter Card Block Diagram

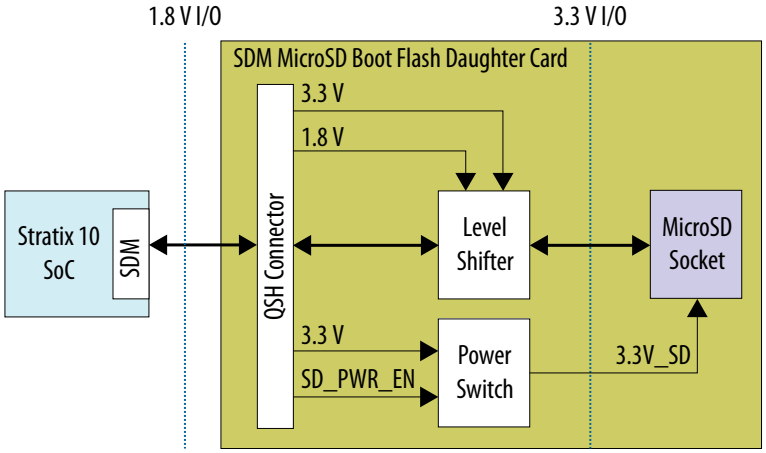


4.8.3.2. Boot MicroSD Daughter Card

This card suppports a 4-bit Micro SD Card with a Micro SD card socket. There is a voltage level shifter between Intel Stratix 10 SoC SDM bank and MicroSD card which can translate between 1.8 V I/O and 3.3 V I/O.

There is an extra signal called SD_PWR_EN is from CPLD on the Intel Stratix 10 SoC development kit. This signal is used to power cycle/reset MicroSD Card on this board.

Figure 21. Boot MicroSD Daughter Card Block Diagram



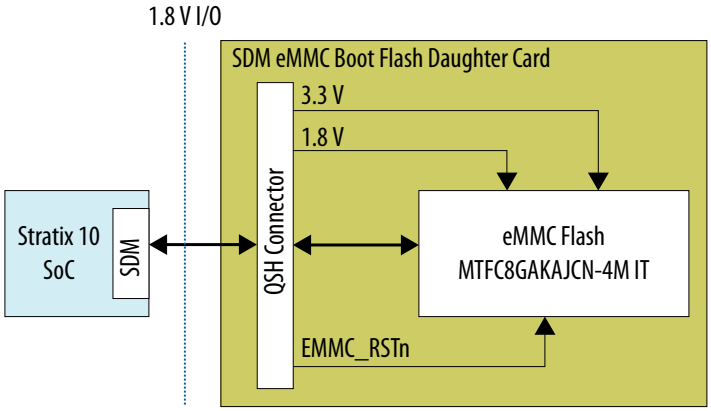
4.8.3.3. Boot eMMC Daughter Card

This card supports an 8-bit eMMC Flash manufactured by Micron. The NAND Flash uses VFBGA-153 package.

The key features of the eMMC Flash are:

- Micron MTFC8GAKAJCN-4M IT
- Type: eMMC with 5.0-compliant (JESD84-B50)
- Density: 8 GB
- Data Width: 8-bit
- Voltage: 3.3V VCC and 1.8V/3.3V VCCQ operation
- Package: VFBGA-153
- Operation Temperature: -40 C to +85 C

Figure 22. Boot eMMC Daughter Card Block Diagram



4.9. System Memory

4.9.1. FPGA Memory (DDR4 SO-DIMM)

The 72-bit memory interface connected to the SO-DIMM card is assigned to four I/O banks (3I, 3J, 3K and 3L). The reference clock of the DDR4 port is the 133.33 MHz clock generated by Silicon Lab Si5338. The SODIMM memory part number is MTA18ASF2G72Hz. Its I^2C EEPROM Address is 0b1010101. Its Temp Sensor Address is 0b0011101.

Table 44. SO-DIMM FPGA Pin Map

Pin Name	Schematic Signal Name	Description
PIN_V21	SL_DQB3	DDR4 DQ
PIN_V22	SL_DQB1	DDR4 DQ
PIN_T21	SL_DQB7	DDR4 DQ
PIN_R21	SL_DQB6	DDR4 DQ
PIN_V23	SL_DQB4	DDR4 DQ
PIN_V24	SL_DQB5	DDR4 DQ
PIN_U20	SL_DQSN0	DDR4 DQSN
PIN_T20	SL_DQSP0	DDR4 DQSP
PIN_R22	SL_DQB0	DDR4 DQ
PIN_T22	SL_DQB2	DDR4 DQ
PIN_U23	SL_DM0	DDR4 DM
PIN_E11	SL_DQB37	DDR4 DQ
PIN_F11	SL_DQB33	DDR4 DQ
PIN_G10	SL_DQB39	DDR4 DQ
PIN_H10	SL_DQB35	DDR4 DQ

continued...

Pin Name	Schematic Signal Name	Description
PIN_D10	SL_DQB36	DDR4 DQ
PIN_D11	SL_DQB32	DDR4 DQ
PIN_G12	SL_DQSN4	DDR4 DQSN
PIN_H12	SL_DQSP4	DDR4 DQSP
PIN_F10	SL_DQB34	DDR4 DQ
PIN_E10	SL_DQB38	DDR4 DQ
PIN_F12	SL_DM4	DDR4 DM
PIN_J11	SL_DQB56	DDR4 DQ
PIN_H11	SL_DQB61	DDR4 DQ
PIN_K11	SL_DQB58	DDR4 DQ
PIN_K12	SL_DQB59	DDR4 DQ
PIN_K10	SL_DQB63	DDR4 DQ
PIN_J10	SL_DQB62	DDR4 DQ
PIN_M12	SL_DQSN7	DDR4 DQSN
PIN_L12	SL_DQSP7	DDR4 DQSP
PIN_L10	SL_DQB60	DDR4 DQ
PIN_L11	SL_DQB57	DDR4 DQ
PIN_K13	SL_DM7	DDR4 DM
PIN_N13	SL_DQB46	DDR4 DQ
PIN_P14	SL_DQB47	DDR4 DQ
PIN_M13	SL_DQB41	DDR4 DQ
PIN_M14	SL_DQB44	DDR4 DQ
PIN_P15	SL_DQB42	DDR4 DQ
PIN_P16	SL_DQB40	DDR4 DQ
PIN_P13	SL_DQSN5	DDR4 DQSN
PIN_P12	SL_DQSP5	DDR4 DQSP
PIN_R16	SL_DQB45	DDR4 DQ
PIN_R17	SL_DQB43	DDR4 DQ
PIN_R14	SL_DM5	DDR4 DM
PIN_T19	SL_DQB14	DDR4 DQ
PIN_U19	SL_DQB9	DDR4 DQ
PIN_R18	SL_DQB10	DDR4 DQ
PIN_R19	SL_DQB11	DDR4 DQ
PIN_W18	SL_DQB12	DDR4 DQ

continued...

Pin Name	Schematic Signal Name	Description
PIN_V17	SL_DQB13	DDR4 DQ
PIN_T17	SL_DQSN1	DDR4 DQSN
PIN_U17	SL_DQSP1	DDR4 DQSP
PIN_U18	SL_DQB15	DDR4 DQ
PIN_V18	SL_DQB8	DDR4 DQ
PIN_T16	SL_DM1	DDR4 DM
PIN_M15	SL_CK1N	DDR4 Bank 1 ClockN
PIN_N15	SL_CK1P	DDR4 Bank 1 ClockP
PIN_K16	SL_ALERTN	DDR4 ALERTn
PIN_L16	SL_EVENTN	DDR4 SO-DIMM Eventn
PIN_M18	SL_C1N	DDR4 Bank 1 C1
PIN_M17	SL_C0N	DDR4 Bank 0 C0
PIN_J14	SL_BG0	DDR4 BG0
PIN_K14	SL_BA1	DDR4 BA1
PIN_H17	SL_BA0	DDR4 BA0
PIN_F15	SL_RASN	DDR4 RASN
PIN_G15	SL_CASN	DDR4 CASN
PIN_J15	SL_WEN	DDR4 WEN
PIN_H15	SL_A13	DDR4 A13
PIN_L14	SL_A12	DDR4 A12
PIN_H16	CLK_EMI_1N	DDR4 EMIF Reference Clock N
PIN_J16	CLK_EMI_1P	DDR4 EMIF Reference Clock P
PIN_F16	SL_A11	DDR4 A11
PIN_E16	SL_A10	DDR4 A10
PIN_D15	SL_A9	DDR4 A9
PIN_C15	SL_A8	DDR4 A8
PIN_B15	SL_A7	DDR4 A7
PIN_A16	SL_A6	DDR4 A6
PIN_B13	SL_A5	DDR4 A5
PIN_B14	SL_A4	DDR4 A4
PIN_A15	SL_A3	DDR4 A3
PIN_A14	SL_A2	DDR4 A2
PIN_D16	SL_A1	DDR4 A1
PIN_C16	SL_A0	DDR4 A0

continued...

Pin Name	Schematic Signal Name	Description
PIN_A12	SL_PARITY	DDR4 Parity
PIN_B12	SL_CS1N	DDR4 BANK 1 CSN
PIN_D14	SL_CK0N	DDR4 BANK 0 Clock N
PIN_E14	SL_CK0P	DDR4 BANK 0 Clock P
PIN_C12	SL_CKE1	DDR4 BANK 1 CKE
PIN_C13	SL_CKE0	DDR4 BANK 0 CKE
PIN_F14	SL_ODT1N	DDR4 BANK 1 ODTN
PIN_G14	SL_ODT0N	DDR4 BANK 0 ODTN
PIN_D13	SL_ACTN	DDR4 ACTn
PIN_E13	SL_CS0N	DDR4 CS0n
PIN_H13	SL_RESETN	DDR4 SO-DIMM RESETN
PIN_G13	SL_BG1	DDR4 BG1
PIN_B20	SL_DQB28	DDR4 DQ
PIN_A19	SL_DQB26	DDR4 DQ
PIN_B17	SL_DQB27	DDR4 DQ
PIN_A17	SL_DQB31	DDR4 DQ
PIN_A21	SL_DQB30	DDR4 DQ
PIN_A20	SL_DQB24	DDR4 DQ
PIN_C18	SL_DQSN3	DDR4 DQSN
PIN_C17	SL_DQSP3	DDR4 DQSP
PIN_B22	SL_DQB29	DDR4 DQ
PIN_A22	SL_DQB25	DDR4 DQ
PIN_B19	SL_DM3	DDR4 DM
PIN_E17	SL_DQB23	DDR4 DQ
PIN_F17	SL_DQB19	DDR4 DQ
PIN_D18	SL_DQB20	DDR4 DQ
PIN_E18	SL_DQB18	DDR4 DQ
PIN_D19	SL_DQB16	DDR4 DQ
PIN_E19	SL_DQB22	DDR4 DQ
PIN_C20	SL_DQSN2	DDR4 DQSN
PIN_D20	SL_DQSP2	DDR4 DQSP
PIN_D21	SL_DQB17	DDR4 DQ
PIN_E21	SL_DQB21	DDR4 DQ
PIN_C21	SL_DM2	DDR4 DM

continued...

Pin Name	Schematic Signal Name	Description
PIN_J19	SL_DQB54	DDR4 DQ
PIN_J20	SL_DQB50	DDR4 DQ
PIN_F19	SL_DQB52	DDR4 DQ
PIN_G19	SL_DQB49	DDR4 DQ
PIN_K18	SL_DQB48	DDR4 DQ
PIN_J18	SL_DQB53	DDR4 DQ
PIN_F21	SL_DQSN6	DDR4 DQSN
PIN_F20	SL_DQSP6	DDR4 DQSP
PIN_H18	SL_DQB55	DDR4 DQ
PIN_G18	SL_DQB51	DDR4 DQ
PIN_H20	SL_DM6	DDR4 DM
PIN_H21	SL_DQB69	DDR4 DQ
PIN_J21	SL_DQB68	DDR4 DQ
PIN_L19	SL_DQB70	DDR4 DQ
PIN_K19	SL_DQB64	DDR4 DQ
PIN_L21	SL_DQB71	DDR4 DQ
PIN_K21	SL_DQB65	DDR4 DQ
PIN_L20	SL_DQSN8	DDR4 DQSN
PIN_M20	SL_DQSP8	DDR4 DQSP
PIN_N21	SL_DQB66	DDR4 DQ
PIN_P21	SL_DQB67	DDR4 DQ
PIN_N20	SL_DM8	DDR4 DM

4.9.2. HPS Memory (External 4 GB HILO x72 DDR4)

The 72-bit HPS DDR4 memory interface (64-bit data and 8-bit ECC data), assigned in FPGA 2L, 2M and 2N I/O banks, is connected to a 4 GB HILO x72 memory daughter card. The target design speed is 1333 MHz DDR4 bus.

Table 45. HPS HILO DDR4 Memory Map

Pin Name	Schematic Signal Name	Description
PIN_E27	MEM_DMA0	DDR4 DM
PIN_D26	MEM_DQA6	DDR4 DQ
PIN_G27	MEM_DQA0	DDR4 DQ
PIN_F27	MEM_DQA3	DDR4 DQ
PIN_C27	MEM_DQA1	DDR4 DQ
PIN_B27	MEM_DQA2	DDR4 DQ

continued...

Pin Name	Schematic Signal Name	Description
PIN_F26	MEM_DQSA_N0	DDR4 DQSN
PIN_E26	MEM_DQSA_P0	DDR4 DQSP
PIN_B25	MEM_DQA5	DDR4 DQ
PIN_C26	MEM_DQA4	DDR4 DQ
PIN_D25	MEM_DQA7	DDR4 DQ
PIN_L26	MEM_DMA3	DDR4 DM
PIN_K27	MEM_DQA29	DDR4 DQ
PIN_M27	MEM_DQA24	DDR4 DQ
PIN_L27	MEM_DQA25	DDR4 DQ
PIN_H27	MEM_DQA28	DDR4 DQ
PIN_H26	MEM_DQA30	DDR4 DQ
PIN_K26	MEM_DQSA_N3	DDR4 DQSN
PIN_J26	MEM_DQSA_P3	DDR4 DQSP
PIN_G25	MEM_DQA26	DDR4 DQ
PIN_F25	MEM_DQA31	DDR4 DQ
PIN_H25	MEM_DQA27	DDR4 DQ
PIN_V30	MEM_DMA1	DDR4 DM
PIN_U30	MEM_DQA8	DDR4 DQ
PIN_T30	MEM_DQA9	DDR4 DQ
PIN_T29	MEM_DQA10	DDR4 DQ
PIN_U28	MEM_DQA11	DDR4 DQ
PIN_U29	MEM_DQA15	DDR4 DQ
PIN_V27	MEM_DQSA_N1	DDR4 DQSN
PIN_V28	MEM_DQSA_P1	DDR4 DQSP
PIN_V26	MEM_DQA14	DDR4 DQ
PIN_V25	MEM_DQA12	DDR4 DQ
PIN_U27	MEM_DQA13	DDR4 DQ
PIN_N25	MEM_DMA2	DDR4 DM
PIN_P25	MEM_DQA18	DDR4 DQ
PIN_P26	MEM_DQA22	DDR4 DQ
PIN_R26	MEM_DQA21	DDR4 DQ
PIN_T25	MEM_DQA17	DDR4 DQ
PIN_U25	MEM_DQA16	DDR4 DQ
PIN_R27	MEM_DQSA_N2	DDR4 DQSN

continued...

Pin Name	Schematic Signal Name	Description
PIN_T26	MEM_DQSA_P2	DDR4 DQSP
PIN_M25	MEM_DQA23	DDR4 DQ
PIN_L25	MEM_DQA20	DDR4 DQ
PIN_N27	MEM_DQA19	DDR4 DQ
PIN_U34	MEM_DQ_ADDR_CMD0	DDR4 DM
PIN_U33	MEM_DQ_ADDR_CMD3	DDR4 DQ
PIN_T31	MEM_DQ_ADDR_CMD4	DDR4 DQ
PIN_R31	MEM_DQ_ADDR_CMD2	DDR4 DQ
PIN_T34	MEM_DQ_ADDR_CMD1	DDR4 DQ
PIN_R34	MEM_DQ_ADDR_CMD5	DDR4 DQ
PIN_T32	MEM_DQS_ADDR_CMD_N	DDR4 DQSN
PIN_R32	MEM_DQS_ADDR_CMD_P	DDR4 DQSP
PIN_U32	MEM_DQ_ADDR_CMD6	DDR4 DQ
PIN_V32	MEM_DQ_ADDR_CMD7	DDR4 DQ
PIN_P33	MEM_DQ_ADDR_CMD8	DDR4 DQ
PIN_R36	MEM_ADDR_CMD18	DDR4 BG0
PIN_T35	MEM_ADDR_CMD17	DDR4 BA1
PIN_L36	MEM_ADDR_CMD16	DDR4 BA0
PIN_L35	MEM_ADDR_CMD19	DDR4 A17
PIN_P36	MEM_ADDR_CMD26	DDR4 A16
PIN_N36	MEM_ADDR_CMD15	DDR4 A15
PIN_K37	MEM_ADDR_CMD14	DDR4 A14
PIN_K36	MEM_ADDR_CMD13	DDR4 A13
PIN_P35	MEM_ADDR_CMD12	DDR4 A12
PIN_N35	CLK_EMI_N	EMIF Ref clockN
PIN_M35	CLK_EMI_P	EMIF Ref clockP
PIN_P38	MEM_ADDR_CMD11	DDR4 A11
PIN_N37	MEM_ADDR_CMD10	DDR4 A10
PIN_R37	MEM_ADDR_CMD9	DDR4 A9
PIN_P37	MEM_ADDR_CMD8	DDR4 A8
PIN_L39	MEM_ADDR_CMD7	DDR4 A7
PIN_K39	MEM_ADDR_CMD6	DDR4 A6
PIN_J38	MEM_ADDR_CMD5	DDR4 A5
PIN_J39	MEM_ADDR_CMD4	DDR4 A4

continued...

Pin Name	Schematic Signal Name	Description
PIN_M38	MEM_ADDR_CMD3	DDR4 A3
PIN_M37	MEM_ADDR_CMD2	DDR4 A2
PIN_L37	MEM_ADDR_CMD1	DDR4 A1
PIN_K38	MEM_ADDR_CMD0	DDR4 A0
PIN_H40	MEM_ADDR_CMD31	DDR4 PAR
PIN_J40	MEM_ADDR_CMD30	DDR4 CSN1 (not use)
PIN_G39	MEM_CLK_N	DDR4 BANK CLKN
PIN_F39	MEM_CLK_P	DDR4 BANK CLKP
PIN_K40	MEM_ADDR_CMD21	DDR4 CKe1 (no use)
PIN_L40	MEM_ADDR_CMD20	DDR4 CKe0
PIN_F40	MEM_ADDR_CMD25	DDR4 ODT1 (no use)
PIN_G40	MEM_ADDR_CMD24	DDR4 ODT0
PIN_H38	MEM_ADDR_CMD23	DDR4 ACTn
PIN_G38	MEM_ADDR_CMD22	DDR4 CSn0
PIN_E40	MEM_ADDR_CMD27	DDR4 Resetn
PIN_D40	MEM_ADDR_CMD28	DDR4 BG1
PIN_J34	MEM_DMB0	DDR4 DM
PIN_K34	MEM_DQB1	DDR4 DQ
PIN_N32	MEM_DQB3	DDR4 DQ
PIN_N31	MEM_DQB6	DDR4 DQ
PIN_K33	MEM_DQB0	DDR4 DQ
PIN_K32	MEM_DQB4	DDR4 DQ
PIN_L31	MEM_DQSB_N0	DDR4 DQSN
PIN_L32	MEM_DQSB_P0	DDR4 DQSP
PIN_N33	MEM_DQB5	DDR4 DQ
PIN_M33	MEM_DQB2	DDR4 DQ
PIN_M34	MEM_DQB7	DDR4 DQ
PIN_F34	MEM_DMB2	DDR4 DM
PIN_E34	MEM_DQB17	DDR4 DQ
PIN_J35	MEM_DQB21	DDR4 DQ
PIN_H35	MEM_DQB22	DDR4 DQ
PIN_F35	MEM_DQB18	DDR4 DQ
PIN_G35	MEM_DQB20	DDR4 DQ
PIN_G34	MEM_DQSB_N2	DDR4 DQSN

continued...

Pin Name	Schematic Signal Name	Description
PIN_G33	MEM_DQSB_P2	DDR4 DQSP
PIN_H36	MEM_DQB23	DDR4 DQ
PIN_J36	MEM_DQB19	DDR4 DQ
PIN_H33	MEM_DQB16	DDR4 DQ
PIN_D39	MEM_DMB1	DDR4 DM
PIN_E39	MEM_DQB9	DDR4 DQ
PIN_E38	MEM_DQB11	DDR4 DQ
PIN_D38	MEM_DQB12	DDR4 DQ
PIN_D35	MEM_DQB14	DDR4 DQ
PIN_D34	MEM_DQB13	DDR4 DQ
PIN_F36	MEM_DQSB_N1	DDR4 DQSN
PIN_E36	MEM_DQSB_P1	DDR4 DQSP
PIN_F37	MEM_DQB10	DDR4 DQ
PIN_E37	MEM_DQB15	DDR4 DQ
PIN_H37	MEM_DQB8	DDR4 DQ
PIN_C36	MEM_DMB3	DDR4 DM
PIN_D36	MEM_DQB26	DDR4 DQ
PIN_C35	MEM_DQB29	DDR4 DQ
PIN_B35	MEM_DQB25	DDR4 DQ
PIN_B37	MEM_DQB27	DDR4 DQ
PIN_C37	MEM_DQB31	DDR4 DQ
PIN_A35	MEM_DQSB_N3	DDR4 DQSN
PIN_A36	MEM_DQSB_P3	DDR4 DQSP
PIN_B38	MEM_DQB28	DDR4 DQ
PIN_C38	MEM_DQB30	DDR4 DQ
PIN_A37	MEM_DQB24	DDR4 DQ
PIN_A38	HPS_ALERT_N2	DDR4 Altertn

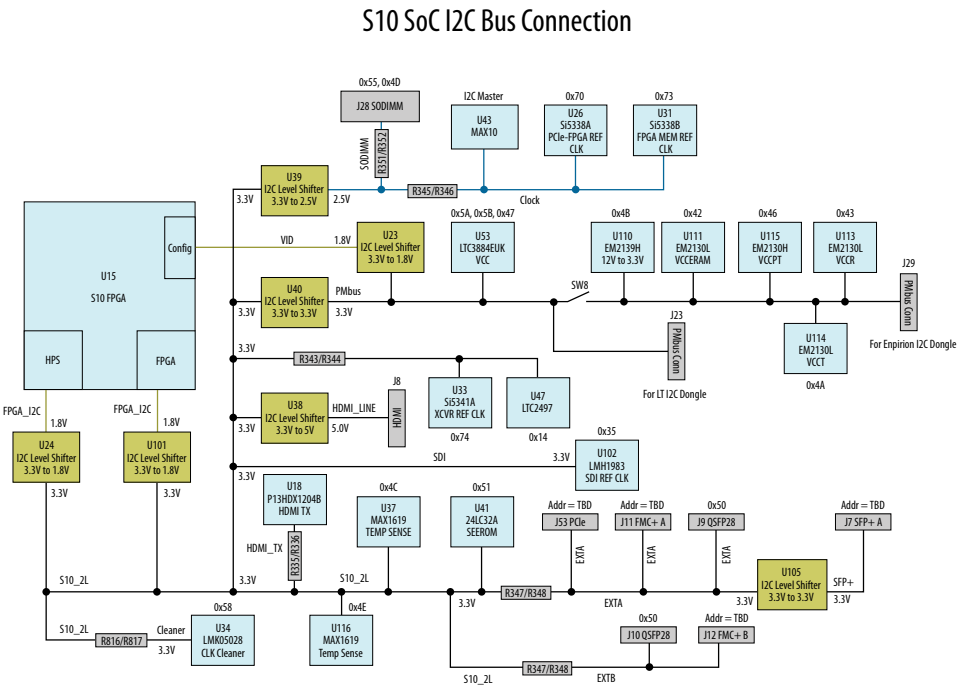
4.9.3. HPS I²C Interface

HPS I²C interface is assigned to HPS GPIO IO1, IO6 and IO7. HPS I²C controller can scan the board and collect MAC address, board temperature and power data of FPGA. A control signal generated by MAX10 system controller is used to enable HPS I²C system port .

Table 46. I²C Device Address

Type	Address	Device
HPS I²C Address	0x14	LTC2497 ADC
	0x74	SI5341 Clock Generator
	0x51	24LC32A EEPROM
	0x5C	DS1339C RTC
	0x4C	MAX1619 TEMP
	0x55	SODIMM EEPROM
	0x1D	SODIMM TEMP
	0x70	SI5338 Clock Generator
	0x73	SI5338 EMIF Clock Generator
	0x47	LTC3884 Core power Controller
	0x43	LTM4677 VCCR Power Controller
	0x42	LTM4677 VCCERAM_HPS Power controller
	0x46	LTM4677 VCCPT_VCCT Power controller
	0x4E	LTM4676A 3.3V power controller
FPGA I²C Address	0x70	SFP+
	0x70	ZQSFP+ port 0/1
	0x00	LMK05028 Clock Cleaner
	0x65	LMH1983 SDI clock generator
	0x73	HDMI port

Figure 23. HPS I²C Interface



4.10. System Power

4.10.1. Power Supply Options

Table 47. Power Supply List

Power Source Name	Power Name	Maximum Output Current (A)	Actual Current (A)
LTC3884 240A	Core Power (0.85V)	240	190
EM2130L, EN63A0QI	Output 0 (0.95V)	18	13
	Output 1 (0.9V)	18	6
EM2130L	Output 0 & 1 (1.12V)	36	23
EM2130L/EM2130H	Output 0 (1.12V)	18	6
	Output 1 (1.8V)	18	16
EM2130H	Output 0 & 1 (3.3V)	26	20
LTM4625	Output (5V)	5	3
EN63A0Q1	Output (1.8V)	12	8
EN6337QI	Output (2.5V)	3	1
EP5348UI	Output (2.4V)	0.4	0.1
EN63A0QI	Output (1.2V)	12	8
EN6360QI	Output (1.2V)	8	4
TPS51200 (DDR VTT)	Output (0.6V)	5	2

4.10.2. Power Sequence

The power-up/down sequence design follows power-up and power-down sequence requirements for Intel Stratix 10 devices, PCIe Plug-in Card power up/down requirement, and FMC plug-in card power up/down requirement.

The following figures show the development kit power up/down sequence.

Figure 24. Power Up Sequence

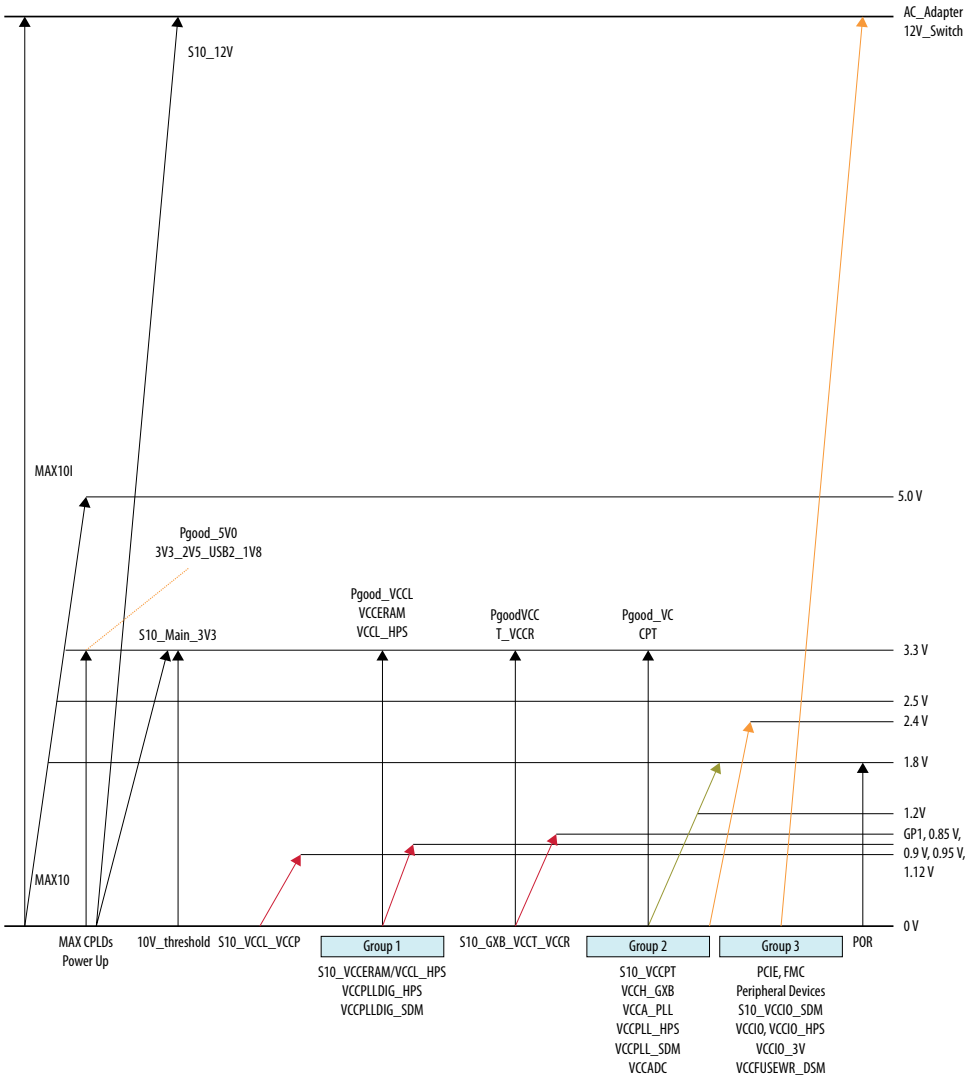
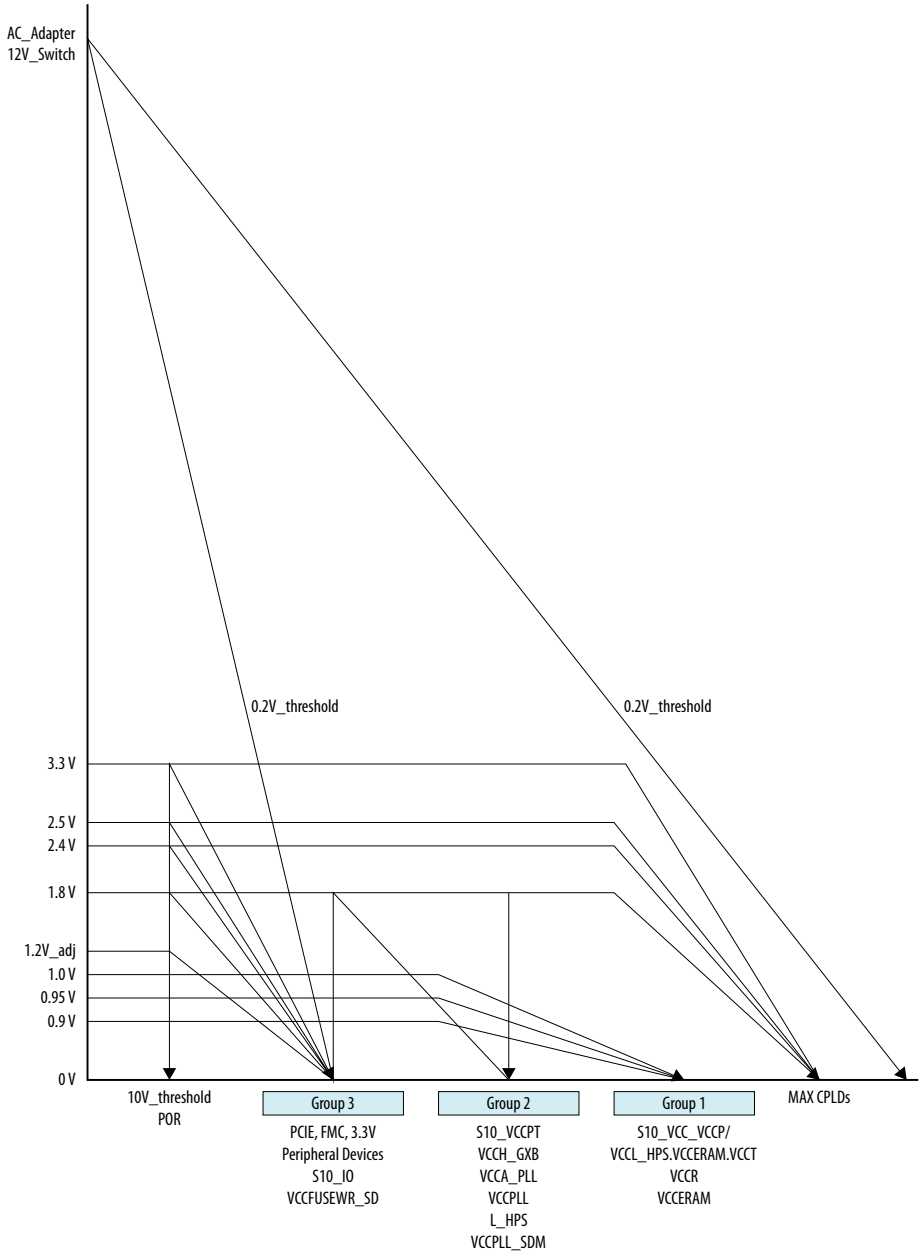


Figure 25. Power Down Sequence

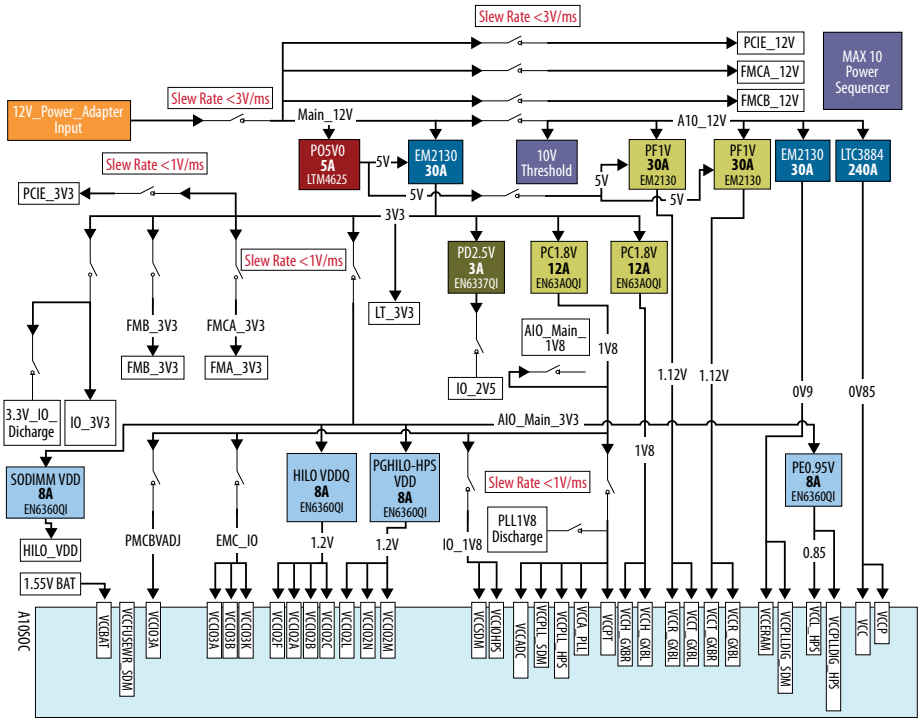


4.10.3. Power Distribution Network

The Intel Stratix 10 Development Kit uses the Intel MAX 10 CPLD (U46) as a power sequencer. J26 needs to be shorted to program Intel MAX 10 Power CPLD (U46). During normal operation, J26 needs to be open. The Intel MAX 10 CPLD monitors all power good signals, the 12V input voltage threshold signal (>10.2V), and turns on each FPGA power supply based on the power sequence requirements.

If 12V input voltage is below 12V input threshold voltage, the power down sequence is triggered. The Intel MAX 10 Power CPLD turns on the quick discharge circuit and turns off each power supply based on power down sequence requirements.

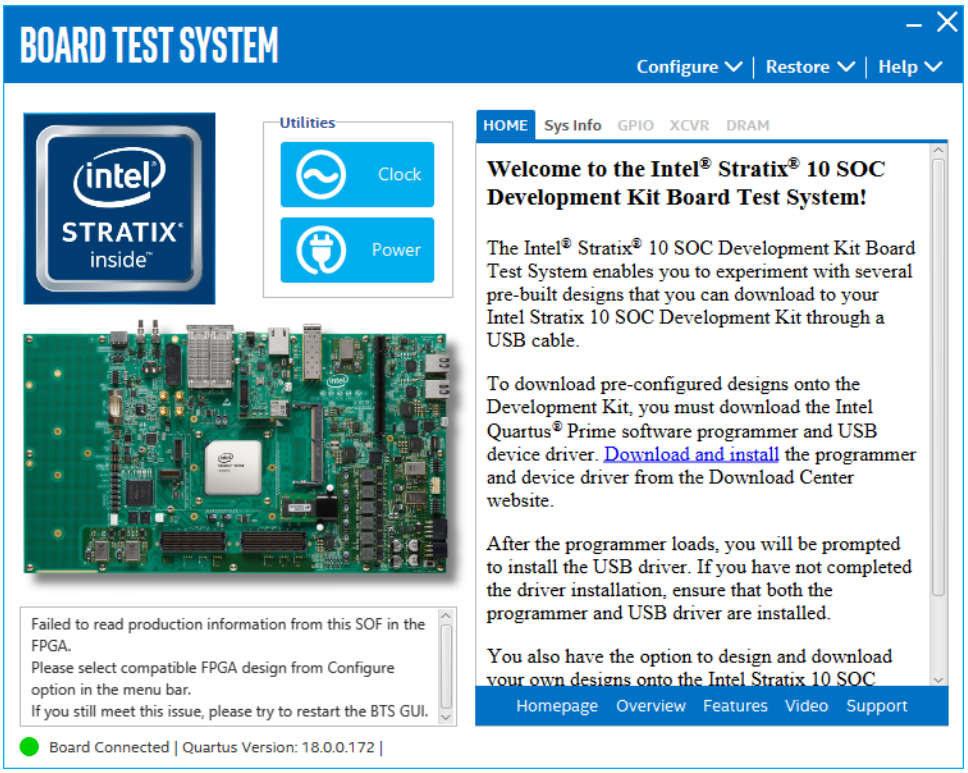
Figure 26. Power Distribution Network



5. Board Test System

This development kit includes an application called the Board Test System (BTS). The BTS is an easy-to-use interface to alter functional settings of the FPGA portion of the SoC.

Figure 27. BTS Graphical User Interface (GUI)



You can use the BTS to test board components, modify functional parameters, observe performance and measure power usage. While using the BTS, you reconfigure the FPGA several times with test designs specific to the functionality you are testing.

Several designs are provided to test the major board features. Each design provides data for one or more tabs in the application. The Configure menu identifies the appropriate design to download to the FPGA.

After successful FPGA configuration, the appropriate tab appears that allows you to exercise control over the related board features. Highlights appear in the board picture around the corresponding components.

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The BTS communicates over the JTAG bus to a test design running in the FPGA. The BTS and Power Monitor share the JTAG bus with other applications like Nios II debugger and the Signal Tap Embedded Logic Analyzer.

5.1. Preparing the Board

After successful FPGA configuration, with the power to the board off, follow these steps:

- Connect the USB cable to your PC and the Intel FPGA Download Cable II port.
- Change SW1 and SW4 to the following configuration.
- Turn on power to the board and run the Board Test System.

Note: To ensure operating stability, keep the USB cable connected and the board powered on when running the demostration application.

Table 48. SW1 GUI Mode

Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8
OFF	OFF	ON	ON	ON	ON	ON	ON

Table 49. SW4 GUI Mode

Bit 1	Bit 2	Bit 3	Bit 4
ON	OFF	ON	ON

5.2. Running the BTS

To run the BTS, navigate to the `<Package Root Dir>\examples\board_test_system` directory and run the `BoardTestSystem.exe` application.

The BTS relies on the Intel Quartus Prime software's specific library. Before running the BTS, set the environment variable `$QUARTUS_ROOTDIR` to the correct directory on your manually or open the Intel Quartus Prime software to automatically set the environment variable. The BTS uses this environment variable to locate the Intel Quartus Prime library.

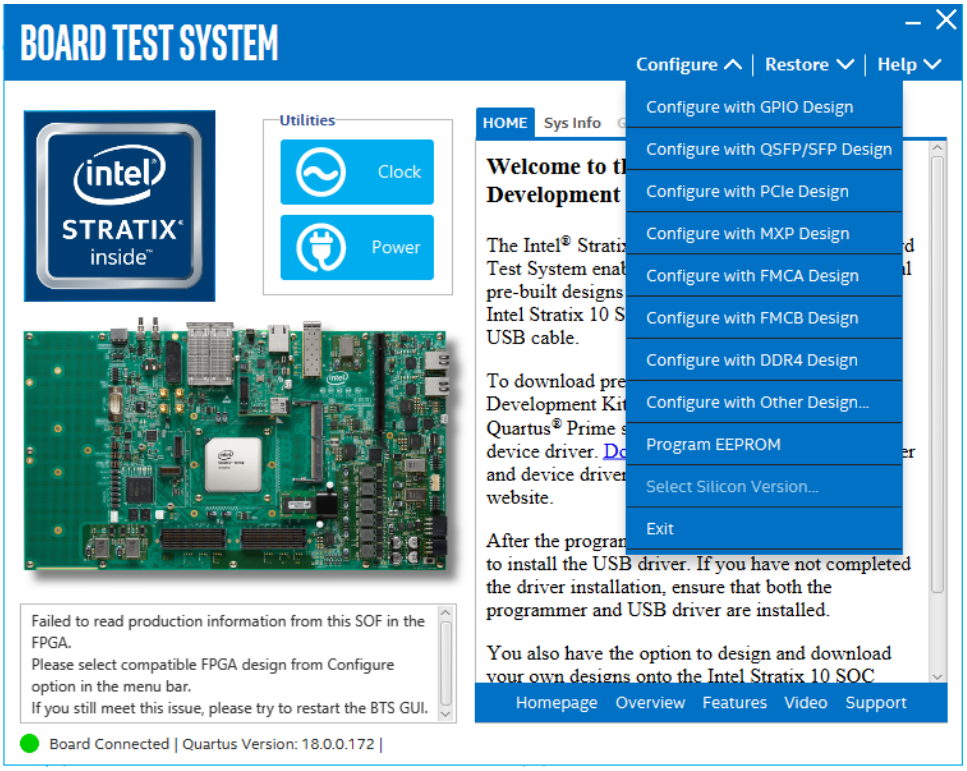
5.3. Using the BTS

This section describes each control in the BTS.

5.3.1. The Configure Menu

Use Configure Menu to select the design you want to use. Each design example tests different board features. Select a design from this menu and the corresponding tabs become active for testing.

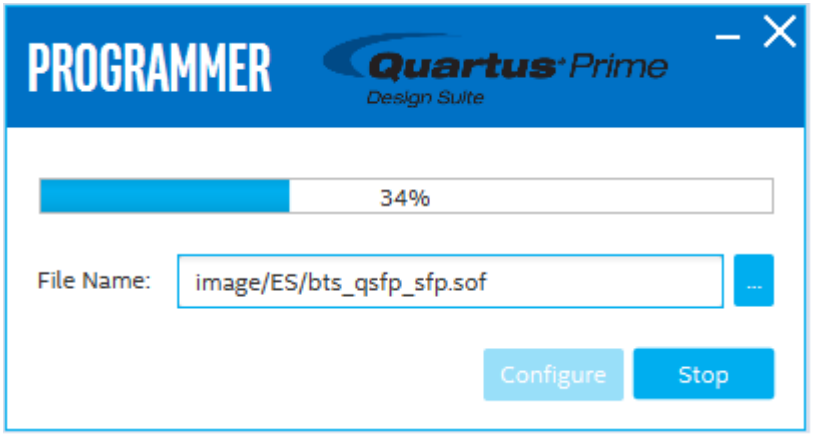
Figure 28. The Configure Menu



To configure the FPGA with a test system design, perform the following steps:

- On the Configure menu, click the configure command that corresponds to the functionality you wish to test.
- In the dialog box that appears, click Configure to download the corresponding design to the FPGA.

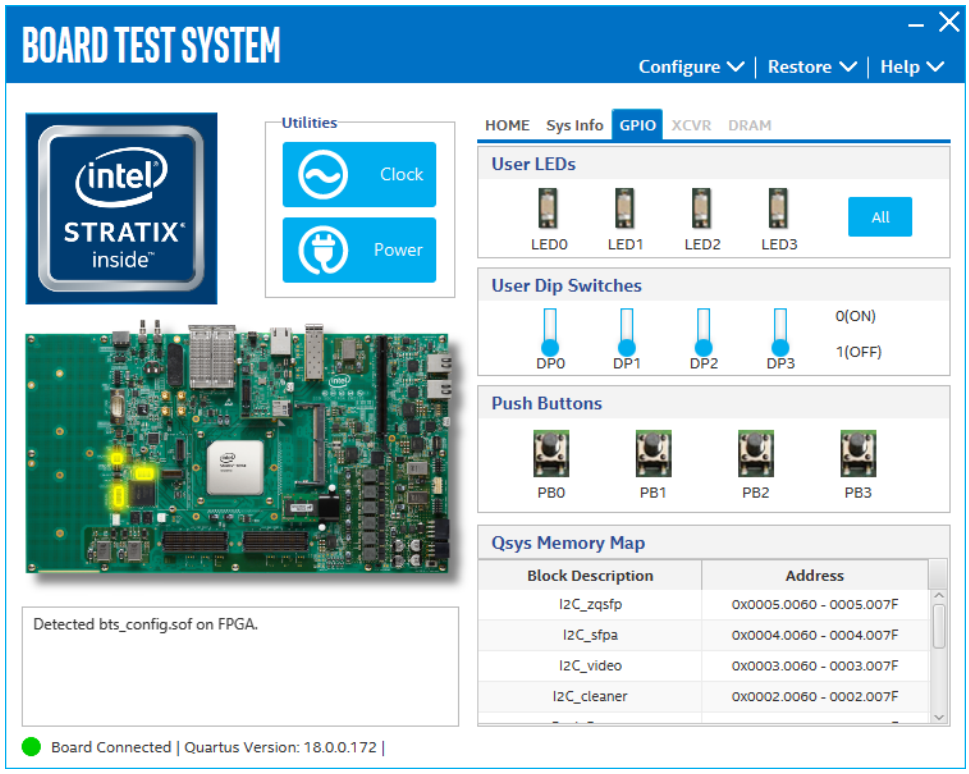
Figure 29. Programmer Dialog Window



5.3.2. The GPIO Tab

The GPIO tab allows you to interact with all the general purpose user I/O components on the board. You can read DIP switch settings, turn LEDs on/off and detect presses of push buttons.

Figure 30. The GPIO Tab



The following sections describe the controls on the GPIO tab.

User DIP Switches

The read-only User DIP Switches control displays the current positions of the switches in the user DIP switch bank (SW1). Change the switches on the board to see the graphical display change.

User LEDs

The User LEDs control displays the current state of the User LEDs. Toggle the LED buttons to turn the board LEDs on or off.

Push Buttons

Read-only control displays the current state of the board user push buttons. Press a push button on the board to view the graphical display change accordingly.

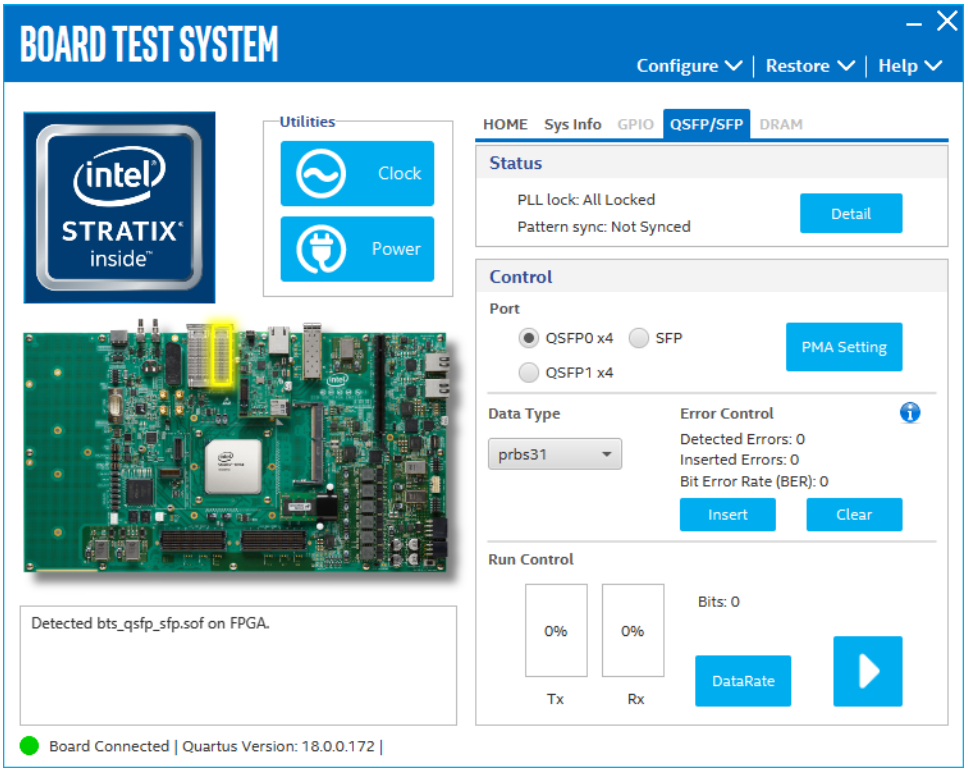
Qsys Memory Map

The Qsys memory map control shows the memory map of the `bts_config.sof` design running on your board. The memory map is visible only when `bts_config.sof` design is running on the board.

5.3.3. The QSFP/SFP Tab

This tab allows you to perform loopback tests on the QSFP and SFP ports.

Figure 31. The QSFP/SFP Tab



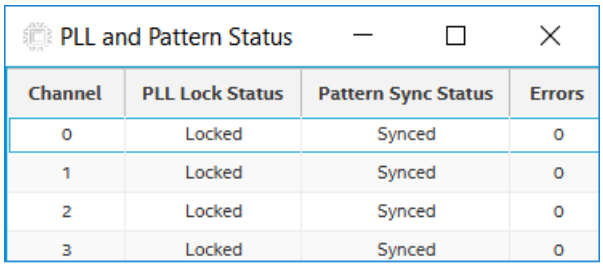
The controls on this tab are described below.

Status

Displays the following status information during a loopback test:

- PLL Lock: Shows the PLL locked or unlocked state.
- Pattern Sync: Shows the pattern synced or not synced state. The pattern is considered synced when the start of the data sequence is detected.
- Details: Shows the PLL lock and pattern status.

Figure 32. PLL and Pattern Status



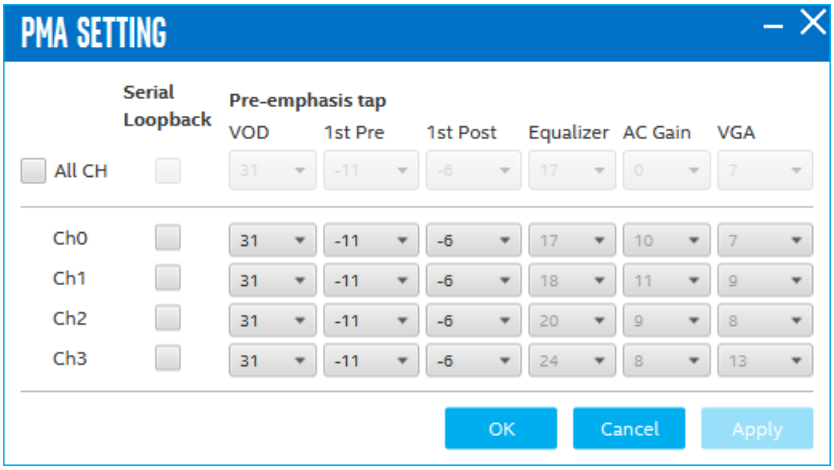
Channel	PLL Lock Status	Pattern Sync Status	Errors
0	Locked	Synced	0
1	Locked	Synced	0
2	Locked	Synced	0
3	Locked	Synced	0

Port

Allows you to specify which interface to test. The following port tests are available:

- QSFP0 x4
- QSFP1 x4
- SFP x1

PMA Setting



Allows you to make chnages to the PMA parameters that affect the active transceiver interface. The following settings are available for analysis.

Serial Loopback: Routes signals between the transmitter and the receiver.

VOD: Specifies the voltage output differential of the transmitter buffer.

Pre-emphasis tap

- 1st pre: Specifies the amount of pre-emphasis on the first pre-tap of the transmitter buffer.
- 1st post: Specifies the amount of pre-emphasis on the first post-tap of the transmitter buffer.

Equalizer: Specifies the CLTE EQ Gain for the receiver.

AC Gain: Specifies the CLTE AC Gain for the receiver.

VGA: Specifies the VGA Gain for the receiver.

Data Type

Specifies the type of data contained in the transactions. The following data types are available for analysis.

- PRBS 7: Selects pseudo-random 7-bit sequences
- PRBS 15: Selects pseudo-random 15-bit sequences
- PRBS 23: Selects pseudo-random 23-bit sequences
- PRBS 31: Selects pseudo-random 31-bit sequences
- HF: Selects highest frequency divide-by-2 data pattern `10101010`
- LF: Selects lowest frequency divide-by-33 data pattern

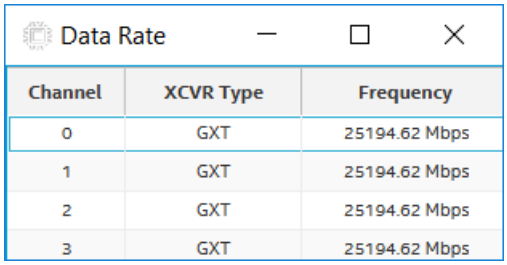
Error Control

Displays data errors detected during analysis and allows you to insert errors

- Detected Errors: Displays the number of data errors detected in the hardware.
- Inserted Errors: Displays the number of errors inserted into the transmit data stream.
- Insert: Inserts a one-word error into the transmit data stream each time you click the button. Insert is only enabled during transaction performance analysis.
- Clear: Resets the Detected Error counter and Inserted Errors counter to zero.

Run Control

- TX and RX performance bars: Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve.
- Start: Initiates the loopback tests.
- Tx (Mbps) and Rx (Mbps): Show the number of bytes of data analyzed per second.
- Data Rate: Shows the data rate for each link.

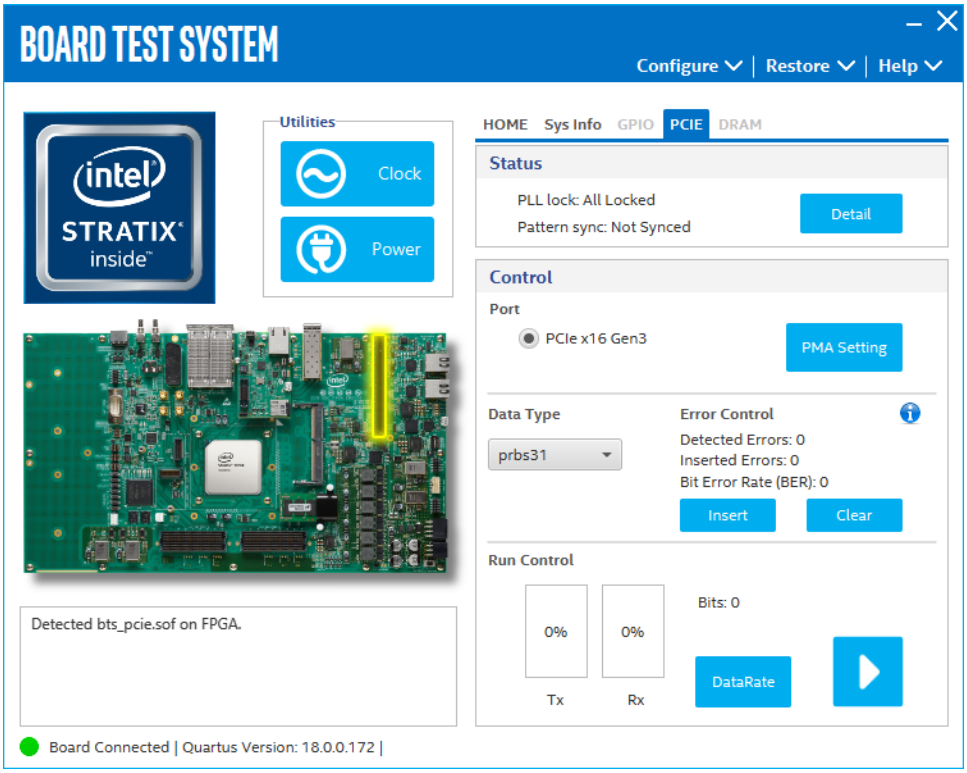


Channel	XCVR Type	Frequency
0	GXT	25194.62 Mbps
1	GXT	25194.62 Mbps
2	GXT	25194.62 Mbps
3	GXT	25194.62 Mbps

5.3.4. The PCIE Tab

The PCIE Tab allows you to perform loopback tests on the PCIE port.

Figure 33. The PCIE Tab

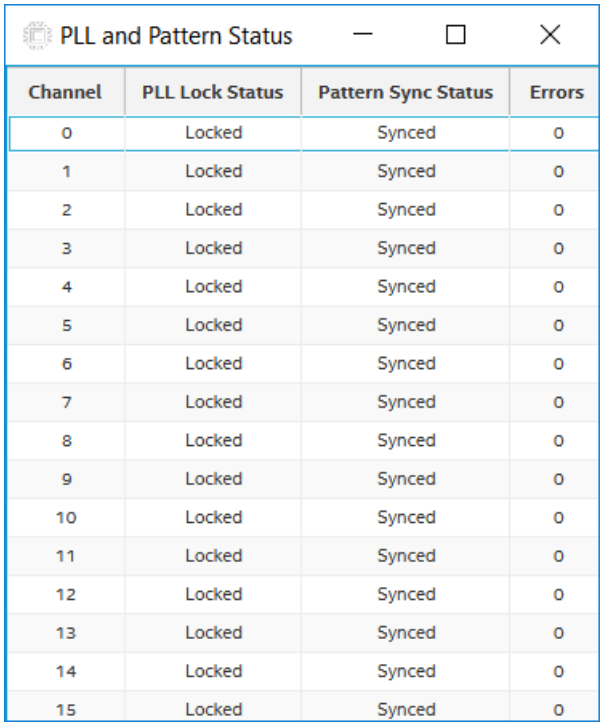


The following sections describe the controls on the PCIE tab.

Status

Displays the following status information during a loopback test:

- PLL Lock: Shows the PLL locked or unlocked state.
- Pattern Sync: Shows the pattern synced or not synced state. The pattern is considered synced when the start of the data sequence is detected.
- Details: Shows the PLL lock and pattern status.



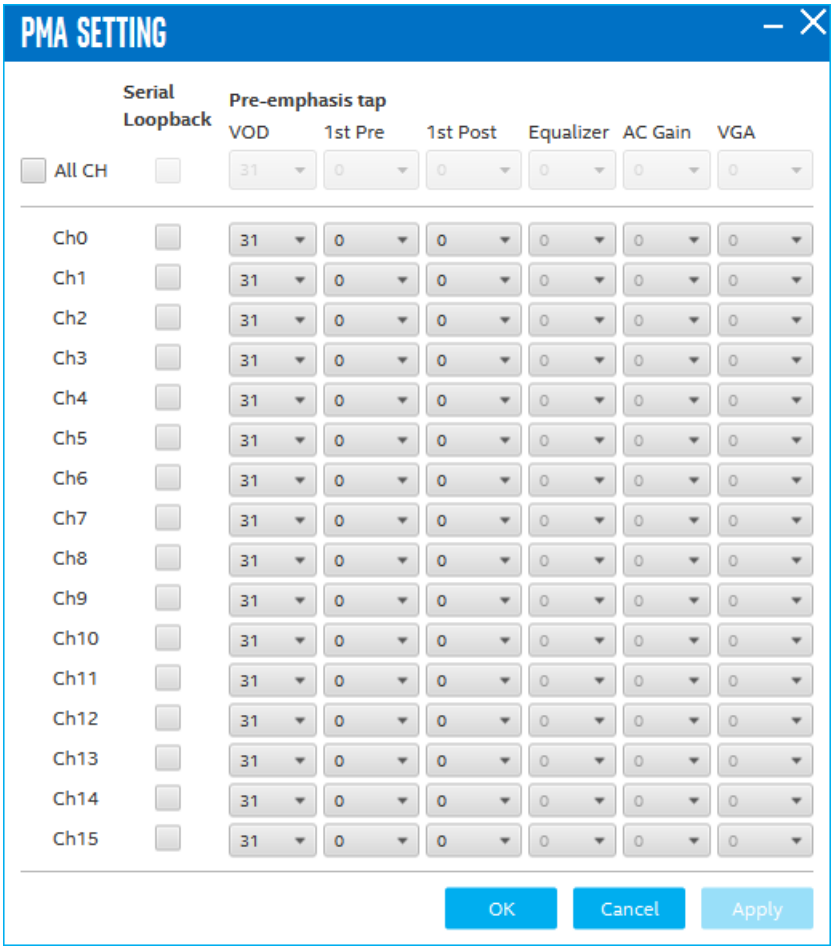
Channel	PLL Lock Status	Pattern Sync Status	Errors
0	Locked	Synced	0
1	Locked	Synced	0
2	Locked	Synced	0
3	Locked	Synced	0
4	Locked	Synced	0
5	Locked	Synced	0
6	Locked	Synced	0
7	Locked	Synced	0
8	Locked	Synced	0
9	Locked	Synced	0
10	Locked	Synced	0
11	Locked	Synced	0
12	Locked	Synced	0
13	Locked	Synced	0
14	Locked	Synced	0
15	Locked	Synced	0

Port

Allows you to specify which interface to test. The following port tests are available:

- PCIE x16

PMA Setting



Allows you to make changes to the PMA parameters that affect the active transceiver interface. The following settings are available for analysis:

- Serial Loopback: Routes signals between the transmitter and the receiver.
- VOD: Specifies the voltage output differential of the transmitter buffer.
- Pre-emphasis tap:
  - 1st pre: Specifies the amount of pre-emphasis on the pre-tap of the transmitter buffer.
  - 1st post: Specifies the amount of pre-emphasis on the first post tap of the transmitter buffer.
- Equalizer: Specifies the CLTE EQ Gain for the receiver.
- AC Gain: Specifies the CLTE AC Gain for the receiver.
- VGA: Specifies the VGA gain of the receiver.

Data Type

Specifies the type of data contained in the transactions. The following data types are available for analysis.

- PRBS 7: Selects pseudo-random 7-bit sequences.
- PRBS 15: Selects pseudo-random 15-bit sequences.
- PRBS 23: Selects pseudo-random 23-bit sequences.
- PRBS 31: Selects pseudo-random 31-bit sequences.
- HF: Selects highest frequency divide-by-2 data pattern `10101010`.
- LF: Selects lowest frequency divide-by-33 data pattern.

Error Control

Displays data errors detected during analysis and allows you to insert errors:

- Detected Errors: Displays the number of data errors detected in the hardware.
- Inserted Errors: Displays the number of errors inserted into the transmit data stream.
- Insert: Inserts a one-word error into the transmit data stream each time you click the button. Insert is enabled only during transaction performance analysis.
- Clear: Resets the Detected Errors counter and Inserted Errors counter to zero.

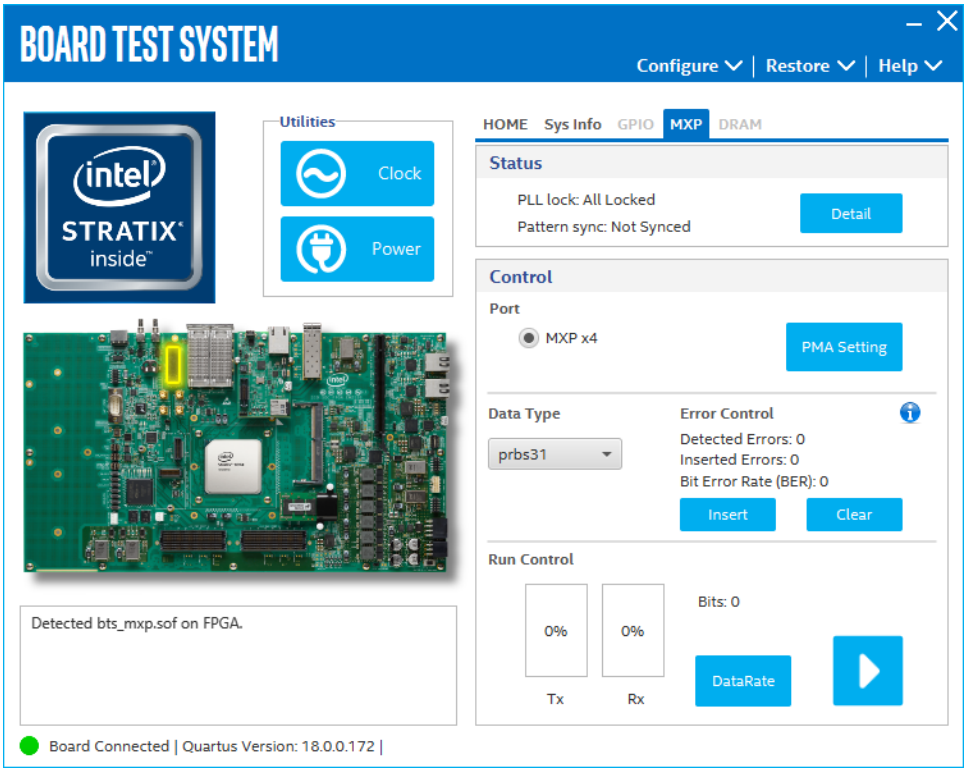
Run Control

- TX and RX performance bars: Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve.
- start: this control initates the loopback tests.
- Tx (Mbps) and Rx (Mbps): Show the number of bytes of data analyzed per second.
- Data Rate: Shows the data rate for each link.

5.3.5. The MXP Tab

The MXP tab allows you to perform loopback tests on the MXP port.

Figure 34. The MXP Tab



The following sections describe the controls on the MXP tab.

Status

Displays the following status information during a loopback test:

- PLL Lock: Shows the PLL locked or unlocked state.
- Pattern Sync: Shows the pattern synced or not synced state. The pattern is considered synced when the start of the data sequence is detected.
- Details: Shows the PLL lock and pattern status:

PLL and Pattern Status

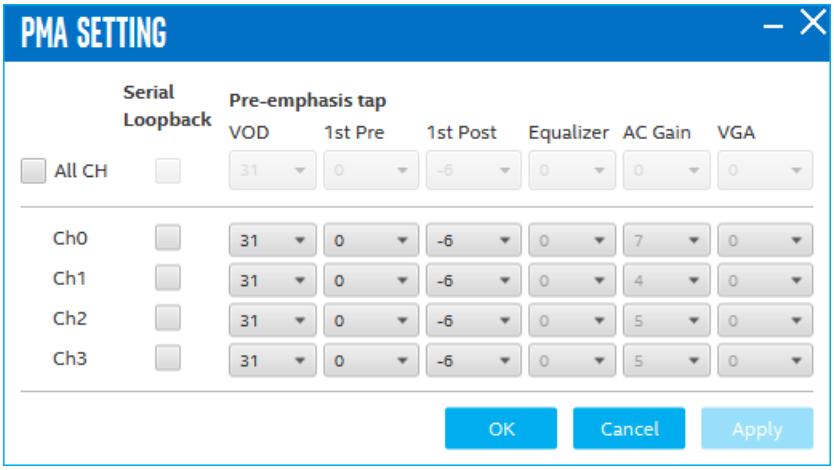
Channel	PLL Lock Status	Pattern Sync Status	Errors
0	Locked	Synced	0
1	Locked	Synced	0
2	Locked	Synced	0
3	Locked	Synced	0

Port

Allows you to specify which interface to test. The following port tests are available:

- MXP x4

PMA Setting



Allows you to make changes to the PMA paratmeters that affect the active transceiver interface. The following settings are available for analysis:

- Serial Loopback: Routes signals between the transmitter and the receiver.
- VOD: Specifies the voltage output differential of the transmitter buffer.
- Pre-emphasis tap:
  - 1st Pre: Specifies the amount of pre-emphasis on the pre-tap of the transmitter buffer.
  - 1st Post: Specifies the amount of pre-emphasis on the first post tap of the transmitter buffer.
- Equalizer: Specifies the CLTE EQ Gain for the receiver.
- AC Gain: Specifies the CLTE AC Gain for the receiver.
- VGA: Specifies the VGA gain for the receiver.

Data Type

Specifies the type of data contained in the transactions. The following data types are available for analysis.

- PRBS 7: Selects pseudo-random 7-bit sequences.
- PRBS 15: Selects pseudo-random 15-bit sequences.
- PRBS 23: Selects pseudo-random 23-bit sequences.
- PRBS 31: Selects pseudo-random 31-bit sequences.
- HF: Selects highest frequency divide-by-2 data pattern `10101010`.
- LF: Selects lowest frequency divide-by-33 data pattern.

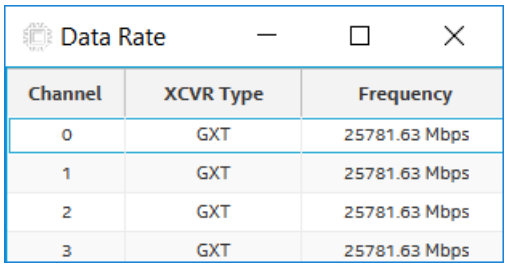
Error Control

Displays data errors detected during analysis and allows you to insert errors:

- Detected Errors: Displays the number of data errors detected in the hardware.
- Inserted Errors: Displays the number of errors inserted into the transmit data stream.
- Insert: Inserts a one-word error into the transmit data stream each time you click the button. Insert is enabled only during transaction performance analysis.
- Clear: Resets the Detected Errors counter and Inserted Errors counter to zero.

Run Control

- TX and RX performance bars: Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve.
- Start: this control initates the loopback tests.
- Tx (Mbps) and Rx (Mbps): Show the number of bytes of data analyzed per second.
- Data Rate: Shows the data rate for each link.

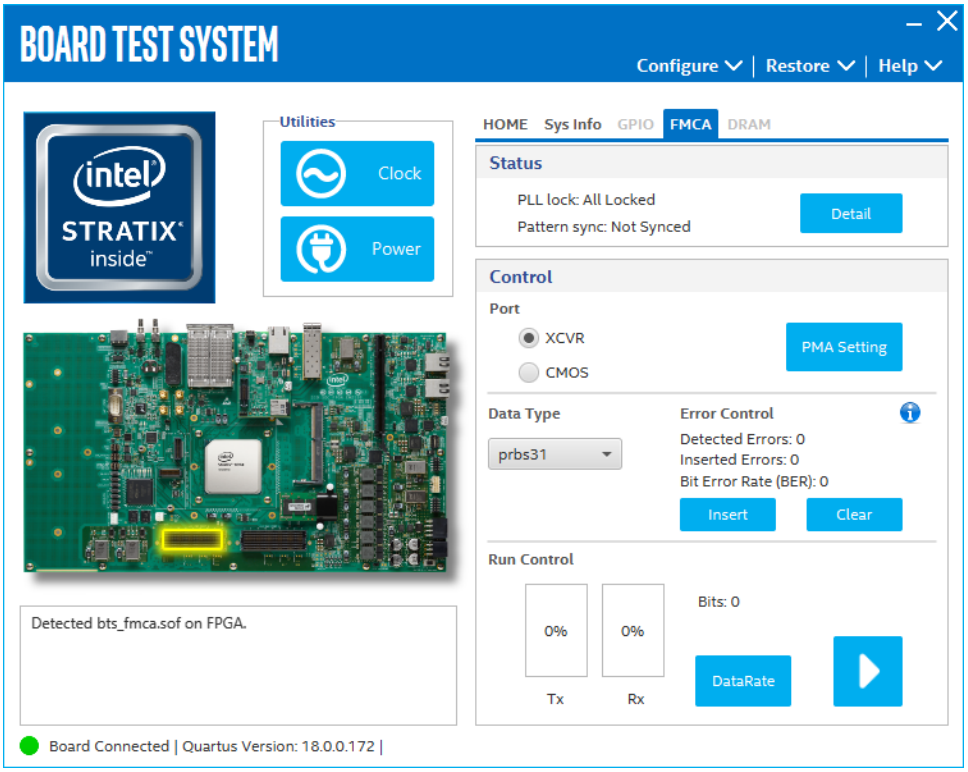


Channel	XCVR Type	Frequency
0	GXT	25781.63 Mbps
1	GXT	25781.63 Mbps
2	GXT	25781.63 Mbps
3	GXT	25781.63 Mbps

5.3.6. The FMCA Tab

The FMCA tab allows you to perform loopback tests on the FMCA port.

Figure 35. The FMCA Tab



The following sections describe the controls on the FMCA tab.

Status

Displays the following status information during a loopback test:

- PLL Lock: Shows the PLL locked or unlocked state.
- Pattern Sync: Shows the pattern synced or not synced state. The pattern is considered synced when the start of the data sequence is detected.
- Details: Shows the PLL lock and pattern status:

PLL and Pattern Status

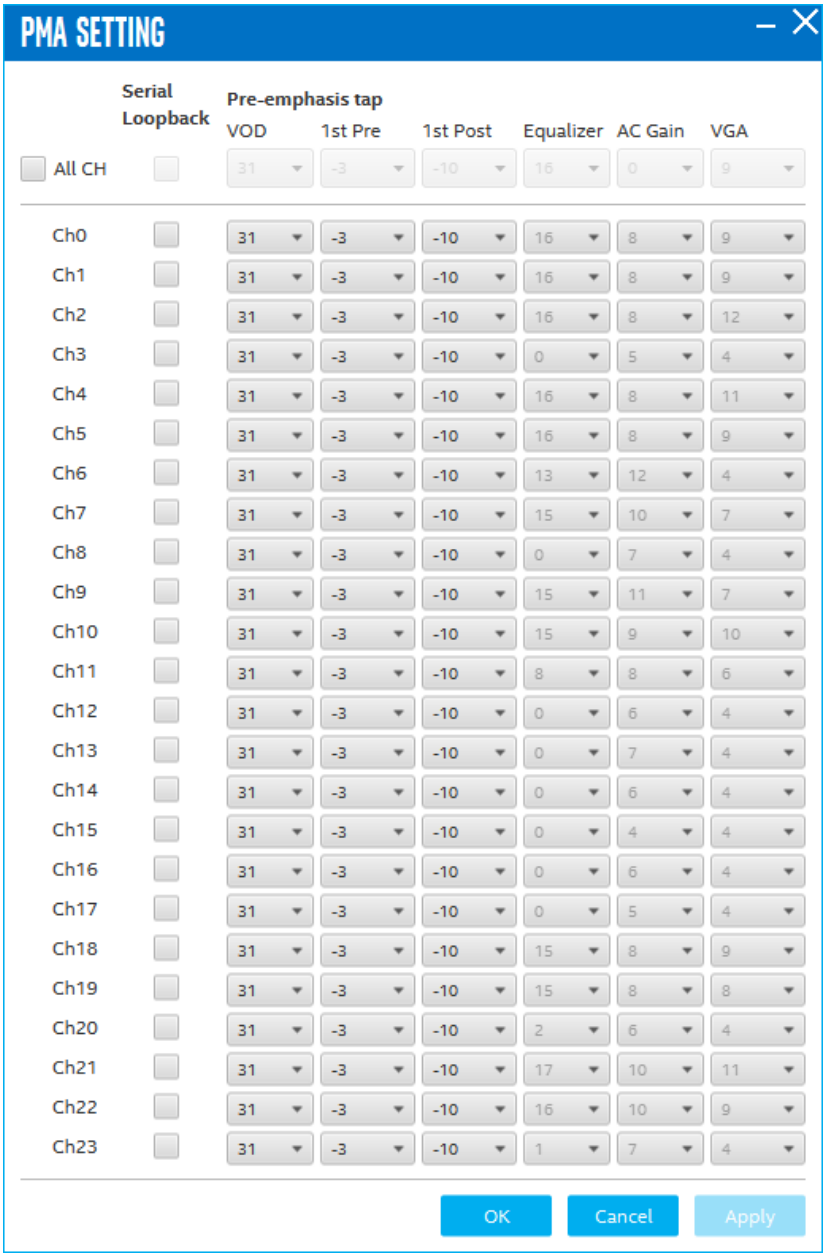
Channel	PLL Lock Status	Pattern Sync Status	Errors
0	Locked	Synced	0
1	Locked	Synced	0
2	Locked	Synced	0
3	Locked	Synced	0
4	Locked	Synced	0
5	Locked	Synced	0
6	Locked	Synced	0
7	Locked	Synced	0
8	Locked	Synced	0
9	Locked	Synced	0
10	Locked	Synced	0
11	Locked	Synced	0
12	Locked	Synced	0
13	Locked	Synced	0
14	Locked	Synced	0
15	Locked	Synced	0
16	Locked	Synced	0
17	Locked	Synced	0
18	Locked	Synced	0
19	Locked	Synced	0
20	Locked	Synced	0
21	Locked	Synced	0
22	Locked	Synced	0
23	Locked	Synced	0

Port

Allows you to specify which interface to test. The following port tests are available:

- XCVR
- CMOS

PMA Setting



Allows you to make changes to the PMA parameters that affect the active transceiver interface. The following settings are available for analysis:

- Serial Loopback: Routes signals between the transmitter and the receiver.
- VOD: Specifies the voltage output differential of the transmitter buffer.
- Pre-emphasis tap:
  - 1st Pre: Specifies the amount of pre-emphasis on the pre-tap of the transmitter buffer.
  - 1st Post: Specifies the amount of pre-emphasis on the first post tap of the transmitter buffer.
- Equalizer: Specifies the CLTE EQ Gain for the receiver.
- AC Gain: Specifies the CLTE AC Gain for the receiver.
- VGA: Specifies the VGA gain for the receiver.

Data Type

Specifies the type of data contained in the transactions. The following data types are available for analysis.

- PRBS 7: Selects pseudo-random 7-bit sequences.
- PRBS 15: Selects pseudo-random 15-bit sequences.
- PRBS 23: Selects pseudo-random 23-bit sequences.
- PRBS 31: Selects pseudo-random 31-bit sequences.
- HF: Selects highest frequency divide-by-2 data pattern `10101010`.
- LF: Selects lowest frequency divide-by-33 data pattern.

Error Control

Displays data errors detected during analysis and allows you to insert errors:

- Detected Errors: Displays the number of data errors detected in the hardware.
- Inserted Errors: Displays the number of errors inserted into the transmit data stream.
- Insert: Inserts a one-word error into the transmit data stream each time you click the button. Insert is enabled only during transaction performance analysis.
- Clear: Resets the Detected Errors counter and Inserted Errors counter to zero.

Run Control

- TX and RX performance bars: Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve.
- Start: this control initates the loopback tests.
- Tx (Mbps) and Rx (Mbps): Show the number of bytes of data analyzed per second.
- Data Rate: Shows the data rate for each link.

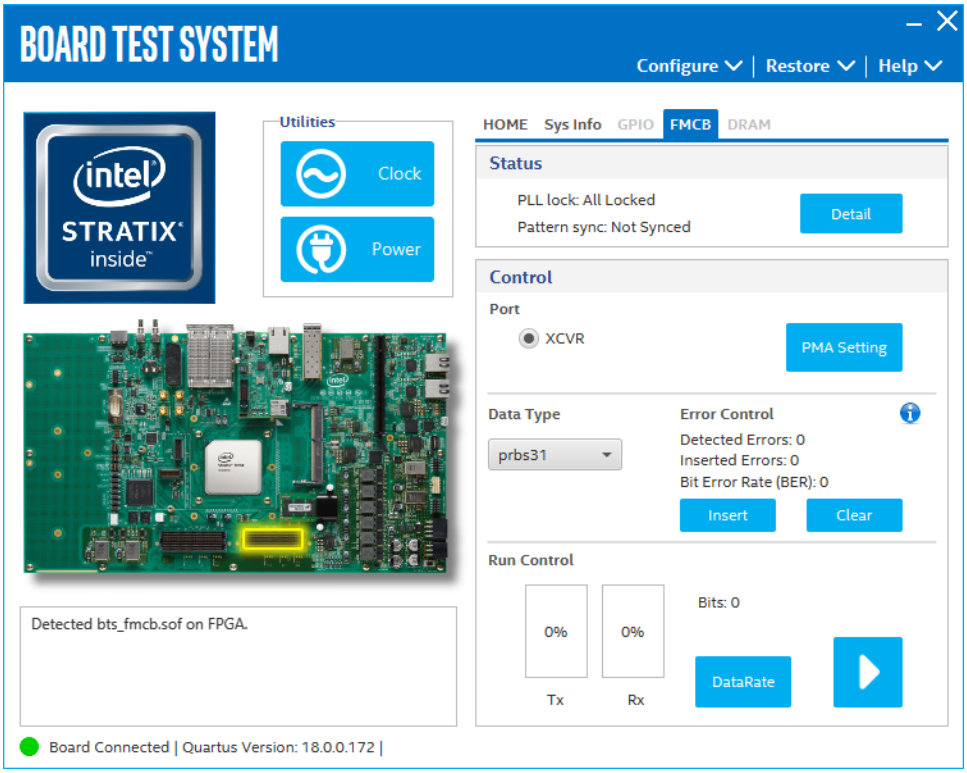
Data Rate

Channel	XCVR Type	Frequency
0	GX	17080.06 Mbps
1	GX	17080.19 Mbps
2	GX	17080.06 Mbps
3	GX	17080.19 Mbps
4	GX	17080.06 Mbps
5	GX	17080.19 Mbps
6	GXT	25624.96 Mbps
7	GXT	25624.96 Mbps
8	GX	12246.02 Mbps
9	GXT	25625.09 Mbps
10	GXT	25624.96 Mbps
11	GX	12246.14 Mbps
12	GX	17080.06 Mbps
13	GX	17080.19 Mbps
14	GX	17080.06 Mbps
15	GX	17080.06 Mbps
16	GX	17080.06 Mbps
17	GX	17080.06 Mbps
18	GXT	25624.96 Mbps
19	GXT	25625.09 Mbps
20	GX	12246.02 Mbps
21	GXT	25624.96 Mbps
22	GXT	25624.96 Mbps
23	GX	12246.14 Mbps

5.3.7. The FMCB Tab

The FMCB tab allows you to perform loopback tests on the FMCB port.

Figure 36. The FMCB Tab



The following sections describe the controls on the FMCB tab.

Status

Displays the following status information during a loopback test:

- PLL Lock: Shows the PLL locked or unlocked state.
- Pattern Sync: Shows the pattern synced or not synced state. The pattern is considered synced when the start of the data sequence is detected.
- Details: Shows the PLL lock and pattern status:

PLL and Pattern Status

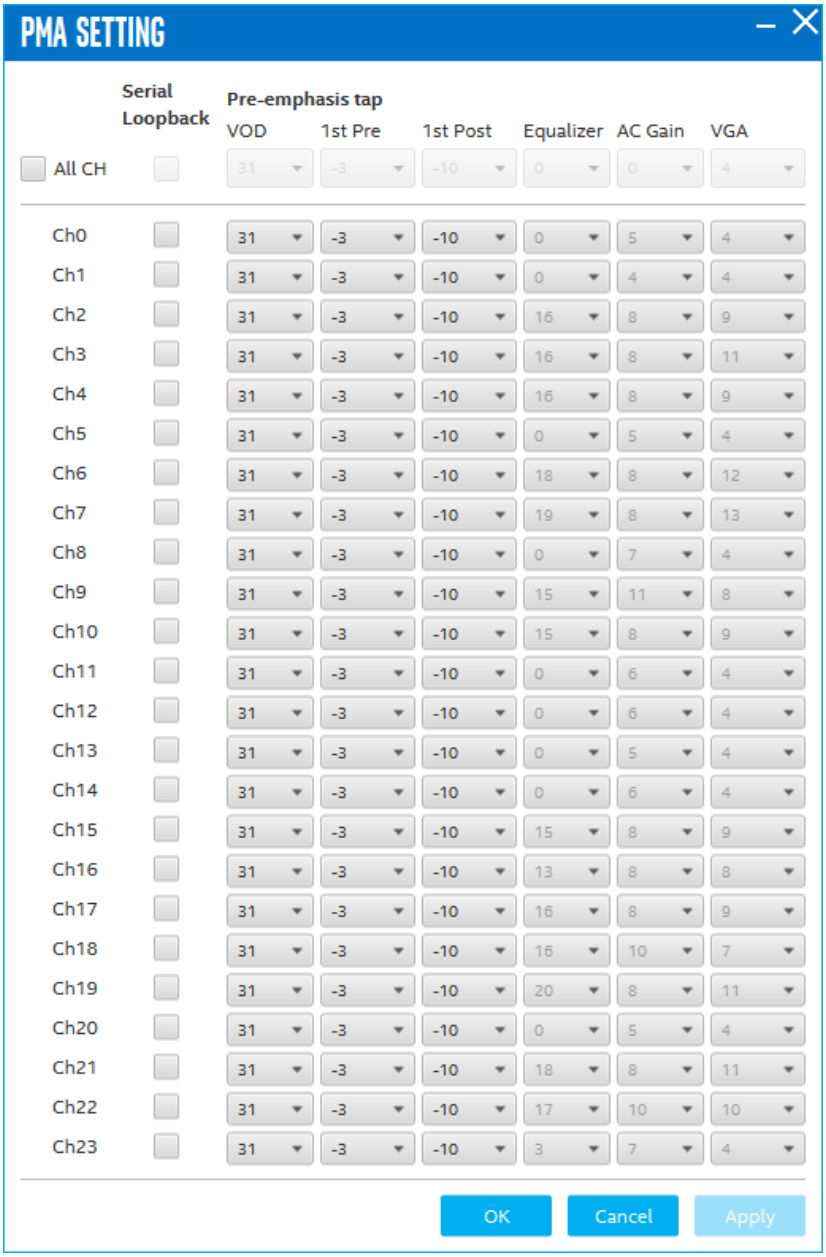
Channel	PLL Lock Status	Pattern Sync Status	Errors
0	Locked	Synced	0
1	Locked	Synced	0
2	Locked	Synced	0
3	Locked	Synced	0
4	Locked	Synced	0
5	Locked	Synced	0
6	Locked	Synced	0
7	Locked	Synced	0
8	Locked	Synced	0
9	Locked	Synced	0
10	Locked	Synced	0
11	Locked	Synced	0
12	Locked	Synced	0
13	Locked	Synced	0
14	Locked	Synced	0
15	Locked	Synced	0
16	Locked	Synced	0
17	Locked	Synced	0
18	Locked	Synced	0
19	Locked	Synced	0
20	Locked	Synced	0
21	Locked	Synced	0
22	Locked	Synced	0
23	Locked	Synced	0

Port

Allows you to specify which interface to test. The following port tests are available:

- XCVR
- CMOS

PMA Setting



Allows you to make changes to the PMA paratmeters that affect the active transceiver interface. The following settings are available for analysis:

- Serial Loopback: Routes signals between the transmitter and the receiver.
- VOD: Specifies the voltage output differential of the transmitter buffer.
- Pre-emphasis tap:
  - 1st Pre: Specifies the amount of pre-emphasis on the pre-tap of the transmitter buffer.
  - 1st Post: Specifies the amount of pre-emphasis on the first post tap of the transmitter buffer.
- Equalizer: Specifies the CLTE EQ Gain for the receiver.
- AC Gain: Specifies the CLTE AC Gain for the receiver.
- VGA: Specifies the VGA gain for the receiver.

Data Type

Specifies the type of data contained in the transactions. The following data types are available for analysis.

- PRBS 7: Selects pseudo-random 7-bit sequences.
- PRBS 15: Selects pseudo-random 15-bit sequences.
- PRBS 23: Selects pseudo-random 23-bit sequences.
- PRBS 31: Selects pseudo-random 31-bit sequences.
- HF: Selects highest frequency divide-by-2 data pattern `10101010`.
- LF: Selects lowest frequency divide-by-33 data pattern.

Error Control

Displays data errors detected during analysis and allows you to insert errors:

- Detected Errors: Displays the number of data errors detected in the hardware.
- Inserted Errors: Displays the number of errors inserted into the transmit data stream.
- Insert: Inserts a one-word error into the transmit data stream each time you click the button. Insert is enabled only during transaction performance analysis.
- Clear: Resets the Detected Errors counter and Inserted Errors counter to zero.

Run Control

- TX and RX performance bars: Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve.
- Start: this control initates the loopback tests.
- Tx (Mbps) and Rx (Mbps): Show the number of bytes of data analyzed per second.
- Data Rate: Shows the data rate for each link.

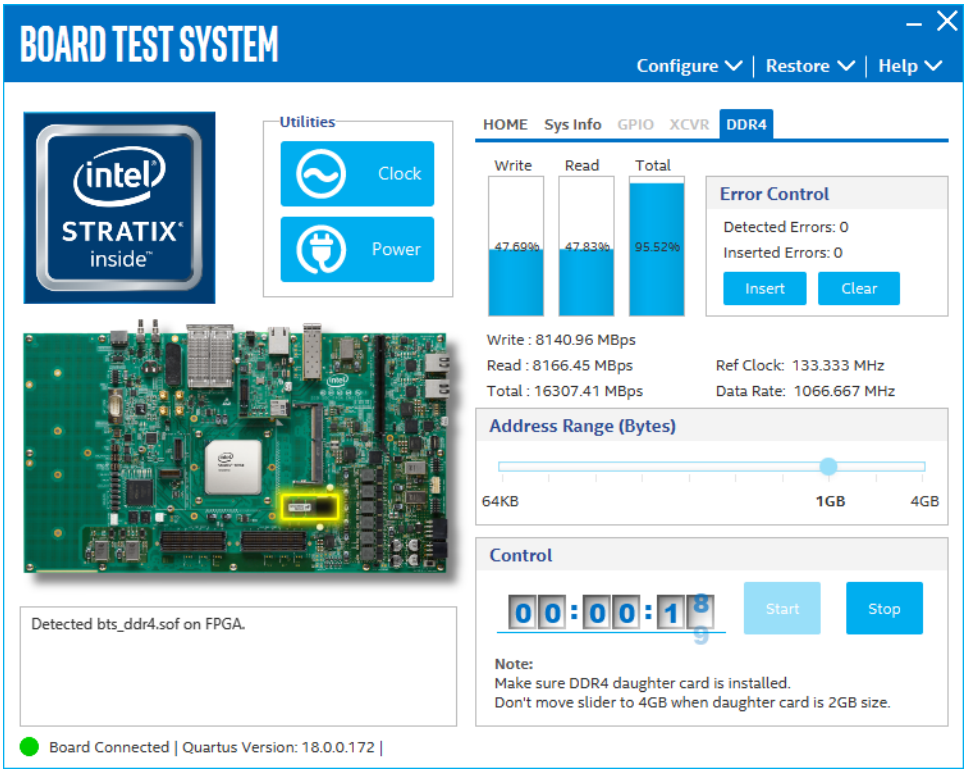
Data Rate

Channel	XCVR Type	Frequency
0	GX	17080.06 Mbps
1	GX	17080.06 Mbps
2	GX	17080.06 Mbps
3	GX	17080.06 Mbps
4	GX	17080.06 Mbps
5	GX	17080.06 Mbps
6	GXT	25624.96 Mbps
7	GXT	25624.96 Mbps
8	GX	12246.14 Mbps
9	GXT	25624.96 Mbps
10	GXT	25624.96 Mbps
11	GX	12246.14 Mbps
12	GX	17080.06 Mbps
13	GX	17080.06 Mbps
14	GX	17080.06 Mbps
15	GX	17080.19 Mbps
16	GX	17080.06 Mbps
17	GX	17080.06 Mbps
18	GXT	25624.96 Mbps
19	GXT	25624.96 Mbps
20	GX	12246.02 Mbps
21	GXT	25624.96 Mbps
22	GXT	25624.96 Mbps
23	GX	12246.14 Mbps

5.3.8. The DDR4 Tab

This tab allows you to read and write DDR4 memory on the board.

Figure 37. The DDR4 Tab



The controls on this tab are described below.

Start

Initiates DDR4 memory transaction performance analysis

Stop

Terminates transaction performance analysis

Performance Indicators

These controls display current transaction performance analysis information collected since you last clicked **Start**:

- Write, Read and Total performance bars: Show the percentage of maximum theoretical data rate that requested transactions are able to achieve.
- Write, Read and Total (MBps): Show the number of bytes analyzed per second.
- Data Bus: 72 bits (8 bits ECC) wide and frequency is 1066 MHz double data rate. 2133 Mbps per pin.

Error Control

Displays data errors detected during analysis and allows you to insert errors

- Detected errors: Displays the number of data errors detected in the hardware.
- Inserted errors: Displays the number of errors inserted into the transmit data stream.
- Insert Error: Inserts a one-word error into the transmit data stream each time you click the button. Insert Error is only enabled during transaction performance analysis.
- Clear: Resets the Detected Errors counter and Inserted Errors counter to zero.

Address Range

Determines the number of addresses to use in each iteration of reads and writes

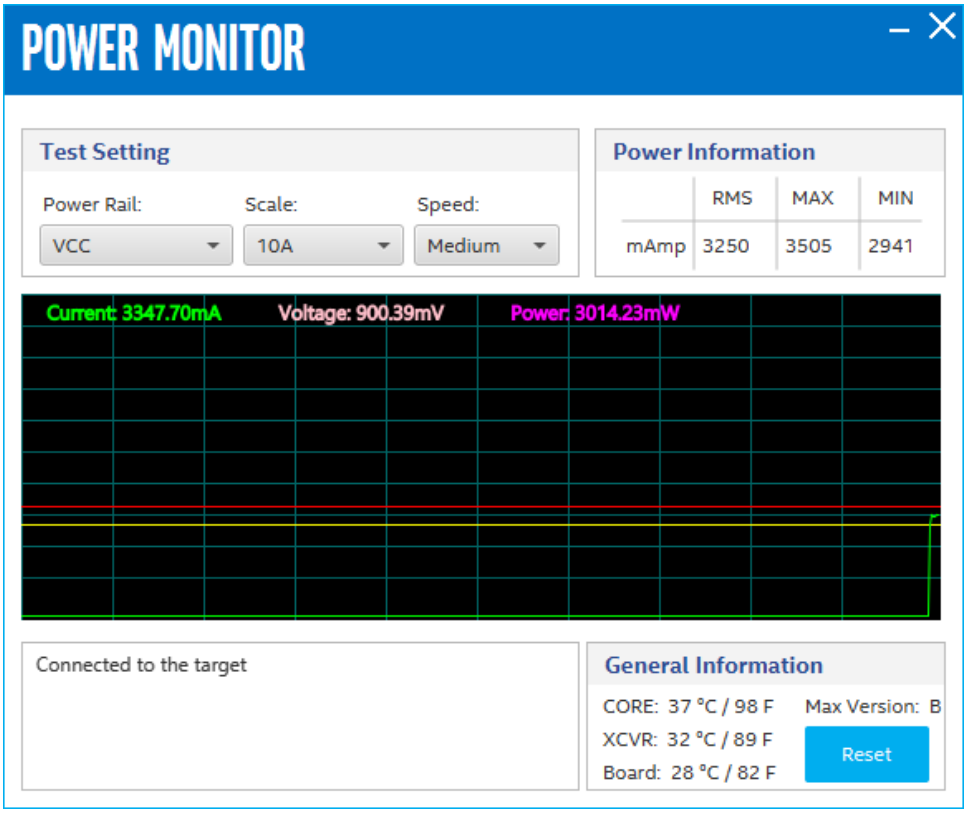
5.3.9. Power Monitor

The Power Monitor measures and reports current power information and communicates with the Intel MAX 10 device on the board through the JTAG bus. A power monitor circuit attached to the Intel MAX 10 device allows you to measure the power that the FPGA is consuming.

To start the application, click the **Power Monitor** icon in the BTS. You can also run the Power Monitor as a stand-alone application. The `PowerMonitor.exe` resides in the `<packagedir>\examples\board_test_system` directory.

Note: You cannot run the stand-alone power application and the BTS simultaneously. Also, you cannot run power and clock interface at the same time.

Figure 38. Power Monitor



The controls on the Power Monitor are described below.

Test Settings

Displays the following controls:

- Power Rails: Indicates the currently selected power rail. After selecting the desired rail, click **Reset** to refresh the screen with updated board readings.
- Scale: Specifies the amount to scale the power graph. Select a smaller number to zoom-in to see finer detail. Select a larger number to zoom-out to view the entire range of recorded values.
- Speed: Specifies how often to refresh the power graph.

Power Information

Displays the root mean square (RMS) current, maximum and minimum numerical power readings in mA.

Graph

Displays the mA power consumption of your board over time. The green line indicates the current value. The red line indicates the maximum value read since the last reset. The yellow line indicates the minimum value read since the last reset.

General Information

Displays the MAX V version and current temperature of the FPGA and the board.

Reset

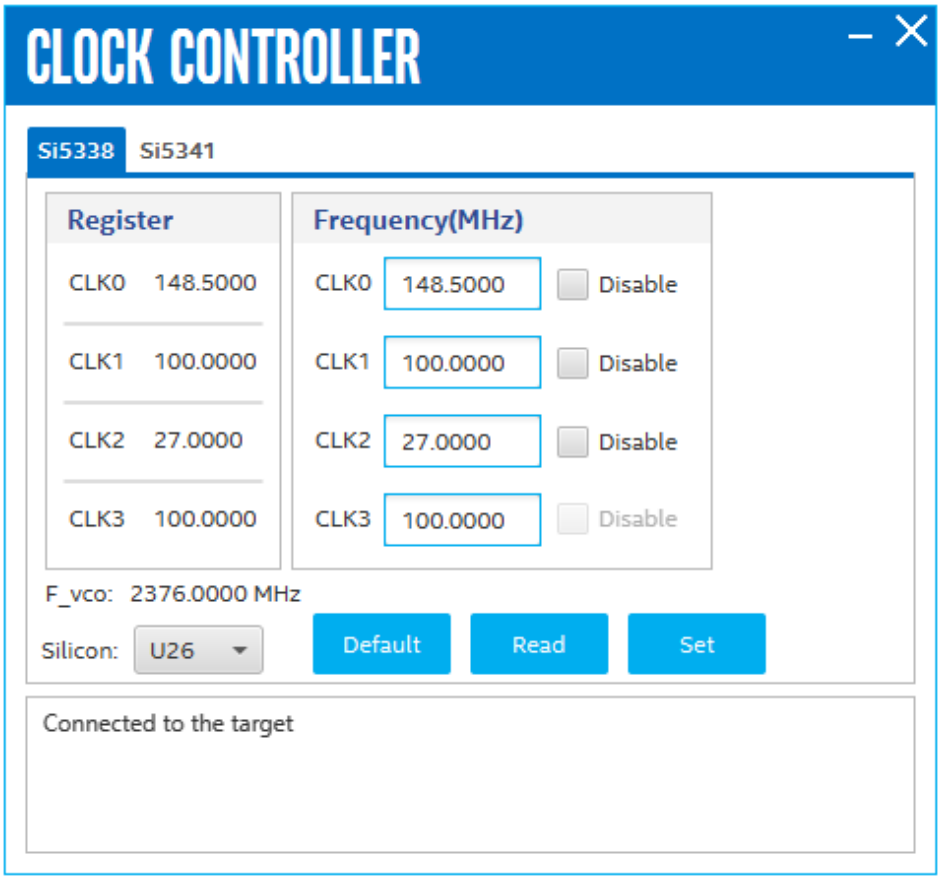
Clears the graph, resets the minimum and maximum values and restarts the Power Monitor.

5.3.10. The Clock Control

The Clock Control application sets the three programmable oscillators to any frequency between 10 MHz and 810 MHz. The frequencies support eight digits of precision to the right of the decimal point.

The Clock Control communicates with the Intel MAX 10 device on the board through the JTAG bus. The programmable oscillators are connected to the Intel MAX 10 device through a 2-wire serial bus.

Figure 39. Clock Control



The **Si5338** tab and **Si5341** tab displays the same GUI controls for each clock generators. Each tab allows for separate control. The **Si5338** is capable of synthesizing four independent user-programmble clock frequencies up t0 350 MHz and select frequencies up to 710 MHz.

F_vco

Displays the generating signal value of the voltage-controlled oscillator.

Registers

Display the current frequency of the clock.

Frequency (MHz)

Allows you to specify the frequency of the clock.

Default

Sets the frequency for the oscillator associated with the active tab back to its default value. The default is restored by power cycling the board.

Read

Reads the current frequency setting for the oscillator associated with the active tab.

Set

Sets the programmable oscillator frequency for the selected clock to the value in the CLK0 to CLK3 controls for each Si5338. Frequency changes might take several milliseconds to take effect. You might see glitches on the clock during this time. Intel recommends resetting the FPGA logic after changing frequencies.

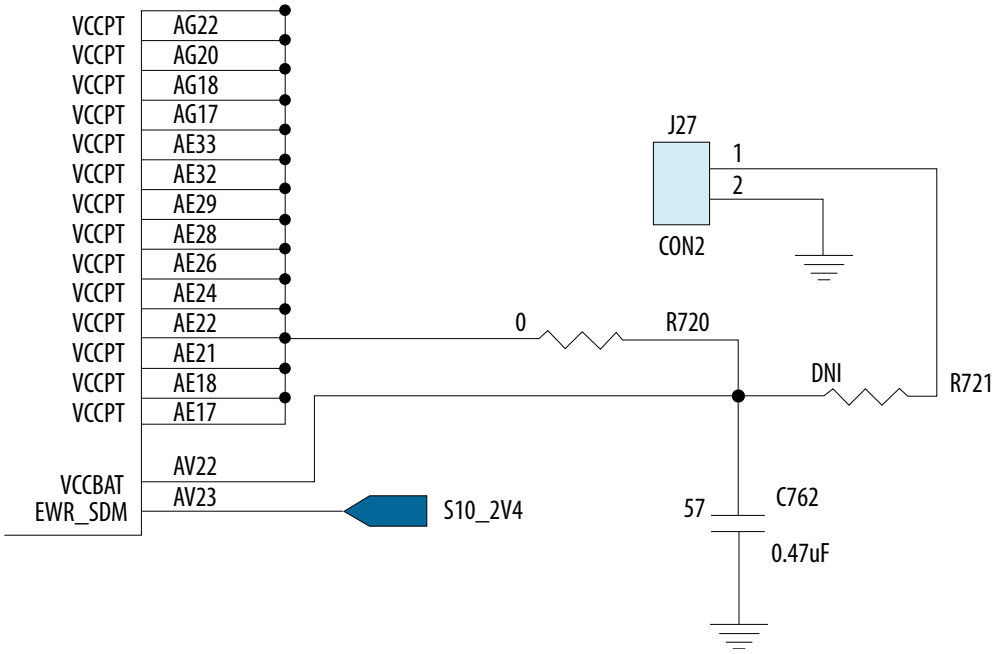
A. Additional Information

A.1. Modify the Intel Stratix 10 SX SoC Development Kit to use a battery for the BBRAM

The Intel Stratix 10 device contains a Battery Backed-up RAM (BBRAM) that is used by the Secure Device Manager. The BBRAM is powered by a special pin on the FPGA named VCCBAT. On the Intel Stratix 10 SX SoC Development Kit, this pin is connected to the main power, and the contents of the BBRAM are lost when the board is powered down. This section describes how to modify the board to accommodate a battery so the BBRAM contents can be preserved when the board loses power.

The modification to the board involves moving a zero-ohm surface mount resistor from one location to another, and then adding a suitable battery power source to a header.

The following schematic diagram shows the default board layout.



By default, the VCCBAT pin is powered by the VCCPT power rail through the zero ohm resistor R720. Removing R720 and inserting it in the unpopulated R721 position will cause the power for VCCBAT to come from J27, which is a simple 2 pin 0.1” spaced header. Power can be provided to J27 using a battery with a voltage of 1.2 – 1.8 volts.

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A.2. Modify the Intel Stratix 10 SX SoC Development Kit HPS DDR4 memory width and ECC configuration using the Golden Hardware Reference Design project

The supported HPS DDR4 configurations are:

- 72 bits : 64 bit data + 8 bit ECC
- 64 bits : 64 bit data
- 40 bits : 32 bit data + 8 bit ECC
- 32 bits : 32 bit data
- 24 bits : 16 bit data + 8 bit ECC
- 16 bits : 16 bit data

The Golden Hardware Reference Design (GHRD) project has an HPS DDR4 interface configuration with a width of 72 bits.

Flow to modify the HPS DDR4 memory width and ECC Configuration

1. Open the `qsys_top.qsys` file. Select the `emif_hps` component and open the **Parameter Editor**. Change the **Memory tab > DQ width** as required. If ECC isn't required, unselect the **Controller** tab parameters **Enable Error Detection and Correction Logic with ECC** and **Enable Auto Error Correction to External Memory**. Generate the qsys component.
2. Open the top level RTL file `ghrd_s10_top.v`. At the top, change the inout wire bus width declarations for `emif_hps_mem_mem_dbi_n`, `emif_hps_mem_mem_dq`, `emif_hps_mem_mem_dqs` and `emif_hps_mem_mem_dqs_n` for your required DDR4 configuration.
3. In the **Quartus Assignment Editor** or in the project **.qsf** file, make these changes:
   - For the required DDR4 interface width, disable all the location assignments of the unused `mem_dbi_n`, `mem_dqs`, `mem_dqs_n` and `mem_dq` signals.
   - For narrower width interfaces with ECC, in order to meet the pinout rules in the *Intel Stratix 10 SoC Design Guidelines* and the *Intel Stratix 10 EMIF IP User Guide*'s HPS DQS group placements, the DQS group used for the ECC bits needs to move so it is placed in lane 3 of I/O bank 2M.
   - For a DDR4 interface width of 16 bit + ECC, copy the pin locations for `emif_hps_mem_mem_dbi_n [8]`, `emif_hps_mem_mem_dqs[8]`, `emif_hps_mem_mem_dqs_n[8]`, `emif_hps_mem_mem_dq[71:64]`, to `emif_hps_mem_mem_dbi_n[2]`, `emif_hps_mem_mem_dqs[2]`, `emif_hps_mem_mem_dqs_n[2]`, `emif_hps_mem_mem_dq[23:16]` respectively.
   - For a DDR4 interface width of 32 bit + ECC, copy the pin locations for `emif_hps_mem_mem_dbi_n [8]`, `emif_hps_mem_mem_dqs[8]`, `emif_hps_mem_mem_dqs_n[8]`, `emif_hps_mem_mem_dq[71:64]`, to `emif_hps_mem_mem_dbi_n[4]`, `emif_hps_mem_mem_dqs[4]`, `emif_hps_mem_mem_dqs_n[4]`, `emif_hps_mem_mem_dq[39:32]` respectively.

Note: Note the `alert#` pin is placed in DQS group 0 which is always in the GHRD project regardless of the HPS DDR4 interface width, so no changes are needed.

Note: Further details for some configurations are shown in Enabling ECC for HPS SDRAM Article on RocketBoards website.

A.3. Safety and Regulatory Information

ENGINEERING DEVELOPMENT PRODUCT - NOT FOR RESALE OR LEASE

This development kit is intended for laboratory development and engineering use only.

This development kit is designed to allow:

- Product developers and system engineers to evaluate electronic components, circuits, or software associated with the development kit to determine whether to incorporate such items in a finished product.
- Software developers to write software applications for use with the end product.

This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required Federal Communications Commission (FCC) equipment authorizations are first obtained.

Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference.

Unless the assembled kit is designed to operate under Part 15, Part 18 or Part 95 of the United States Code of Federal Regulations (CFR) Title 47, the operator of the kit must operate under the authority of an FCC licenseholder or must secure an experimental authorization under Part 5 of the United States CFR Title 47.

Safety Assessment and CE mark requirements have been completed, however, other certifications that may be required for installation and operation in your region have not been obtained.

A.3.1. Safety Warnings

Power Supply Hazardous Voltage

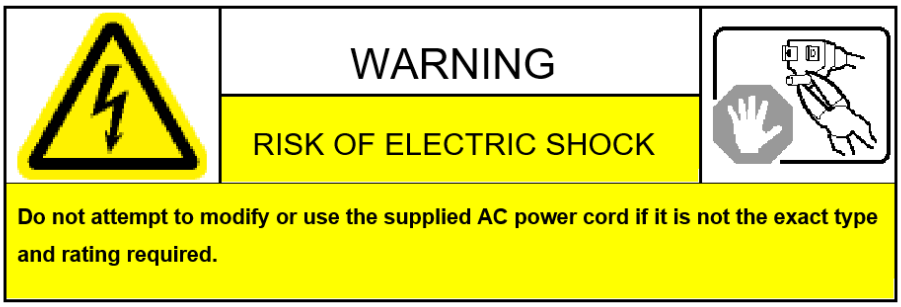
AC mains voltages are present within the power supply assembly. No user serviceable parts are present inside the power supply.

Power Connect and Disconnect

The AC power supply cord is the primary disconnect device from mains (AC power) and used to remove all DC power from the board/system. The socket outlet must be installed near the equipment and must be readily accessible.

System Grounding (Earthing)

To avoid shock, you must ensure that the power cord is connected to a properly wired and grounded receptacle. Ensure that any equipment to which this product will be attached is also connected to properly wired and grounded receptacles.



Power Cord Requirements

The connector that plugs into the wall outlet must be a grounding-type male plug designed for use in your region. It must have marks showing certification by an agency in your region. The connector that plugs into the AC receptacle on the power

supply must be an IEC 320, sheet C13, female connector. If the power cord supplied with the system does not meet requirements for use in your region, discard the cord and do not use it with adapters.

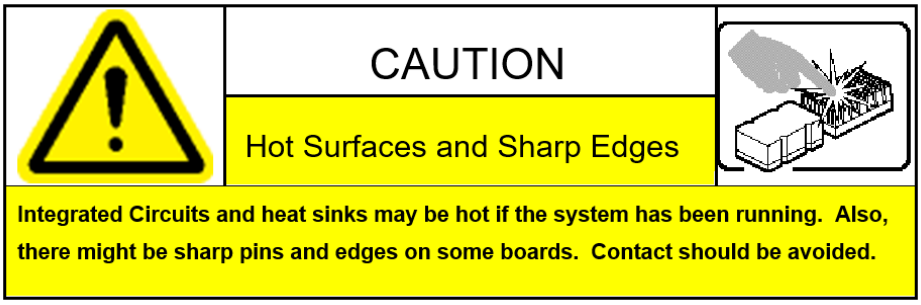
Lightning/Electrical Storm

Do not connect/disconnect any cables or perform installation/maintenance of this product during an electrical storm.

Risk of Fire

To reduce the risk of fire, keep all flammable materials a safe distance away from the boards and power supply. You must configure the development kit on a flame retardant surface.

A.3.2. Safety Cautions



Caution: Hot Surfaces and Sharp Edges. Integrated Circuits and heat sinks may be hot if the system has been running. Also, there might be sharp edges on some boards. Contact should be avoided.

Thermal and Mechanical Injury

Certain components such as heat sinks, power regulators, and processors may be hot. Heatsink fans are not guarded. Power supply fan may be accessible through guard. Care should be taken to avoid contact with these components.

Cooling Requirements

Maintain a minimum clearance area of 5 centimeters (2 inches) around the isde, front and back of the board for cooling purposes. Do not block power supply ventilation holes and fan.

Electro-Magnetic Interference (EMI)

This equipment has not been tested for compliance with emission limits of FCC and similar international regulations. Use of this equipment in a residential location is prohibited. This equipment generates, uses and can radiate radio frequency energy which may result in harmful interference to radio communications. If this equipment does cause harmful interfence to radio or television reception, which can be determined by turning the equipment on and off, the user is required to take measures to eliminate this interference.

Telecommunications Port Restrictions

The wireline telecommunications ports (modem, xDSL, T1/E1) on this product must not be connected to the Public Switched Telecommunication Network (PSTN) as it might result in disruption of the network. No formal telecommunication certification to FCC, R&TTE Directive, or other national requirements have been obatined.

Electrostatic Discharge (ESD) Warning

A properly grounded ESD wrist strap must be worn during operation/installation of the boards, connection of cables, or during installation or removal of daughter cards. Failure to use wrist straps can damage components within the system.

Attention: Please return this product to Intel for proper disposition. If it is not returned, refer to local environmental regulations for proper recycling. Do not dispose of this product in unsorted municipal waste.

A.4. Compliance Information

A.4.1. Compliance and Conformity Statements

CE EMI Conformity Caution

This development board is delivered conforming to relevant standards mandated by Directive 2014/30/EU. Because of the nature of programmable logic devices, it is possible for the user to modify the development kit in such a way as to generate electromagnetic interference (EMI) that exceeds the limits established for this equipment. Any EMI caused as a result of modifications to the delivered material is the responsibility of the user of this development kit.

CE

B. Revision History

B.1. Revision History for Intel Stratix 10 SX SoC Development Kit User Guide

Document Version	Changes
2019.09.20	Added sections: • Modify the Intel Stratix 10 SX SoC Development Kit to use a battery for the BBRAM on page 113 • Modify the Intel Stratix 10 SX SoC Development Kit HPS DDR4 memory width and ECC configuration using the Golden Hardware Reference Design project on page 114 • Installing the Intel Stratix 10 SX SoC Development Kit Package on page 7 • Intel MAX 10 System Controller Updates on page 10

Document Version	Changes
2019.03.20	Removed reference to an internal daughter card.
2018.09.20	Removed references to NAND x8 Configuration in FPGA Configuration on page 24
2018.08.06	SDM Support of NAND dropped. Removed references to SDM Boot NAND Flash Daughter Card. Updated these sections: • Inspect the Development Kit on page 9 • Development Kit Feature Summary on page 12 • HPS Boot Flash Card on page 66
2018.07.20	Added device variant SX in the document title
2018.04.04	Initial Release.

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