ATWINC3400

Single Chip IEEE 802.11 b/g/n Network Controller with Integrated Bluetooth 4.0

PRELIMINARY DATASHEET

Description

The Atmel® ATWINC3400 is a single chip IEEE® 802.11 b/g/n RF/Baseband/MAC network controller and Bluetooth® Low Energy (BLE) 4.0 optimized for low-power mobile applications. The ATWINC3400 supports single stream 1x1 802.11n mode providing up to 72Mbps PHY rate. The ATWINC3400 features fully integrated Power Amplifier, LNA, Switch, and Power Management. ATWINC3400 also features an on-chip microcontroller and integrated Flash memory for system software. Implemented in 65nm CMOS technology, the ATWINC3400 offers very low power consumption while simultaneously providing high performance and minimal bill of materials.

The ATWINC3400 utilizes highly optimized 802.11-BLE coexistence protocols. The ATWINC3400 provides multiple peripheral interfaces including UART, SPI, I^2C, and SDIO. The only external clock sources needed for the ATWINC3400 is a high-speed crystal or oscillator with a wide range of reference clock frequencies supported (14-40MHz) and a 32.768kHz clock for sleep operation. The ATWINC3400 is available in QFN packaging.

Features

IEEE 802.11

- IEEE 802.11 b/g/n 20MHz (1x1) solution
- Single spatial stream in 2.4GHz ISM band
- Integrated PA and T/R Switch
- Superior Sensitivity and Range via advanced PHY signal processing
- Advanced Equalization and Channel Estimation
- Advanced Carrier and Timing Synchronization
- Wi-Fi Direct and Soft-AP support
- Supports IEEE 802.11 WEP, WPA, and WPA2 Security
- Supports China WAPI security
- Superior MAC throughput via hardware accelerated two-level A-MSDU/A-MPDU frame aggregation and block acknowledgement
- On-chip memory management engine to reduce host load
- SPI, SDIO, I^2C, and UART host interfaces
- Operating temperature range of -40°C to +85°C
- Fast boot options:
  - On-Chip Boot ROM (firmware instant boot)
  - SPI flash boot (firmware patches and state variables)
  - Low-leakage on-chip memory for state variables

  - Fast AP re-association (150ms)
- On-Chip Network Stack to offload MCU:
  - Integrated Network IP stack to minimize host CPU requirements
  - Network features: TCP, UDP, DHCP, ARP, HTTP, SSL, and DNS

BLE

- BLE 4.0
- Adaptive Frequency Hopping
- HCI (Host Control Interface) via high speed UART
- Integrated PA and T/R Switch
- Superior Sensitivity and Range
- UART host and audio interfaces

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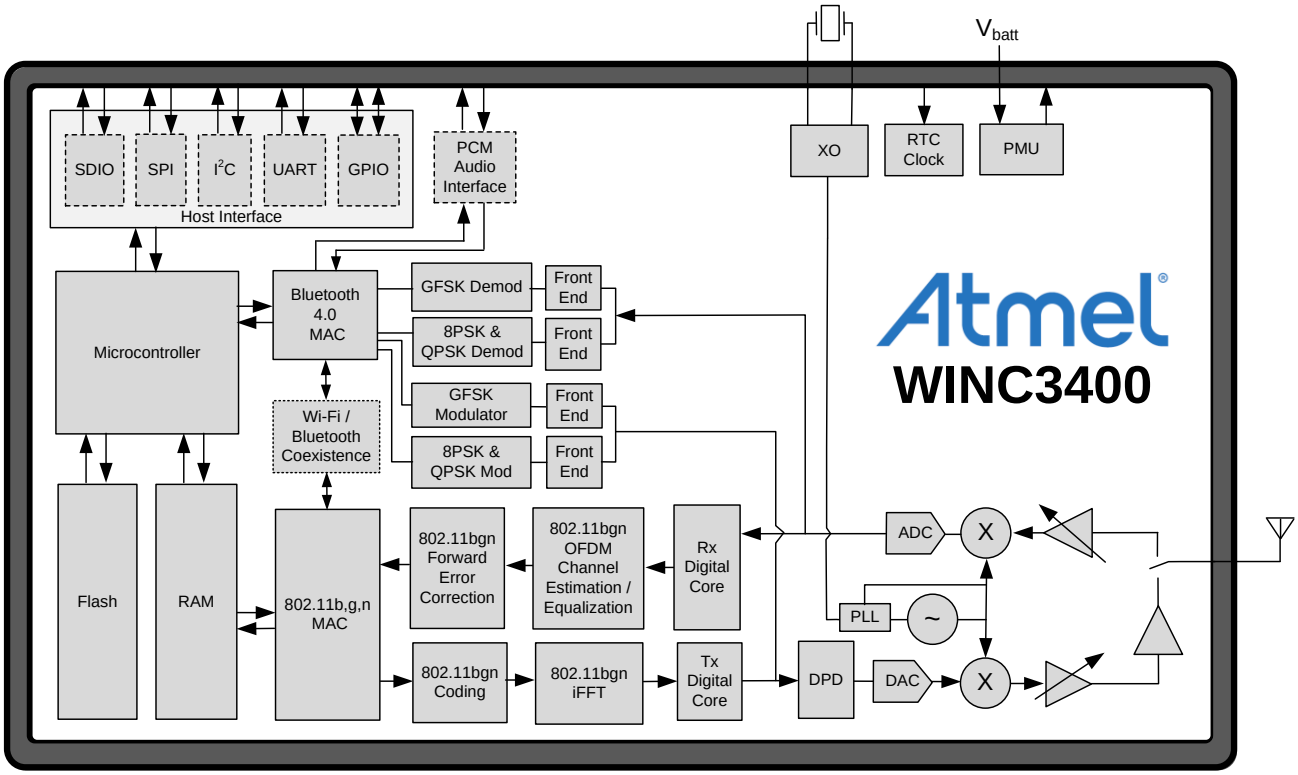
1 Ordering Information and IC Marking

Table 1-1. Ordering Details

Atmel Official Part Number (for ordering)	Package Type	IC Marking
ATWINC3400-MU-T	6x6 QFN in Tape and Reel	ATWINC3400

2 Block Diagram

Figure 2-1. ATWINC3400 Block Diagram



3 Pinout and Package Information

3.1 Pin Description

ATWINC3400 is offered in an exposed pad 40-pin QFN package. This package has an exposed paddle that must be connected to the system board ground. The QFN package pin assignment is shown in Figure 3-1. The color shading is used to indicate the pin type as follows:

- Green – power
- Red – analog
- Blue – digital I/O
- Yellow – digital input
- Grey – unconnected or reserved

The ATWINC3400 pins are described in Table 3-1.

Figure 3-1. Pin Assignment

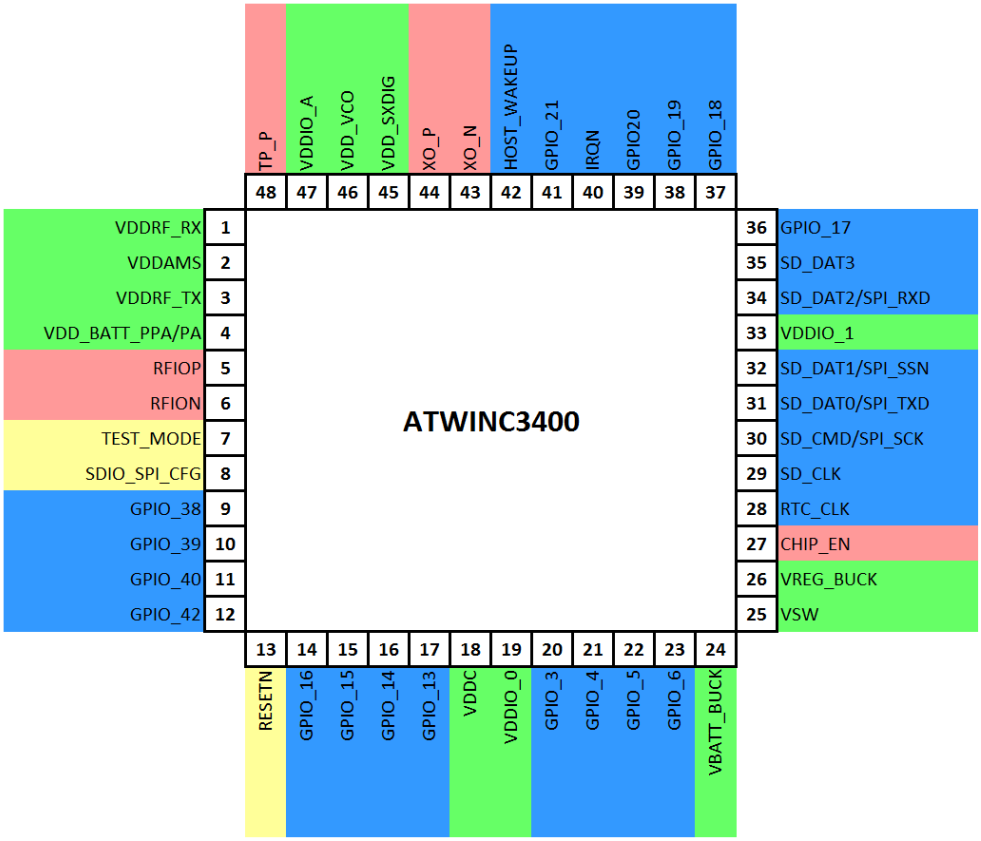


Table 3-1. Pin Description

Pin #	Pin Name	Pin Type	Description
1	VDDRF_RX	Power	Tuner RF RX Supply (see Section 10.1)
2	VDDAMS	Power	Tuner BB Supply (see Section 10.1)
3	VDDRF_TX	Power	Tuner RF TX Supply (see Section 10.1)
4	VDDBATT_PPA/PA	Power	Battery Supply for PA (see Section 10.1)
5	RFIOP	Analog	Wi-Fi/BLE Pos RF Differential I/O
6	RFION	Analog	Wi-Fi /BLE Neg RF Differential I/O
7	TEST_MODE	Digital Input	Test Mode – Customer Tie to GND
8	SDIO_SPI_CFG	Digital Input	Tie to VDDIO for SPI, GND for SDIO
9	GPIO_38	Digital I/O, Programmable Pull-Down	GPIO_38
10	GPIO_39	Digital I/O, Programmable Pull-Up	GPIO_39
11	GPIO_40	Digital I/O, Programmable Pull-Down	GPIO_40
12	GPIO_42	Digital I/O, Programmable Pull-Down	GPIO_42
13	RESETN	Digital Input	Active-Low Hard Reset
14	GPIO_16	Digital I/O, Programmable Pull-Up	GPIO_16/BLE UART Transmit Data Output
15	GPIO_15	Digital I/O, Programmable Pull-Up	GPIO_15/BLE UART Receive Data Input
16	GPIO_14	Digital I/O, Programmable Pull-Up	GPIO_14/BLE UART RTS output/I^2C Slave Data

Pin #	Pin Name	Pin Type	Description
17	GPIO_13	Digital I/O, Programmable Pull-Up	GPIO_13/BLE UART CTS Input/I^{2}C Slave Clock/Wi-Fi UART TXD Output
18	VDDC	Power	Digital Core Power Supply (see Section 10.1)
19	VDDIO_0	Power	Digital I/O Power Supply (see Section 10.1)
20	GPIO_3	Digital I/O, Programmable Pull-Up	GPIO_3/SPI Flash Clock Output
21	GPIO_4	Digital I/O, Programmable Pull-Up	GPIO_4/SPI Flash SSN Output
22	GPIO_5	Digital I/O, Programmable Pull-Up	GPIO_5/Wi-Fi UART TXD Output/SPI Flash TX Output (MOSI)
23	GPIO_6	Digital I/O, Programmable Pull-Up	GPIO_6/Wi-Fi UART RXD Input/SPI Flash RX Input (MISO)
24	VBATT_BUCK	Power	Battery Supply for DC/DC Converter (see Section 10.1)
25	VSW	Power	Switching Output of DC/DC Converter (see Section 10.1)
26	VREG_BUCK	Power	Core Power from DC/DC Converter (see Section 10.1)
27	CHIP_EN	Analog	PMU Enable
28	RTC_CLK	Digital I/O, Programmable Pull-Up	RTC Clock Input/GPIO_1/Wi-Fi UART RXD Input/Wi-Fi UART TXD Output/BT UART CTS Input
29	SD_CLK	Digital I/O, Programmable Pull-Up	SDIO Clock/GPIO_8/Wi-Fi UART RXD Input/BT UART CTS Input
30	SD_CMD/SPI_SCK	Digital I/O, Programmable Pull-Up	SDIO Command/SPI Clock
31	SD_DAT0/SPI_TXD	Digital I/O, Programmable Pull-Up	SDIO Data0/SPI TX Data
32	SD_DAT1/SPI_SSN	Digital I/O, Programmable Pull-Up	SDIO Data1/SPI Slave Select
33	VDDIO_1	Power	Digital I/O Power Supply (see Section 10.1)
34	SD_DAT2/SPI_RXD	Digital I/O, Programmable Pull-Up	SDIO Data2/SPI RX Data
35	SD_DAT3	Digital I/O, Programmable Pull-Up	SDIO Data3/GPIO_7/Wi-Fi UART TXD output/BT UART RTS Output
36	GPIO_17	Digital I/O, Programmable Pull-Down	GPIO_17
37	GPIO_18	Digital I/O, Programmable Pull-Down	GPIO_18
38	GPIO_19	Digital I/O, Programmable Pull-Down	GPIO_19
39	GPIO_20	Digital I/O, Programmable Pull-Down	GPIO_20
40	IRQN	Digital I/O, Programmable Pull-Up	Host Interrupt Request Output/Wi-Fi UART RXD Input/BT UART RTS Output
41	GPIO_21	Digital I/O, Programmable Pull-Up	GPIO_21/RTC Clock/Wi-Fi UART RXD Input/Wi-Fi UART TXD Output/BT UART RTS Output
42	HOST_WAKEUP	Digital I/O, Programmable Pull-Up	SLEEP Mode Control/Wi-Fi UART TXD output
43	XO_N	Analog	Crystal Oscillator N
44	XO_P	Analog	Crystal Oscillator P
45	VDD_SXDIG	Power	SX Power Supply (see Section 10.1)
46	VDD_VCO	Power	VCO Power Supply (see Section 10.1)
47	VDDIO_A	Power	Tuner VDDIO Power Supply (see Section 10.1)
48	TP_P	Analog	Test Pin/Customer No Connect
49	PADDLE VSS	Power	Connect to System Board Ground

3.2 Package Description

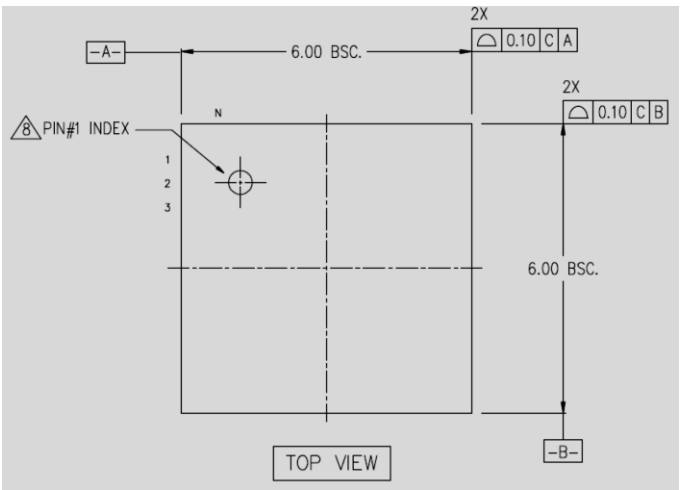
The ATWINC3400 QFN package information is provided in Table 3-2.

Table 3-2. QFN Package Information

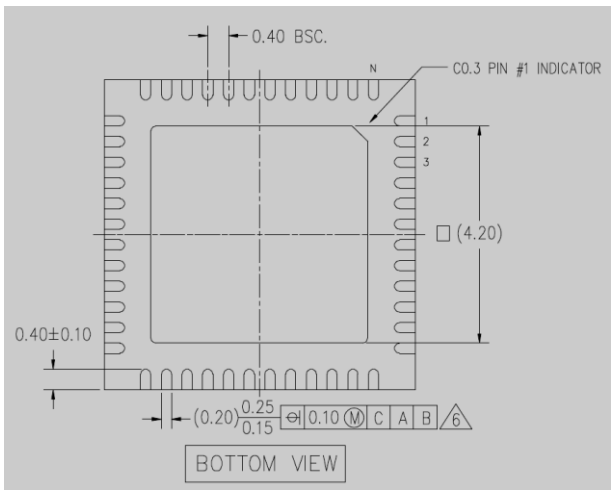
Parameter	Value	Unit	Tolerance
Package Size	6x6	mm	±0.1mm
QFN Pad Count	48		
Total Thickness	0.85	mm	±0.05mm
QFN Pad Pitch	0.40		
Pad Width	0.25		
Exposed Pad size	4.7x4.7		

The ATWINC3400 48 QFN package view is shown in Figure 3-2.

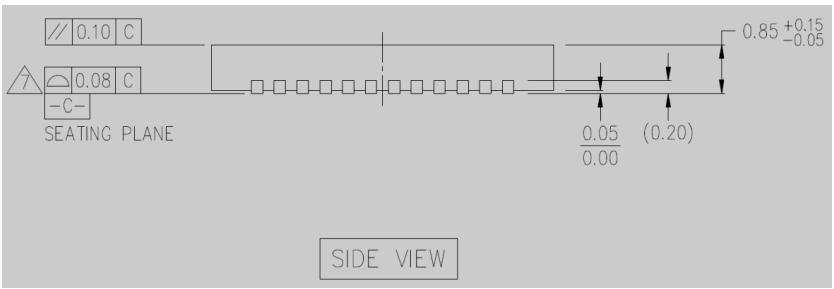
Figure 3-2. QFN Package



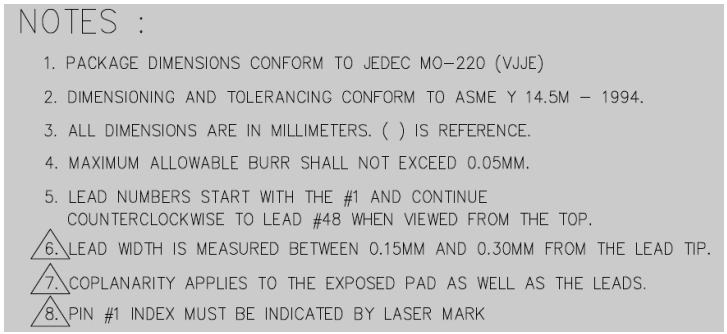
ATWILC3400 QFN Package Top View



ATWILC3400 QFN Package Bottom View



ATWILC3400 QFN Package Side View



ATWILC3400 QFN Package Notes

The QFN package is a qualified Green Package.

4 Electrical Specifications

4.1 Absolute Ratings

Table 4-1. Absolute Maximum Ratings

Characteristic	Symbol	Min.	Max.	Unit
Core Supply Voltage	VDDC	-0.3	1.5	V
I/O Supply Voltage	VDDIO	-0.3	5.0	
Battery Supply Voltage	VBATT	-0.3	5.0	
Digital Input Voltage	V_{IN}	-0.3	VDDIO	
Analog Input Voltage	V_{AIN}	-0.3	1.5	
ESD Human Body Model	V_{ESDHBM}	-1000, -2000 (see notes below)	+1000, +2000 (see notes below)	
Storage Temperature	T_A	-65	150	ºC
Junction Temperature			125	
RF input power max			23	dBm

Notes:
1. V_{IN} corresponds to all the digital pins.
2. V_{AIN} corresponds to the following analog pins: VDD_RF_RX, VDD_RF_TX, VDD_AMS, RFIOP, RFION, XO_N, XO_P, VDD_SXDIG, and VDD_VCO.
3. For V_{ESDHBM}, each pin is classified as Class 1, or Class 2, or both:
   - The Class 1 pins include all the pins (both analog and digital)
   - The Class 2 pins are all digital pins only
   - V_{ESDHBM} is ±1kV for Class1 pins. V_{ESDHBM} is ±2kV for Class2 pins

4.2 Recommended Operating Conditions

Table 4-2. Recommended Operating Conditions

Characteristic	Symbol	Min.	Typ.	Max.	Unit
I/O Supply Voltage[1]	VDDIO	2.7	3.3	3.6	V
Battery Supply Voltage[2]	VBATT	3.0	3.6	4.2	
Operating Temperature		-40		85	ºC

Notes: 1. I/O supply voltage is applied to the following pins: VDDIO_A, VDDIO.
2. Battery supply voltage is applied to following pins: VDD_BATT_PPA, VDD_BATT_PA, VBATT_BUCK.
3. Refer to Section 10.1 and 11 for the details of power connections.

4.3 DC Electrical Characteristics

Table 4-3 provides the DC characteristics for the ATWINC3400 digital pads.

Table 4-3. DC Electrical Characteristics

Characteristic	Min.		Max.	Unit
Input Low Voltage V_{IL}	-0.30		0.60	V
Input High Voltage V_{IH}	VDDIO-0.60		VDDIO+0.30	
Output Low Voltage V_{OL}			0.45	
Output High Voltage V_{OH}	VDDIO-0.50			
Input Low Voltage V_{IL}	-0.30		0.63	V
Input High Voltage V_{IH}	VDDIO-0.60		VDDIO+0.30	
Output Low Voltage V_{OL}			0.45	
Output High Voltage V_{OH}	VDDIO-0.50			
Input Low Voltage V_{IL}	-0.30		0.65	V
Input High Voltage V_{IH}	VDDIO-0.60		VDDIO+0.30 (up to 3.60)	
Output Low Voltage V_{OL}			0.45	
Output High Voltage V_{OH}	VDDIO-0.50			
Output Loading			20	pF
Digital Input Load			6	
Pad Drive Strength	8	13.5		mA

5 Clocking

5.1 Crystal Oscillator

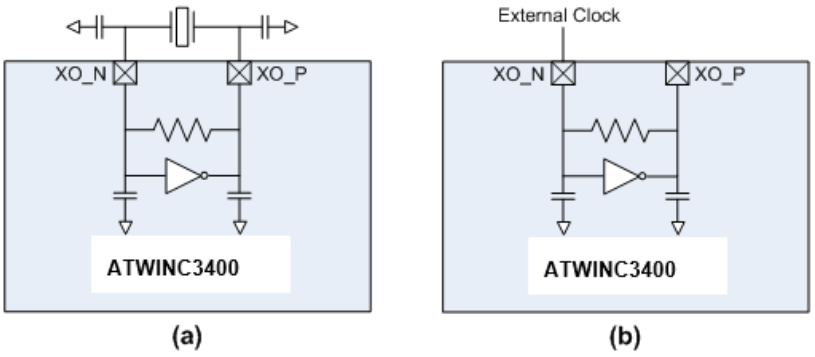
Table 5-1. Crystal Oscillator Parameters

Parameter	Min.	Typ.	Max.	Unit
Crystal Resonant Frequency	12	26	40	MHz
Crystal Equivalent Series Resistance		50	150	Ω
Stability – Initial Offset[1]	-100		100	ppm
Stability - Temperature and Aging	-25		25	

Note 1. Initial offset must be calibrated to maintain ±25ppm in all operating conditions. This calibration is performed during final production testing.

The block diagram in Figure 5-1(a) shows how the internal Crystal Oscillator (XO) is connected to the external crystal. The XO has 5pF internal capacitance on each terminal XO_P and XO_N. To bypass the crystal oscillator with an external reference, an external signal capable of driving 5pF can be applied to the XO_N terminal as shown in Figure 5-1(b).

Figure 5-1. XO Connections



(a) Crystal Oscillator is Used (b) Crystal Oscillator is Bypassed

Table 5-2 specifies the electrical and performance requirements for the external clock.

Table 5-2. Bypass Clock Specification

Parameter	Min.	Max.	Unit	Comments
Oscillation frequency	12	32	MHz	Must be able to drive 5pF load @ desired frequency
Voltage swing	0.5	1.2	V_{pp}	Must be AC coupled
Stability – Temperature and Aging	-25	+25	ppm	
Phase Noise		-130	dBc/Hz	At 10kHz offset
Jitter(RMS)		<1psec		Based on integrated phase noise spectrum from 1kHz to 1MHz

5.2 Low Power Oscillator

ATWILC3400 requires an external 32.768kHz clock to be used for sleep operation, which is provided through Pin 28 or Pin 41. The frequency accuracy of the external clock has to be within ±200ppm.

6 CPU and Memory Subsystems

6.1 Processor

ATWILC3400 has a Cortus APS3 32-bit processor. This processor performs many of the MAC functions, including but not limited to association, authentication, power management, security key management, and MSDU aggregation/de-aggregation. In addition, the processor provides flexibility for various modes of operation, such as STA and AP modes.

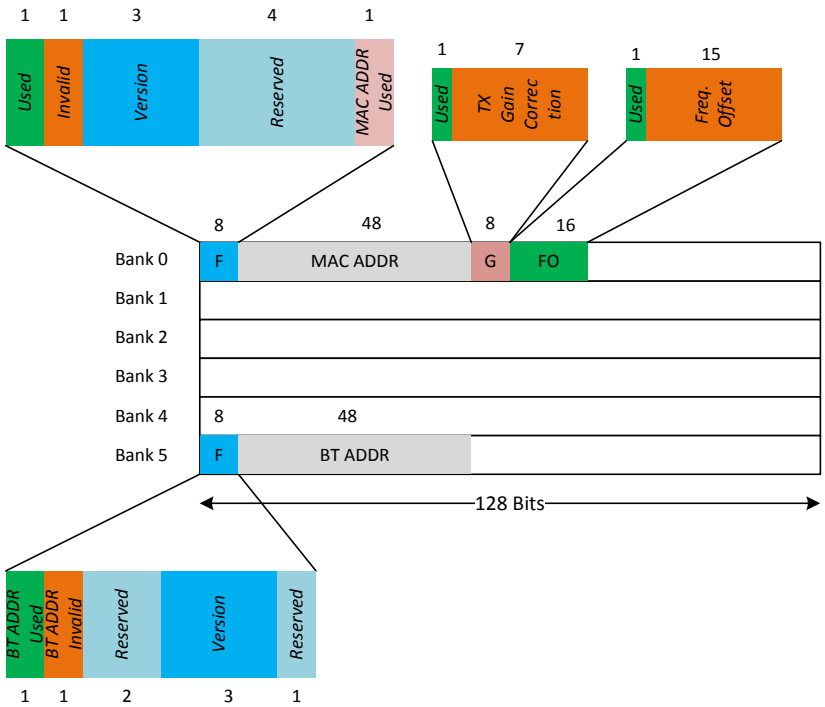
6.2 Memory Subsystem

The APS3 core uses a 256KB instruction/boot ROM (160KB for 802.11 and 96KB for BLE) along with a 420KB instruction RAM (128KB for 802.11 and 292KB for BLE), and a 128KB data RAM (64KB for 802.11 and 64KB for BLE). In addition, the device uses a 160KB shared/exchange RAM (128KB for 802.11 and 32KB for BLE), accessible by the processor and MAC, which allows the processor to perform various data management tasks on the TX and RX data packets.

6.3 Non-Volatile Memory (eFuse)

ATWILC3400 has 768 bits of non-volatile eFuse memory that can be read by the CPU after device reset. This non-volatile one-time-programmable memory can be used to store customer-specific parameters, such as 802.11 MAC address, BLE address, and various calibration information, such as TX power, crystal frequency offset, etc., as well as other software-specific configuration parameters. The eFuse is partitioned into six 128-bit banks. The bit map of the first and last banks is shown in Figure 6-1. The purpose of the first 80 bits in bank 0 and the first 56 bits in bank 5 is fixed, and the remaining bits are general-purpose software dependent bits, or reserved for future use. Since each bank and each bit can be programmed independently, this allows for several updates of the device parameters following the initial programming, e.g., updating 802.11 MAC address or BLE address (this can be done by invalidating the last programmed bank and programming a new bank). Refer to ATWILC3400 Programming Guide for the eFuse programming instructions.

Figure 6-1. eFuse Bit Map



7 WLAN Subsystem

The WLAN subsystem is composed of the Media Access Controller (MAC) and the Physical Layer (PHY). The following two subsections describe the MAC and PHY in detail.

7.1 MAC

7.1.1 Features

The ATWILC3400 IEEE802.11 MAC supports the following functions:

- IEEE 802.11b/g/n
- IEEE 802.11e WMM QoS EDCA/PCF multiple access categories traffic scheduling
- Advanced IEEE 802.11n features:
  - Transmission and reception of aggregated MPDUs (A-MPDU)
  - Transmission and reception of aggregated MSDUs (A-MSDU)
  - Immediate Block Acknowledgement
  - Reduced Interframe Spacing (RIFS)
- Support for IEEE802.11i and WFA security with key management
  - WEP 64/128
  - WPA-TKIP
  - 128-bit WPA2 CCMP (AES)
- Support for WAPI security
- Advanced power management:
  - Standard 802.11 Power Save Mode
  - Wi-Fi Alliance WMM-PS (U-APSD)

- RTS-CTS and CTS-self support
- Supports either STA or AP mode in the infrastructure basic service set mode
- Supports independent basic service set (IBSS)

7.1.2 Description

The ATWILC3400 MAC is designed to operate at low power while providing high data throughput. The IEEE 802.11 MAC functions are implemented with a combination of dedicated data path engines, hardwired control logic, and a low-power, high-efficiency microprocessor. The combination of dedicated logic with a programmable processor provides optimal power efficiency and real-time response while providing the flexibility to accommodate evolving standards and future feature enhancements.

Dedicated data path engines are used to implement data path functions with heavy computational. For example, an FCS engine checks the CRC of the transmitting and receiving packets, and a cipher engine performs all the required encryption and decryption operations for the WEP, WPA-TKIP, WPA2 CCMP-AES, and WAPI security requirements.

Control functions which have real-time requirements are implemented using hardwired control logic modules. These logic modules offer real-time response while maintaining configurability via the processor. Examples of hardwired control logic modules are the channel access control module (implements EDCA/HCCA, Beacon TX control, interframe spacing, etc.), protocol timer module (responsible for the Network Access Vector, back-off timing, timing synchronization function, and slot management), MPDU handling module, aggregation/de-aggregation module, block ACK controller (implements the protocol requirements for burst block communication), and TX/RX control FSMs (coordinate data movement between PHY-MAC interface, cipher engine, and the DMA interface to the TX/RX FIFOs).

The MAC functions implemented solely in software on the microprocessor have the following characteristics:

- Functions with high memory requirements or complex data structures. Examples are association table management and power save queuing
- Functions with low computational load or without critical real-time requirements. Examples are authentication and association
- Functions which need flexibility and upgradeability. Examples are beacon frame processing and QoS scheduling

7.2 PHY

7.2.1 Features

The ATWILC3400 IEEE802.11 PHY supports the following functions:

- Single antenna 1x1 stream in 20MHz channels
- Supports IEEE 802.11b DSSS-CCK modulation: 1, 2, 5.5, and 11Mbps
- Supports IEEE 802.11g OFDM modulation: 6, 9, 12,18, 24, 36, 48, and 54Mbps
- Supports IEEE 802.11n HT modulations MCS0-7, 20MHz, 800 and 400ns guard interval: 6.5, 7.2, 13.0, 14.4, 19.5, 21.7, 26.0, 28.9, 39.0, 43.3, 52.0, 57.8, 58.5, 65.0, and 72.2Mbps
- IEEE 802.11n mixed mode operation
- Per packet TX power control
- Advanced channel estimation/equalization, automatic gain control, CCA, carrier/symbol recovery, and frame detection

7.2.2 Description

The ATWILC3400 WLAN PHY is designed to achieve reliable and power-efficient physical layer communication specified by IEEE 802.11b/g/n in single stream mode with 20MHz bandwidth. Advanced algorithms have been employed to achieve maximum throughput in a real world communication environment with impairments and interference. The PHY implements all the required functions such as FFT, filtering, FEC (Viterbi decoder), frequency and timing acquisition and tracking, channel estimation and equalization, carrier sensing and clear channel assessment, as well as the automatic gain control.

7.3 Radio

7.3.1 Receiver Performance

Radio Performance under Typical Conditions: VBATT=3.6V; VDDIO=3.3V; Temperature: 25°C.

Table 7-1. Receiver Performance

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency		2,412		2,484	MHz
Sensitivity 802.11b	1Mbps DSS		-98.0		dBm
	2Mbps DSS		-95.0		
	5.5Mbps DSS		-93.0		
	11Mbps DSS		-89.0		
Sensitivity 802.11g	6Mbps OFDM		-90.6		dBm
	9Mbps OFDM		-89.0		
	12Mbps OFDM		-87.9		
	18Mbps OFDM		-86.0		
	24Mbps OFDM		-83.0		dBm
	36Mbps OFDM		-79.8		
	48Mbps OFDM		-76.0		
	54Mbps OFDM		-74.3		
Sensitivity 802.11n (BW=20MHz)	MCS 0		-89.0		dBm
	MCS 1		-86.9		
	MCS 2		-84.9		
	MCS 3		-82.4		
	MCS 4		-79.2		
	MCS 5		-75.0		
	MCS 6		-73.2		
	MCS 7		-71.2		
Maximum Receive Signal Level	1-11Mbps DSS	-10	5		dBm
	6-54Mbps OFDM	-10	-3		
	MCS 0 – 7	-10	-3		
Adjacent Channel	1Mbps DSS (30MHz offset)		50		dB

Parameter	Description	Min.	Typ.	Max.	Unit
Rejection	11Mbps DSS (25MHz offset)		43		
	6Mbps OFDM (25MHz offset)		40		
	54Mbps OFDM (25MHz offset)		25		
	MCS 0 – 20MHz BW (25MHz offset)		40		
	MCS 7 – 20MHz BW (25MHz offset)		20		

7.3.2 Transmitter Performance

Radio Performance under Typical Conditions: VBATT=3.6V; VDDIO=3.3V; Temp: 25°C.

Table 7-2. Transmitter Performance

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency		2,412		2,484	MHz
Output Power	802.11b DSSS 1Mbps		20[1]		dBm
	802.11b DSSS 11Mbps		17[1]		
	802.11g OFDM 6Mbps		16[1]		
TX Power Accuracy			±1.5[2]		dB
Carrier Suppression			30.0		dBc
Harmonic Output Power	2nd		-125		dBm/Hz
	3rd		-125		

Notes: 1. Measured at 802.11 spec compliant EVM/Spectral Mask.
2. Measured at RF Pin assuming 50Ω differential.
3. RF performance guaranteed for Temp range -30 to 85°C. 1dB derating in performance at -40°C.

8 BLE Subsystem

The BLE subsystem implements all the mission critical real-time functions. It encodes/decodes HCI packets, constructs baseband data packages and manages and monitors connection status, slot usage, data flow, routing, segmentation, and buffer control.

The BLE subsystem performs Link Control Layer management supporting the following states:

- Standby
- Connection
- Page and Page Scan
- Inquiry and Inquiry Scan
- Sniff

The BLE subsystem supports BLE profiles allowing connection to advanced low energy application such as:

- Smart Energy
- Consumer Wellness
- Home Automation
- Security
- Proximity Detection

- Entertainment
- Sports and Fitness
- Automotive

8.1 BLE Radio

8.1.1 Receiver Performance

Radio Performance under Typical Conditions: VBATT=3.6V; VDDIO=3.3V; Temp: 25°C.

Table 8-1. ATWILC3400 BLE Receiver Performance

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency		2,402		2,480	MHz
Sensitivity Ideal TX	BLE (GFSK)		-96		dBm
Maximum Receive Signal Level	BLE (GFSK)	-10	0		dBm

8.1.2 Transmitter Performance

Radio Performance under Typical Conditions: VBATT=3.6V; VDDIO=3.3V; Temp: 25°C.

Table 8-2. ATWILC3400 BLE Transmitter Performance

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency		2,402		2,480	MHz
Output Power	BLE (GFSK)	-30	8	10	dBm

9 External Interfaces

ATWINC3400 external interfaces include: SPI Slave, SDIO Slave, and UART for 802.11 control and data transfer, UART for BLE control and data transfer, I^2C Slave for control, SPI Master for external Flash, I^2C Master for external EEPROM, and General Purpose Input/Output (GPIO) pins. With the exception of the SPI Slave and SDIO Slave host interfaces, which are selected using the dedicated SDIO_SPI_CFG pin, the other interfaces can be assigned to various pins by programming the corresponding pin muxing control register for each pin to a specific value between 0 and 6.The default values of these registers are 0, which is GPIO mode. Each digital I/O pin also has a programmable pull-up or pull-down. The summary of the available interfaces and their corresponding pin mux settings is shown in Table 9-1. For specific programming instructions refer to ATWINC3400 Programming Guide.

Table 9-1. Pin-Mux Matrix of External Interfaces

Pin name	Pin #	Pull	Mux0	Mux1	Mux2	Mux3	Mux4	Mux5	Mux6
GPIO_38	9	Down							I_WAKEUP
GPIO_39	10	Up							I_WAKEUP
GPIO_40	11	Down							I_WAKEUP
GPIO_42	12	Down							
GPIO_16	14	Up	GPIO_16	O_BT_UART1_TXD					
GPIO_15	15	Up	GPIO_15	I_BT_UART1_RXD					
GPIO_14	16	Up	GPIO_14	O_BT_UART1_RTS	IO_I2C_SDA				I_WAKEUP
GPIO_13	17	Up	GPIO_13	I_BT_UART1_CTS	IO_I2C_SCL	O_WIFI_UART_TXD			I_WAKEUP
GPIO_3	20	Up	GPIO_3	O_SPI_SCK_FLASH					O_BT_UART2_TXD
GPIO_4	21	Up	GPIO_4	O_SPI_SSN_FLASH					I_BT_UART2_RXD
GPIO_5	22	Up	GPIO_5	O_SPI_TXD_FLASH		O_WIFI_UART_TXD			I_WAKEUP
GPIO_6	23	Up	GPIO_6	I_SPI_RXD_FLASH		I_WIFI_UART_RXD			I_WAKEUP
RTC_CLK	28	Up	GPIO_1	I_RTC_CLK		I_WIFI_UART_RXD	O_WIFI_UART_TXD	I_BT_UART1_CTS	
SD_CLK/GPIO_8	29	Up	GPIO_8	I_SD_CLK		I_WIFI_UART_RXD	I_BT_UART1_CTS		
SD_CMD/SPI_SCK	30	Up		IO_SD_CMD	IO_SPI_SCK				
SD_DAT0/SPI_TXD	31	Up		IO_SD_DAT0	O_SPI_TXD				
SD_DAT1/SPI_SSN	32	Up		IO_SD_DAT1	IO_SPI_SSN				
SD_DAT2/SPI_RXD	34	Up		IO_SD_DAT2	I_SPI_RXD				
SD_DAT3/GPIO_7	35	Up	GPIO_7	IO_SD_DAT3		O_WIFI_UART_TXD	O_BT_UART1_RTS		
GPIO_17	36	Down	GPIO_17						I_WAKEUP
GPIO_18	37	Down	GPIO_18						I_WAKEUP
GPIO_19	38	Down	GPIO_19						I_WAKEUP

Pin name	Pin #	Pull	Mux0	Mux1	Mux2	Mux3	Mux4	Mux5	Mux6
GPIO_20	39	Down	GPIO_20						I_WAKEUP
IRQN	40	Up	GPIO_2	O_IRQN		I_WIFI_UART_RXD	O_BT_UART1_RTS		
GPIO_21	41	Up	GPIO_21	I_RTC_CLK		I_WIFI_UART_RXD	O_WIFI_UART_TXD	O_BT_UART1_RTS	IO_I2C_MASTER_SCL
HOST_WAKEUP	42	Up	GPIO_0	I_WAKEUP		O_WIFI_UART_TXD			IO_I2C_MASTER_SDA

9.1 I²C Slave Interface

The I²C Slave interface, used primarily for control by the host processor, is a two-wire serial interface consisting of a serial data line (SDA) on Pin 16 (GPIO14) and a serial clock line (SCL) on Pin 17 (GPIO13). I²C Slave responds to the seven bit address value 0x60. The ATWILC3400 I²C supports I²C bus Version 2.1 - 2000 and can operate in standard mode (with data rates up to 100Kb/s) and fast mode (with data rates up to 400Kb/s).

The I²C Slave is a synchronous serial interface. The SDA line is a bidirectional signal and changes only while the SCL line is low, except for STOP, START, and RESTART conditions. The output drivers are open-drain to perform wire-AND functions on the bus. The maximum number of devices on the bus is limited by only the maximum capacitance specification of 400pF. Data is transmitted in byte packages.

For specific information, refer to the Philips Specification entitled “The I²C -Bus Specification, Version 2.1”.

Figure 9-1. I²C Slave Timing Diagram

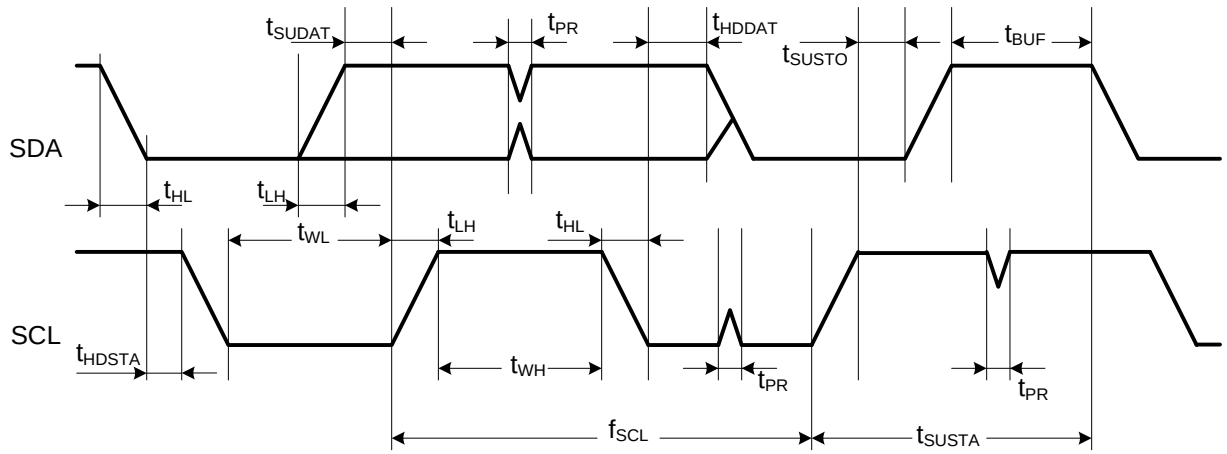


Table 9-2. I²C Slave Timing Parameters

Parameter	Symbol	Min.	Max.	Unit	Remarks
SCL Clock Frequency	f_{SCL}	0	400	kHz	
SCL Low Pulse Width	t_{WL}	1.3		µs	
SCL High Pulse Width	t_{WH}	0.6			
SCL, SDA Fall Time	t_{HL}		300	ns	
SCL, SDA Rise Time	t_{LH}		300		This is dictated by external components
START Setup Time	t_{SUSTA}	0.6		µs	
START Hold Time	t_{HDSTA}	0.6			
SDA Setup Time	t_{SUDAT}	100		ns	
SDA Hold Time	t_{HDDAT}	0			Slave and Master Default
		40			Master Programming Option
STOP Setup Time	t_{SUSTO}	0.6		µs	
Bus Free Time Between STOP and START	t_{BUF}	1.3			
Glitch Pulse Reject	t_{PR}	0	50	ns	

9.2 I²C Master Interface

ATWILC3400 provides an I²C bus master, which is intended primarily for accessing an external EEPROM memory through a software-defined protocol. The I²C Master is a two-wire serial interface consisting of a serial data line (SDA) and a serial clock line (SCL). SDA can be configured on pin 42 (HOST_WAKEUP), and SCL can be configured on pin 41 (GPIO21).

The I²C Master interface supports three speeds:

- Standard mode (100kb/s)
- Fast mode (400kb/s)
- High-speed mode (3.4Mb/s)

The timing diagram of the I²C Master interface is the same as that of the I²C Slave interface (see Figure 9-1). The timing parameters of I²C Master are shown in Table 9-3.

Table 9-3. I²C Master Timing Parameters

Parameter	Symbol	Standard Mode		Fast Mode		High-Speed Mode		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
SCL Clock Frequency	f_{SCL}	0	100	0	400	0	3400	kHz
SCL Low Pulse Width	t_{WL}	4.7		1.3		0.16		µs
SCL High Pulse Width	t_{WH}	4		0.6		0.06		
SCL Fall Time	t_{HLSCL}		300		300	10	40	ns
SDA Fall Time	t_{HLSDA}		300		300	10	80	
SCL Rise Time	t_{LHSCL}		1000		300	10	40	
SDA Rise Time	t_{LHSDA}		1000		300	10	80	

Parameter	Symbol	Standard Mode		Fast Mode		High-Speed Mode		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
START Setup Time	t_{SUSTA}	4.7		0.6		0.16		µs
START Hold Time	t_{HDSTA}	4		0.6		0.16		
SDA Setup Time	t_{SUDAT}	250		100		10		ns
SDA Hold Time	t_{HDDAT}	5		40		0	70	
STOP Setup time	t_{SUSTO}	4		0.6		0.16		µs
Bus Free Time Between STOP and START	t_{BUF}	4.7		1.3				
Glitch Pulse Reject	t_{PR}				50			ns

9.3 SPI Slave Interface

ATWILC3400 provides a Serial Peripheral Interface (SPI) that operates as a SPI slave. The SPI Slave interface can be used for control and for serial I/O of 802.11 data. The SPI Slave pins are mapped as shown in Table 9-4. The RXD pin is same as Master Output, Slave Input (MOSI), and the TXD pin is same as Master Input, Slave Output (MISO). The SPI Slave is a full-duplex slave-synchronous serial interface that is available immediately following reset when Pin 12 (SDIO_SPI_CFG) is tied to VDDIO.

Table 9-4. SPI Slave Interface Pin Mapping

Pin #	SPI Function
12	CFG: Must be tied to VDDIO
32	SSN: Active Low Slave Select
30	SCK: Serial Clock
34	RXD: Serial Data Receive (MOSI)
31	TXD: Serial Data Transmit (MISO)

When the SPI is not selected, i.e., when SSN is high, the SPI interface will not interfere with data transfers between the serial-master and other serial-slave devices. When the serial slave is not selected, its transmitted data output is buffered, resulting in a high impedance drive onto the serial master receive line.

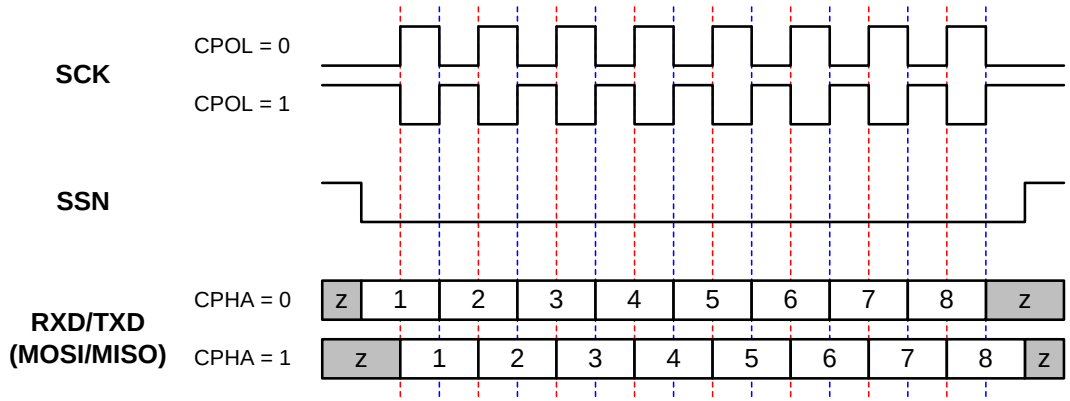
The SPI Slave interface responds to a protocol that allows an external host to read or write any register in the chip as well as initiate DMA transfers. For the details of the SPI protocol and more specific instructions refer to ATWILC3400 Programming Guide.

The SPI Slave interface supports four standard modes as determined by the Clock Polarity (CPOL) and Clock Phase (CPHA) settings. These modes are illustrated in Table 9-5 and Figure 9-2. The red lines in Figure 9-2 correspond to Clock Phase = 0 and the blue lines correspond to Clock Phase = 1.

Table 9-5. SPI Slave Modes

Mode	CPOL	CPHA
0	0	0
1	0	1
2	1	0
3	1	1

Figure 9-2. SPI Slave Clock Polarity and Clock Phase Timing



The SPI Slave timing is provided in Figure 9-3 and Table 9-6.

Figure 9-3. SPI Slave Timing Diagram

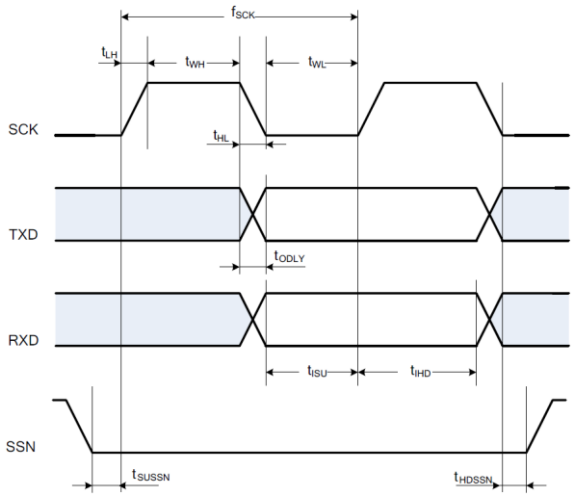


Table 9-6. SPI Slave Timing Parameters

Parameter	Symbol	Min.	Max.	Unit
Clock Input Frequency	f_{SCK}		48	MHz
Clock Low Pulse Width	t_{WL}	5		ns
Clock High Pulse Width	t_{WH}	5		
Clock Rise Time	t_{LH}		5	

Parameter	Symbol	Min.	Max.	Unit
Clock Fall Time	t_{HL}		5	
Input Setup Time	t_{ISU}	5		
Input Hold Time	t_{IHD}	5		
Output Delay	t_{ODLY}	0	20	
Slave Select Setup Time	t_{SUSSN}	5		
Slave Select Hold Time	t_{HDSSN}	5		

9.4 SPI Master Interface

ATWILC3400 provides a SPI Master interface for accessing external Flash memory. The SPI Master pins are mapped as shown in Table 9-7. The TXD pin is same as Master Output and Slave Input (MOSI). The RXD pin is same as Master Input and Slave Output (MISO). The SPI Master interface supports all four standard modes of clock polarity and clock phase shown in Table 9-5. External SPI Flash memory is accessed by a processor programming commands to the SPI Master interface, which in turn initiates a SPI master access to the Flash. For more specific instructions refer to ATWILC3400 Programming Guide.

Table 9-7. SPI Master Interface Pin Mapping

Pin #	Pin Name	SPI Function
20	GPIO3	SCK: Serial Clock Output
21	GPIO4	SCK: Active Low Slave Select Output
22	GPIO5	TXD: Serial Data Transmit Output (MOSI)
23	GPIO6	RXD: Serial Data Receive Input (MISO)

The SPI Master timing is provided in Figure 9-4 and Table 9-8.

Figure 9-4. SPI Master Timing Diagram

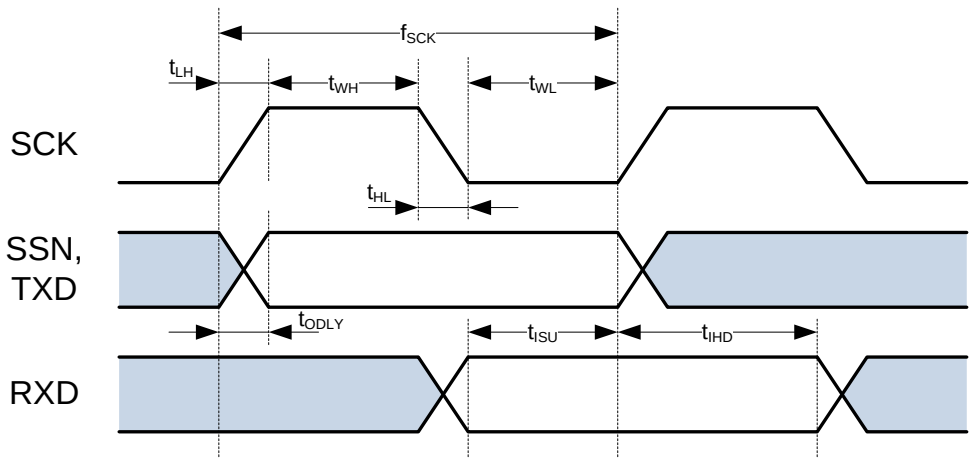


Table 9-8. SPI Master Timing Parameters

Parameter	Symbol	Min.	Max.	Unit
Clock Output Frequency	f_{SCK}		48	MHz

Parameter	Symbol	Min.	Max.	Unit
Clock Low Pulse Width	t_{WL}	5		ns
Clock High Pulse Width	t_{WH}	5		
Clock Rise Time	t_{LH}		5	
Clock Fall Time	t_{HL}		5	
Input Setup Time	t_{ISU}	5		
Input Hold Time	t_{IHD}	5		
Output Delay	t_{ODLY}	0	5	

9.5 SDIO Slave Interface

The ATWINC3400 SDIO Slave is a full speed interface. The interface supports the 1-bit/4-bit SD transfer mode at the clock range of 0-50MHz. The Host can use this interface to read and write from any register within the chip as well as configure the ATWINC3000 for data DMA. To use this interface, pin 12 (SDIO_SPI_CFG) must be grounded. The SDIO Slave pins are mapped as shown in Table 9-9.

Table 9-9. SDIO Interface Pin Mapping

Pin #	SPI Function
12	CFG: Must be tied to ground
35	DAT3: Data 3
34	DAT2: Data 2
32	DAT1: Data 1
31	DAT0: Data 0
30	CMD: Command
29	CLK: Clock

When the SDIO card is inserted into an SDIO aware host, the detection of the card will be via the means described in SDIO specification. During the normal initialization and interrogation of the card by the host, the card will identify itself as an SDIO device. The host software will obtain the card information in a tuple (linked list) format and determine if that card's I/O function(s) are acceptable to activate. If the card is acceptable, it will be allowed to power up fully and start the I/O function(s) built into it.

The SD memory card communication is based on an advanced 9-pin interface (Clock, Command, and four data and three power lines) designed to operate at maximum operating frequency of 50MHz.

The SDIO Slave interface has the following features:

- Meets SDIO card specification version 2.0
- Host clock rate variable between 0 and 50MHz
- 1 bit/4-bit SD bus modes supported
- Allows card to interrupt host
- Responds to Direct read/write (IO52) and Extended read/write (IO53) transactions
- Supports Suspend/Resume operation

The SDIO Slave interface timing is provided in Figure 9-5 and Table 9-10.

Figure 9-5. SDIO Slave Timing Diagram

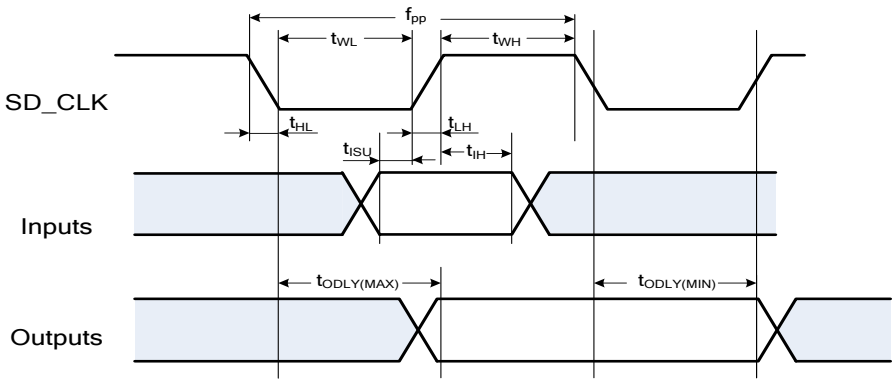


Table 9-10. SDIO Slave Timing Parameters

Parameter	Symbol	Min.	Max.	Unit
Clock Input Frequency	f_{PP}	0	50	MHz
Clock Low Pulse Width	t_{WL}	10		ns
Clock High Pulse Width	t_{WH}	10		
Clock Rise Time	t_{LH}		10	
Clock Fall Time	t_{HL}		10	
Input Setup Time	t_{ISU}	5		
Input Hold Time	t_{IH}	5		
Output Delay	t_{ODLY}	0	14	

9.6 UART

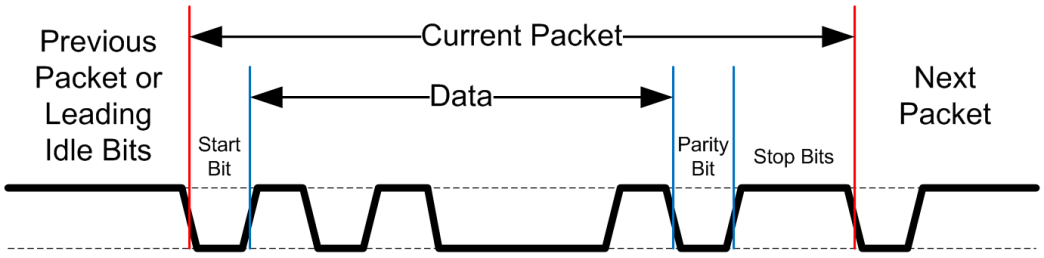
ATWILC3400 provides Universal Asynchronous Receiver/Transmitter (UART) interfaces for serial communication. The BLE subsystem has two UART interfaces: a 4-pin interface for control, data transfer, and audio (BT UART1), and a 2-pin interface for debugging (BT UART2). The 802.11 subsystem has one 2-pin UART interface (Wi-Fi UART), which can be used for control, data transfer, or debugging. The UART interfaces are compatible with the RS-232 standard, where ATWILC3400 operates as Data Terminal Equipment (DTE). The 2-pin UART has the receive and transmit pins (RXD and TXD), and the 4-pin UART has two additional pins used for flow control/handshaking: Request To Send (RTS) and Clear To Send (CTS). The pins associated with each UART interfaces can be enabled on several alternative pins by programming their corresponding pin MUX control registers (see Table 9-1 for available options).

The UART features programmable baud rate generation with fractional clock division, which allows transmission and reception at a wide variety of standard and non-standard baud rates. The BLE UART input clock is selectable between 104MHz, 52MHz, 26MHz, and 13MHz. The clock divider value is programmable as 13 integer bits and three fractional bits (with 8.0 being the smallest recommended value for normal operation). This results in the maximum supported baud rate of 10MHz/8.0 = 13MBd. The 802.11 UART input clock is selectable between 10MHz, 5MHz, 2.5MHz, and 1.25MHz. The clock divider value is programmable as 13 integer bits and three fractional bits (with 8.0 being the smallest recommended value for normal operation). This results in the maximum supported baud rate of 10MHz/8.0 = 1.25MBd.

The UART can be configured for seven or eight bit operation, with or without parity, with four different parity types (odd, even, mark, or space), and with one or two stop bits. It also has RX and TX FIFOs, which ensure reliable high speed reception and low software overhead transmission. FIFO size is 4 x8 for both RX and TX direction. The UART also has status registers showing the number of received characters available in the FIFO and various error conditions, as well the ability to generate interrupts based on these status bits.An example of UART receiving or transmitting a single packet is shown in Figure 9-6. This example shows 7-bit data (0x45), odd parity, and two stop bits.

For more specific instructions refer to ATWILC3400 Programming Guide.

Figure 9-6. Example of UART RX or TX Packet



9.7 GPIOs

18 General Purpose Input/Output (GPIO) pins, labeled GPIO 0-8 and 13-21, are available to allow for application specific functions. Each GPIO pin can be programmed as an input (the value of the pin can be read by the host or internal processor) or as an output (the output values can be programmed by the host or internal processor), where the default mode after power-up is input. GPIOs 7 and 8 are only available when the host does not use the SDIO interface, which shares two of its pins with these GPIOs. Therefore, for SDIO-based applications, 16 GPIOs (0-6 and 13-21) are available. For more specific usage instructions refer to ATWILC3400 Programming Guide.

10 Power Management

10.1 Power Architecture

ATWILC3400 uses an innovative power architecture to eliminate the need for external regulators and reduce the number of off-chip components. This architecture is shown in Figure 10-1. The Power Management Unit (PMU) has a DC/DC Converter that converts VBATT to the core supply used by the digital and RF/AMS blocks. Table 10-1 shows the typical values for the digital and RF/AMS core voltages. The PA and eFuse are supplied by dedicated LDOs, and the VCO is supplied by a separate LDO structure.

Figure 10-1. Power Architecture

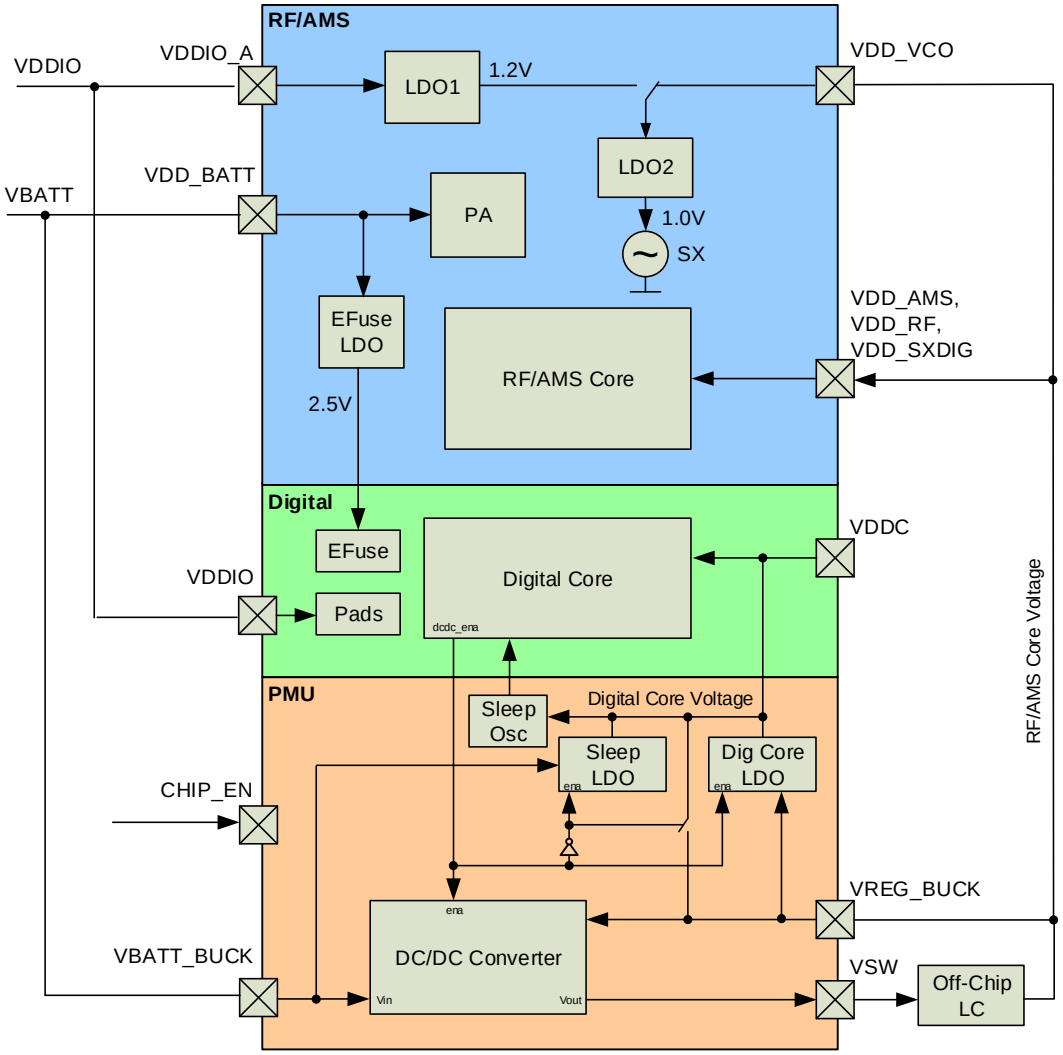


Table 10-1. PMU Output Voltages

Parameter	Typical
RF/AMS Core Voltage (VREG_BUCK)	1.3V
Digital Core Voltage (VDDC)	1.1V

The power connections in Figure 10-1 provide a conceptual framework for understanding the ATWILC3400 power architecture. Refer to the reference design for an example of power supply connections, including proper isolation of the supplies used by the digital and RF/AMS blocks.

10.2 Power Consumption

10.2.1 Description of Device States

ATWILC3400 has several devices states:

- ON_WiFi_Transmit: Device is actively transmitting an 802.11 signal
- ON_WiFi_Receive: Device is actively receiving an 802.11 signal

- ON_BT_Transmit: Device is actively transmitting a BLE signal
- ON_BT_Receive: Device is actively receiving a BLE signal
- ON_Doze: Device is on but is neither transmitting nor receiving
- Power_Down: Device core supply off (Leakage)

The following pins are used to switch between the ON and Power_Down states:

- CHIP_EN: Device pin (pin #27) used to enable DC/DC Converter
- VDDIO: I/O supply voltage from external supply

In the ON states, VDDIO is on and CHIP_EN is high (at VDDIO voltage level). To switch between the ON states and Power_Down state CHIP_EN has to change between high and low (GND) voltage. When VDDIO is off and CHIP_EN is low, the chip is powered off with no leakage (also see Note 1 in Table 10-2).

10.2.2 Current Consumption in Various Device States

Table 10-2. Current Consumption

Device State	Code Rate	Output Power, dBm	Power Consumption[1,2]	
			I_{VBATT}	I_{VDDIO}
ON_WiFi_Transmit	802.11b 1Mbps	19.2	325 mA	2.7 mA
	802.11b 11Mbps	20.1	322 mA	2.7 mA
	802.11g 6Mbps	17.8	318 mA	2.7 mA
	802.11g 54Mbps	16.2	280 mA	2.7 mA
	802.11n MCS 0	19.5	321 mA	2.7 mA
	802.11n MCS 7	15.3	276 mA	2.7 mA
ON_WiFi_Receive	802.11b 1Mbps	N/A	83.7 mA	2.5 mA
	802.11b 11Mbps	N/A	84.9 mA	2.5 mA
	802.11g 6Mbps	N/A	85.8 mA	2.5 mA
	802.11g 54Mbps	N/A	90.1 mA	2.5 mA
	802.11n MCS 0	N/A	86 mA	2.5 mA
	802.11n MCS 7	N/A	91.8 mA	2.5 mA
ON_BT_Transmit	TBD	TBD	TBD	TBD
ON_BT_Receive	TBD	N/A	<45mA	<2.5mA
Doze	N/A	N/A	<0.65mA	<7µA
Power_Down	N/A	N/A	<0.5µA	<3.5µA

Notes: 1. Conditions: VBATT @3.6v, VDDIO @2.8V, 25°C
2. Power consumption numbers are preliminary

10.2.3 Restrictions for Power States

When no power supplied to the device, i.e., the DC/DC Converter output and VDDIO are both off (at ground potential). In this case, a voltage cannot be applied to the device pins because each pin contains an ESD diode from the pin to supply. This diode will turn on when voltage higher than one diode-drop is supplied to the pin.

If a voltage must be applied to the signal pads while the chip is in a low power state, the VDDIO supply must be on, so the SLEEP or Power_Down state must be used.

Similarly, to prevent the pin-to-ground diode from turning on, do not apply a voltage that is more than one diode-drop below ground to any pin.

10.3 Power-Up/Down Sequence

The power-up/down sequence for ATWILC3400 is shown in Figure 10-2. The timing parameters are provided in Table 10-3.

Figure 10-2. Power Up/Down Sequence

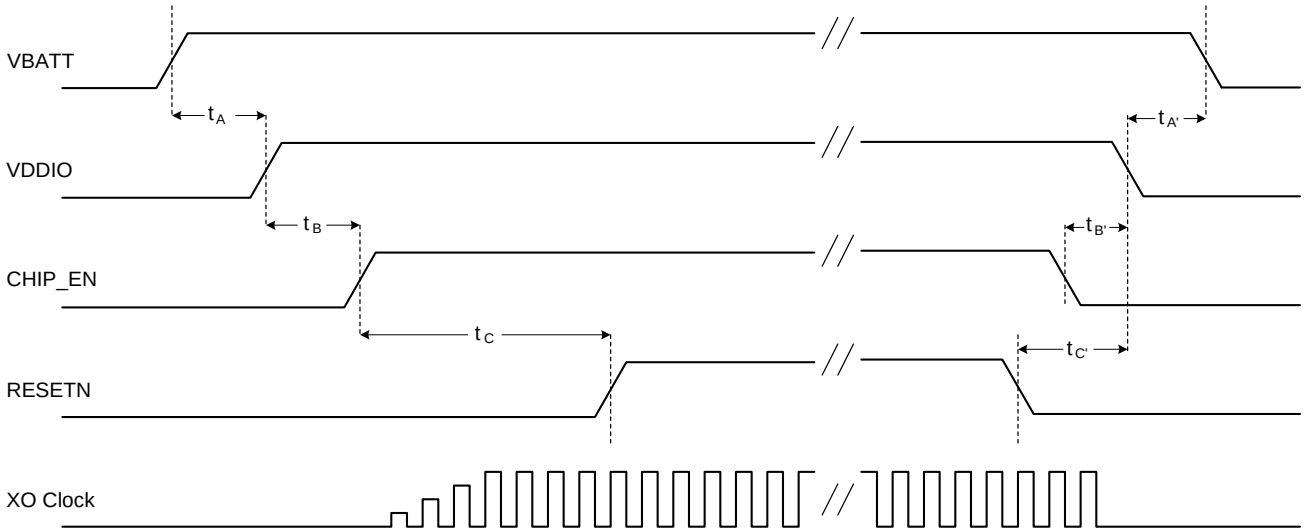


Table 10-3. Power-Up/Down Sequence Timing

Parameter	Min.	Max.	Unit	Description	Notes
t_A	0		ms	VBATT rise to VDDIO rise	VBATT and VDDIO can rise simultaneously or can be tied together. VDDIO must not rise before VBATT.
t_B	0			VDDIO rise to CHIP_EN rise	CHIP_EN must not rise before VDDIO. CHIP_EN must be driven high or low, not left floating.
t_C	5			CHIP_EN rise to RESETN rise	This delay is needed because XO clock must stabilize before RESETN removal. RESETN must be driven high or low, not left floating.
$t_{A'}$	0			VDDIO fall to VBATT fall	VBATT and VDDIO can fall simultaneously or can be tied together. VBATT must not fall before VDDIO.
$t_{B'}$	0			CHIP_EN fall to VDDIO fall	VDDIO must not fall before CHIP_EN. CHIP_EN and RESETN can fall simultaneously.
$t_{C'}$	0			RESETN fall to VDDIO fall	VDDIO must not fall before RESETN. RESETN and CHIP_EN can fall simultaneously.

10.4 Digital I/O Pin Behavior During Power-Up Sequences

The following table represents digital I/O Pin states corresponding to device power modes.

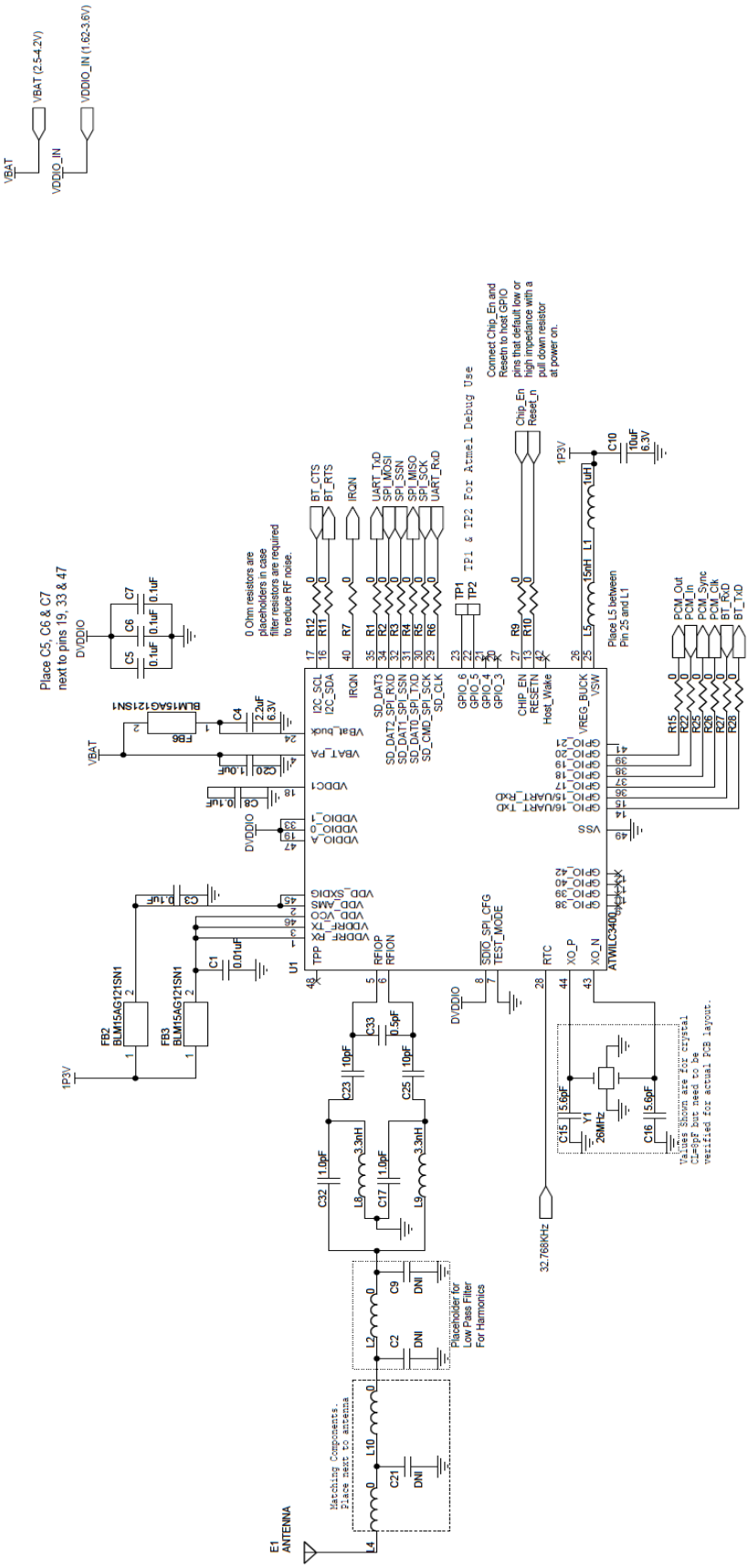
Table 10-4. Digital I/O Pin Behavior in Different Device States

Device State	VDDIO	CHIP_EN	RESETN	Output Driver	Input Driver	Pull Up/Down Resistor (96kΩ)
Power_Down: core supply off	High	Low	Low	Disabled (Hi-Z)	Disabled	Disabled
Power-On Reset: core supply on, hard reset on	High	High	Low	Disabled (Hi-Z)	Disabled	Enabled
Power-On Default: core supply on, device out of reset but not programmed yet	High	High	High	Disabled (Hi-Z)	Enabled	Enabled
On_Doze/ On_Transmit/ On_Receive: core supply on, device programmed by firmware	High	High	High	Programmed by firmware for each pin: Enabled or Disabled	Opposite of Output Driver state	Programmed by firmware for each pin: Enabled or Disabled

11 Reference Design

The ATWINC3400 reference design schematic is shown in Figure 11-1.

Figure 11-1. ATWINC3400 Reference Schematic



12 Reference Design Guidelines

- RFIOP and RFION pins must be AC coupled
- It is recommended that the balun is located right next to the pins – if this is not possible, RFIOP and RFION should be routed as 50Ω differential pair to the balun
- ATWINC3400 provides programmable pull-up resistors on various pins (see Table 3-1). The purpose of these resistors is to keep any unused input pins from floating which can cause excess current to flow through the input buffer from the VDDIO supply. Any unused pin on the device should leave these pull-up resistors enabled so the pin will not float.

  The default state at power up is for the pull-up resistor to be enabled. However, any pin which is used should have the pull-up resistor disabled. The reason for this is that if any pins are driven to a low level while the device is in the low power sleep state, current will flow from the VDDIO supply through the pull-up resistors, increasing the current consumption of the module.

  Since the value of the pull-up resistor is approximately 100KΩ, the current through any pull-up resistor that is being driven low will be VDDIO/100K. For VDDIO = 3.3V, the current would be approximately 33µA.

  Pins which are used and have had the programmable pull-up resistor disabled should always be actively driven to either a high or low level and not be allowed to float
- If SDIO interface is used, each SDIO pin should use a 70Ω resistor in series for RF noise filtering
- Refer to ATWINC3400 Programming Guide for information on enabling/disabling the programmable pull-up resistors

13 Reference Documentation and Support

Atmel offers a set of collateral documentation to ease integration and device ramp.

The following list of documents available on Atmel web or integrated into development tools.

Title	Content
Datasheet	This Document
Design Files Package	User Guide, Schematic, PCB layout, Gerber, BOM and System notes on: RF/Radio Full Test Report, radiation pattern, design guidelines, temperature performance, ESD.
Platform Getting Started Guide	How to use package: Out of the Box starting guide, HW limitations and notes, SW Quick start guidelines.
HW Design Guide	Best practices and recommendations to design a board with the product. Including: Antenna Design for Wi-Fi (layout recommendations, types of antennas, impedance matching, using a power amplifier etc.), SPI/UART protocol between Wi-Fi SoC and the Host MCU.
SW Design Guide	Integration guide with clear description of: High level Arch, overview on how to write a networking application, list all API, parameters and structures. Features of the device, SPI/handshake protocol between device and host MCU, with flow/sequence/state diagram, timing.
SW Programmer Guide	Explain in details the flow chart and how to use each API to implement all generic use cases (e.g. start AP, start STA, provisioning, UDP, TCP, http, TLS, p2p, errors management, connection/transfer recovery mechanism/state diagram) - usage and sample application note.

For a complete listing of development-support tools and documentation, visit http://www.atmel.com/, or contact the nearest Atmel field representative.

14 Revision History

Doc Rev.	Date	Comments
42396C	07/2015	1. Modified sections 10.2.1 and 10.2.2 to add new current consumption numbers, update state names, and correct some typos 2. Fixed typos for SPI Slave interface timing (Table 9-6) 3. Fixed typos for battery supply name: changed from VBAT to VBATT 4. Corrected PMU output voltages (Table 10-1) 5. Updated reference schematic drawing (Section 11) 6. Added comment regarding resistors on SDIO pins (Section 12) 7. Replaced Bluetooth with BLE throughout the document, updated content accordingly 8. Removed PCM functionality 9. Added back SDIO interface description (Section 9.5) 10. Updated power architecture drawing (Section 10.1) 11. Added pad drive strength in Table 4-3 and removed the note under Table 3-1 12. Updated operating temperature in the feature list 13. Corrected current in Power_Down state in Table 10-2 14. Miscellaneous minor formatting and content corrections
42396B	03/2015	Ordering information (Table 1-1) and QFN Package Information (Table 3-2) have been corrected.
42396A	02/2015	Initial document release.

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