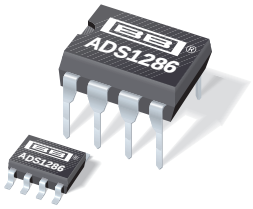
BURR-BROWN®




# ADS1286

# 12-Bit Micro Power Sampling ANALOG-TO-DIGITAL CONVERTER

## FEATURES

- SERIAL INTERFACE
- GUARANTEED NO MISSING CODES
- 20kHz SAMPLING RATE
- LOW SUPPLY CURRENT: 250µA

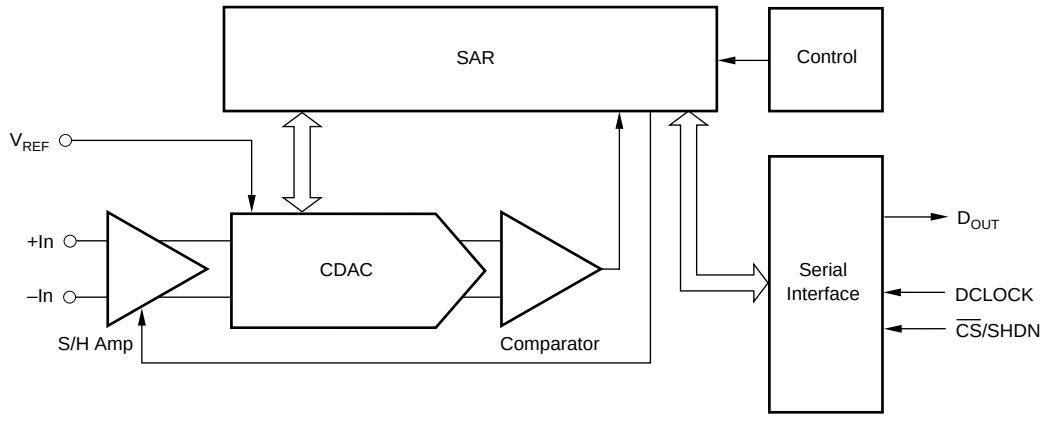
## APPLICATIONS

- REMOTE DATA ACQUISITION
- ISOLATED DATA ACQUISITION
- TRANSDUCER INTERFACE
- BATTERY OPERATED SYSTEMS

## DESCRIPTION

The ADS1286 is a 12-bit, 20kHz analog-to-digital converter with a differential input and sample and hold amplifier and consumes only 250µA of supply current. The ADS1286 offers an SPI and SSI compatible serial interface for communications over a two or three wire interface. The combination of a serial two wire interface and micropower consumption makes the ADS1286 ideal for remote applications and for those requiring isolation.

The ADS1286 is available in a 8-pin plastic mini DIP and a 8-lead SOIC.




International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111
Twx: 910-952-1111 • Internet: http://www.burr-brown.com/ • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

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SBAS053

# SPECIFICATIONS

At $T_A = T_{MIN}$ to $T_{MAX}$, $+V_{CC} = +5V$, $V_{REF} = +5V$, $f_{SAMPLE} = 12.5kHz$, , $f_{CLK} = 16 \bullet f_{SAMPLE}$, unless otherwise specified.

| PARAMETER | CONDITIONS | ADS1286, ADS1286A | | | ADS1286K, ADS1286B | | | ADS1286C, ADS1286L | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| **ANALOG INPUT** | | | | | | | | | | | |
| Full-Scale Input Range | +In – (–In) | 0 | | $V_{REF}$ | * | | * | * | | * | V |
| Absolute Input Voltage | +In | –0.2 | | $V_{CC}$ +0.2 | * | | * | * | | * | V |
| | –In | –0.2 | | +0.2 | * | | * | * | | * | V |
| Capacitance | | | 25 | | | * | | | * | | pF |
| Leakage Current | | | ±1 | | | * | | | * | | µA |
| **SYSTEM PERFORMANCE** | | | | | | | | | | | |
| Resolution | | | 12 | | | * | | | * | | Bits |
| No Missing Codes | | 12 | | | * | | | * | | | Bits |
| Integral Linearity | | | ±1 | ±2 | | * | * | | ±0.5 | ±1 | LSB |
| Differential Linearity | | | ±0.5 | ±1.0 | | * | ±0.75 | | ±0.25 | ±0.75 | LSB |
| Offset Error | | | 0.75 | ±3 | | * | * | | * | * | LSB |
| Gain Error | | | ±2 | ±8 | | * | * | | * | * | LSB |
| Noise | | | 50 | | | * | | | * | | µVrms |
| Power Supply Rejection | | | 82 | | | * | | | * | | dB |
| **SAMPLING DYNAMICS** | | | | | | | | | | | |
| Conversion Time | | | | 12 | | | * | | | * | Clk Cycles |
| Acquisition Time | | 1.5 | | | * | | | * | | | Clk Cycles |
| Small Signal Bandwidth | | | 500 | | | * | | | * | | kHz |
| **DYNAMIC CHARACTERISTICS** | | | | | | | | | | | |
| Total Harmonic Distortion | $V_{IN}$ = 5.0Vp-p at 1kHz | | –85 | | | * | | | * | | dB |
| | $V_{IN}$ = 5.0Vp-p at 5kHz | | –83 | | | * | | | * | | dB |
| SINAD | $V_{IN}$ = 5.0Vp-p at 1kHz | | 72 | | | * | | | * | | dB |
| Spurious Free Dynamic Range | $V_{IN}$ = 5.0Vp-p at 1kHz | | 90 | | | * | | | * | | dB |
| **REFERENCE INPUT** | | | | | | | | | | | |
| REF Input Range | | 1.25 | 2.5 | $V_{CC}$+0.05V | * | * | * | * | * | * | V |
| Input Resistance | $\overline{CS}$ = $V_{CC}$ | | 5000 | | | * | | | * | | MΩ |
| | $\overline{CS}$ = GND, $f_{CLK}$ = 0Hz | | 5000 | | | * | | | * | | MΩ |
| Current Drain | $\overline{CS}$ = $V_{CC}$ | | 0.01 | 2.5 | | * | * | | * | * | µA |
| | $t_{CYC} \geq 640\mu s$, $f_{CLK} \leq 25kHz$ | | 2.4 | 20 | | * | * | | * | * | µA |
| | $t_{CYC} = 80\mu s$, $f_{CLK} = 200kHz$ | | 2.4 | 20 | | * | * | | * | * | µA |
| **DIGITAL INPUT/OUTPUT** | | | | | | | | | | | |
| Logic Family | | | CMOS | | | * | | | * | | |
| Logic Levels: | | | | | | | | | | | |
| $V_{IH}$ | $I_{IH}$ = +5µA | 3 | | $+V_{CC}$ | * | | * | * | | * | V |
| $V_{IL}$ | $I_{IL}$ = +5µA | 0.0 | | 0.8 | * | | * | * | | * | V |
| $V_{OH}$ | $I_{OH}$ = 250µA | 3 | | $+V_{CC}$ | * | | * | * | | * | V |
| $V_{OL}$ | $I_{OL}$ = 250µA | 0.0 | | 0.4 | * | | * | * | | * | V |
| Data Format | | | Straight Binary | | | * | | | * | | |
| **POWER SUPPLY REQUIREMENTS** | | | | | | | | | | | |
| Power Supply Voltage $V_{CC}$ | | +4.50 | 5 | 5.25 | * | * | * | * | * | * | V |
| Quiescent Current, $V_{ANA}$ | $t_{CYC} \geq 640\mu S$, $f_{CLK} \leq 25kHz$ | | 200 | 400 | | * | * | | * | * | µA |
| | $t_{CYC} = 90\mu S$, $f_{CLK} = 200kHz$ | | 250 | 500 | | * | * | | * | * | µA |
| Power Down | $\overline{CS}$ = $V_{CC}$ | | | 3 | | | * | | | * | µA |
| **TEMPERATURE RANGE** | | | | | | | | | | | |
| Specified Performance | ADS1286, K, L | 0 | | +70 | * | | * | * | | * | °C |
| | ADS1286A, B, C | –40 | | +85 | * | | * | * | | * | °C |

* Specifications same as grade to the left.

# TIMING CHARACTERISTICS

$f_{CLK}$ = 200kHz, $T_A = T_{MIN}$ to $T_{MAX}$.

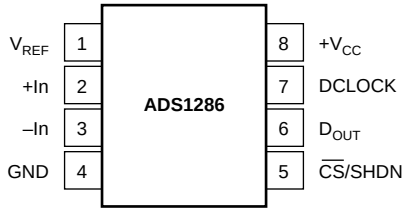
| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| $t_{SMPL}$ | Analog Input Sample Time | See Operating Sequence | 1.5 | | 2.0 | Clk Cycles |
| $t_{SMPL\ (MAX)}$ | Maximum Sampling Frequency | ADS1286 | | | 20 | kHz |
| $t_{CONV}$ | Conversion Time | See Operating Sequence | | 12 | | Clk Cycles |
| $t_{dDO}$ | Delay TIme, DCLOCK↓ to $D_{OUT}$ Data Valid | See Test Circuits | | 85 | 150 | ns |
| $t_{dis}$ | Delay TIme, $\overline{CS}$↑ to $D_{OUT}$ Hi-Z | See Test Circuits | | 25 | 50 | ns |
| $t_{en}$ | Delay TIme, DCLOCK↓ to $D_{OUT}$ Enable | See Test Circuits | | 50 | 100 | ns |
| $t_{hDO}$ | Output Data Remains Valid After DCLOCK↓ | $C_{LOAD}$ = 100pF | 15 | 30 | | ns |
| $t_f$ | $D_{OUT}$ Fall Time | See Test Circuits | | 70 | 100 | ns |
| $t_r$ | $D_{OUT}$ Rise Time | See Test Circuits | | 60 | 100 | ns |
| $t_{CSD}$ | Delay Time, $\overline{CS}$↓ to DCLOCK↓ | See Operating Sequence | | | 0 | ns |
| $t_{SUCS}$ | Delay Time, $\overline{CS}$↓ to DCLOCK↑ | See Operating Sequence | 30 | | | ns |

## ABSOLUTE MAXIMUM RATINGS[1]

| | |
|---|---|
| $+V_{CC}$ | +6V |
| Analog Input | –0.3V to ($+V_{CC}$ + 300mV) |
| Logic Input | –0.3V to ($+V_{CC}$ + 300mV) |
| Case Temperature | +100°C |
| Junction Temperature | +150°C |
| Storage Temperature | +125°C |
| External Reference Voltage | +5.5V |

NOTE: (1) Stresses above these ratings may permanently damage the device.

## PIN CONFIGURATION




8-Pin Mini PDIP
8-Lead SOIC

## ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

## PIN ASSIGNMENTS

| PIN | NAME | DESCRIPTION |
|---|---|---|
| 1 | $V_{REF}$ | Reference Input. |
| 2 | +In | Non Inverting Input. |
| 3 | –In | Inverting Input. Connect to ground or remote ground sense point. |
| 4 | GND | Ground. |
| 5 | $\overline{CS}$/SHDN | Chip Select when low, Shutdown Mode when high. |
| 6 | $D_{OUT}$ | The serial output data word is comprised of 12 bits of data. In operation the data is valid on the falling edge of DCLOCK. The second clock pulse after the falling edge of $\overline{CS}$ enables the serial output. After one null bit the data is valid for the next 12 edges. |
| 7 | DCLOCK | Data Clock synchronizes the serial data transfer and determines conversion speed. |
| 8 | $+V_{CC}$ | Power Supply. |

## PACKAGE/ORDERING INFORMATION

| PRODUCT | INTEGRAL LINEARITY | TEMPERATURE RANGE | PACKAGE | PACKAGE DRAWING NUMBER[1] |
|---|---|---|---|---|
| ADS1286P | ±2 | 0°C to +70°C | Plastic DIP | 006 |
| ADS1286PK | ±2 | 0°C to +70°C | Plastic DIP | 006 |
| ADS1286PL | ±1 | 0°C to +70°C | Plastic DIP | 006 |
| ADS1286U | ±2 | 0°C to +70°C | SOIC | 182 |
| ADS1286UK | ±2 | 0°C to +70°C | SOIC | 182 |
| ADS1286UL | ±1 | 0°C to +70°C | SOIC | 182 |
| ADS1286PA | ±2 | –40°C to +85°C | Plastic DIP | 006 |
| ADS1286PB | ±2 | –40°C to +85°C | Plastic DIP | 006 |
| ADS1286PC | ±1 | –40°C to +85°C | Plastic DIP | 006 |
| ADS1286UA | ±2 | –40°C to +85°C | SOIC | 182 |
| ADS1286UB | ±2 | –40°C to +85°C | SOIC | 182 |
| ADS1286UC | ±1 | –40°C to +85°C | SOIC | 182 |

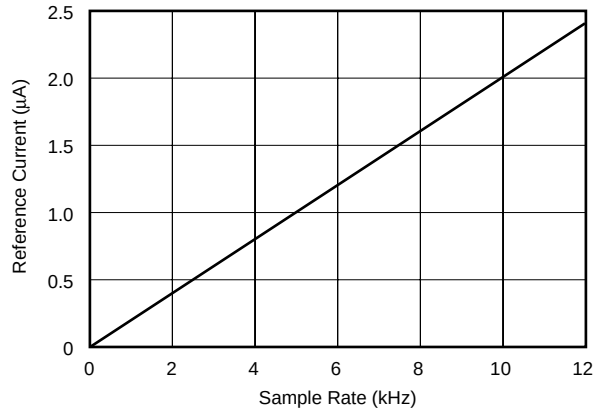
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

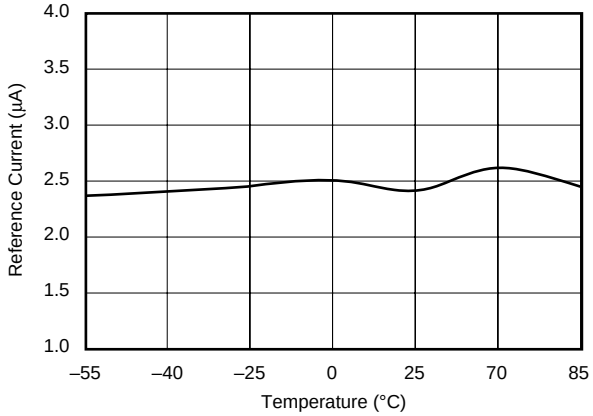
# TYPICAL PERFORMANCE CURVES

At $T_A$ = +25, $V_{CC}$ = +5V, $V_{REF}$ = +5V, $f_{SAMPLE}$ = 12.5kHz, $f_{CLK}$ = 16 • $f_{SAMPLE}$, unless otherwise specified.

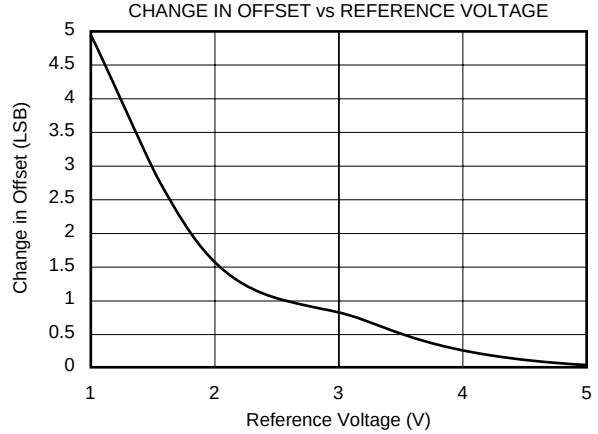
REFERENCE CURRENT vs SAMPLE RATE



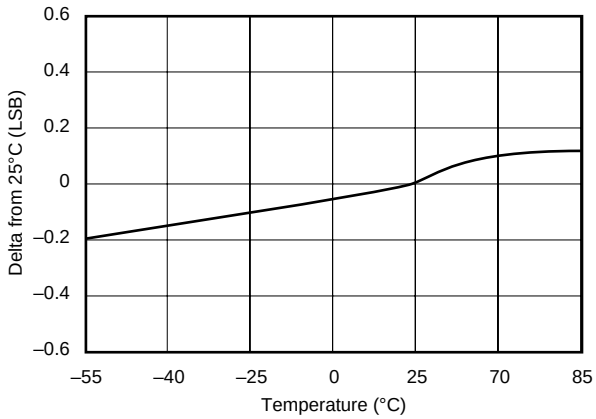

REFERENCE CURRENT vs TEMPERATURE



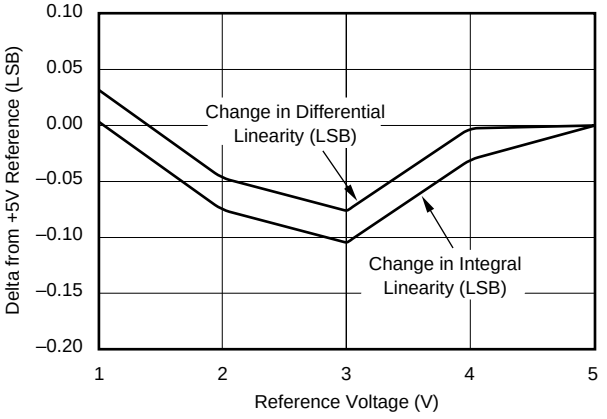

CHANGE IN OFFSET vs REFERENCE VOLTAGE



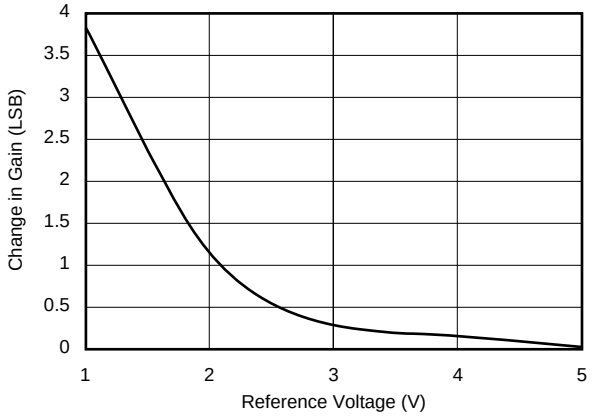

CHANGE IN OFFSET vs TEMPERATURE




CHANGE IN INTEGRAL LINEARITY AND DIFFERENTIAL LINEARITY vs REFERENCE VOLTAGE



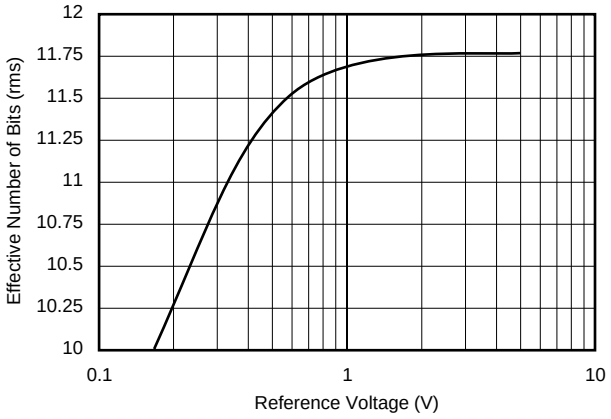

CHANGE IN GAIN vs REFERENCE VOLTAGE



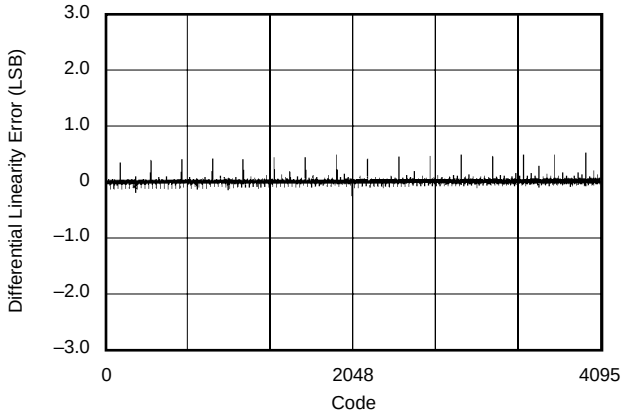
# TYPICAL PERFORMANCE CURVES (CONT)

At $T_A$ = +25, $V_{CC}$ = +5V, $V_{REF}$ = +5V, $f_{SAMPLE}$ = 12.5kHz, $f_{CLK}$ = 16 • $f_{SAMPLE}$, unless otherwise specified.

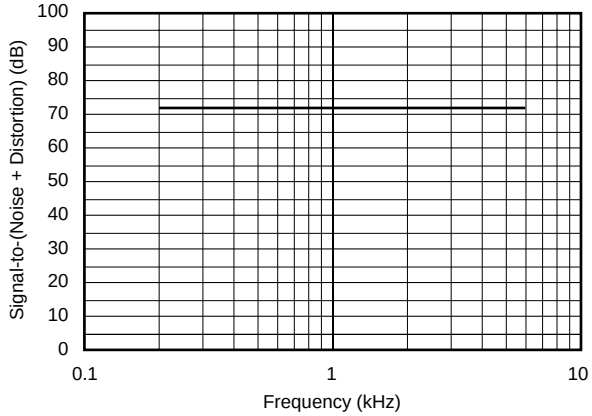
EFFECTIVE NUMBER OF BITS
vs REFERENCE VOLTAGE



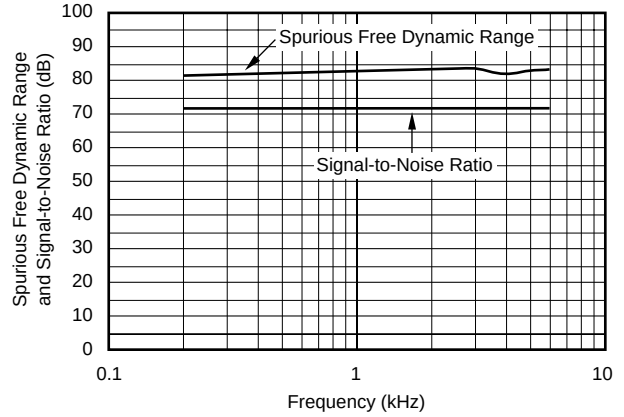

DIFFERENTIAL LINEARITY ERROR vs CODE



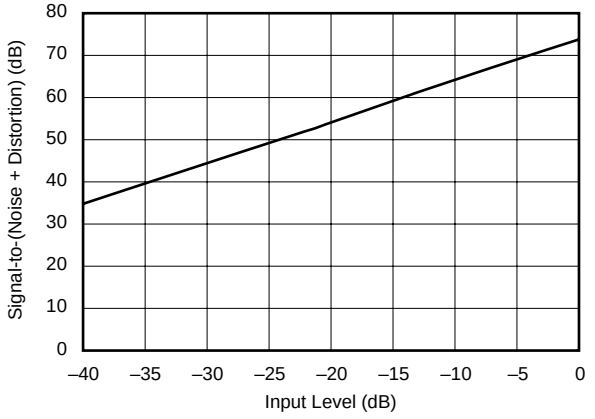

SIGNAL-TO-(NOISE + DISTORTION)
vs FREQUENCY



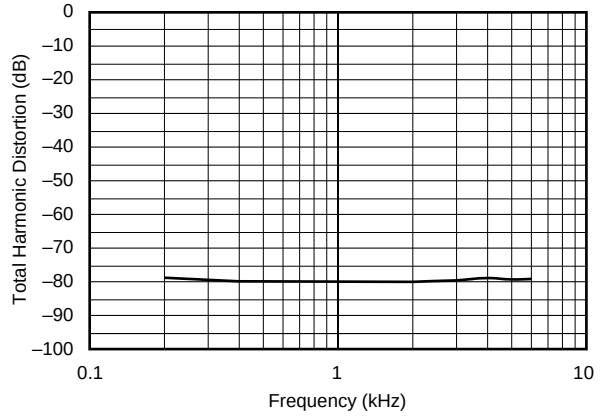

SPURIOUS FREE DYNAMIC RANGE
AND SIGNAL-TO-NOISE RATIO vs FREQUENCY




SIGNAL-TO-(NOISE + DISTORTION) vs INPUT LEVEL



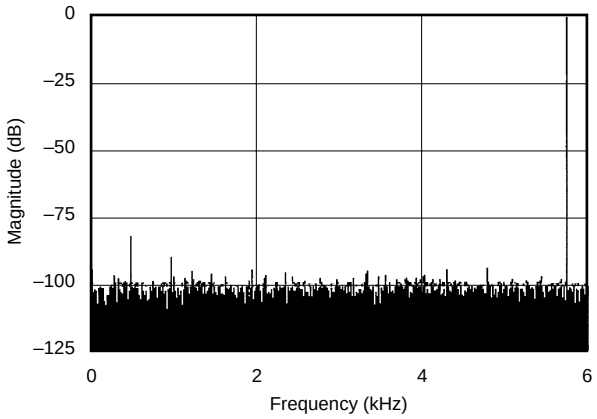

TOTAL HARMONIC DISTORTION vs FREQUENCY



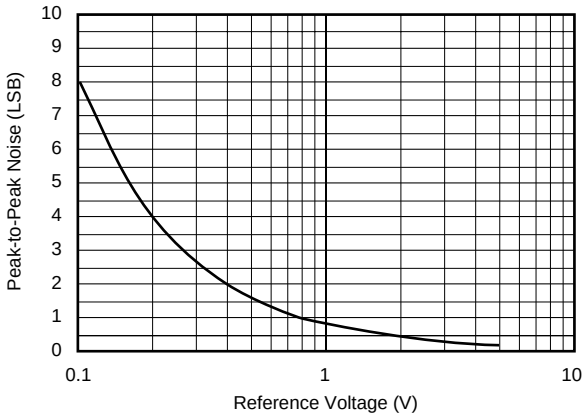
# TYPICAL PERFORMANCE CURVES (CONT)

At $T_A$ = +25, $V_{CC}$ = +5V, $V_{REF}$ = +5V, $f_{SAMPLE}$ = 12.5kHz, $f_{CLK}$ = 16 • $f_{SAMPLE}$, unless otherwise specified.

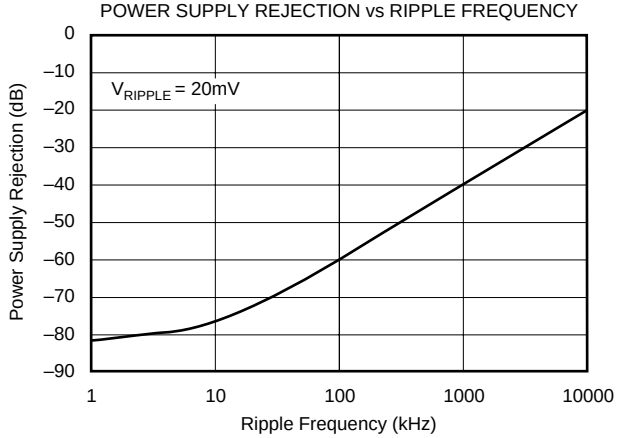
4096 POINT FFT



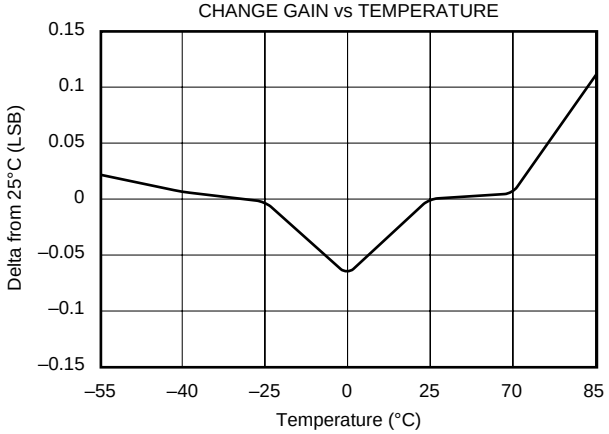

PEAK-TO-PEAK NOISE vs REFERENCE VOLTAGE



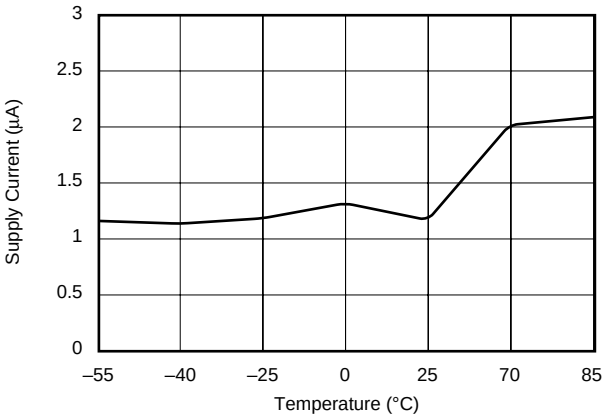

POWER SUPPLY REJECTION vs RIPPLE FREQUENCY



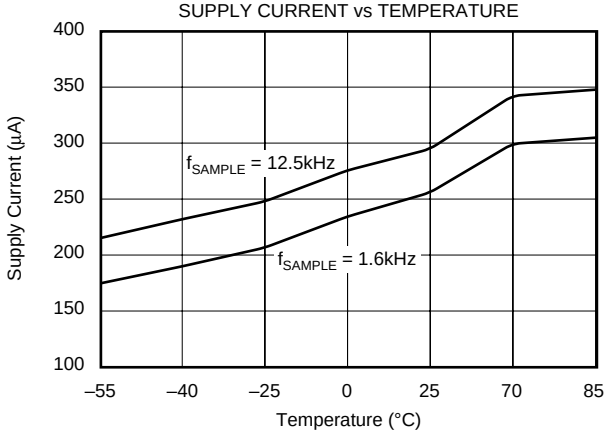

CHANGE GAIN vs TEMPERATURE




POWER DOWN SUPPLY CURRENT
vs TEMPERATURE



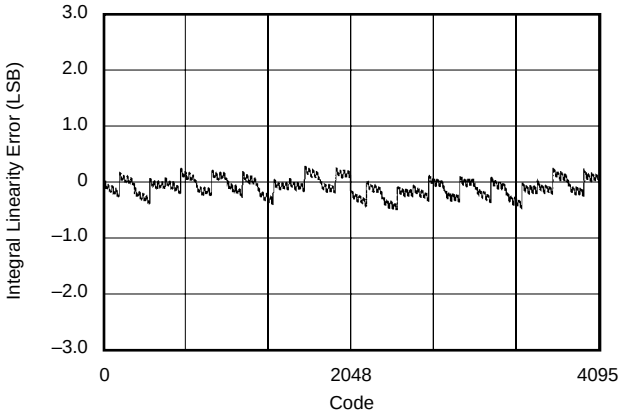

SUPPLY CURRENT vs TEMPERATURE



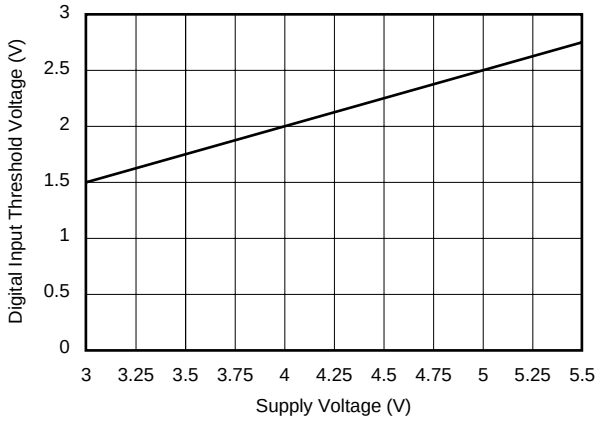
# TYPICAL PERFORMANCE CURVES (CONT)

At $T_A$ = +25, $V_{CC}$ = +5V, $V_{REF}$ = +5V, $f_{SAMPLE}$ = 12.5kHz, $f_{CLK}$ = 16 • $f_{SAMPLE}$, unless otherwise specified.

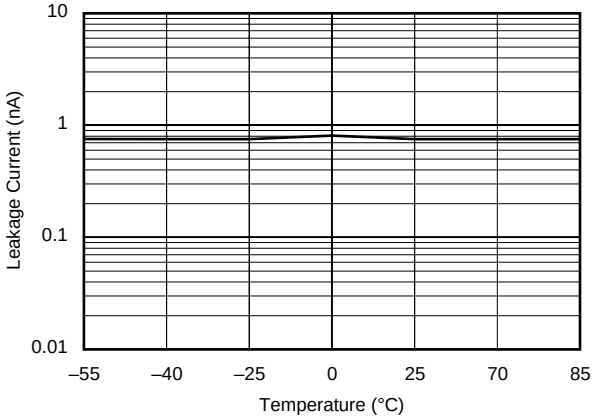
INTEGRAL LINEARITY ERROR vs CODE



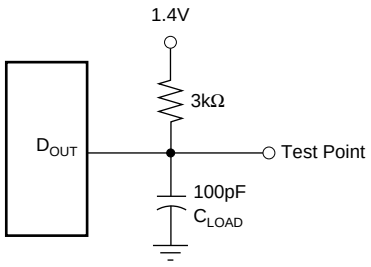

DIGITAL INPUT LINE THRESHOLD vs SUPPLY VOLTAGE



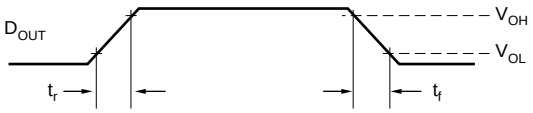

INPUT LEAKAGE CURRENT vs TEMPERATURE



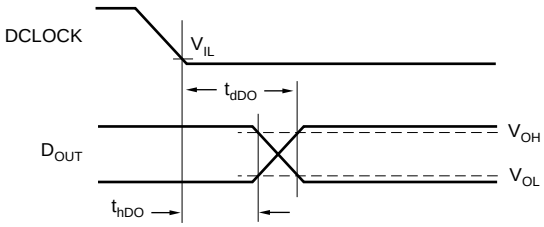
## TIMING DIAGRAMS AND TEST CIRCUITS



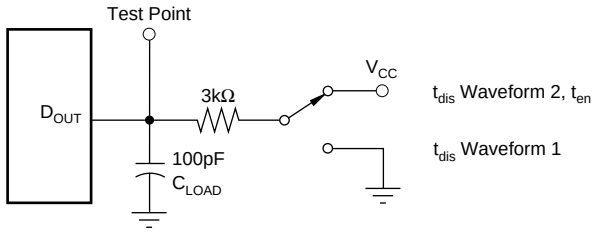

Load Circuit for $t_{dDO}$, $t_r$, and $t_f$



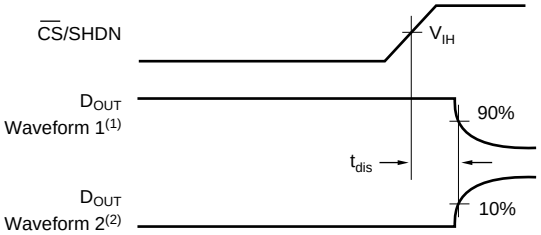

Voltage Waveforms for $D_{OUT}$ Rise and Fall Times $t_r$, and $t_f$



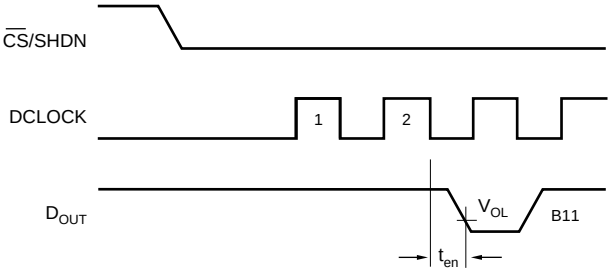

Voltage Waveforms for $D_{OUT}$ Delay Times, $t_{dDO}$




Load Circuit for $t_{dis}$ and $t_{den}$




Voltage Waveforms for $t_{dis}$




Voltage Waveforms for $t_{en}$

NOTES: (1) Waveform 1 is for an output with internal conditions such that the output is HIGH unless disabled by the output control. (2) Waveform 2 is for an output with internal conditions such that the output is LOW unless disabled by the output control.

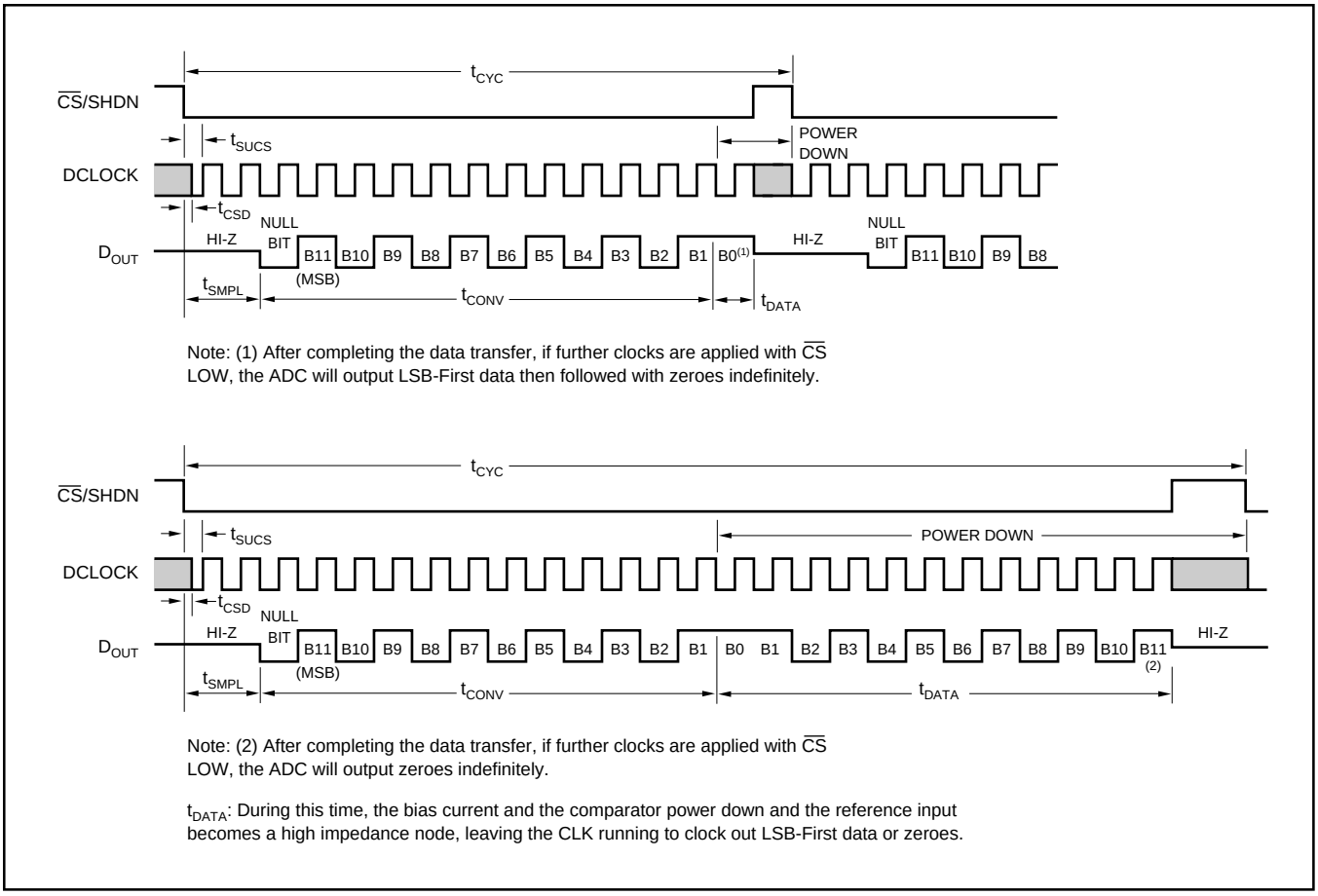



FIGURE 1. ADS1286 Operating Sequence.

# SERIAL INTERFACE

The ADS1286 communicates with microprocessors and other external digital systems via a synchronous 3-wire serial interface. DCLOCK synchronizes the data transfer with each bit being transmitted on the falling DCLOCK edge and captured on the rising DCLOCK edge in the receiving system. A falling $\overline{CS}$ initiates data transfer as shown in Figure 1. After $\overline{CS}$ falls, the second DCLOCK pulse enables $D_{OUT}$. After one null bit, the A/D conversion result is output on the $D_{OUT}$ line. Bringing $\overline{CS}$ high resets the ADS1286 for the next data exchange.

# MICROPOWER OPERATION

With typical operating currents of 250µA and automatic shutdown between conversions, the ADS1286 achieves extremely low power consumption over a wide range of sample rates (see Figure 2). The auto-shutdown allows the supply current to drop with sample rate.

### SHUTDOWN

The ADS1286 is equipped with automatic shutdown features. The device draws power when the $\overline{CS}$ pin is LOW and shuts down completely when the pin is HIGH. The bias circuit and comparator powers down and the reference input becomes high impedance at the end of each conversion leaving the DCLOCK running to clock out the LSB first data or zeroes. If the $\overline{CS}$ input is not running rail-to-rail, the input logic buffer will draw current. This current may be large compared to the typical supply current. To obtain the lowest supply current, bring the $\overline{CS}$ pin to ground when it is low and to supply voltage when it is high.

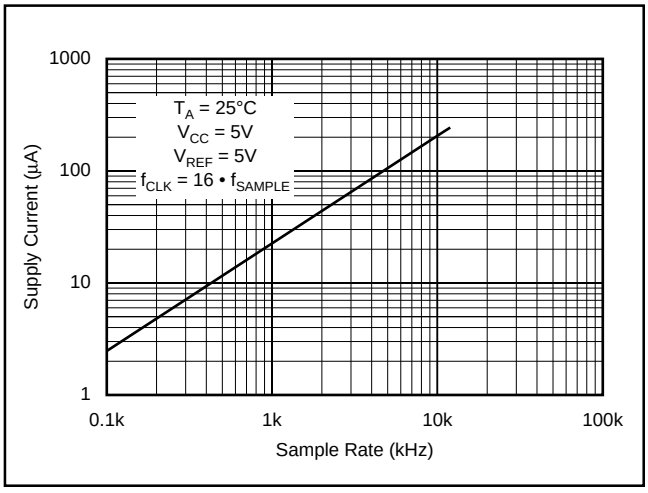



FIGURE 2. Automatic Power Shutdown Between Conversions Allows Power Consumption to Drop with Sample Rate.

### MINIMIZING POWER DISSIPATION

In systems that have significant time between conversions, the lowest power drain will occur with the minimum $\overline{CS}$ LOW time. Bringing $\overline{CS}$ LOW, transferring data as quickly as possible, and then bringing it back HIGH will result in the lowest current drain. This minimizes the amount of time the device draws power. After a conversion the A/D automatically shuts down even if $\overline{CS}$ is held LOW. If the clock is left running to clock out LSB-data or zero, the logic will draw a small amount of current (see Figure 3).

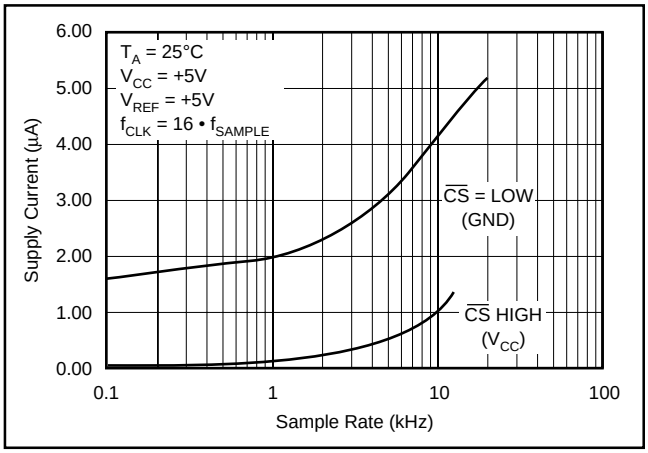



FIGURE 3. Shutdown Current with $\overline{CS}$ HIGH is Lower than with $\overline{CS}$ LOW.

## RC INPUT FILTERING

It is possible to filter the inputs with an RC network as shown in Figure 4. For large values of $C_{FILTER}$ (e.g., 1µF), the capacitive input switching currents are averaged into a net DC current. Therefore, a filter should be chosen with a small resistor and large capacitor to prevent DC drops across the resistor. The magnitude of the DC current is approximately $I_{DC} = 20pF \times V_{IN}/t_{CYC}$ and is roughly proportional to $V_{IN}$. When running at the minimum cycle time of 64µs, the input current equals 1.56µA at $V_{IN}$ = 5V. In this case, a filter resistor of 75Ω will cause 0.1LSB of full-scale error. If a larger filter resistor must be used, errors can be eliminated by increasing the cycle time.

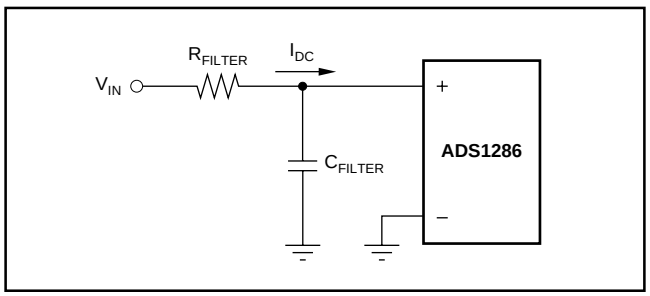



FIGURE 4. RC Input Filtering.

## REDUCED REFERENCE OPERATION

The effective resolution of the ADS1286 can be increased by reducing the input span of the converter. The ADS1286 exhibits good linearity and gain over a wide range of reference voltages (see Typical Performance Curves " Change in Linearity vs Reference Voltage" and "Change in Gain vs Reference Voltage"). However, care must be taken when operating at low values of $V_{REF}$ because of the reduced LSB size and the resulting higher accuracy requirement placed on the converter. The following factors must be considered when operating at low $V_{REF}$ values:

1. Offset
2. Noise

### OFFSET WITH REDUCED $V_{REF}$

The offset of the ADS1286 has a larger effect on the output code. When the ADC is operated with reduced reference voltage. The offset (which is typically a fixed voltage) becomes a larger fraction of an LSB as the size of the LSB is reduced. The Typical Performance Curve "Change in Offset vs Reference Voltage" shows how offset in LSBs is related to reference voltage for a typical value of $V_{OS}$. For example, a $V_{OS}$ of 122µV which is 0.1 LSB with a 5V reference becomes 0.5LSB with a 1V reference and 2.5LSBs with a 0.2V reference. If this offset is unacceptable, it can be corrected digitally by the receiving system or by offsetting the negative input of the ADS1286.

### NOISE WITH REDUCED $V_{REF}$

The total input referred noise of the ADS1286 can be reduced to approximately 200µV peak-to-peak using a ground plane, good bypassing, good layout techniques and minimizing noise on the reference inputs. This noise is insignificant with a 5V reference but will become a larger fraction of an LSB as the size of the LSB is reduced.

For operation with a 5V reference, the 200µV noise is only 0.15LSB peak-to-peak. In this case, the ADS1286 noise will contribute virtually no uncertainty to the output code. However, for reduced references, the noise may become a significant fraction of an LSB and cause undesirable jitter in the output code. For example, with a 2.5V reference this same 200µV noise is 0.3LSB peak-to-peak. If the reference is further reduced to 1V, the 200µV noise becomes equal to 0.8LSBs and a stable code may be difficult to achieve. In this case averaging multiple readings may be necessary.

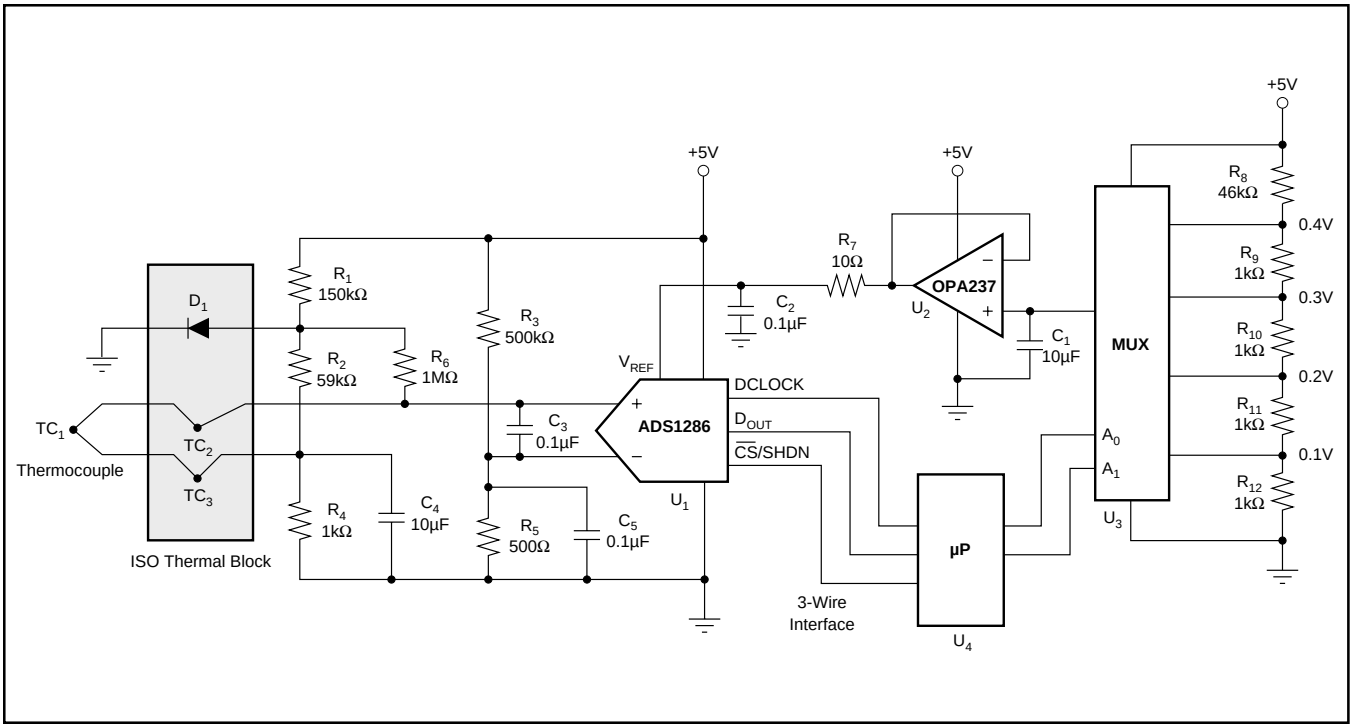



FIGURE 5. Thermocouple Application Using a MUX to Scale the Input Range of the ADS1286.

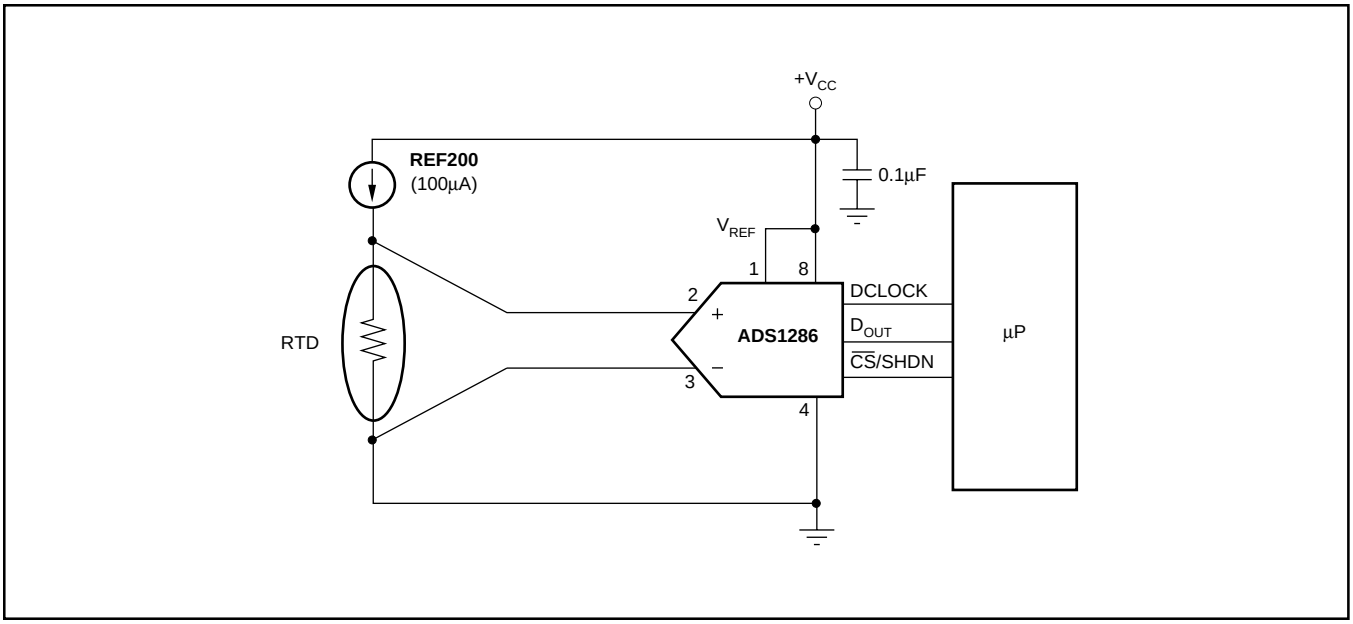



FIGURE 6. ADS1286 with RTD Sensor.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) |
|---|---|---|---|---|---|---|---|---|
| ADS1286P | ACTIVE | PDIP | P | 8 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type |
| ADS1286PA | ACTIVE | PDIP | P | 8 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type |
| ADS1286PB | ACTIVE | PDIP | P | 8 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type |
| ADS1286PBG4 | ACTIVE | PDIP | P | 8 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type |
| ADS1286PC | ACTIVE | PDIP | P | 8 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type |
| ADS1286PG4 | ACTIVE | PDIP | P | 8 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type |
| ADS1286PK | ACTIVE | PDIP | P | 8 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type |
| ADS1286PL | ACTIVE | PDIP | P | 8 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type |
| ADS1286U | ACTIVE | SOIC | D | 8 | 100 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| ADS1286U/2K5 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| ADS1286U/2K5G4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| ADS1286UA | ACTIVE | SOIC | D | 8 | 100 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| ADS1286UA/2K5 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| ADS1286UA/2K5G4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| ADS1286UAG4 | ACTIVE | SOIC | D | 8 | 100 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| ADS1286UB | ACTIVE | SOIC | D | 8 | 100 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| ADS1286UBG4 | ACTIVE | SOIC | D | 8 | 100 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| ADS1286UC | ACTIVE | SOIC | D | 8 | 100 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR |
| ADS1286UCG4 | ACTIVE | SOIC | D | 8 | 100 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR |
| ADS1286UG4 | ACTIVE | SOIC | D | 8 | 100 | TBD | Call TI | Call TI |
| ADS1286UK | ACTIVE | SOIC | D | 8 | 100 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| ADS1286UKG4 | ACTIVE | SOIC | D | 8 | 100 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| ADS1286UL | ACTIVE | SOIC | D | 8 | 100 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| ADS1286UL/2K5 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| ADS1286ULG4 | ACTIVE | SOIC | D | 8 | 100 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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